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One issue was found in Test and updates made:

At 18Vin applying the Kikisui 20A load from no load would trigger a brief shutdown. This was seen on both t1 and t2 models. A circuit review with John Betten (who did PCB PMP6680) raised the potential issue of two high side FETs with zero ohms between the gates. The layout had placeholders for separate gate resistors for each, but they were not used in earlier builds on the PCB PMP6680. With our faster CSD18537BQ5A's they are really needed. The change ended these shutdowns (on both models) and reduced peak Vds at max input and full load by 3V. Effect on efficiency was only 0.1% at full load and 24-36 Vin and less in other conditions. The value used for each of these added R8 & R9 (on schematic / PCB) was 2.2 ohms. (They were zero ohms before.)

In general adding gate resistors to paralleled FETs is considered a good design practice to prevent destructive oscillations (in the several hundred MHz range) on the gates. They are not needed with FETs used only as synchronous rectifiers, such as low side FETs in buck converters.

Model shipped March 6, 2014 was "model t2".

Efficiency and Losses: model t2: 36, 24 & 18Vin, Vout set at 5.0V
101kHz actual switching at 18vin, 100kHz at 24vin and 99kHz at 36Vin; output current measured on 0.5003mOhm shunt down to 10uV increments or 20mA increments; other measurements on Flukes 83 & 87 with cal due later this month
This test run after 2.2 ohm resistors added to each of gates of high side FETs Q1 & Q2
For main inductor L1: Used SER2918H-103KL from Coilcraft
No fan used and ran at load to achieve steady state before recording

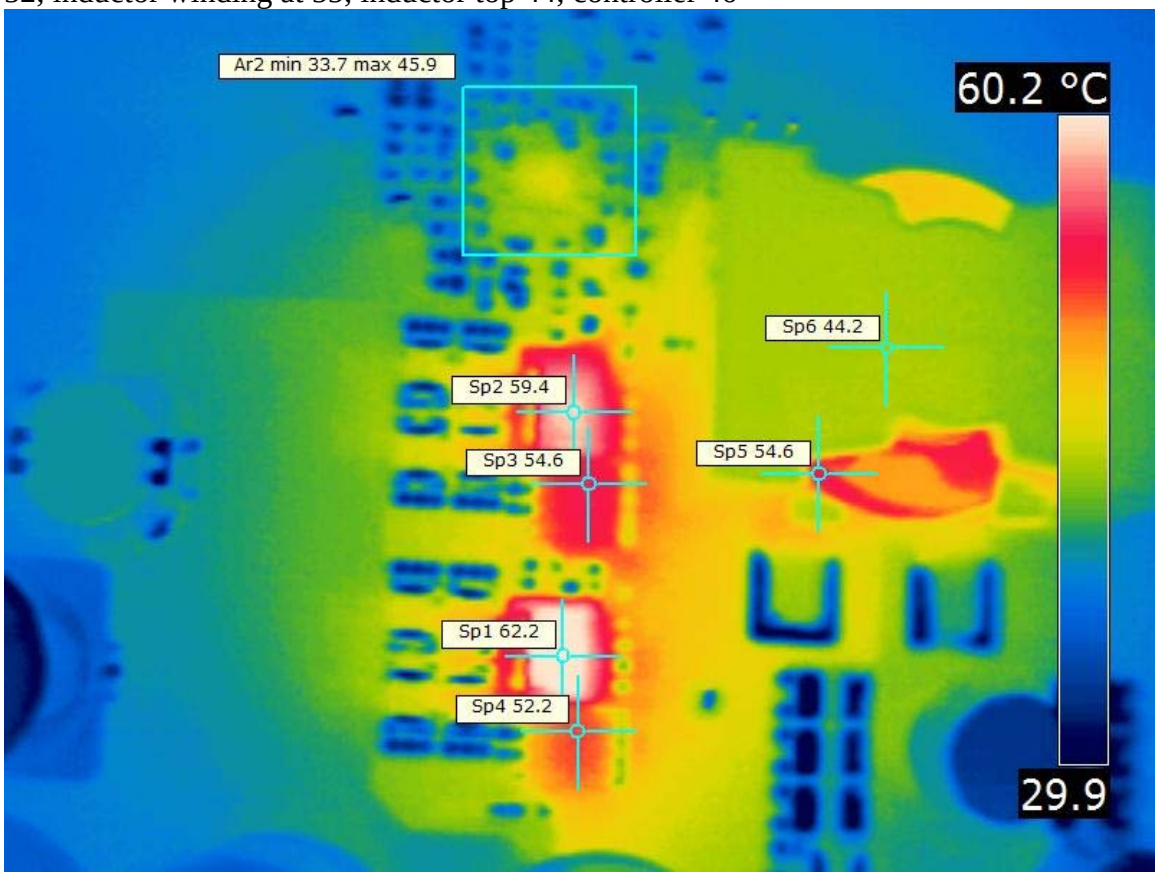
Vin Volts	Iin A	Vout Volts	Iout A	% Effi ciency	Losses in W
36.04	2.9395	5.008	20.00	94.5	5.780
36.06	2.1885	5.005	15.00	95.1	3.842
36.04	1.456	5.0045	10.00	95.4	2.429
36.04	0.735	5.003	5.00	94.4	1.474
36.11	0.0205	5.006	0	0.0	0.740
36	<1mA		off		
24.03	4.387	5.003	20.00	94.9	5.360
24.02	3.262	4.999	15.00	95.7	3.368
24.07	2.160	4.999	10.00	96.2	2.001
24.03	1.085	5.000	5.00	95.9	1.073
24.03	0.0207	5.005	0	0.0	0.497
24	<1mA		off		
18.02	5.8515	5.003	20.00	94.9	5.384
18.01	4.3445	4.998	15.00	95.8	3.274
18.01	2.875	4.997	10.00	96.5	1.809
18.07	1.4325	4.999	5.00	96.6	0.890
18.03	0.0208	5.004	0	0.0	0.375
18	<1mA		off		

Qq
Model t2 before R8 & R9 updated:

36.05	2.939	5.008	20.02	94.6	5.691
36.03	1.457	5.0055	10.00	95.4	2.441
36.03	0.021	5.008	0	0.0	0.757
24.02	4.3865	5.0025	20.00	95.0	5.314
24.04	2.162	5.000	10.00	96.2	1.974
24.05	0.021	5.007	0	0.0	0.505
18.04	5.8485	5.004	20.00	94.9	5.427
18.01	2.875	4.997	10.00	96.5	1.809
18.05	0.021	5.007	0	0.0	0.379

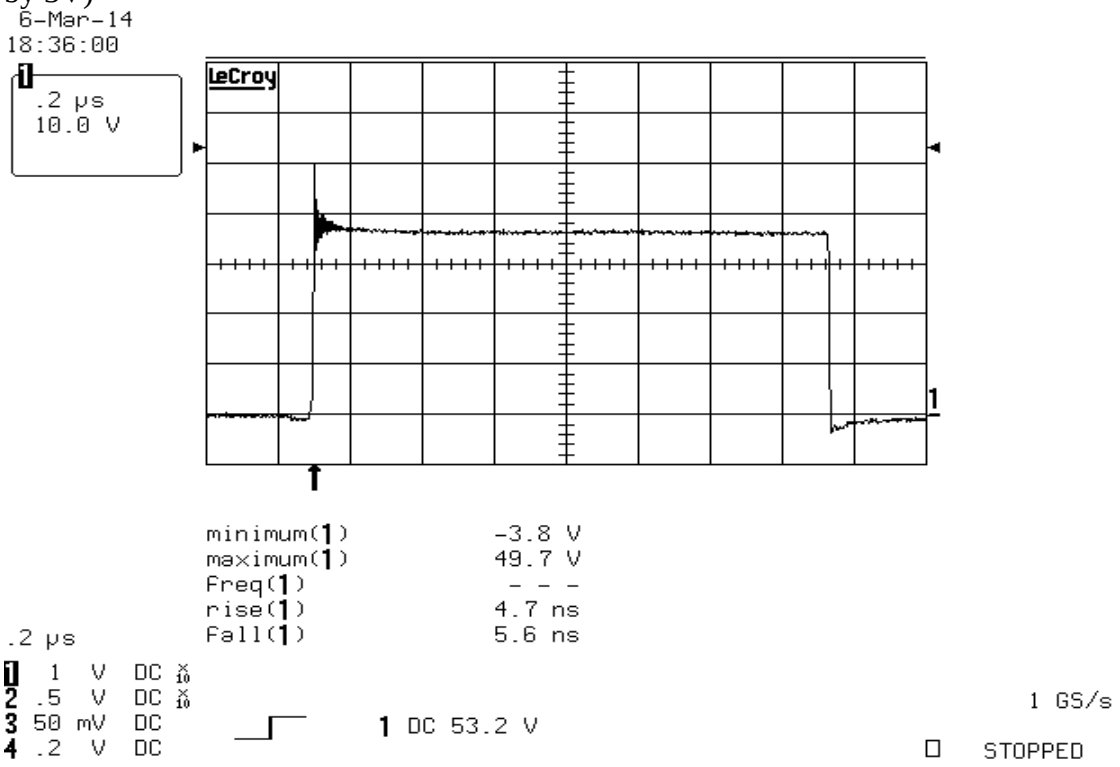
Adding gate resistors had very little effect on efficiency, only 0.1% reduction at full load for 36 and 24 Vin:

Thermal Image: Full 20A load of 5V, max Vin of 36V and no fans: model t2
PMP9621: 36vin 5Vout at 20A 99kHz switching 21-23 degrees Celsius ambient no fans
5.78W loss on PWB
Hottest Q2 hi side FET 62 deg. C; Q1 at 59, Q3 at 55; Q4 at
52; inductor winding at 55; inductor top 44; controller 46

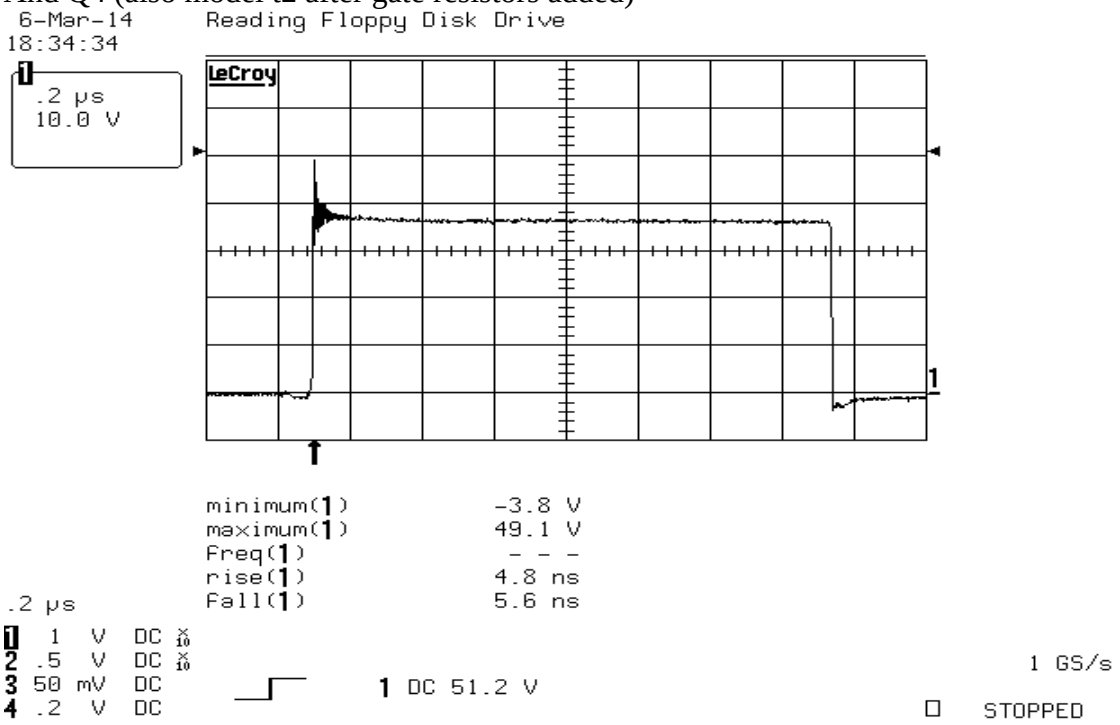


Qq

Main switching waveform: Max 36Vin and max 20A load off 5Vout: Switching frequency 99kHz actual per scope frequency function; after 2.2 ohms gate resistors added to each hi side FET: Q3 Vds with close-in 500MHz 10x probe and 500kHz scope
Q3 rated to 60V, hence, 10V of margin on Vds stress (adding gate resistors reduced peak by 3V)

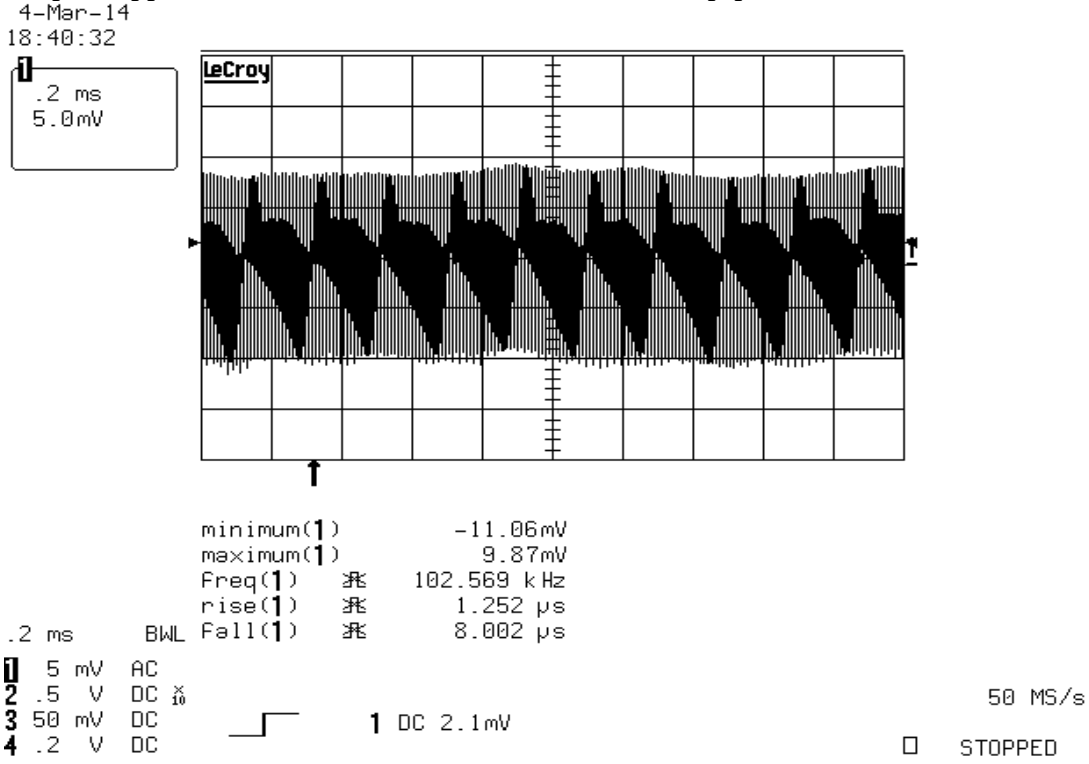


And Q4 (also model t2 after gate resistors added)

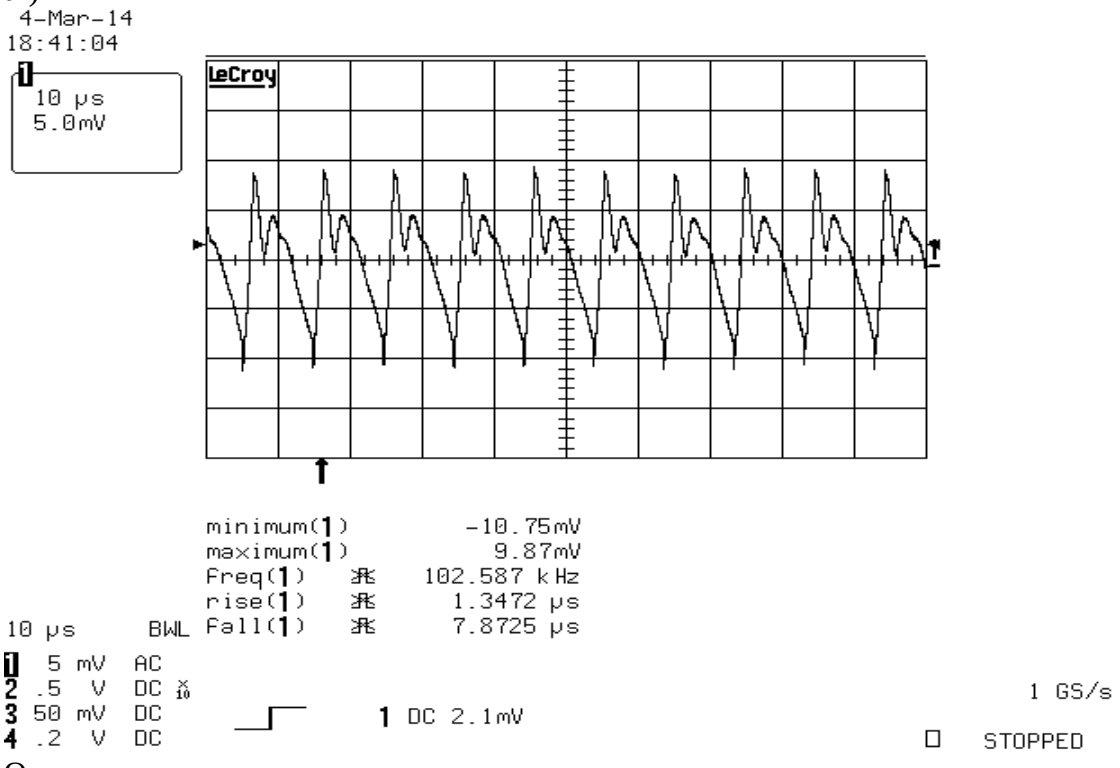


Qq

Output Ripple at full load and max Vin: overall 21mV p-p: Model t1

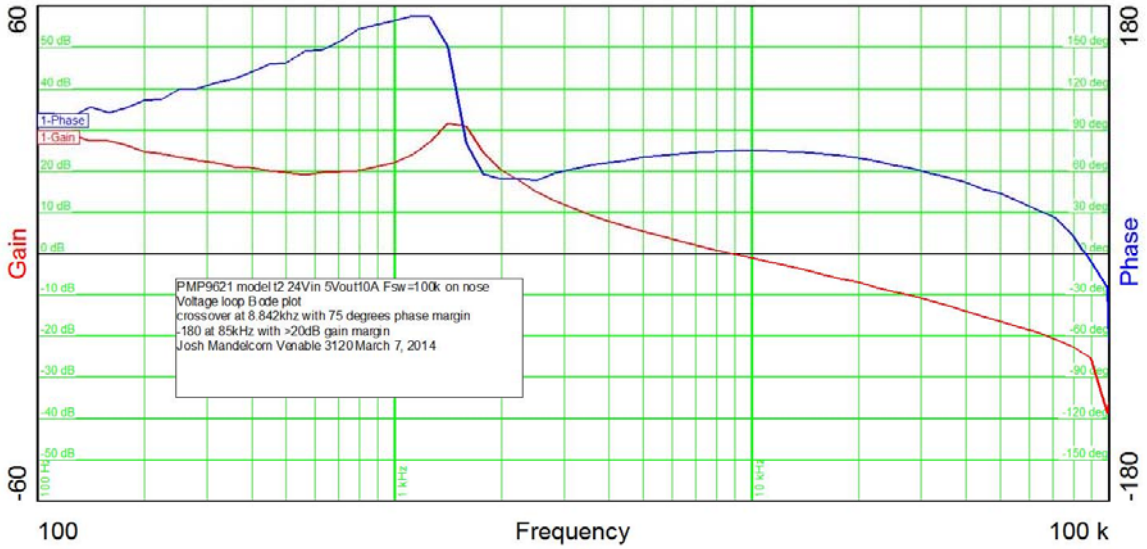


And same with time scale to show detail of ripple: Model t1(similar ripple seen on model t2)



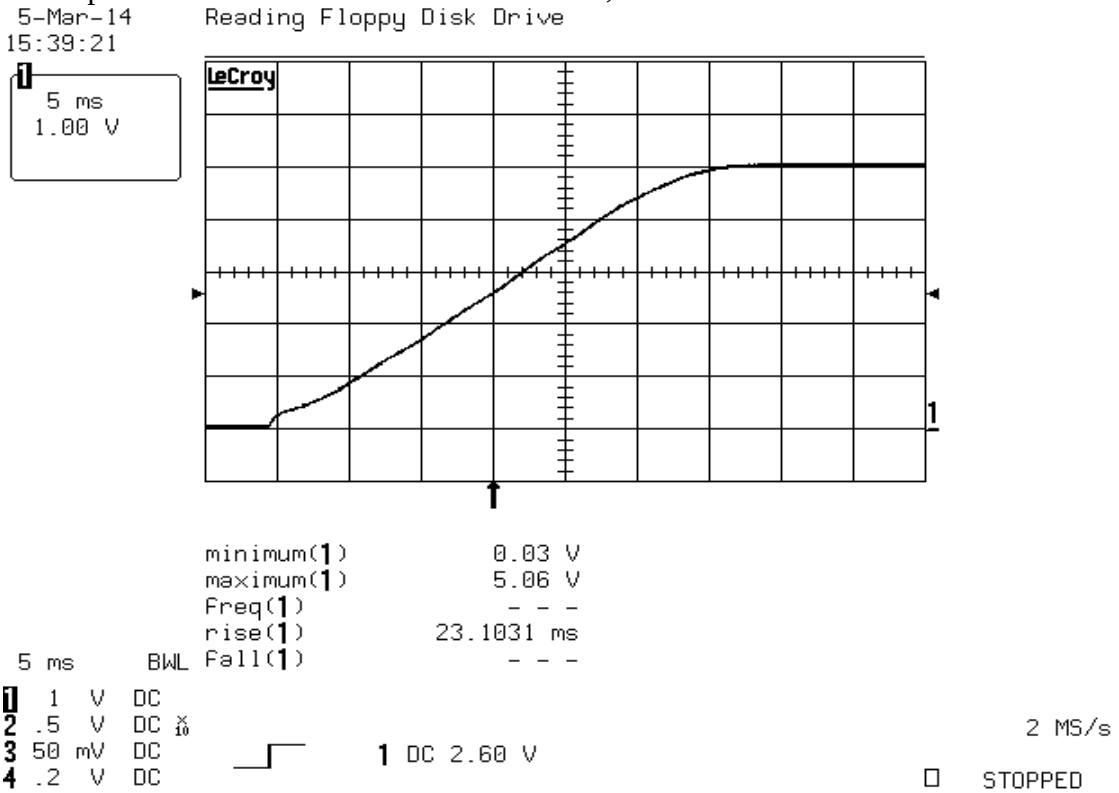
Qq

Overall Bode plot of main 5V loop: model t2 run at 10A load 24Vin:



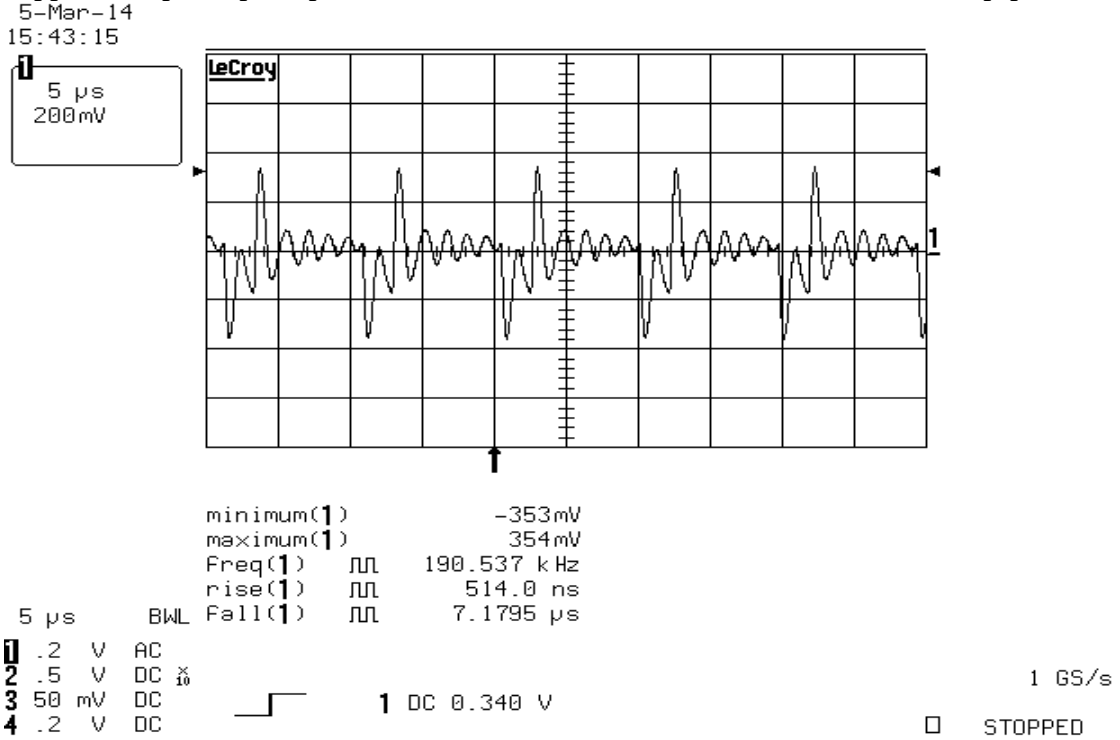
Qq

Start up with Enable at 24Vin: model t1 shown, model t2 same with 30msec rise



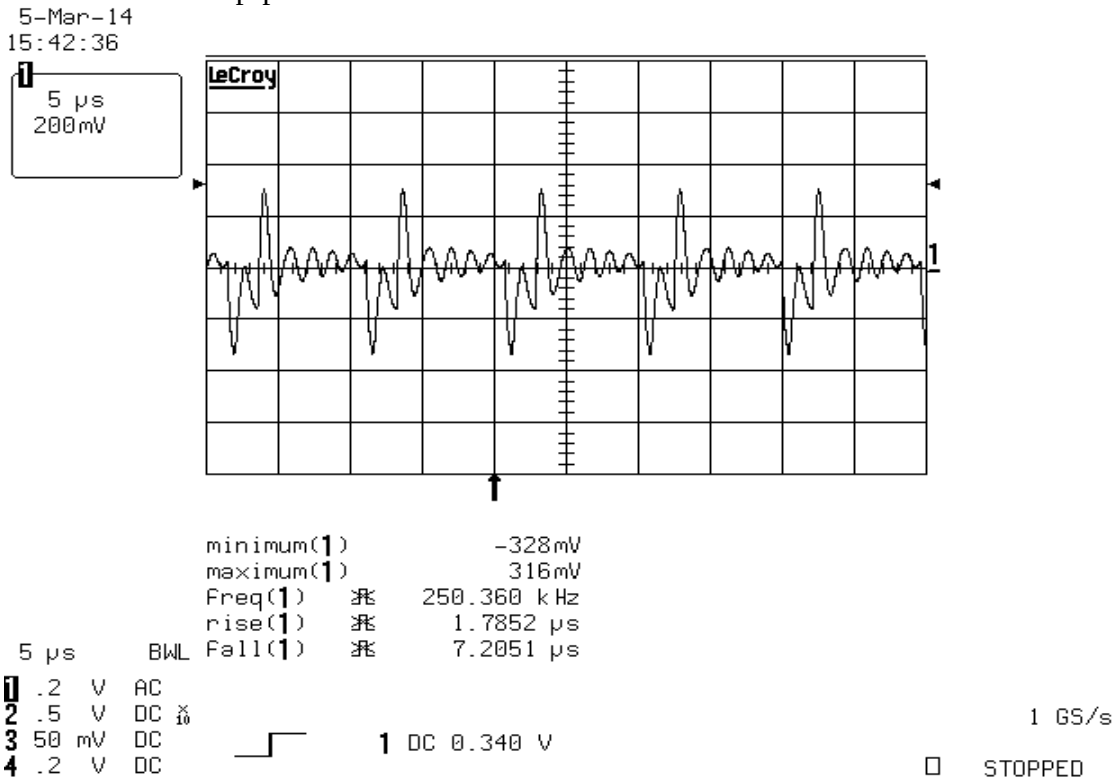
Qq

Ripple on input caps to power trains at full load and 24Vin:C4 first: 707mV p-p: model t1



Q

Then C8: 644mV p-p: also model t1 same conditions



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