User's Guide
SLVUAF0–May 2016

Build a High-Density, High-Refresh Rate, Multiplexing Panel With the TLC5957

This application report describes how to build high-density, high refresh rate, multiplexing panel with the TLC5957; a 48 channel, 16-bit ES-PWM LED driver with pre-charge FET, LED open detection and caterpillar cancelling.

Contents

List of Figures

List of Tables

1 Introduction

The TLC5957 device is a 48-channel, constant-current sink driver. Each channel has an individually-adjustable, 65536-step, pulse-width modulation (PWM) grayscale (GS) brightness control.

The output channels are divided into three groups, each group has a 512-step color brightness control (CC). CC adjusts brightness control between colors. The maximum current value of all 48 channels can be set with the 8-step global brightness control (BC). BC adjusts brightness deviation between LED drivers. GS, CC, and BC data are accessible via a serial interface port.

The TLC5957 has one error flag: LED open detection (LOD), which can be read via a serial interface port. Each constant-current has a pre-charge field-effect transistor (FET), which can reduce ghosting and improve display performance on the multiplexing LED display. The TLC5957 also has an enhanced circuit, it can cancel the caterpillar issue caused by LED open.

The TLC5957 has a poker transmission mode, the length of the PWM bit can be configured flexible in this mode, from 9 bit to 16 bit, according to the application environment.

The TLC5957 has the following features:

- 48 channel, constant-current sink output
- Low Gray Scale Enhancement (LGSE™) technology
- Sink current capability with maximum BC/CC data:
  - 25 mA at 5 V_{CC}
  - 20 mA at 3.3 V_{CC}
- Global brightness control (BC) : 3-bit (8 Step)
- Color control (CC) for each color
  Group: 9-bit (512 step), three groups
- Gray Scale (GS) control with Multiplexed Enhanced Spectrum (ES) PWM: 16 bit
- Knee voltage VOUT = 0.24 V at 10 mA
- LED power-supply voltage up to 10 V
- V_{CC} = 3.0 V to 5.5 V
- Constant current accuracy
  - Channel to Channel = ±1% (Typ), ±3% (Max)
  - Device to Device = ±1% (Typ), ±3% (Max)
- Data transfer rate: 33 MHz
- Gray Scale clock: 33MHz
- LED Open Detection (LOD)
- Thermal Shut Down (TSD)
- I_{REF} Resistor Short Protection (ISP)
- PWM Bit Selectable (9 bit to 16 bit)
- Traditional PWM and ES-PWM
- Grouped delay to prevent inrush current
- Auto display repeat/Auto data refresh
- Enhanced circuit for caterpillar cancelling
- Pre-charge FET to avoid ghosting phenomenon
- Operating temperature : -40°C to +85°C

The TLC5957 is mainly targeted for the following applications:

- LED video displays
- LED signboards

Figure 1 is a typical application circuit of TLC5957.

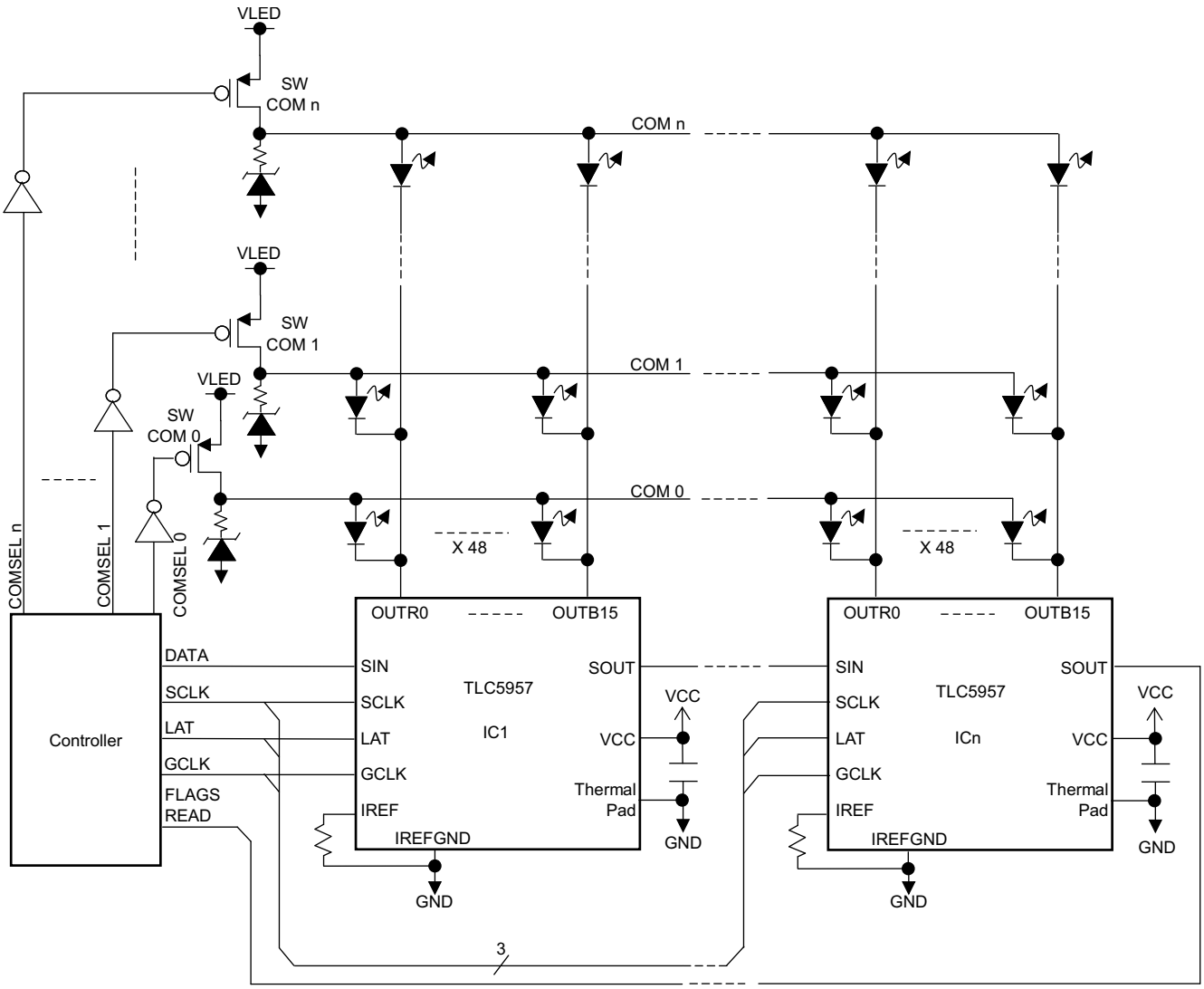


Figure 1. Typical Application Circuit (Multiple Daisy-Chained TLC5957s)

2 Device Specification

2.1 Basic Information

Basic information, such as electrical characteristics, thermal, package information, and recommended operation conditions, are found in the datasheet (SLVSCQ4).

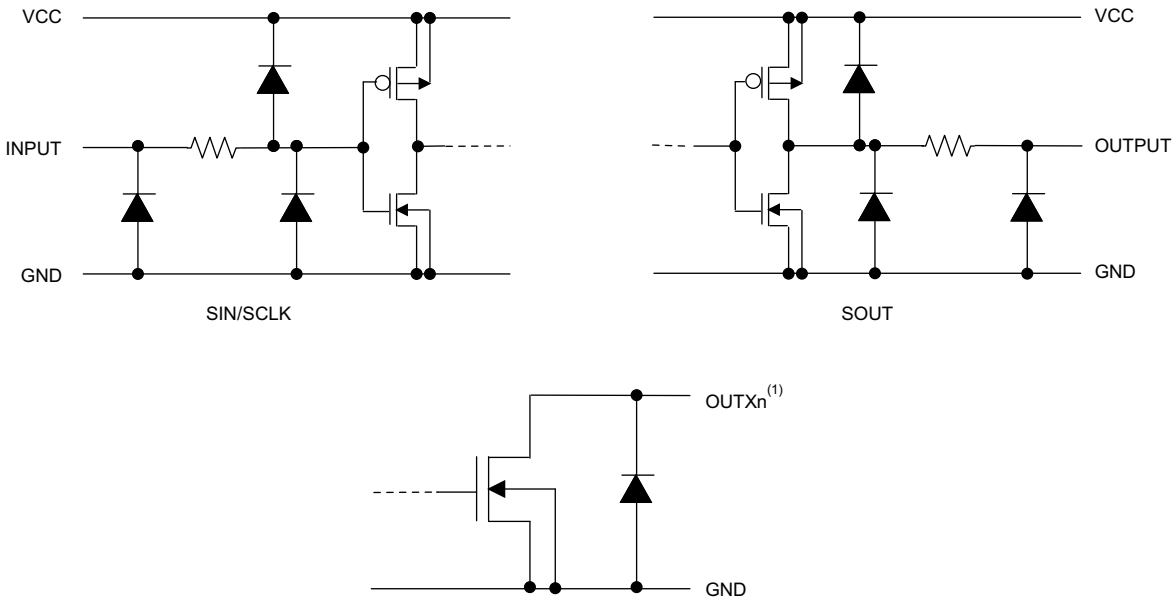
The TLC5957 functional block diagram, pin-out information, and pin description are also in the datasheet (SLVSCQ4).

2.2 Switching Characteristics

At V_{CC} = 3.0−5.5 V, T_A = −40°C to 85°C, C_L = 15 pF, R_L = 4 kΩ, target at 1-mA I_{OLC}, V_{LED} = 5.0 V, Typical values are at V_{CC} = 3.3 V, T_A = 25°C (unless otherwise noted).

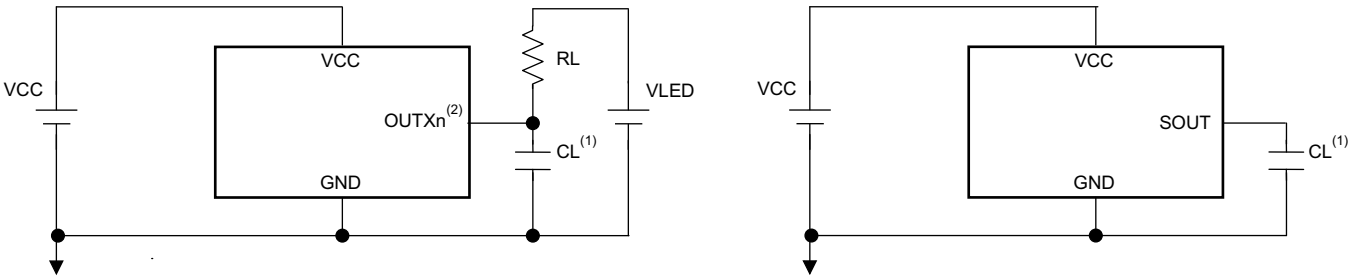
Parameter		Test Conditions		MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SOUT			2	5	ns
t_{R1}		OUTx0-15, x = R/G/B, BC = 7h, CCR/G/B = 1FFh, R_{IREF} = 7.41 kΩ (25-mA target), T_A = +25°C, R_L = 160 Ω			40		ns
t_{F0}	Fall time	SOUT			2	5	ns
t_{F1}		OUTx0-15, x = R/G/B, BC = 4h, CCR/G/B = 1FFh, R_{IREF} = 12 kΩ (10-mA target), T_A = +25°C, R_L = 400 Ω			16		ns
t_{D0}	Propagation delay time	SCLK ↑ to SOUT, SEL_TD0 = 00b			16		ns
		SCLK ↑ to SOUT, SEL_TD0 = 01b			19		ns
		SCLK ↑ to SOUT, SEL_TD0 = 10b			22		ns
		SCLK↓to SOUT, SEL_TD0 = 11b			16		ns
t_{D1}		LAT↓ to SOUT, ReadFC, ReadSID			80		ns
t_{D2}		GCLK↓ to OUTR0/7/8/15 turn on or turn off	R_{IREF} = 7.41 kΩ (25-mA target), BC = 7h, CCR/G/B = 1FFh, T_A = +25°C, SEL_GDLY = 1		30		ns
t_{D3}		Propagation delay time between group and next group (OUTR0/7/8/15 turn-on/off to OUTR1/6/9/14 turn-on/off; OUTR1/6/9/14 turn-on/off to OUTR2/5/10/13 turn-on/off; OUTR2/5/10/13 turn-on/off to OUTR3/4/11/12 turn-on/off)			5		ns
t_{D4}		Propagation delay time between color and next color in same group (OUTRx turn-on/off to OUTGx turn-on/off; OUTGx turn-on/off to OUTBx turn-on/off, x = 0 ≈ 15)			1.67		ns

2.3 Parameter Measurement Information



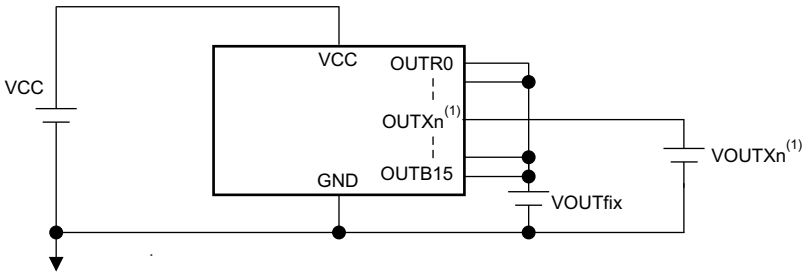
(1) X = R or G or B, n = 0–15

Figure 2. Pin Schematic Diagrams



(1) C_L includes measurement probe and Jig capacitance.

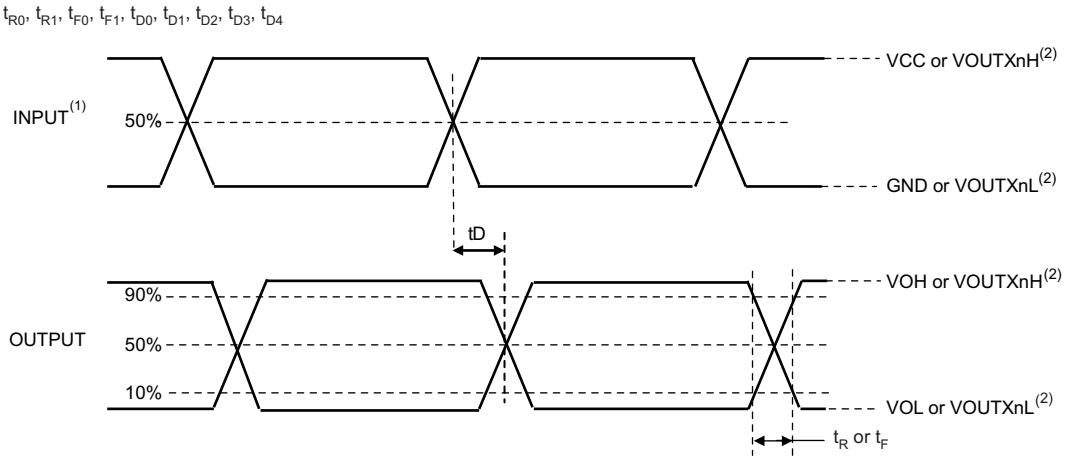
Figure 3. Rise Time and Fall Time Test Circuit



(1) X = R or G or B, n = 0–15

Figure 4. Constant Current Test Circuit for OUTXn

2.4 Timing Diagrams



(1) Input pulse rise and fall time is 1–3 ns

(2) X = R or G or B, n = 0–15

Figure 5. Output Timing

3 Detailed Description

3.1 How to Use TLC5957

After power on, all OUTXn of TLC5957 are turned off. All internal counters and function control registers are initialized. A brief summary of sequences is provided in the following list providing a general introduction to how this part works. After that, the function block related to each step is detailed in the following sections.

1. According to maximum LED current target, choose BC and CC code, then select the current programming resistor R_{IREF}.
2. Send FCWRTEN and WRTFC command to set FC register value. (see Section 3.3)
3. Write GS data of line 1 into GS data latch. Using the LATGS command for the last group of 48-bit GS data loading, the GS data just written is now displayed.
4. Input GCLK continuously, 2^N GCLK (N ≥ 9) as a segment. Between the interval of two segments, supply voltage should be switched from one line to next line accordingly.
5. During the same period of step 4, GS data for next line should be written into GS data latch. Using LATGS command for loading 48-bit GS data.
6. Repeat steps 4–5 until it comes to the last line for a multiplexing panel. Input 2^N GCLK (N ≥ 9) as a segment, at the same time, GS data for the 1st line should be written into the GS data latch. Using LINRESET command for the 48-bit GS data loading in last line.

Repeat step 4–6…

3.2 Step 1: Choose BC and CC, Select R_{IREF}

3.2.1 What is the BC Function?

The TLC5957 is able to adjust the output current of all constant-current outputs simultaneously. This function is called *global brightness control* (BC). The global BC for all outputs is programmed with a 3-bit word, thus all output currents can be adjusted in 8 steps from 12.9% to 100% (see Table 2) for a given current programming resistor (R_{IREF}).

BC data can be set via the serial interface. When the BC data change, the output current also changes immediately. When the device is powered on, the BC data in the function control (FC) register is set to 4h as the default value.

3.2.2 What is the CC Function?

The TLC5957 is able to adjust the output current of each of the three color groups OUTR0-OUTR15, OUTG0-OUTG15, and OUTB0-OUTB15 separately. This function is called color brightness control (CC). For each color, it has a 9-bit data latch CCR, CCG, or CCB in FC register (see Table 4 for FC register bit assignment). Thus, all color group output currents can be adjusted in 512 steps from 0% to 100% of the maximum output current, I_{OLCMax}. (See Section 3.2.3 for more detail about I_{OLCMax}.) The CC data can be changed via the serial interface.

When the CC data changes, the output current also changes immediately.

When the IC is powered on, the CC data are set to '100h'.

Equation 1 calculates the actual output current.

$$Iout(mA) = IO_{LCMax}(mA) \times (CCR/511d \text{ or } CCG/511d \text{ or } CCB/511d) \quad (1)$$

Where:

I_{OLCMax} = the maximum channel current for each channel determined by BC data and R_{IREF}
CCR/G/B = the color brightness control value for each color group in the FC register (000h to 1FFh)

Table 1 shows the CC data versus the constant-current against I_{OLCMax}.

Table 1. CC Data vs Current Ratio and Set Current Value

CC Data (CCR or CCG or CCB)			Ratio of Output Current to I_{OLCMax} (%, typical)	Output Current (mA, R_{IREF} = 7.41kΩ)	
Binary	Decimal	Hex		BC = 7h (I_{OLCMax} = 25 mA)	BC = 0h (I_{OLCMax} = 3.2 mA)
0 0000 0000	0	00	0	0	0
0 0000 0001	1	01	0.2	0.05	0.006
0 0000 0010	2	02	0.4	0.1	0.013
—	—	—	—	—	—
1 0000 0000 (Default)	250 (Default)	100 (Default)	50.1	12.52	1.621
—	—	—	—	—	—
1 1111 1101	509	1FD	99.6	24.90	3.222
1 1111 1110	510	1FE	99.8	24.95	3.229
1 1111 1111	511	1FF	100	25	3.235

3.2.3 How to Select R_{IREF} for a Given BC

The maximum output current per channel, I_{OLCMax}, is decided by a resistor, R_{IREF}, which is placed between the IREF and IREFGND pins, and the BC code in FC register (See Table 4 for FC register bit assignment.) The voltage on I_{REF} is typically 1.2 V. R_{IREF} can be calculated with Equation 2.

$$R_{IREF}(k\Omega) = V_{IREF}(V) / I_{OLCMax}(mA) \times Gain \quad (2)$$

Where:

V_{IREF} = the internal reference voltage on IREF (1.20 V, typical)
I_{OLCMax} is the largest current for each output at CCR/G/B = 1FFh.
Gain = the current gain at a selected BC code (see Table 2)

Table 2. Current Gain vs BC Code(1)

BC Data		Gain	Ratio of Gain/Gain_max (at Max BC)
Binary	Hex		
000 (recommend)	0 (recommend)	20.0	12.90%
1	1	39.5	25.60%
10	2	58.6	37.90%
11	3	80.9	52.40%
100 (default)	4 (default)	100.0	64.70%
101	5	113.3	73.30%
110	6	141.6	91.70%
111	7	154.5	100%

(1) TI recommends using smaller BC code for better performance. For noise immunity purpose, TI suggests R_{IREF} < 60 kΩ.

3.2.4 How to Choose BC/CC for Different Application

BC is mainly used for global brightness adjustment between day and night. Suggested BC is 4h, which is in the middle of the range, thus, one can change brightness up and down flexibly.

CC can be used to fine tune the brightness in 512 steps, this is suitable for white balance adjustment between RGB color group. To get a pure white color, the general requirement for the luminous intensity ratio of R, G, B LED is 3:6:1. Depending on LED's characteristics (Electro-Optical conversion efficiency), the current ratio of R, G, B LED is much different from this ratio. Usually, the Red LED will need the largest current. One can choose 511d(the max value) CC code for the color group which need the largest current at first, then choose proper CC code for the other two color groups according to the current ratio requirement of the LED used

3.2.4.1 Example 1: Red LED Current is 20 mA, Green LED needs 12 mA, Blue LED Needs 8 mA

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 × 12 mA / 20 mA = 306.6, thus choose 307d for CCG. With same method, choose 204d for CCB.
3. According to the required Red LED current, choose 7h for BC.
4. According to Equation 2, R_{IREF} = 1.2 V / 20 mA × 154.5 = 9.27 kΩ

In this example, we choose 7h for BC, instead of using the default 4h. This is because the Red LED current is 20 mA, which is approaching the upper limit of current range. To prevent the constant output current from exceeding the upper limit in case a larger BC code is input accidently, we choose the max BC code here.

3.2.4.2 Example 2: Red LED Current is 5 mA, Green LED Needs 2 mA, Blue LED Needs 1 mA

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 x 2 mA / 5 mA = 204.4, thus choose 204d for CCG. With same method, choose 102d for CCB.
3. According to the required Blue LED current, choose 0h for BC.
4. According to Equation 2, R_{IREF} = 1.2 V / 5 mA x 20 = 4.8 kΩ

In this example, we choose 0h for BC, instead of using the default 4h. This is because the Blue LED current is 1 mA, which is approaching the lower limit of current range. To prevent the constant output current from exceeding the lower limit in case a lower BC code is input accidently, we choose the min BC code here.

In general, if LED current is in the middle of range(that is, 10 mA), one can just use the default 4h as BC code.

3.3 Step 2: Write Function Control Register FC

3.3.1 Input Data for FC through Common Shift Register

The common shift register is 48-bits long and is used to shift data from the SIN pin into the TLC5957. The data shifted into the register can be latched into the 1st GS data latch, or latched into function control (FC) register which depends on input pattern.

Figure 6 shows the configuration of the common shift register and the data latches.

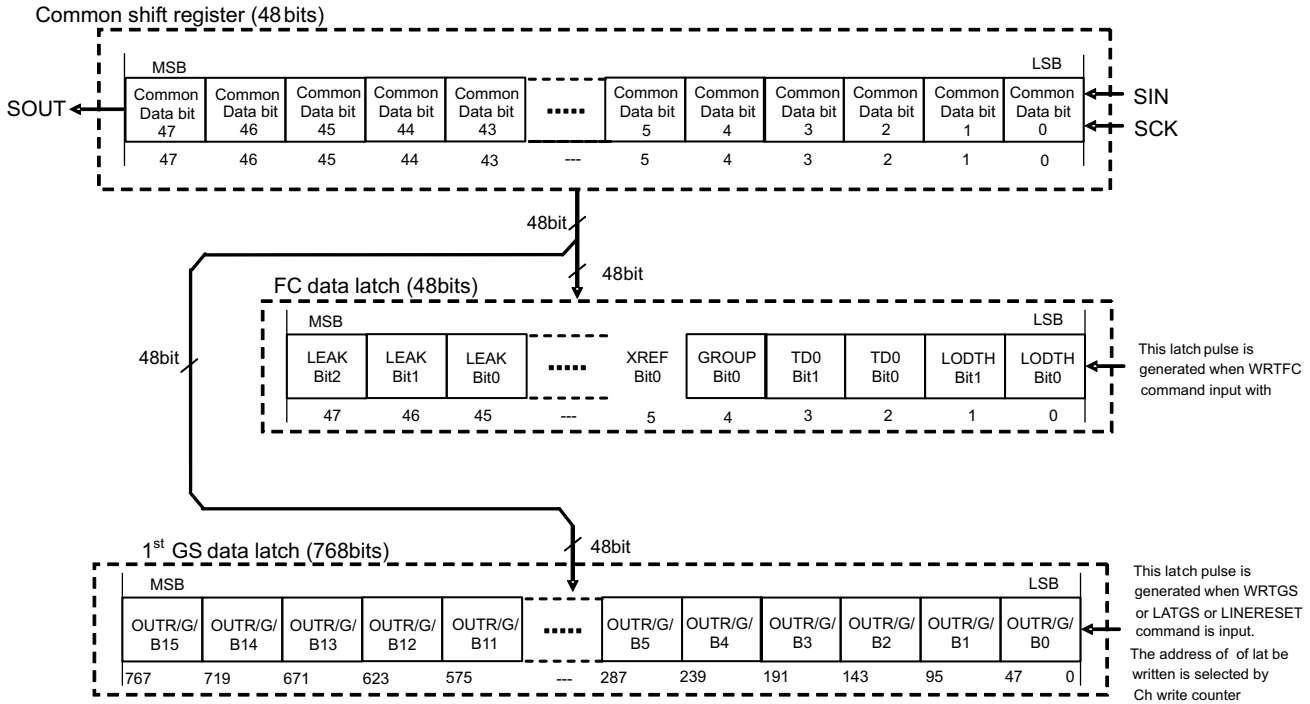


Figure 6. Common Shift Register and Data Latch Configuration

The LSB of the common shift register is connected to SIN and the MSB is connected to SOUT. On each rising edge of SCLK, the data on SIN are shifted into the LSB and all 48 bits are shifted towards the MSB. The register MSB is always connected to SOUT.

When the device is powered on, all 48 bits of the common shift register are set to '0'.

3.3.2 How to Write to the Function Control Register

TLC5957 use commands FCWRTEN and WRTFC to latch the data of the common shift register into the FC register. These commands are distinguished by the number of SCLK rising edge included in the LAT pulse. Table 3 describes these two commands.

Table 3. WRTFC/FCWRTEN Commands Description

Command Name	SCLK Rising Edges While LAT IS High	Description
WRTFC (FC data write)	5	The 48-bit data in common shift register are copied to the FC register if input after FCWRTEN command. Refer to Figure 7 for a timing diagram of this command operation.
FCWRTEN (FC write enable)	15	FC writes are enabled with this command. This command must always be input before the FC data write occurs. Refer to Figure 7 for a timing diagram of this command operation.

Note that FCWRTEN command must be input before inputting WRTFC command, otherwise this WRTFC command is neglected.

Refer to Figure 7 for detailed command input timing diagram.

3.3.3 Function Control (FC) Register

FC is used to select BC/CC code, group delay, low grayscale enhancement feature, and other special function features of the TLC5957.

Table 4 shows the FC register bit assignment.

Table 4. FC Register Bit Assignment

Bit		Default Value (binary)	Description
Number	Name		
1 – 0	LODVTH	01b	LOD detection threshold voltage. These two bits select the detection threshold voltage for the LED open detection (LOD). Table 5 shows the detect voltage truth table.
3 – 2	SEL_TD0	01b	TD0 select. SOUT hold time is decided by TD0 definition and selection. Table 6 shows the detail.
4	SEL_GDLY	1b	Group delay select. When this bit is '0', no delay between channels. All channels turn on at same time. When this bit is '1', channels turn on with different delay time, thus the inrush current is minimized. See Table 6 for more detail.
5	XREFRESH	0b	Auto data refresh mode bit. (0 = enabled, 1 = disabled) If LATGS/LINERESET command is input while this bit is '0', auto data refresh mode is enabled. All data in the 1st GS DATA latch are copied to the second GS DATA latch until GS counter reaches the maximum count value of 65,536. No OUTn are forced off and GS counter continues counting. If LATGS/LINERESET command is input while this bit is '1', all data in the 1st GS DATA latch are copied to the second GS DATA latch. All OUTn are forced off and GS counter is reset to "0". Refer to Figure 10 for detailed timing.
6	SEL_GCK_EDGE	0b	GCLK edge select. When this bit is '0', OUTn only turns on/off at the rising edge of GCLK, this is the default setting; When this bit is '1', OUTn turn on/off at both edges (rising and falling) of GCLK. At this condition, the maximum input GCLK is 16.5 MHz.
7	SEL_PCHG	0b	Pre-charge working mode select. When this bit is '0': After power on, Pre-charge FET is enabled. When the 1st GCLK input, the pre-charge FET state depends on the GS data. If GS = 0, then the pre-charge FET will always keep on. If GS > 0, the pre-charge FET is turned off, and will be turned on again once the output channel is turned off. This means the Pre-charge FET will only remain off during the period in which the channel is on. When this bit is '1' : After power on, Pre-charge FET is enabled. When the 1st GCLK input, Pre-charge FET is turn off and remains off until the GS counter is reset to 0. Once GS counter = '0', pre-charge FET is turned on again. This means the pre-charge FET is kept off during the whole segment period, and remains on during the dead-time (the time between two adjacent segments). See Figure 27 for more detail.
8	ESPWM	0b	ESPWM mode enable bit. (0 = enabled, 1 = disabled) When this bit is '0', the conventional PWM control mode is selected. When this bit is '1', the ES-PWM control mode is selected. If using poker trans mode, this bit has to be set to '1'. See Section 3.5.3 "Multiplexed Enhanced Spectrum(ES) PWM Control" for more detail.
9	LGSE3	0b	Compensation for Blue LED. (0 = disabled, 1 = enabled) When this bit is '0', no compensation for Blue LED. When this bit is '1', internal circuit is enabled for Blue LED compensation.

Table 4. FC Register Bit Assignment (continued)

Bit		Default Value (binary)	Description
Number	Name		
10	SEL_SCK_EDGE	0b	SCLK edge select. When this bit is '0', the GS data at the SIN pin shifts to the common shift register only at the rising edge of SCLK, this is the default setting; When this bit is '1', the GS data at the SIN pin shifts to the common shift register at both edges (rising and falling) of SCLK. At this condition, the maximum input SCLK is 18 MHz. FC (function control) data can only shift at the rising edge of SCLK. See Section 3.13 "Double Edge for data transmission" for more detail.
13 – 11	LGSE1	000b	Low Gray Scale Enhancement for Red/Green/Blue color, can be used to solve the 1st line issue commonly happens in high density, multiplexing panel, also is helpful for the white balance at low grayscale condition. It functions as shown in the following: 000b — no enhancement 001b — weak enhancement 100b — medium enhancement 111b — strong enhancement
22 – 14	CCB	1 0000 0000b	Color brightness control data for Blue color group (Data = 000h-1FFh. See Table 1)
31 – 23	CCG	1 0000 0000b	Color brightness control data for Green color group (Data = 000h-1FFh. See Table 1)
40 – 32	CCR	1 0000 0000b	Color brightness control data for Red color group (Data = 000h-1FFh. See Table 1)
43 – 41	BC	100b	Global brightness control data for all output (Data = 0h- 7h. See Table 2)
44	Poker trans mode	0b	Poker trans mode enable bit. (0 = disabled, 1 = enabled) When this bit is '0', traditional GS trans mode is enabled, PWM bit is 16, need to transfer 16-bit GS data for each OUTn. When this bit is '1', poker GS trans mode enabled, PWM can be configured from 9 bit to 16 bit. Transfer corresponding GS data for each PWM mode. See Section 3.4.3 "Poker trans mode for GS data" for more detail.
47 – 45	LGSE2	000b	Besides LGSE1, these three bits are designed for the first line performance improvement at low grayscale condition. 000b — no improvement 001b — weak improvement 101b — medium improvement 111b — strong improvement

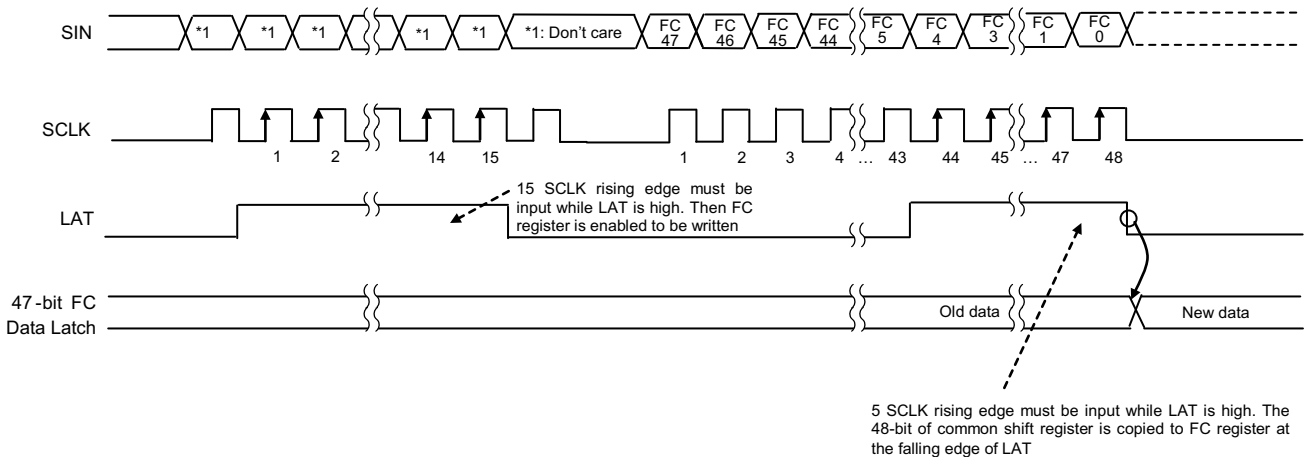


Figure 7. FC Write Enable (FCWRTEN) and FC Data Write (WRTFC) Command

Table 5. LOD Threshold Voltage Truth Table

LODVTH		LED Open Detection (LOD)Threshold Voltage
Bit1	Bit0	
0	0	VLOD0 (0.09 V typ)
0	1	VLOD1 (0.19 V typ, Default value)
1	0	VLOD2 (0.35 V typ)
1	1	VLOD3 (0.50 V typ)

Table 6. TD0 Definition and Selection

SEL_TD0		TD0 Definition and Selection	
Bit3	Bit2	FC BIT10 = 0	FC BIT10 = 1
0	0	TD0 is the time from SCLK↑ to SOUT↑↓, typical value is 18 ns. Once received, SCLK↑, with 18-ns delay, SOUT begins change.	TD0 is the time from SCLK↑↓ to SOUT↑↓, typical value is 18 ns. Once received, SCLK↑↓, with 18-ns delay, SOUT begins change.
0	1	TD0 is the time from SCLK↑ to SOUT↑↓, typical value is 21 ns. Once received, SCLK↑, with 21-ns delay, SOUT begins change.(default value when power up)	TD0 is the time from SCLK↑↓ to SOUT↑↓, typical value is 21 ns. Once received, SCLK↑↓, with 21-ns delay, SOUT begins change.(default value when power up)
1	0	TD0 is the time from SCLK↑ to SOUT↑↓, typical value is 24 ns. Once received, SCLK↑, with 24-ns delay, SOUT begins change.	TD0 is the time from SCLK↑↓ to SOUT↑↓, typical value is 24 ns. Once received SCLK↑↓, with 24ns-delay, SOUT begins change.
1	1	TD0 is the time from SCLK↓ to SOUT↑↓, typical value is 12 ns. Once received, SCLK↓, with 17ns-delay, SOUT begins change. One can adjust the hold time from SCLK↑ to SOUT↑↓ by changing the duty of SCLK	N/A

Table 7. Group Delay when SEL_GDLY = 1

Output Pins	Delay Time From GCLK↑ to Output Channel Turn On/Off (ns)
OUTR0/7/8/15	tD2
OUTG0/7/8/15	tD2 + 1.67
OUTB0/7/8/15	tD2 + 3.34
OUTR1/6/9/14	tD2 + 5
OUTG1/6/9/14	tD2 + 5 + 1.67
OUTB1/6/9/14	tD2 + 5 + 3.34
OUTR2/5/10/13	tD2 + 10
OUTG2/5/10/13	tD2 + 10 + 1.67
OUTB2/5/10/13	tD2 + 10 + 3.34
OUTR3/4/11/12	tD2 + 15
OUTG3/4/11/12	tD2 + 15 + 1.67
OUTB3/4/11/12	tD2 + 15 + 3.34

3.4 Step 3: Write GS Data into GS Data Latch

3.4.1 Overview of GS Data Latch

The TLC5957 has one common register, one function control (FC) data latch, and two GS data latches: 1st GS data latch and second GS data latch. A common shift register is 48-bits long, LSB is connected with the SIN pin, and MSB is connecting with SOUT. The 1st GS data latch is a 768-bit register, it stores the new updated GS data. The second GS data latch is 768-bits long, and controls the on-time of all constant current outputs. Figure 8 shows the structure of common shift register and GS data latch.

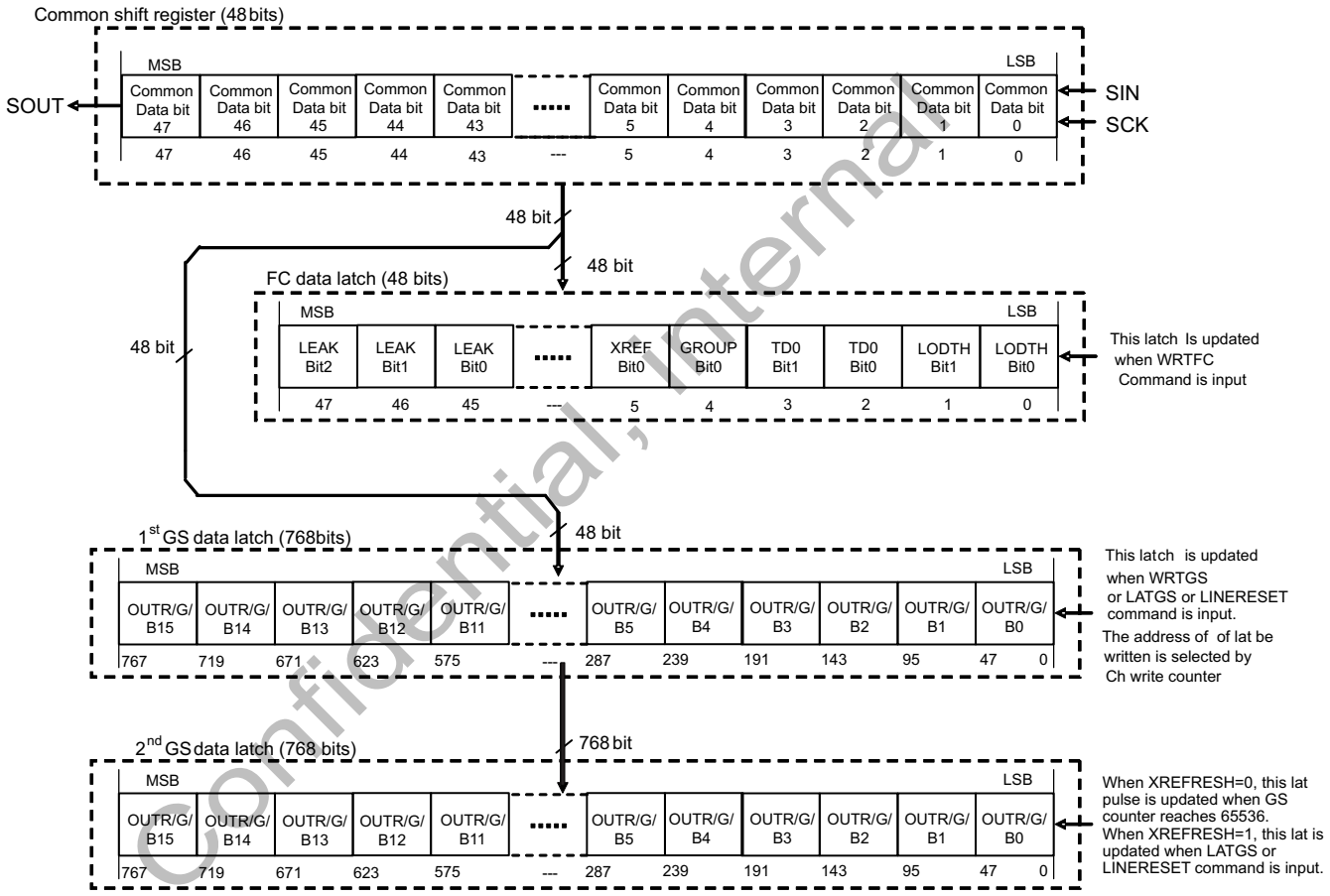


Figure 8. Shift Register and Data Latch Structure

3.4.2 How to Write GS DATA in Traditional Trans Mode

The TLC5957 uses the WRTGS and LATGS commands to latch the data of the common shift register into the 1st and second GS data latch. These commands are distinguished by the number of SCLK rising edges included in the LAT pulse. Table 8 describes more about these two commands.

Table 8. WRTGS/LATGS Commands Description

Command Name	SCLK Rising Edges While LAT is High	Description
WRTGS (48-bit GS data write)	1	The 48-bit data in the common shift register are copied to the 48-bit GS latch in the first latch selected by the GS data latch address counter. Refer to Figure 9 for a timing diagram of this command operation.
LATGS (768-bit GS data latch)	3	The 48-bit data in the common shift register are copied to the corresponding 48-bit GS data latch in the first latch. All data in first data latch are copied to the 2nd GS data latch when the GS counter reaches 65536, if XREFRESH = 0; All data in the 1st data latch are also copied to the 2nd GS data latch, GS counter reset, and all OUTx are forced off if XREFRESH = 1. Refer to Figure 10 for a timing diagram of this command operation.

If the WRTGS command is received, all 48-bit data in the common shift register are copied to the 48-bit GS latch in the first GS data latch, which is selected by the GS data latch address counter.

When the LATGS command is received, if XREFRESH = 0, the LATGS command is the same with WRTGS, all 48-bit data in the common shift register are copied to the 1st GS data latch, the 1st data latch are copied to the second GS data latch when the GS counter reaches 65536. If XREFRESH in FC register = 1, all 48-bit data in common shift register are copied to the 1st GS data latch. Besides, all data in the 1st data latch are copied to the second GS data latch, GS counter reset, and all OUTx are forced off.

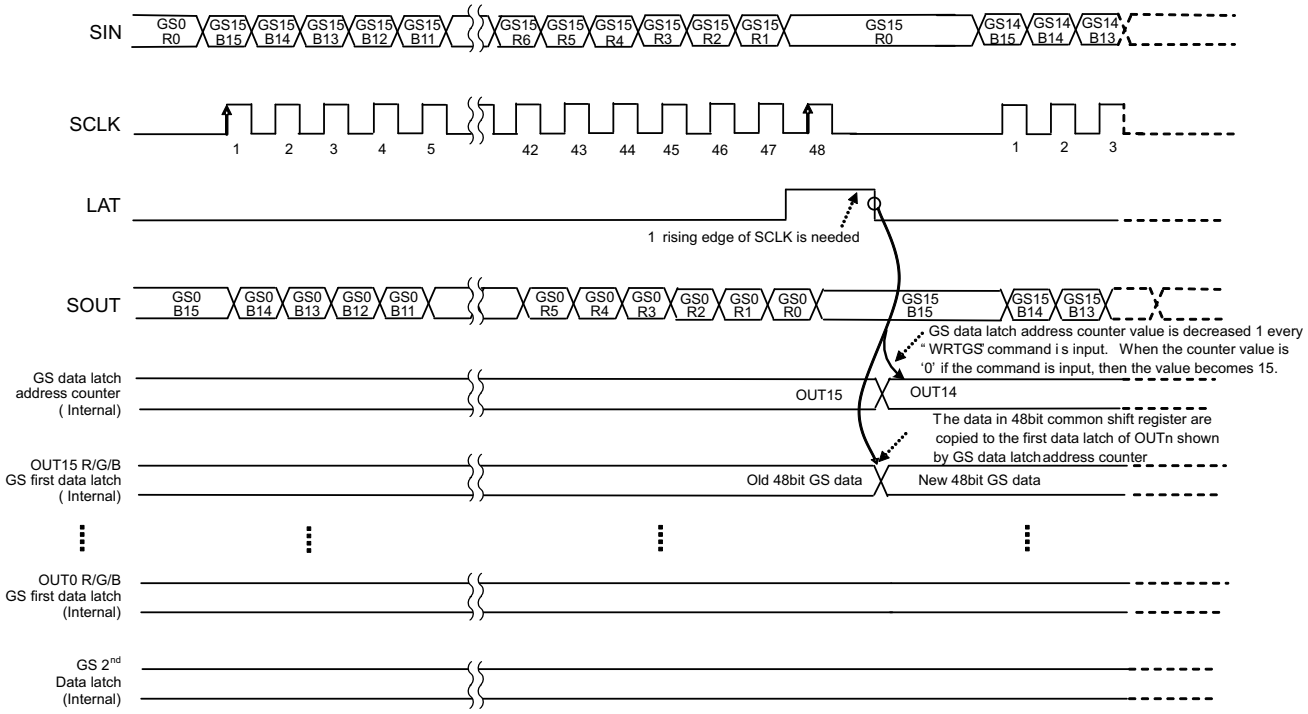


Figure 9. 48-Bit GS Data Write (WRTGS) Command in Traditional Trans Mode

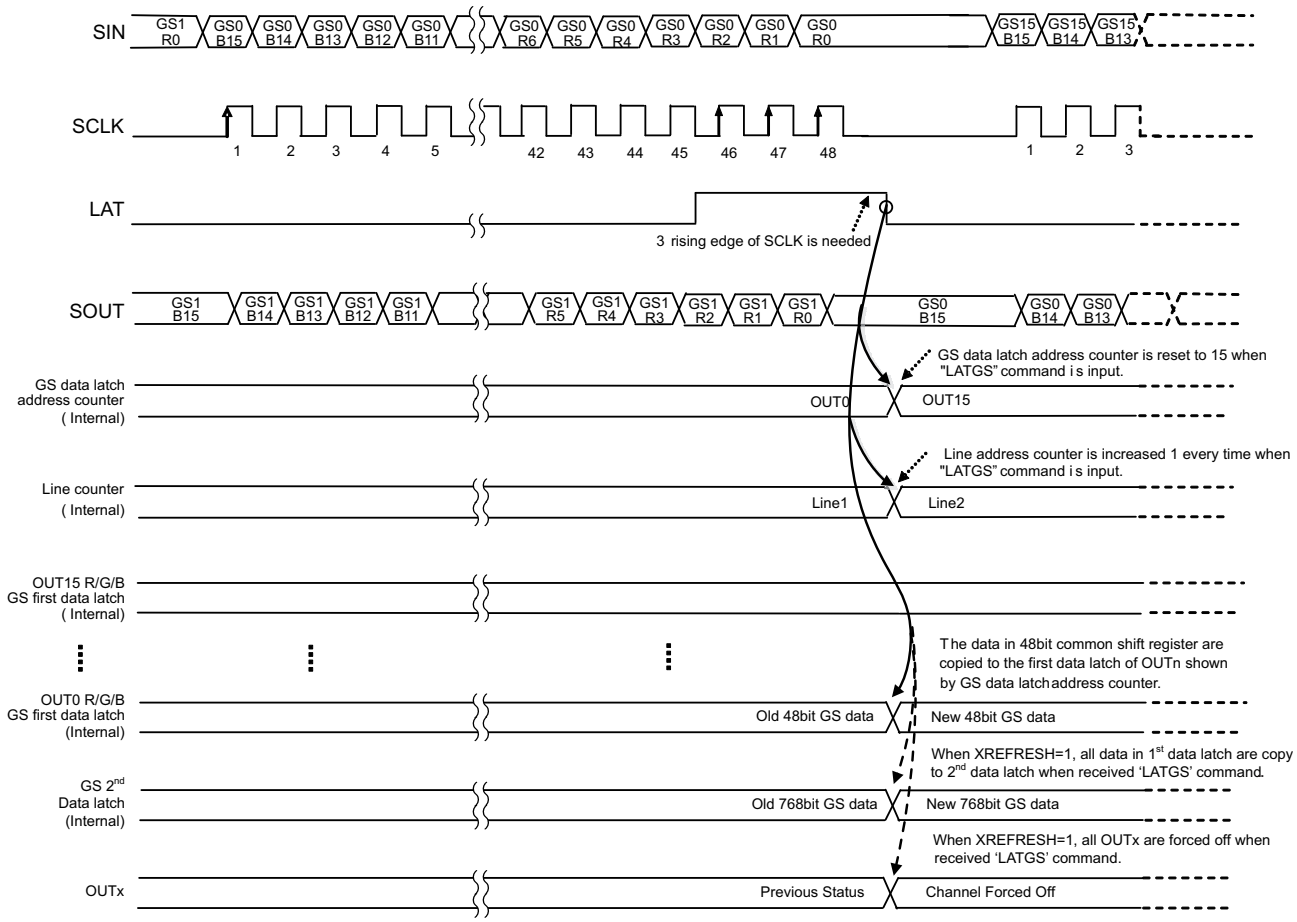


Figure 10. 768-Bit GS Data Latch (LATGS) Command in Traditional Trans Mode

After power on, the GS data address counter, line counter, and all GS data latches are reset to default values.

GS data address counter default value is 15, meaning it should send GS data for OUT15 first, including OUT15R, OUT15G, OUT15B, totaling 48 bits. The sending sequence is from MSB to LSB, from Blue color to Green color, and finally, Red color.

After sending the series of WRTGS commands for OUT15, the GS data address counter decreases by 1, first GS data latch for OUT15 will be updated.

Then, GS data for OUT14 should be written after OUT15, another series of WRTGS commands are input.

After all 15 WRTGS command series are input, the LATGS command should be input for the whole GS data latch.

After LATGS command input, GS data address counter resets to 15, the line counter increases by 1. At the same time, the first GS data latch for OUT0 is updated. If XREFRESH = 1, all data in GS first latch will copy to GS second latch, and all OUTx are forced off.

See Figure 11 for this timing diagram.

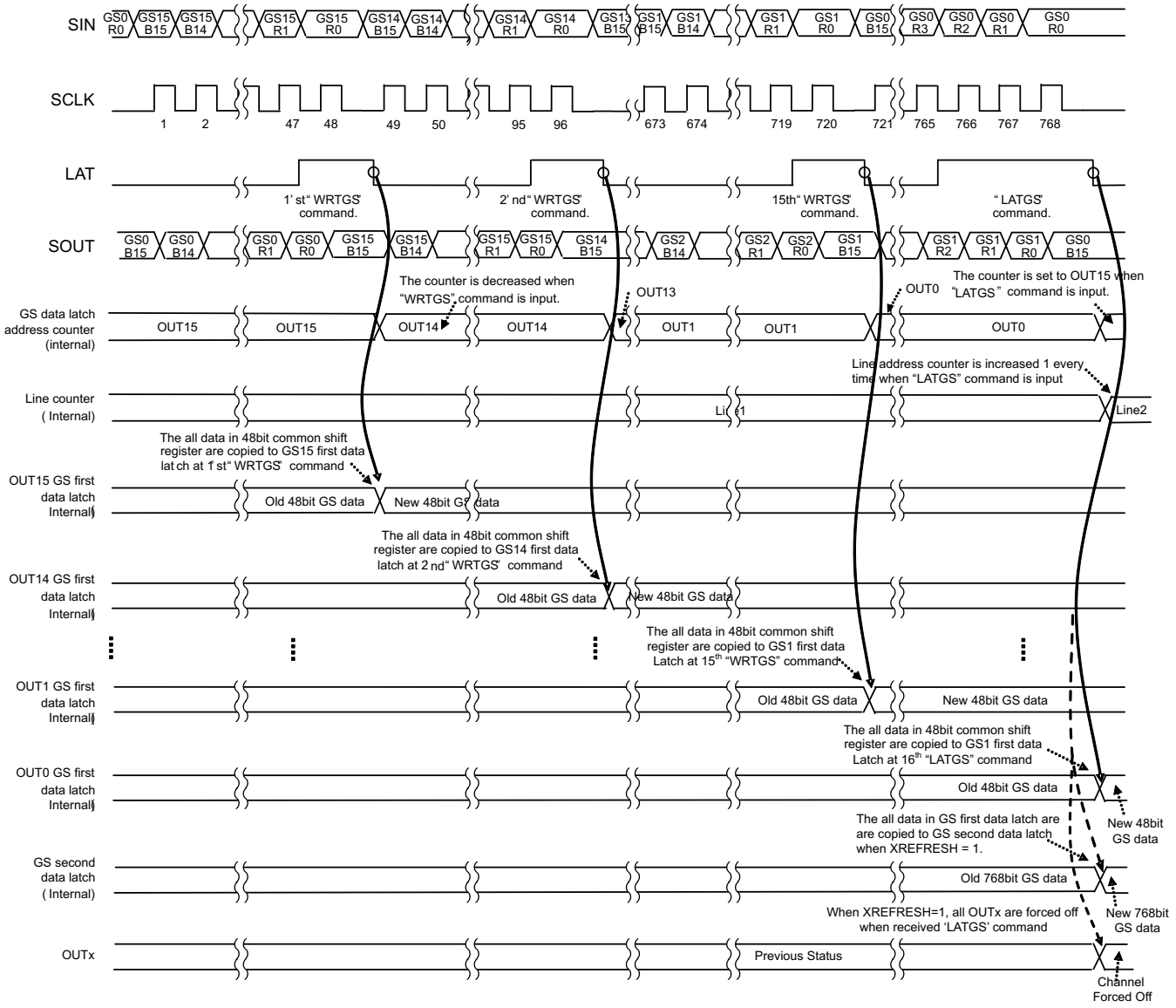


Figure 11. 768-Bit GS Data Write Sequence (15 times of "WRTGS" + 1 times of "LATGS" command)

3.4.3 Poker Mode for GS Data

In some applications, especially when used in high-multiplexing, 16-bit GS data is not necessary. With poker trans mode, the TLC5957 can flexibly configure the PWM bit of GS data, from 9 bits to 16 bits. Unlike traditional transmission mode in Section 3.4.2, Poker mode is a new data transmission mode which trans GS data by byte. When bit 44 in the FC register = 1, poker transmission mode is selected. Notice, if poker mode is chosen, ES-PWM in FC bit 9 and XREFRESH in FC bit 5 should also be 1.

A comparison between traditional GS data trans mode and poker GS data trans mode is illustrated in Figure 12. When bit 44 in FC register = 0, traditional GS data trans mode is selected. In traditional trans mode, GS data are sent by OUTx group. One group consists of 48 bits. For each OUTx group, send Blue color first, Green color second, and the Red color last. For each color, MSB should be sent first, LSB the last.

When bit 44 in FC register = 1, poker GS data trans mode is selected. In poker trans mode, GS data are sent by BIT group. Each BIT group consists of 48-bit data, from OUT15B, OUT15G, OUT15R, to OUT0B, OUT0G, OUT0R. Also, bit of OUT15 should be sent first, and same bit of OUT0 the last.

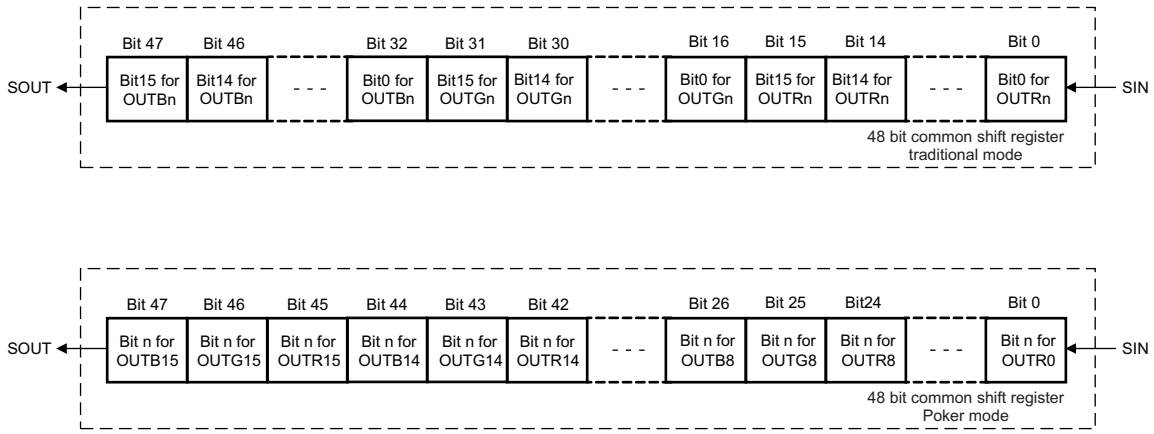


Figure 12. Traditional Mode vs Poker Mode Register

In poker mode, the length of the PWM bit has a flexible configuration, from 9 bits to 16 bits. It depends on how many WRTGS and LATGS commands you have sent. For example, if the PWM bit = 10, it means Tperiod is 1024 GCLK, 9 WRTGS and 1 LATGS should be sent. The 1st WRTGS for GS bit 9, second WRTGS for GS bit 8, third WRTGS for GS bit 7…, the last LATGS command for GS bit 0. Table 9 describes more about these configurations.

Table 9. PWM Bit Length Configure

PWM Bit	Command	Description
9 bit	8 WRTGS + 1 LATGS	Send the 1st WRTGS for GS bit 8, second WRTGS for GS bit 7 …, Send LATGS for GS bit 0. GSCLK = 512.
10 bit	9 WRTGS + 1 LATGS	Send the 1st WRTGS for GS bit 9, second WRTGS for GS bit 8 …, Send LATGS for GS bit 0. GSCLK = 1024.
11 bit	10 WRTGS + 1 LATGS	Send the 1st WRTGS for GS bit 10, second WRTGS for GS bit 9 …, Send LATGS for GS bit 0. GSCLK = 2048.
12 bit	11 WRTGS + 1 LATGS	Send the 1st WRTGS for GS bit 11, second WRTGS for GS bit 10 …, Send LATGS for GS bit 0. GSCLK = 4096.
13 bit	12 WRTGS + 1 LATGS	Send the 1st WRTGS for GS bit 12, second WRTGS for GS bit 11 …, Send LATGS for GS bit 0. GSCLK = 8192.
14 bit	13 WRTGS + 1 LATGS	Send the 1st WRTGS for GS bit 13, second WRTGS for GS bit 12 …, Send LATGS for GS bit 0. GSCLK = 16384.

Figure 13 through Figure 15 show examples for PWM bit 10, WRTGS command, LATGS command and the total timing sequence for GS data writing.

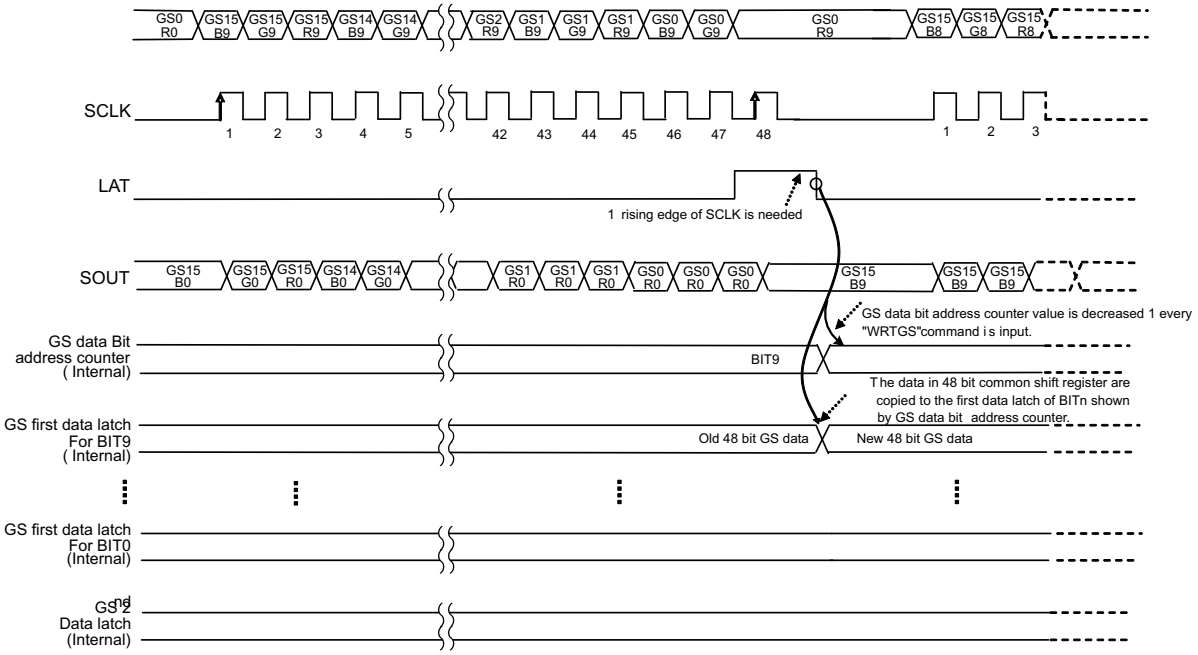


Figure 13. 48-Bit GS Data Write (WRTGS) Command in Poker Mode

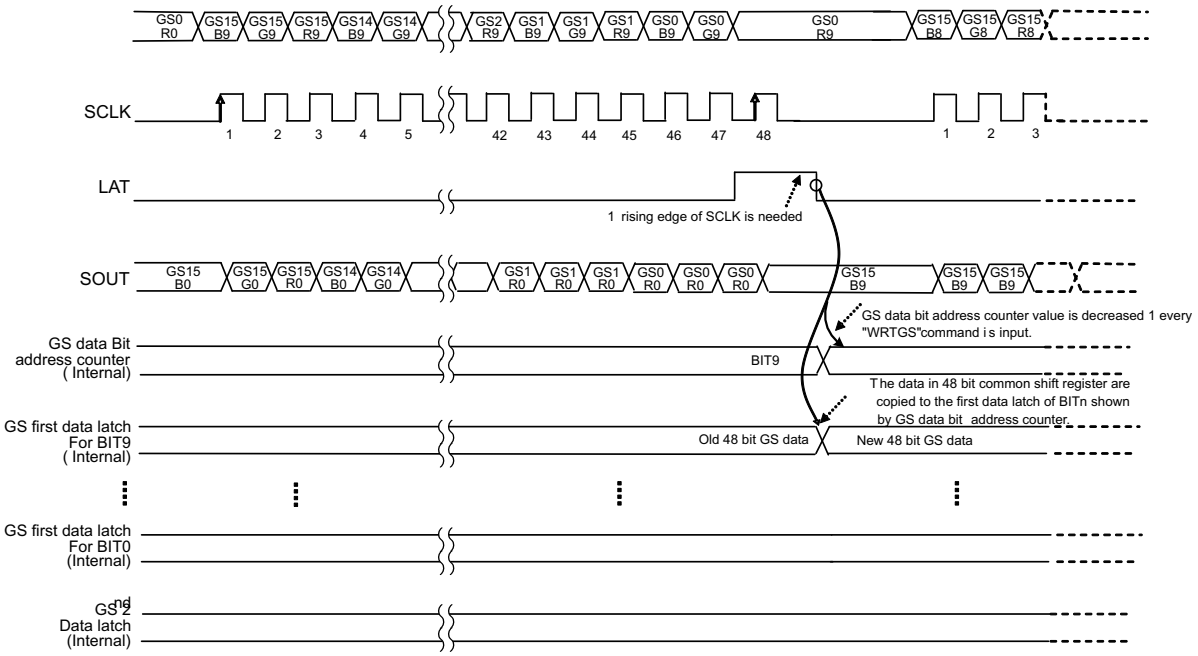


Figure 14. GS Data Latch (LATGS) Command in Poker Mode

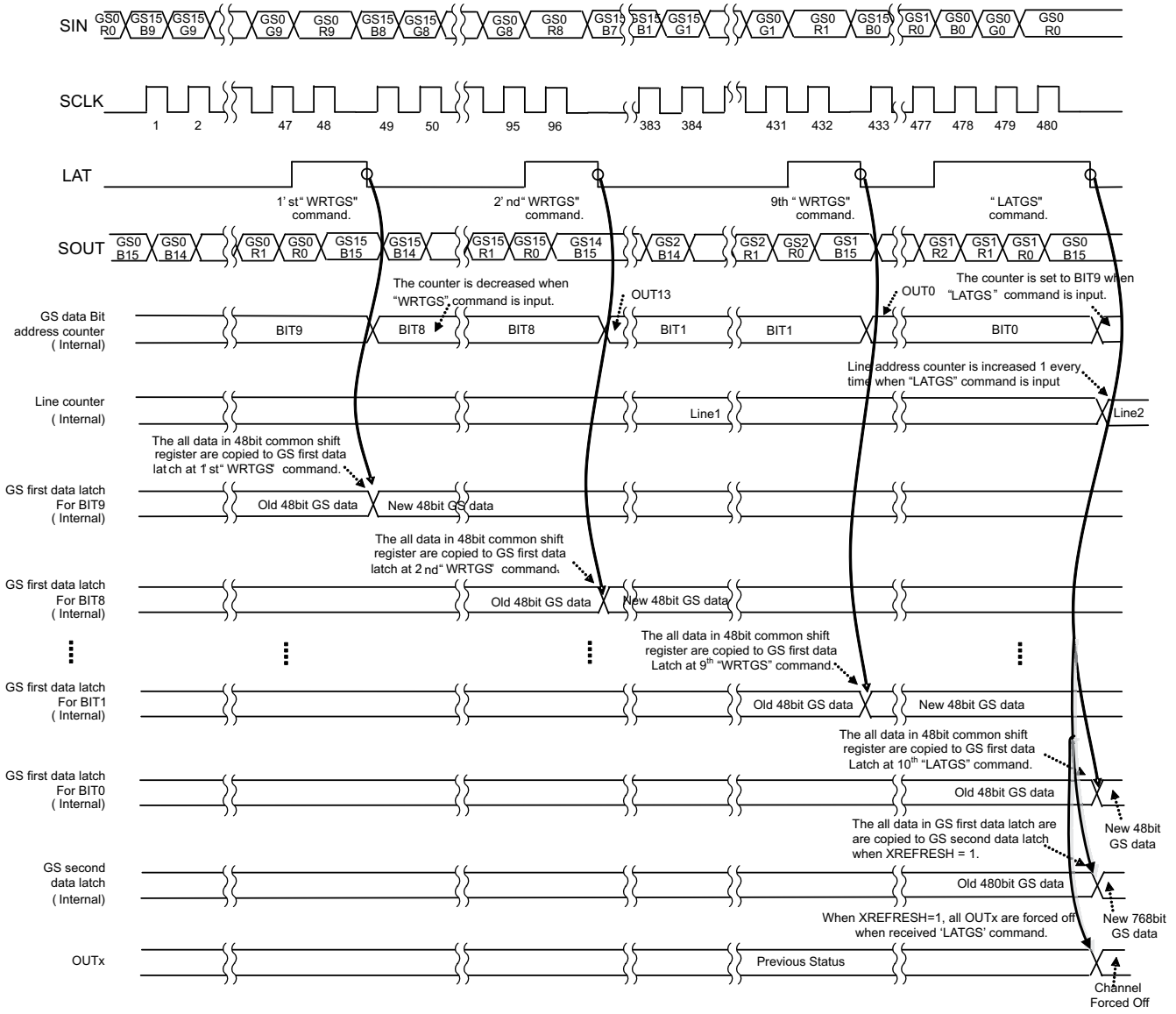


Figure 15. GS Data Write Sequence (9 "WRTGS" + 1 "LATGS" command) in Poker Mode

3.5 Step 4: Input GCLK to Begin Display

Input GCLK continuously, 2^NGCLK (N = 9–16) as a segment. Between the interval of two segments, LED supply voltage should be switched from one line to next line accordingly.

3.5.1 Basic Knowledge: What' is PWM Control?

PWM Control means pulse width modulation (PWM) control scheme, which controls the OUTx pin turn on ratio during one display period proportional to the GrayScale (GS) data of this channel.16-bits GS data per channel results in 65536 brightness steps, from 0% up to 100% brightness.

For example:

If GS = 0, then OUTx will not turn on during one display period (65536 GCLK period totally), the brightness is 0%.

If GS = 500, then during one display period, OUTx will turn on 500 GCLK period, then the brightness ratio will be 500/65535 = 0.763% (Assume 100% brightness if 65535 GCLK period is turned on during one display period).

If GS = 65534, then during one display period, OUTx will turn on 65534 GCLK period, then the brightness ratio will be 65534/65535 = 99.9985%.

3.5.2 Traditional PWM Control

The TLC5957 has two PWM modes: one is traditional PWM, the other is ES-PWM. This is decided with: ES-PWM mode enable bit (bit 8 of FC register). When this bit = 1, ES-PWM mode is selected. When this bit = 0, traditional PWM is selected.

Figure 16 is an operation timing of traditional PWM. When less on/off switch is required in application to avoid noise, this kind of PWM is preferred.

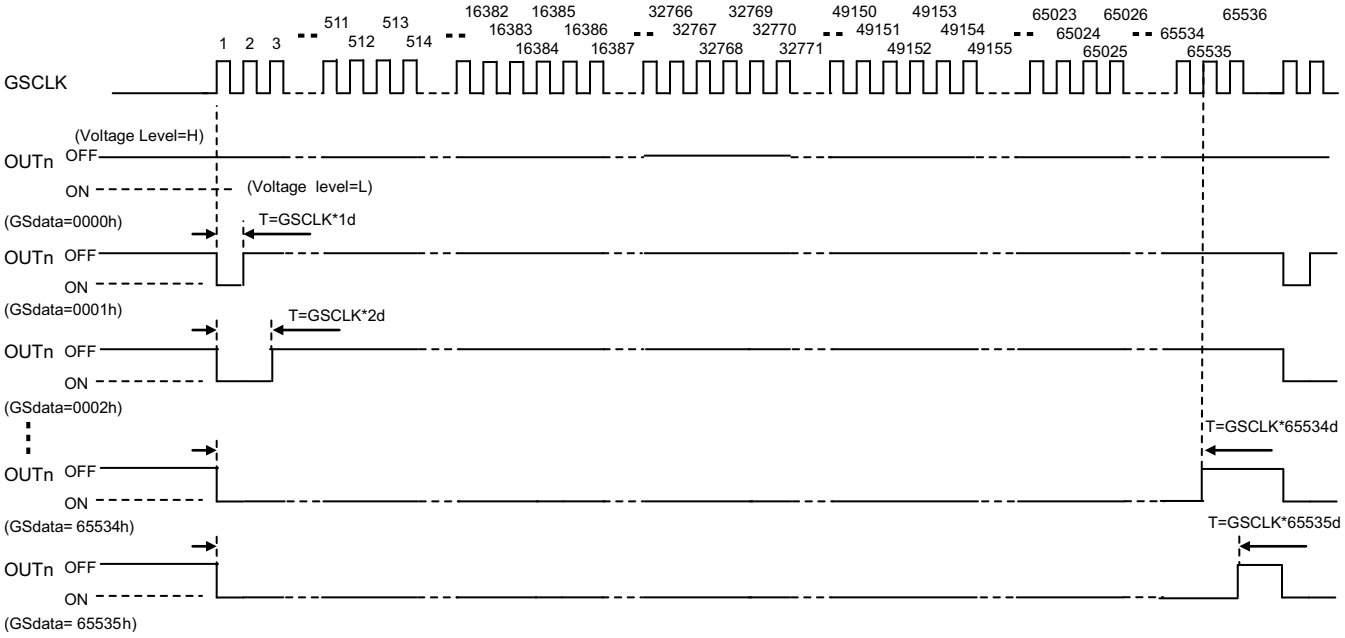


Figure 16. Traditional PWM Operation

3.5.3 Multiplexed Enhanced Spectrum (ES) PWM Control

The TLC5957 is designed for both static and multiplexed display systems. It uses an innovative Multiplexed ES PWM method to improve the visual refresh rate while maintaining the best grayscale performance.

In this PWM control, the entire display period is divided into 128 display segments. Entire display period means the timing from the first Gray Scale clock (GSCLK) to the 65536th Gray Scale clock is input in case of a 16-bit length PWM. Each display period has 512 grayscale as a maximum. The OUTn on time changes depending on the 16-bit grayscale data. Refer to Table 10 for sequence information and Figure 17 for timing information.

Table 10. ES-PWM Drive Turn on Time Length

GS Data		OUTn Driver Operation
(Dec)	(Hex)	
0	0000h	No turn on
1	0001h	Turns on during 1 GSCLK period in **1st** display period
2	0002h	Turns on during 1 GSCLK period in 1st + **65th** display period
3	0003h	Turns on during 1 GSCLK period in 1st + 65th + **33rd** display period
4	0004h	Turns on during 1 GSCLK period in 1st + 65th + 33rd + **97th** display period
5	0005h	Turns on during 1 GSCLK period in 1st + 65th + 33rd + 97th + **17th** display period
6	0006h	Turns on during 1 GSCLK period in 1st + 65th + 33rd + 97th + 17th + **81st** display period

Table 10. ES-PWM Drive Turn on Time Length (continued)

GS Data		OUTn Driver Operation
(Dec)	(Hex)	
—	—	The number of display periods which OUTn is turned on during 1 GSCLK is increased by GS data increasing in the following order: The order of display period which output turns on: 1>65>33>97>17>81>49>113>9>73>41>105>25>89>57>121>5>69>37>101>21>85>53>117 >13>77>45>109>29>93>61>125>3>67>35>99>19>83>51>115>11>75>43>107>27>91>59>123>7> 71>39>103>23>87>55>119>15>79>47>111>31>95>63>127>2>66>34>98>18>82>50>114>10>74>42 >106>26>90>58>122>6>70>38>102>22>86>54>118>14>78>46>110>30>94>62>126>4>68>36> 100>20>84>52>116>12>76>44>108>28>92>60>124>8>72>40>104>24>88>56>120>16>80>48> 112>32>96>64>128.
127	007Fh	Turns on during 1 GSCLK period in 1st–**127th** display period + No turn on in **128th** display period only
128	0080h	Turns on during 1 GSCLK period in all (1st–**128th**) display period
129	0081h	Turns on during 2 GSCLK period in **1st** display period + 1 GSCLK period in other display period
—	—	The number of display period which OUTn is turned on during 2 GSCLK is increased by GS data increasing as in the case GS is 1 through 127
255	00FFh	Turns on during 2 GSCLK period in 1st–**127th** display period + turn on 1 GSCLK period in **128th** display period only
256	0100h	Turns on during 2 GSCLK period in all (1st–**128th**) display period
257	0101h	Turns on during 3 GSCLK period in **1st** display period + 2 GSCLK period in other display period
—	—	Display period which OUTn is turned on time is increased by GS data increasing like the previous operation
65478	FEFFh	Turns on during **511** GSCLK period in 1st–**127th** display period + turns on **510** GSCLK period in **128th** display period only.
65279	FF00h	Turns on during **511** GSCLK period in all (1–128) display period.
65280	FF01h	Turns on during **512** GSCLK period in 1st display period + **511** GSCLK period in 2nd–**128th** display period
—	—	……..
65534	FFFEh	Turns on during **512** GSCLK period in **1st–63th** and **65th– 127th** display period + turns on **511** GSCLK period in **64th** and **128th** display period.
65535	FFFFh	Turns on during **512** GSCLK period in **1st–127th** display period + turns on **511** GSCLK period in **128th** display period only.

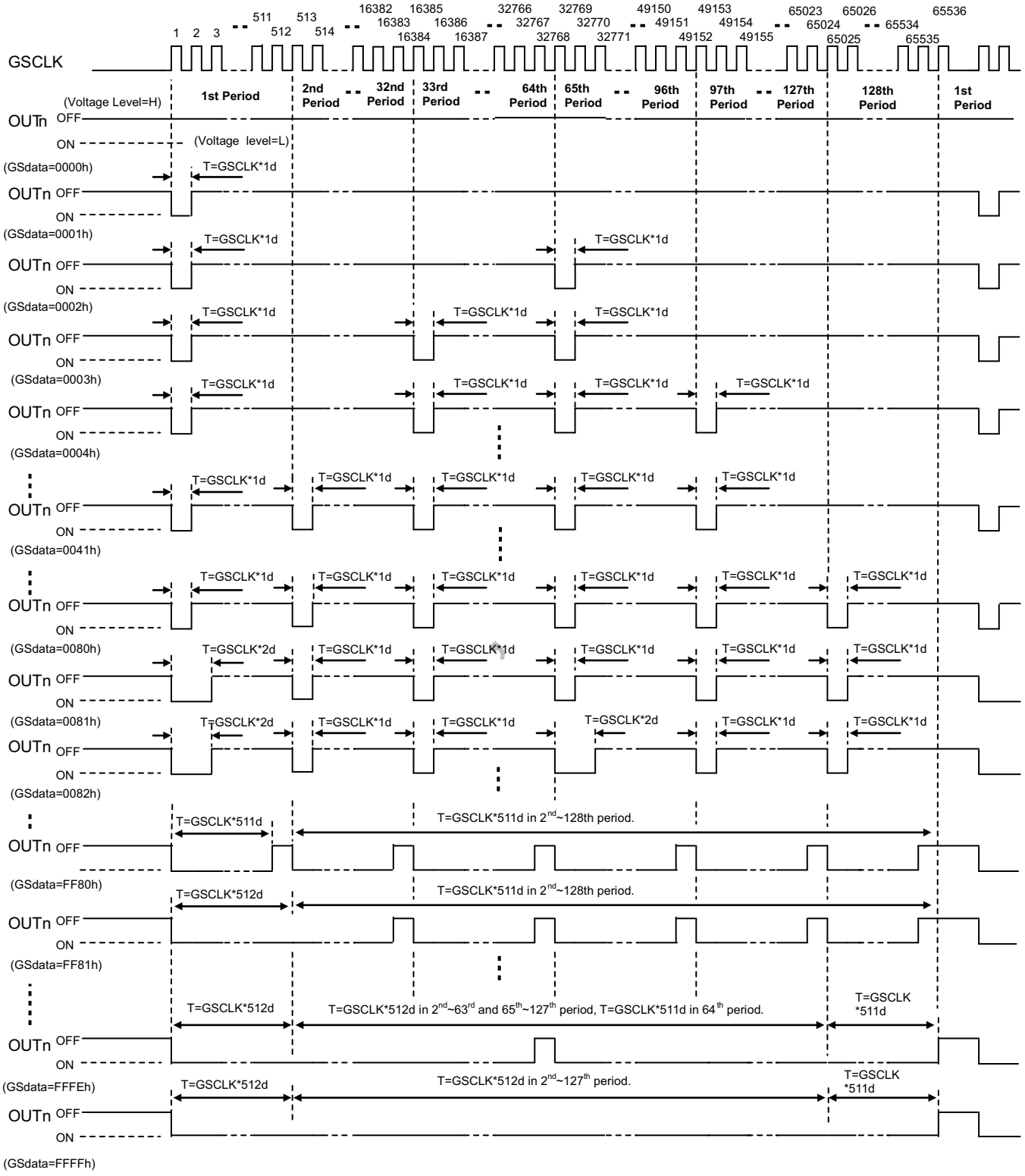


Figure 17. ES PWM Operation

3.6 Step 5: Display the Current Line and Input GS Data for Next Line

The TLC5957 can be used as static driver or multiplexing driver. In multiplexing applications, since no SRAM is built inside, the GS data stored in GS data latch has to be swapped all the time.

Figure 18 shows a timing sequence for a multiplexing application. In order to increase the refresh rate, using 1024 GCLK for new GS data updated. When GCLK is input, GS data for the next line is also shifted in. Be aware that the falling edge of “LATGS” command needs to be input after the rising edge of the 1024th GCLK.

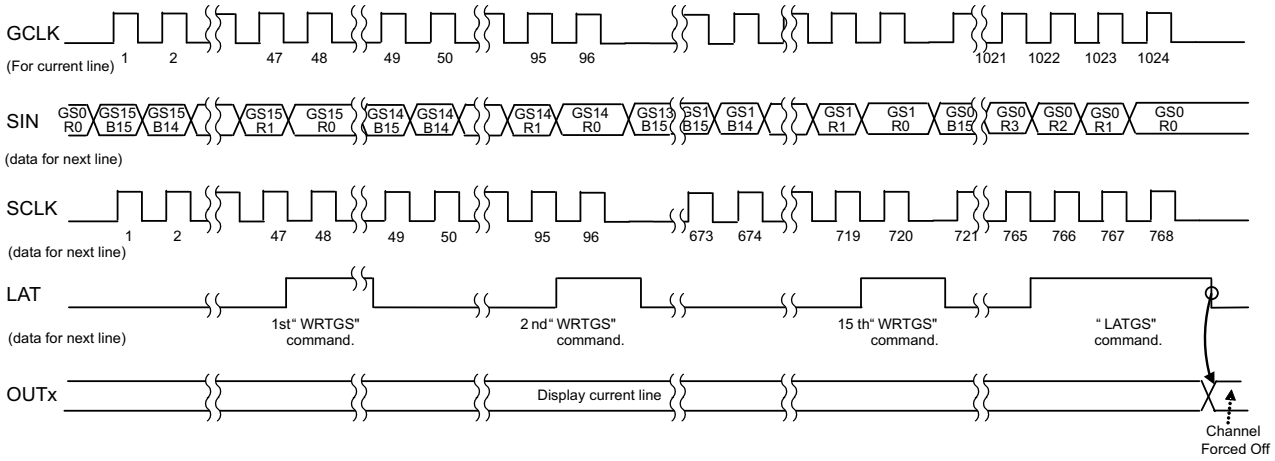


Figure 18. GS Data Writing in Multiplexing Application

3.7 Step 6: GS Data Input for the Last Line in Multiplexing Application

3.7.1 Multiplexing Application Sequence

The TLC5957 can be used in multiplexing applications, but without integrated SRAM, it is difficult to know the current operating line, and total line number. In some cases, the timing sequence of power lines is very important to implement some internal function for better grayscale performance. Therefore, TLC5957 uses the LINERESET Command in the last line to record the timing sequence of power lines.

In multiplexing applications, LINERESET is required to enable the Caterpillar cancelling function. However, the Caterpillar cancelling function and LOD SID reading cannot work at the same time since LOD SID information is not available after the LOD channel has been masked by Caterpillar cancelling circuits.

3.7.2 LINERESET Command

The TLC5957 uses the LINERESET and TMGRST commands to reset the line counter. LINERESET command can be used to replace LATGS command in the last line, not only to latch GS data, but also to reset the line counter. The TMGRST command can be used for GS and Line counter reset, and meanwhile the OUTx are forced off. These commands are distinguished by the number of SCLK rising edges included in the LAT pulse. Table 11 describes these two commands.

Table 11. WRTFC/FCWRTEN Commands Description

Command Name	SCLK Rising Edges While LAT is High	Description
LINERESET	7	Line Counter in register will be clear. Also, Data in Common register copy to the fist GS data latch, 1st data latch counter reset. If XRFRESH = 0, auto refresh enabled, all data is copied to the second lat when the GS counter is set to 65536; If XRFRESH = 1, auto refresh disables, all data in the 1st GS lat copy to 2nd GS lat, GS counter reset, all OUTx force off. Change group pattern when this function is received Refer to Figure 7 for a timing diagram of this command operation.
TMGRST	13	The GS Counter is reset to '0', line counter is reset, and all the outputs are forced off.

Refer to Figure 19 for a detailed command input timing diagram.

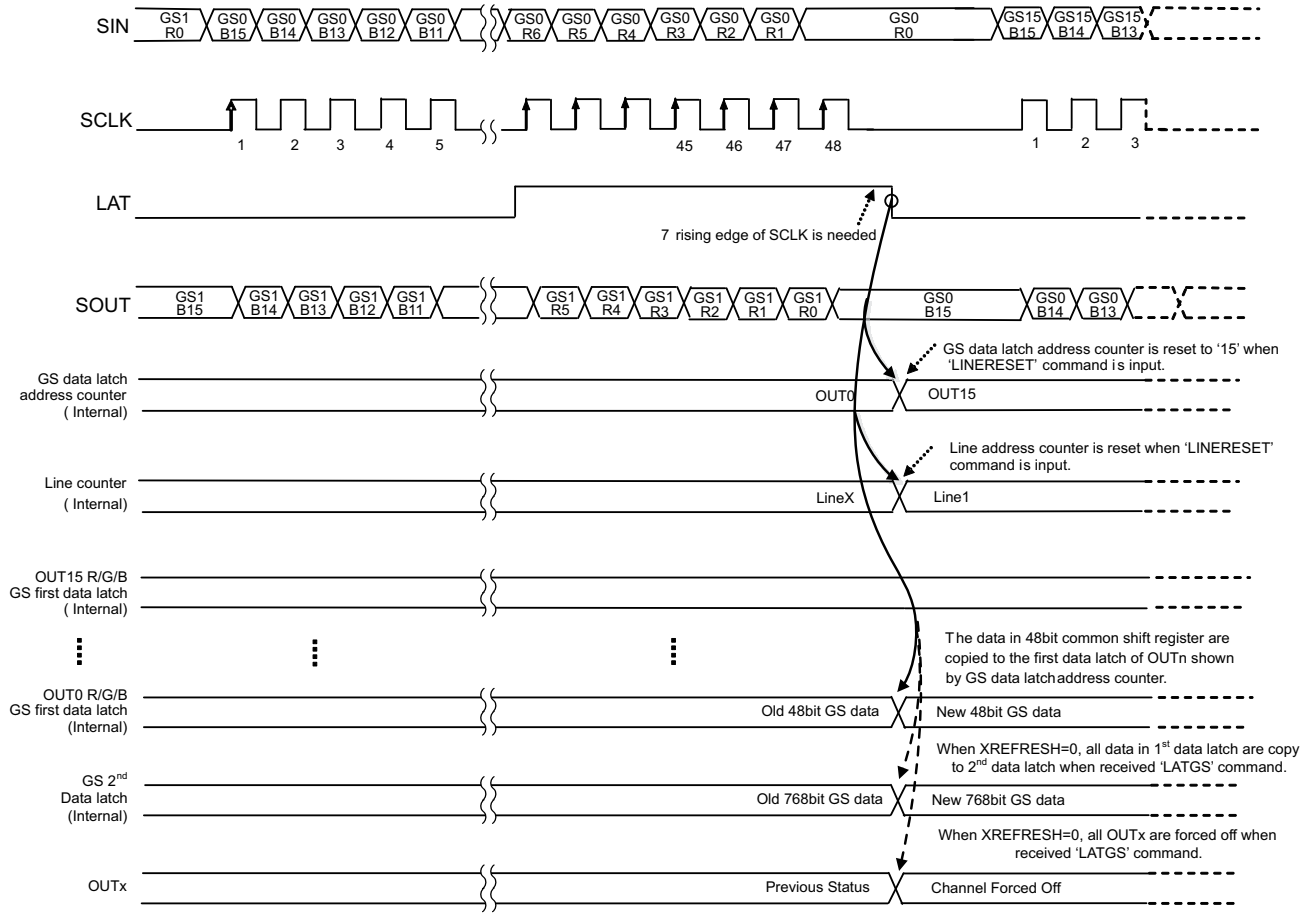


Figure 19. LINERESET Command

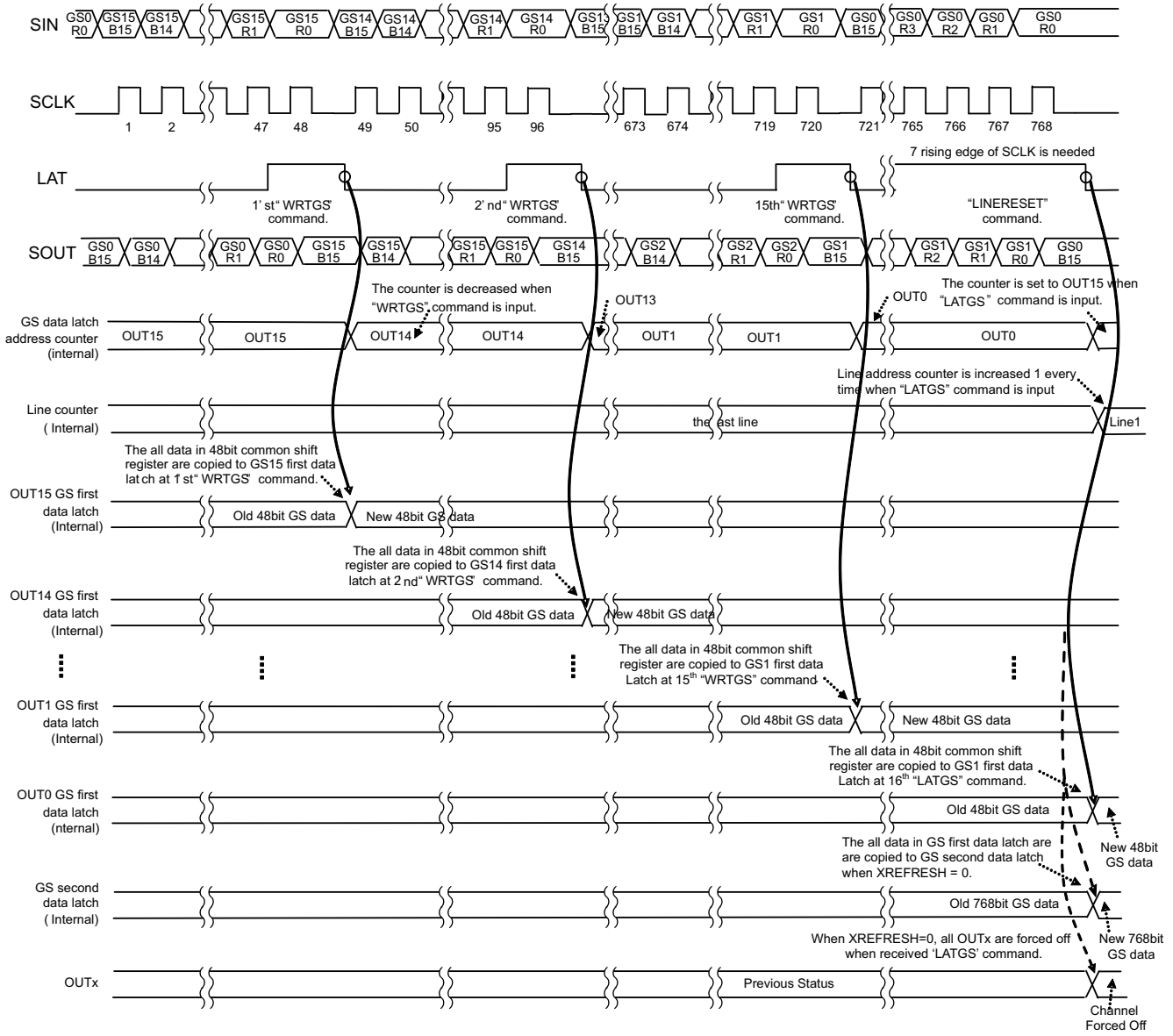


Figure 20. 768-Bit GS Data Write Sequence for the Last Line (15 "WRTGS" + 1 "LINERESET" command)

3.7.3 The Whole Operation Sequence

In a commonly used application, LINERESET is always used for GS data latch for the last line, and LATGS is always used for GS data latch for the other line.

Figure 21 is a typical timing sequence for an 8-multiplexing panel. The whole display period is divided into 64 sub-periods, each sub-period consists of the whole 8 scans for each line. In the first 7 lines of each sub-period, GS data writing is 15 WRTGS + 1 LATGS. If poker mode is used here to decrease the data writing time, the sequence can be 9 WRTGS + 1 LATGS. For the last line of each sub-period, LINERESET should be used to replace LATGS.

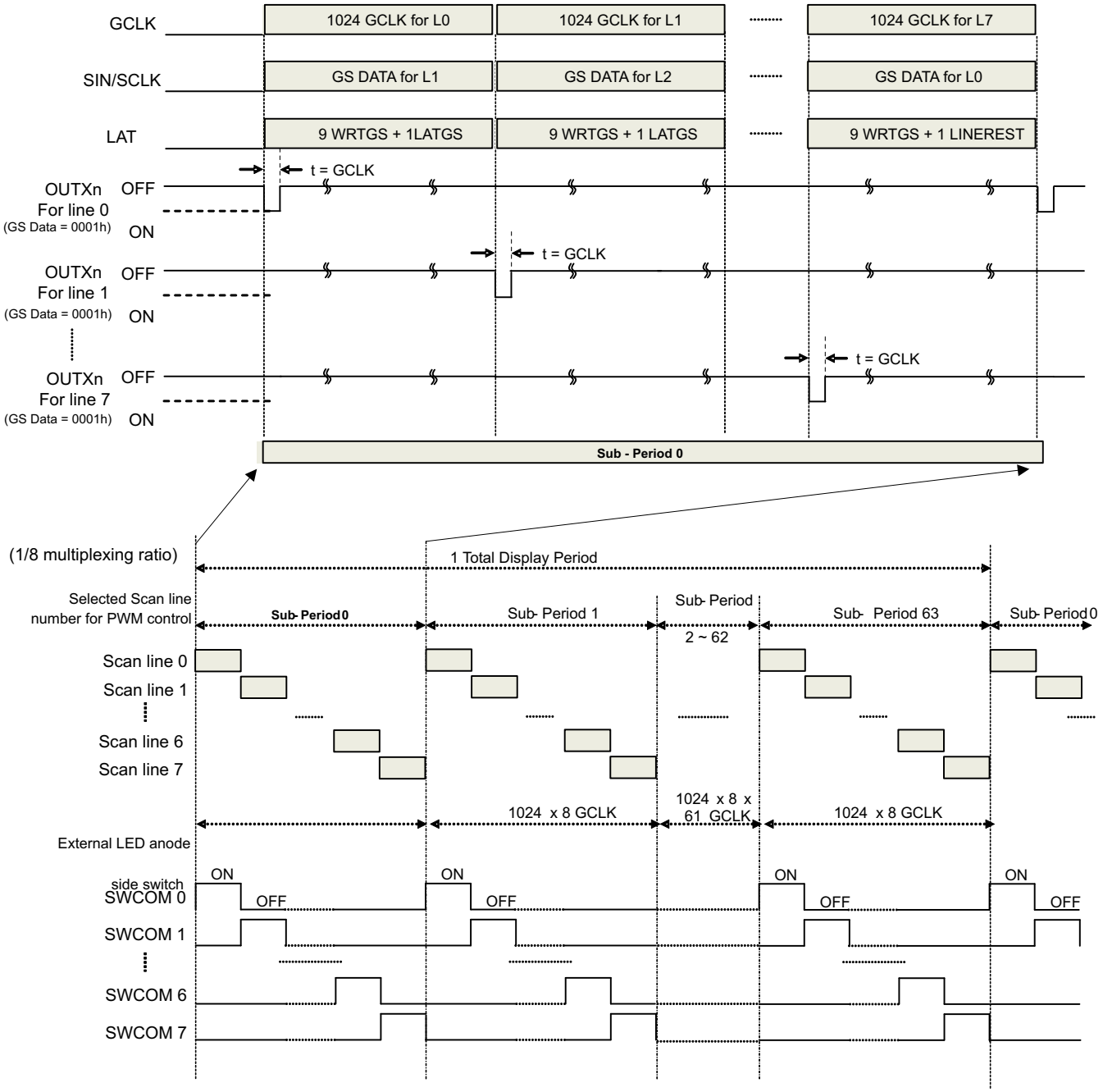


Figure 21. Whole Operation Sequence in 10-Bit Poker Mode

3.8 LED Open Detection (LOD)

The LOD function can detect a fault caused by an open circuit in any LED string, or a short from OUTXn to ground with low impedance, by comparing the OUTXn voltage with the LOD detection threshold voltage level set by LODVLT in the FC1 register (see Table 5). If the OUTXn voltage is lower than the programmed voltage, the corresponding output LOD bit is set to '1' to indicate a opened LED. Otherwise, the output of that LOD bit is '0' (see Figure 22). LOD data output by a detect circuit are valid only during the ‘on’ period of that OUTXn output channel. LOD data are always ‘0’ for outputs that are turned off.

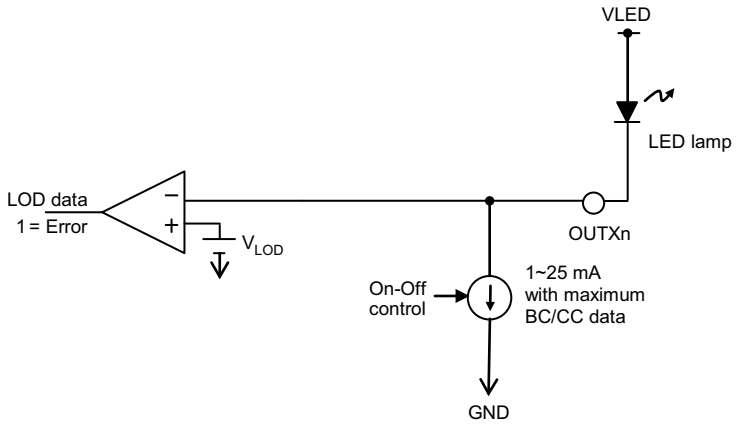


Figure 22. LOD Detect Circuit of One Channel

The output of the LOD detect circuit is loaded into the 48-bit register called SID holder (Figure 23 shows the bit arrangement of this SID holder) at the rising edge of the 15th GCLK in each segment. To get a correct detecting result, it is necessary to make sure OUTXn is kept 'on' in the 15th GCLK period in one segment. See Figure 24 and Figure 25 for the timing diagram.

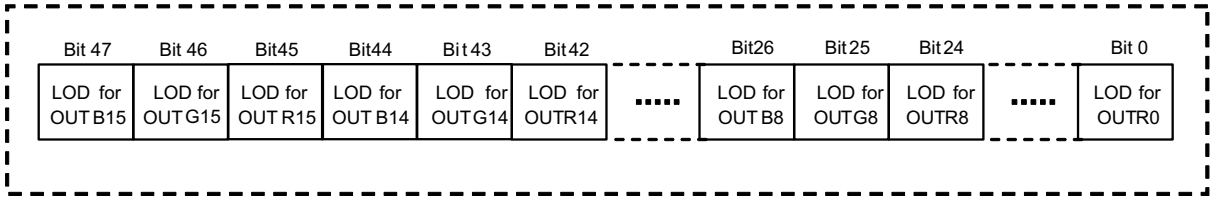


Figure 23. Bit Arrangement of SID Holder

Table 12. LOD Threshold Voltage Truth table

LODVLT		LED Open Detection (LOD) Threshold Voltage
BIT 1	BIT 0	
0	0	VLOD0 (0.09 V typ)
0	1	VLOD1 (0.19 V typ, Default value)
1	0	VLOD2 (0.35 V typ)
1	1	VLOD3 (0.50 V typ)

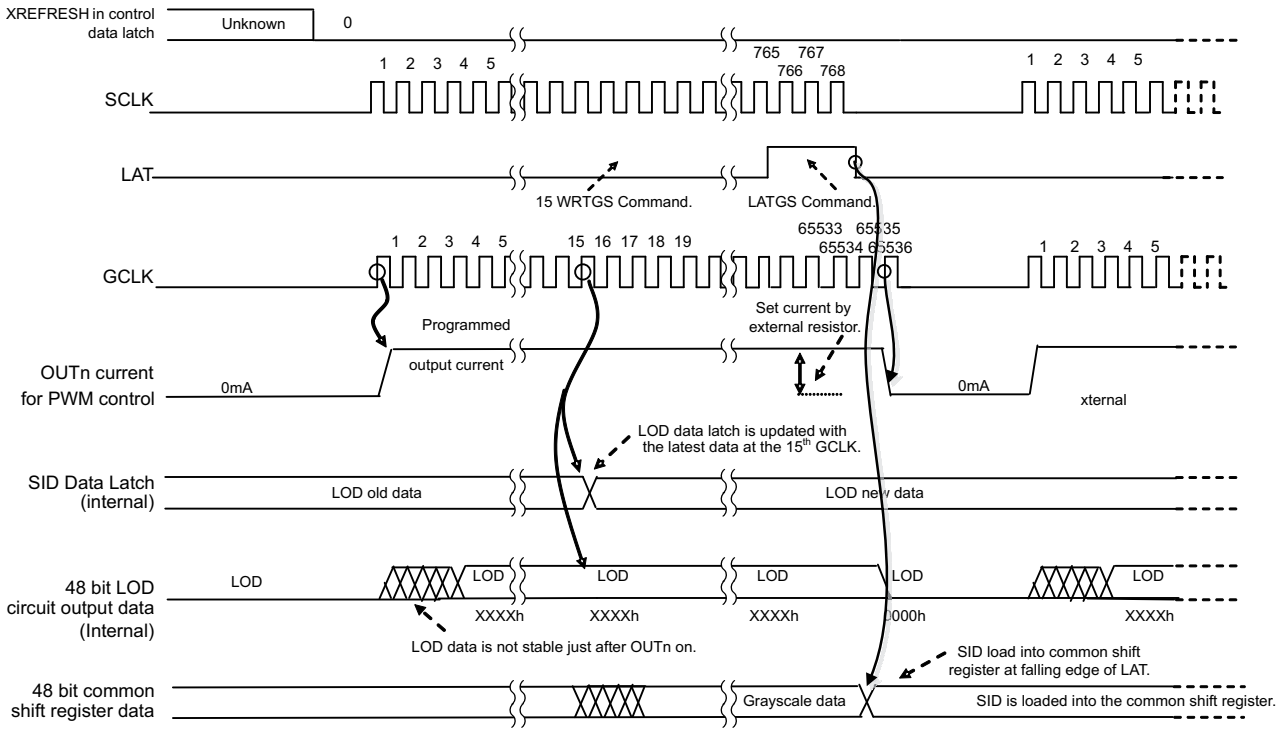


Figure 24. LOD Information Latch into SID Holder(XREFRESH = 0)

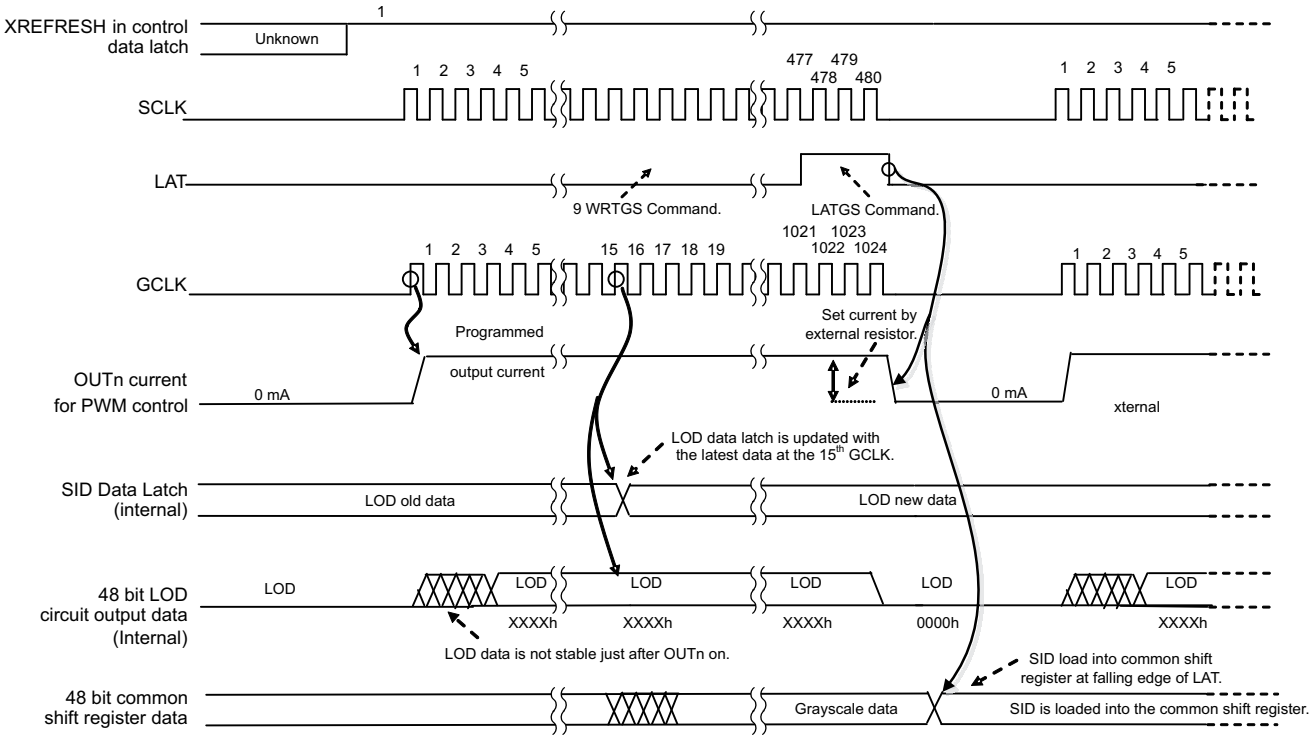


Figure 25. LOD Information Latch into SID Holder(XREFRESH = 1)

3.9 How to Read Function Control Register

Once the TLC5957 detected 11 rising edges of SCLK during LAT high period, it considers this as a READFC command. The 48-bit data in the FC register is latched into the 48 bits of common shift register at the falling edge of the LAT signal. Then the loaded data can be read out from SOUT synchronized with the SCLK rising edge.

Refer to Figure 26 for the timing diagram of this command.

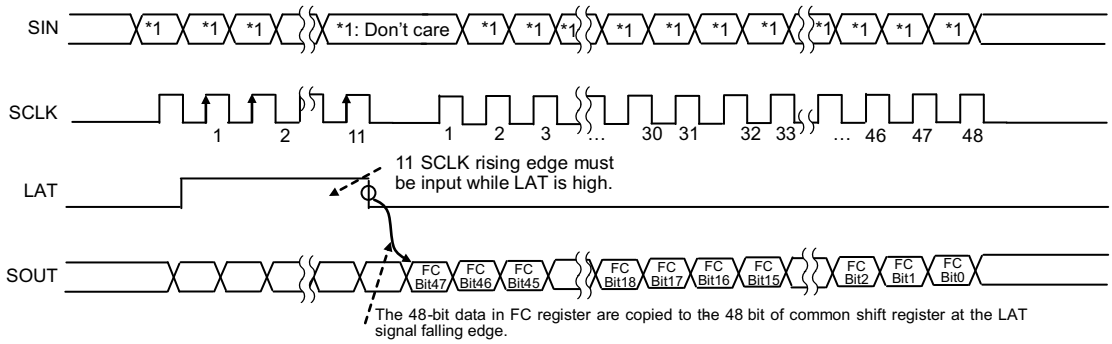


Figure 26. FC Data Read (READFC) Command

3.10 Function Commands Summary

Table 13 is a summary of all the seven commands that can be input with SCLK and LAT signals: WRTGS, LATGS, WRTFC, LINERESET, READFC, TMGRST, and FCWRTEN.

Table 13. Function Commands Summary

Command Name	SCLK Rising Edges While LAT is High	Description
WRTGS (48-bit GS data write)	1	The 48-bit data in common shift register are copied to the 48-bit GS latch in the first latch selected by the GS data latch address counter. Refer to Figure 9 for a timing diagram of this command operation.
LATGS (768-bit GS data latch)	3	The 48-bit data in the common shift register are copied to corresponding 48-bit GS data latch in the first latch. All data in the first data latch are copied to the 2nd GS data latch when the GS counter reaches 65536, if XREFRESH = 0; all data in the 1st data latch are also copied to the 2nd GS data latch, GS counter reset, and all OUTx are forced off if XREFRESH = 1. Refer to Figure 10 for a timing diagram of this command operation.
WRTFC (FC data write)	5	The 48-bit data in common shift register are copied to the FC register if input after FCWRTEN command. Refer to Figure 7 for a timing diagram of this command operation.
LINERESET	7	Line Counter in register will be clear, also data in the common register is copied to the fist GS data latch, the 1st data latch counter is reset. If XRFRESH = 0, auto refresh enabled, all data is copied to 2nd lat when the GS counter to 65536; If XRFRESH = 1, auto refresh disables, all data in 1st GS lat copy to 2nd GS lat, GS counter reset, all OUTx force off. Change group pattern when this function is received. Refer to Figure 7 for a timing diagram of this command operation.
READFC	11	The 48-bit data in the FC register are copied to the 48-bit of shift register. The loaded data can be read out from SOUT synchronized with the SCLK rising edge. Refer to Figure 24 for a timing diagram of this command operation.
TMGRST	13	The GS Counter is reset to '0', Line counter will be reset, and all the outputs are forced off.
FCWRTEN (FC write enable)	15	FC writes are enabled by this command. This command must always be input before the FC data write occurs. Refer to Figure 7 for a timing diagram of this command operation.

3.11 Ghost Cancelling

The pre-charge FET is integrated to remove ghost in multiplexed LED modules. One cause of this issue is the charging current for parasitic capacitance of the OUTXn through the LED when the supply voltage switch from one common line to next common line.

To prevent this unexpected charging current, the TLC5957 uses an internal FET to pull OUTXn up to VCC-1.4 V during the common line switching period. Thus, no charging current flow through LED and the ghost phenomenon is eliminated.

Two working modes of Pre-charge can be selected by SEL_PCHG, Bit 7 of FC register.

When this bit is '0', which is the default setting, the Pre-charge FETs are only off during the period in which the channel is on.

When this bit is '1', the Pre-charge FET keeps off during the whole segment period, and only turns on during the dead-time (the time between two adjacent segments).

Figure 27 shows this difference (take 1024 GCLK per segment, for example).

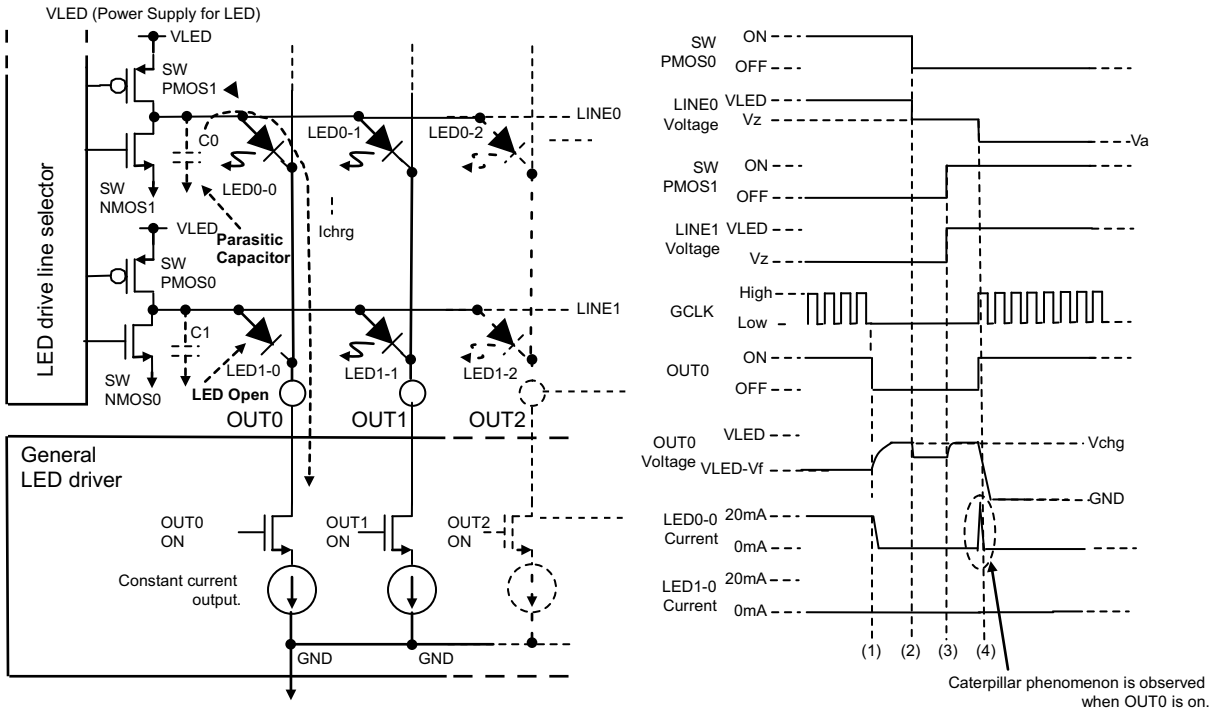


Figure 27. Pre-Charge FET Working Mode

3.12 Caterpillar Cancelling

Caterpillar effect is a phenomenon caused by broken LEDs. The TLC5957 has an internal circuit to remove caterpillar issue in multiplexed LED modules. One cause of this phenomenon is the electric charge on the parasitic capacitor of Line goes through LED when the OUT is pulled down to GND due to LED open of another line. This will make all the LED multiplexing with the open LED turn on during the special time.

To prevent the caterpillar issue, the TLC5957 integrated internal circuits for LED open detection. When LED open is detected, the output channel is turned off for this specific line and then the caterpillar effect is eliminated.

Figure 28 is the detailed explanation of the caterpillar effect.

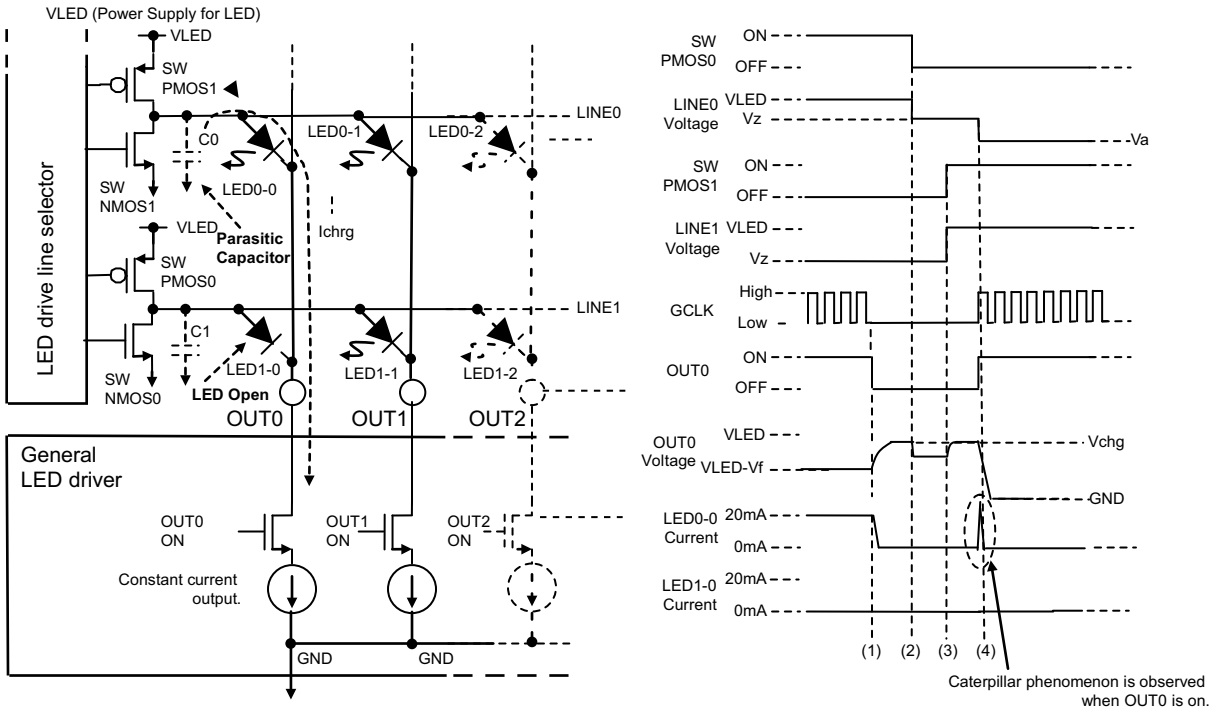


Figure 28. LED Caterpillar Phenomenon Mechanism

This function can be enabled or disabled with the LINERESET command. If the LINERESET command is send any time after the TLC5957 is powered on, the caterpillar effect function is enabled. If LINEREST command is never sent after power on, then this function is disabled, and the caterpillar effect is observed if the LED is open.

NOTE: If caterpillar removal is enabled, then the SID information shifted from the SOUT is not correct, due to internal conflict.

3.13 Double Edge for Data Transmission

3.13.1 Why This Function?

Visual Refresh rate is a critical parameter in LED display. If the TLC5957 is used in multiplexing application, this parameter is limited by GS data transmission time. If the cascaded device is larger, visual refresh rate is even lower.

Double SCLK means GS data can be sent both at rising edge and falling edge of SCLK. Using this method, GS data transmission rates doubly increase compared to traditional transmission methods which send GS data only at the rising edge of SCLK. At the same time, the frequency of SCLK is not increased, so there may not be risk in PCB layout.

3.13.2 How to Send GS Data Using Double Edge

Double edge for SCLK can be enabled by bit 10 in FC register.

If FC bit 10 = 0, double edge SCLK is disabled, GS data only be sent at the rising edge of SCLK. If FC bit 10 = 1, double edge SCLK is enabled, GS data can be sent both at the rising and falling edge of SCLK.

Figure 29 is a detailed timing for WRTGS command at double SCLK mode. Compared to single mode, it needs less SCLK number, and the transmission time is shorter. LATGS, LINERESET command is the similar timing compared to WRTGS command.

In double SCLK mode, SCLK rate should not be more than 18M.

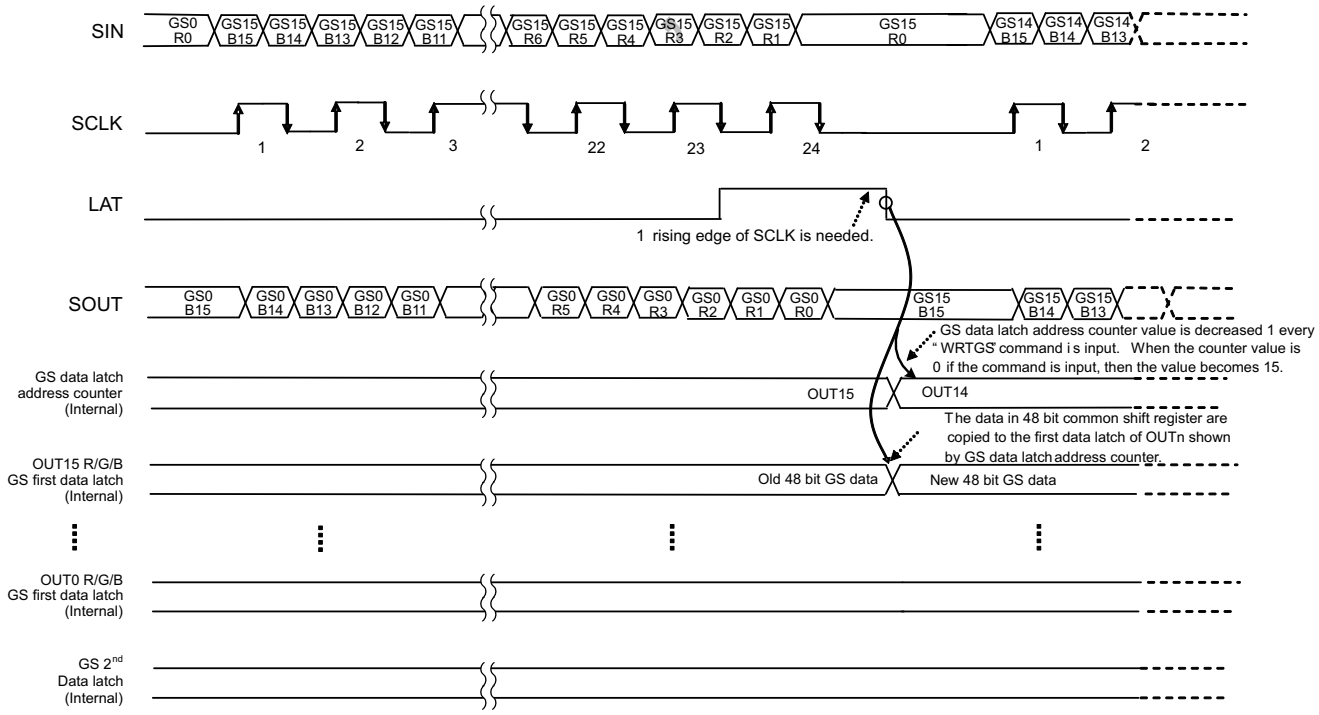


Figure 29. WRTGS Command at Double SCLK Mode

3.13.3 How to Send FC Data

FC data writing sequence is not affected by the double SCLK mode. Whatever double SCLK is enabled or not, FC data can only be written at the rising edge of SCLK.

Figure 30 is a detailed timing for WRTGS command at double SCLK mode

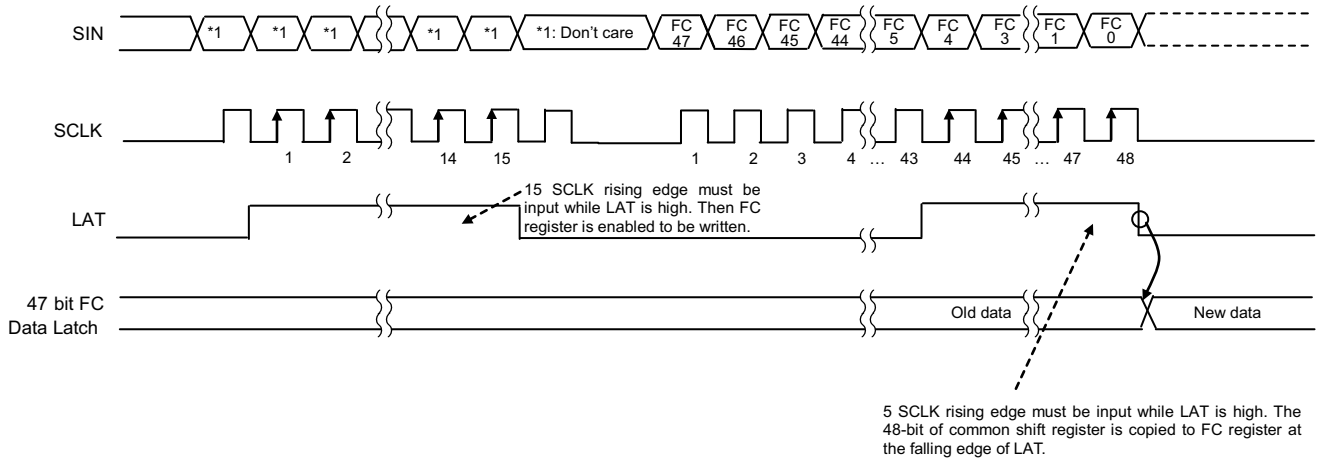


Figure 30. FCWRTEN and WRTFC Command at Double SCLK Mode

3.14 Protection

3.14.1 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all constant-current outputs of the IC when the junction temperature (T_J) exceeds the 170°C (typ). It resumes normal work once T_J returns to lower than 160°C(typ).

3.14.2 IREF Resistor Short Protection (ISP)

The Iref resistor short protection (ISP) function prevents the unwanted large current from flowing though the constant-current output when Iref resistor is shorted accidently. The TLC5958 will turn off all output channels when Iref pin voltage is lower than 0.125 V (typ). When the Iref pin voltage is higher than 0.35 V (typ), the TLC5957 will resume normal work again.

3.15 Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted, if all 48 LED channels turned on simultaneously at the 1st GCLK rising edge. This large surge current could induce detrimental noise and electromagnetic interference (EMI) into other circuits.

The TLC5957 separates the LED channels into 12 groups. Each group includes 4 output channels. It turns on these groups sequentially with a 1.67-ns (typ) delay between one group and the next group. By this means, a soft-start feature is provided. See Table 6 for the detail turn on delay sequence.

The turn-off of LED channels is implemented with a same delay scheme.

This group delay function is enabled by default at power on. However, it can be disabled by setting SEL_GDLY (bit 4 of FC register) to ‘0’.

3.16 Low Gray Scale Enhancement (LGSE)

First (1st) line issue is a common phenomena in multiplexing application, especially in high density, high refresh rate panel. This issue can be solved by choosing a different setting of LGSE1 in FC register. Adjusting these control bits will also help improve the white balance at low grayscale condition.

Table 14. LGSE1 Effect Summary

LGSE1 (FC)			Low Grayscale Enhancement Effect		
BIT13	BIT12	BIT11	Red Color	Green Color	Blue Color
0	0	0	No	No	No
0	0	1	No	Weak	Weak
0	1	0	No	Medium	Medium
0	1	1	No	Strong	Strong
1	0	0	Weak	Medium	Medium
1	0	1	Weak	Strong	Strong
1	1	0	Medium	Medium	Medium
1	1	1	Medium	Strong	Strong

Different multiplexing ratio needs different setting. The general guidelines follow:

1. The higher the multiplexing ratio is, the higher enhancement is needed.
2. The enhancement of G/B should be higher than that of the Red color.

For example, one suggested setting for a 1/16 multiplexing panel is: LGSE1 = 100

Besides the previous countermeasures, choose setting of LGSE2, bit 45–47 of FC register, will also help improve the 1st line issue at LGSE condition.

Table 15. LGSE2 Effect Summary

LGSE2 (FC)			Low Grayscale Enhancement Effect		
BIT47	BIT46	BIT45	Red Color	Green Color	Blue Color
0	0	0	No	No	No
0	0	1	No	Weak	Weak
0	1	0	No	Medium	Medium
0	1	1	No	Strong	Strong
1	0	0	Weak	Medium	Medium
1	0	1	Weak	Strong	Strong
1	1	0	Weak	Medium	Medium
1	1	1	Weak	Strong	Strong

A third method to improve low grayscale performance is to set LGSE3, bit 9 of the FC register. When this bit is set to 1, the Blue color is compensated for keeping white balance; keeping this bit at 0 makes no difference for the R/G/B color.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265