

TPS65084x Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPS65084x evaluation module (EVM). The TPS65084x EVM is a fully assembled platform for evaluating the performance of the TPS65084x power management device. This document should be used with the schematic diagrams, the printed-circuit board (PCB) layout, and the bill of materials (BOM) supplied in conjunction with this document.

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1 Introduction

The TPS65084x is a highly integrated power management solution for the Intel Braswell processors.

Features of the TPS65084x include:

- Three Variable-Output Voltage Step-Down Controllers
 - Wide V_{IN} range from 5.4 V to 21 V
 - Up to 7-A output current for BUCK1 (VCC) and BUCK6 (VDDQ), and 11-A for BUCK2 (VGG) using external FETs
 - I²C DVS Control (0.5 V to 1.45 V in 10-mV steps) for BUCK1 and BUCK2
 - Pin-selectable output voltages (1.1 V, 1.2 V, or 1.35 V) for BUCK6 (VDDQ)
- Three variable-output voltage synchronous step-down converters
 - V_{IN} range from 4.5 V to 5.5 V
 - Up to 3.5 A of output current for BUCK3 (VNN) with I²C DVS control (0.65 V to 1.45 V in 25-mV steps)
 - Up to 3 A of output current for BUCK4 (V1P05A) and up to 1.5 A of output current for BUCK5 (V1P8A)
- Three LDO regulators with I²C-adjustable-output voltage
 - LDOA1: from 1.35 V to 3.3 V for up to 200 mA of output current
 - LDOA2: from 1.05 V, 1.1 V, 1.15 V, and 1.2 V for up to 500 mA of output current
 - LDOA3: from 1.1 V, 1.15 V, 1.2 V, and 1.24 V for up to 500 mA of output current
- VTT LDO for DDR3 and DDR4 memory termination
 - Fixed-output voltage of $0.5 \times V_{BUCK6}$
 - Can sink and source output current up to 500 mA
- Three load switches with slew-rate control
 - Up to 300 mA of output current with voltage drop less than 1.5% of nominal input voltage
 - $R_{DS(ON)} < 96 \text{ m}\Omega$ at input voltage of 1.8 V
- I²C interface (Device Address 0x5E) supports standard mode (100 kHz), fast mode (400 kHz), and fast mode plus (1 MHz)
- 64-Pin, single-row, 0.4-mm pitch QFN package

2 Requirements

2.1 Software

The EVM will power-up and operate without use of software. A GUI is supplied to provide a simple way to communicate to the device via I²C. The GUI can be downloaded from:

<http://www.ti.com/tool/IPG-UI>

Additional installers are needed to update the GUI to contain the register map for this device. They can be downloaded from:

https://ti.com/licreg/docs/swlicexportcontrol.tsp?form_id=184041&prod_no=TPS65084X_94X&ref_url=hval_ipg

The EVM has a built-in USB2ANY module utilizing an MSP430. The GUI uses this to communicate with the device.

2.2 Host Computer

A computer with an available USB port is required to make use of the EVM software. The EVM software runs on the computer and communicates with the EVM via a USB-A to micro-B cable.

2.3 Power Supply

A DC power supply capable of delivering at least 5.6 V and 1 A is required to power on the EVM. If loading the EVM, a power supply with a 10 A limit or higher is recommended.

2.4 EVM Kit

The EVM kit contains the following items:

- TPS65084x HVL116A evaluation board

3 Terminal Block Descriptions

The EVM features 14 terminal blocks around the perimeter of the EVM. These are used for providing VSYS (J1) and loading the outputs. Each terminal block is labeled with the input or output on one side and GND on the other. Each terminal block also has a pair of test points for sense line probing.

4 Test Point Descriptions

Numerous test points are provided for sensing voltages on the EVM. The CTL1–6 test points also provide a way to override the on-board switches, when desired. Note that to override the switches, they must be in the 'OFF' position (not shorted to GND).

Table 1. Test Points⁽¹⁾

Test Point	Description
CTL1	PMICEN
CTL2	DDR_SEL
CTL3	SLP_S0IXB
CTL4	SLP_S3B
CTL5	SLP_S4B
CTL6	DDRVTCTRL
GPO1	RSMRSTB
GPO2	DRAMPWROK
GPO3	COREPWROK
GPO4	VCCAPWROK
V5ANA	External 5-V supply input to internal load switch that connects this pin to LDO5P0 pin.
LDO5V	5-V internal LDO (LDO5P0) sense
LDO3P3	3.3-V internal LDO sense
VREF	Bandgap reference output
GND	Connected to GND planes
DIG_1P8V	1.8-V external LDO sense
USB_3P3V	3.3-V external LDO sense for USB2ANY onboard MSP430
BUCK3P3V	3.3-V external BUCK sense
BUCK5V	5-V external BUCK sense
EPGOOD	Power good indicator of external dual controller (requires pull-up to indicate properly)
Output Sense+ (Unlabeled)	Each rail has a sense+ line connected to the central output cap
Output Sense- (Unlabeled)	Each rail has a sense- line connected to the central output cap
Input Sense+ (TP1)	VSYS sense+ line connected to input cap of PMIC
Input Sense- (TP2)	VSYS sense- line connected to input cap of PMIC

⁽¹⁾ Test points are not designed to carry current. They are intended for measuring voltage.

5 Header Descriptions

There are 7 sets of headers which are used to provide greater access to several signals.

Table 2. Headers

Jumper	Description	Jumper Default Position
J21	Option to bypass the on-board 5-V external buck for the input to BUCK3, BUCK4, BUCK5, and V5ANA. 4 GND pins provided here as well.	VIN_BUCK345_ANA connected to BUCK5V with two jumpers to accommodate high current
J22	Option to bypass LDO5V for the input to DRV5V_2_A1 and DRV5V_1_6	VIN_DRV connected to LDO5V
J23	Option to bypass the on-board 3.3-V external buck for the input to SWA1. 2 GND pins provided here as well.	VIN_SWA1 connected to BUCK3P3V
J24	Option to bypass BUCKX_1P8V (1.8 V) for the input to LDOA2_A3	VIN_LDOA2_A3 connected to BUCKX_1P8V
J25	Option to bypass BUCKX_1P8V (1.8 V) for the input to SWB	VIN_SWB connected to BUCKX_1P8V
J33	SDA, SCL, and GND	Not intended for a jumper

6 Control, GPO, and External VRs

The EVM features a set of DIP switches for controlling CTL1–6 and 6 LEDs for GPO indicators. It also has built-in USB2ANY circuitry which utilizes an on-board MSP430 to enable the GUI to communicate with the device through a USB cable. Finally, it features an on-board TPS51285 device which provides 3.3- and 5-V rails from VSYS for use by BUCK3, BUCK4, BUCK5, V5ANA, and SWA1. Pads exist for the addition of Samtec HSEC8-110-01-S-DV-A vertical edge rate card sockets.

- For the CTL switches, S1, the “OFF” position is an open circuit and the CTL signal is pulled up to the corresponding rail. The “ON” position forces the CTL signal to GND.
- The LED order is D6, D1, D4, D5, D2, D3 with the resulting signal order from left to right being: USB, RSMRSTB, VCCAPWROK, IRQB, DRAMPWROK, COREPWROK.
- Due to the active low polarity of the IRQB signal, the IRQB LED input has been inverted so that a low IRQB turns the LED on. As a result, when VSYS is present but PMIC_EN is low, the IRQB LED turns on even though there is no interrupt since the device is off.

Table 3. Other Connectors

Designator	Description
S1	In order from left to right, the switches are for: PMICEN, DDR_SEL, SLP_S0IXB, SLP_S3B, SLP_S4B, DDRVTCTRL. Note: the “ON” (up) position shorts the CTL signals to GND. As a result, to enable an active high signal, the switch should be set to the “OFF” (down) position.
D6	Indicator light for successful USB connection.
D1	GPO1 - RSMRSTB status indicator
D2	GPO2 – DRAMPWROK status indicator
D3	GPO3 – COREPWROK status indicator
D4	GPO4 – VCCAPWROK status indicator
D5	Inverted IRQB status indicator (since IRQB is active low)

7 Setup

The typical sequence for the switches is CTL1 (PMICEN), CTL5 (SLP_S4B), CTL4 (SLP_S3B) with CTL3 (SLP_S0IXB) already enabled to move through the sequence. From there, the CTL3 (SLP_S0IXB) pin can be toggled to test Connected Standby.

Figure 1 is an example setup for using the TPS65084x EVM:

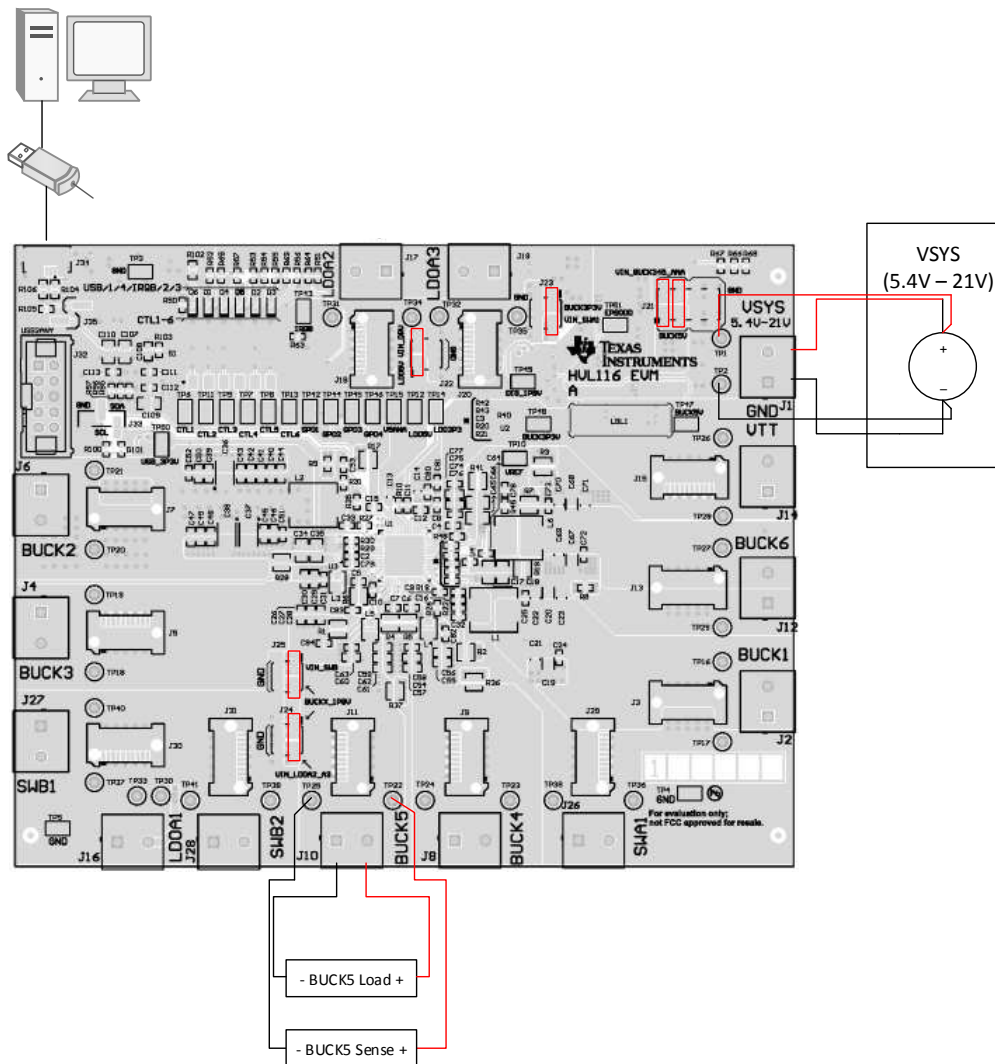


Figure 1. TPS65084x EVM Setup

8 Software

8.1 Software Installation Instruction

A GUI is supplied to provide a simple way to communicate to the device via I²C. The GUI can be downloaded from:

<http://www.ti.com/tool/IPG-UI>

Additional installers are needed to update the GUI to contain the register map for this device. They can be downloaded from:

https://ti.com/licreg/docs/swlicexportcontrol.tsp?form_id=184041&prod_no=TPS65084X_94X&ref_url=hval_jpg

Information on the installation of the IPG-UI can be found in the *IPG-UI User's Guide (SLVUAH9)*

8.2 Using the TPS65084x GUI

Detailed information on the usage of the IPG-UI can also be found in the *IPG-UI User's Guide* (SLVUAH9). A brief overview is provided here for reference.

The proper device must first be selected from the "Select Devices" drop-down menu.

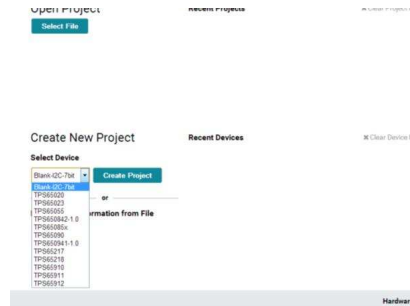


Figure 2. GUI Front Page

From there, the next screen is the device introduction page, which includes a brief overview as well as the functional block diagram for the device.

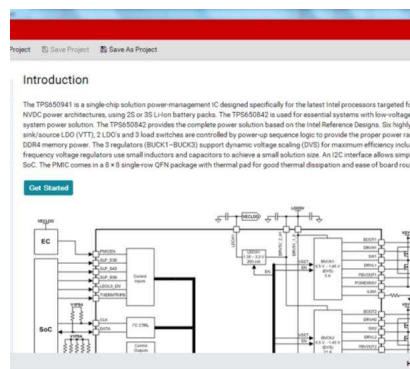


Figure 3. GUI Device Introduction

Finally, clicking on "Get Started" or on "Register Map" takes you to the I²C controls for the device sorted by register address.

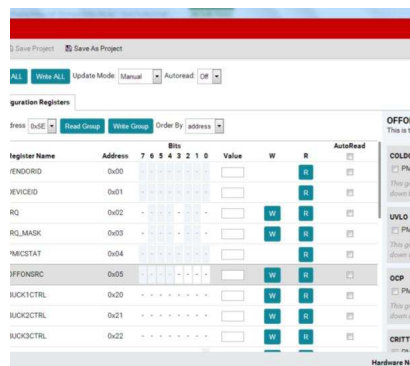


Figure 4. GUI Register Map

With this information, it is possible to begin evaluating the TPS65084x device.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2015) to A Revision	Page
• Fixed typo in URL for the installers in the <i>Software</i> section	2

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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