TPS65291 EVM User's Guide

The TPS65291EVM is an evaluation module (EVM) for the TPS65291 power management unit (PMU) device, which is primarily used in gas and water meters. In addition to gas and water meters, the TPS65291 device can be used in any low-power, portable industrial application powered from a single-cell (1S) or dual-stacked (2S) Lithium-Ion (Li-Ion) battery.

This document provides a description of how to setup and configure the EVM for operation. This document also includes hardware documentation, including the schematic, layout and bill of materials,as well as software instructions for installing the IPG-UI graphical user interface (GUI).

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1 Introduction (Board Overview)

The TPS65291EVM allows designers to evaluate the operation and performance of the TPS65291 PMU. The TPS65291EVM is simple to test, requiring only a single power supply at the input, a USB cable connected to a computer running the GUI, and a load at the output to measure performance. With no load or a light load on the EVM, only the USB cable is required to power the TPS65291 device from the 5 V provided by the VBUS wire of USB. The computer and GUI is used to communicate to the TPS65291 device through the SPI protocol.

The 50-mA BUCK2 output of the TPS65291 device is always-on, meaning it is enabled when an adequately high voltage of at least 3.0 V is applied to the B2_VIN pin by a power supply. The performance of BUCK2 can be measured without additional connections.

The 1-A BUCK1 output and the LDO_SW (configurable LDO or switch) output of the TPS65291 device must be enabled by communicating to the TPS65291 device through SPI from a host controller. On the EVM, an MSP430™ MCU is programmed as a USB2ANY device, and the SPI signals (CLK, MOSI, MISO, and CS) are hard-wired to the TPS65291 device so that only a USB cable must be plugged into the EVM to enable BUCK1 and LDO_SW. The B1_VIN pin can be shorted to the B2_VIN pin to provide power to both DC-DC bucks.

The TPS65291EVM is *perforated* such that the printed circuit board (PCB) is split into two distinct sections. The upper section, shown in Figure 1, contains the TPS65291 device, required passive components, test points, and banana jacks for applying input power and loads. The lower section of the PCB contains components not relevant to the evaluation of the TPS65291 device. Instead, the MSP430 MCU and other simple circuitry on this section of the PCB are used for communicating to the TPS65291 device through SPI and controlling the device from a computer with a USB cable.

If the two sections of the PCB are split apart, they can be connected by using a standard keyed 10-pin ribbon cable with 2 rows by 5 pins and 100-mil pitch. The lower half is now a standard USB2ANY device with SPI, I^2C, 2 GPIOs, and a controllable 3.3-V output rail provided by a 150-mA LDO.

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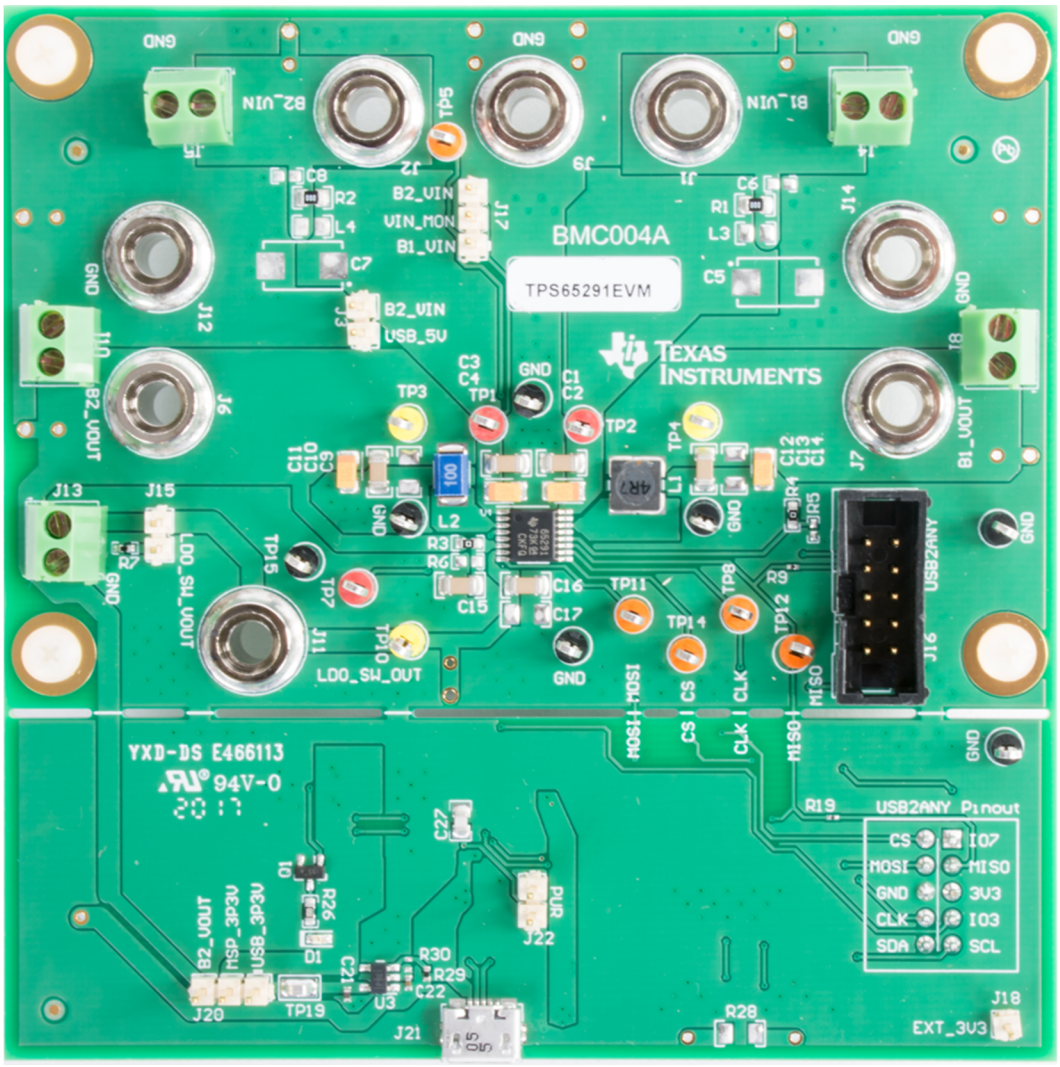

Figure 1. TPS65291EVM Printed Circuit Board (Top View)

1.1 Related Documentation

Texas Instruments, *TPS65291 High-Efficiency Solution for Multi-Stacked Battery Systems* data sheet

1.2 TPS65291 Applications

The TPS65291 can be used in, but not limited to,the following applications:

- Low-power energy harvesting systems
- Battery powered applications
- Gas and water maters
- POL supply from single (1S) or dual (2S) Li-Ion batteries
- Higher-efficiency LDO replacement

2 Getting Started

Figure 2 shows the high-level block diagram of the TPS65291EVM, highlighting important integrated circuits (ICs) and connections, the upper and lower sections of the PCB, and the interface between the EVM and a computer.

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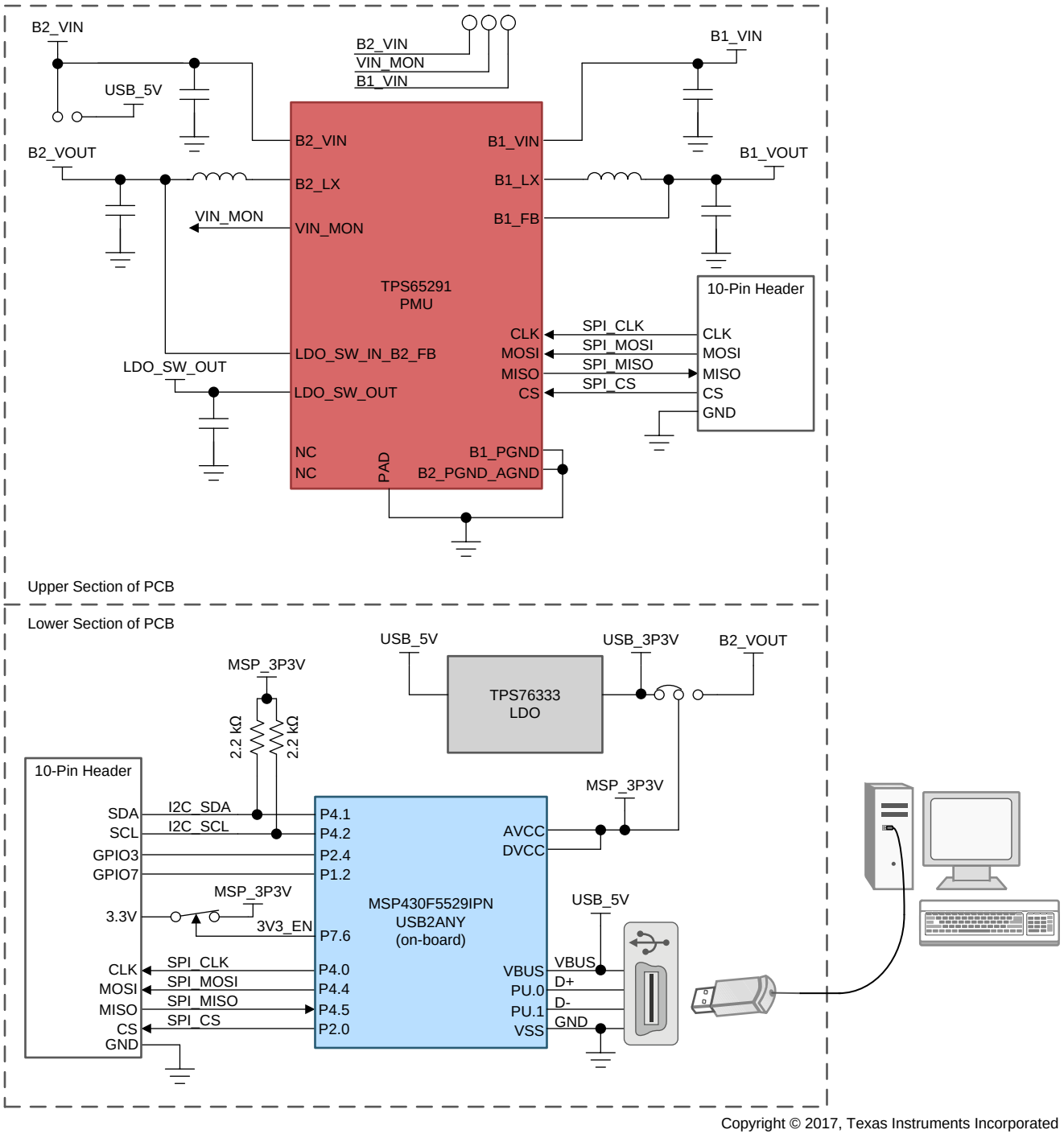

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Figure 2. TPS65291EVM Block Diagram

2.1 Power Connections

This section describes the banana jacks and screw terminals for applying input power to and delivering output power from the TPS65291EVM.

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NOTE: Banana jacks and screw terminals allow two different connection options for providing power to or delivering power from the input and output pins of the TPS65291. For each power connection, use either banana plugs or screwed-in wires; do not use both.

Figure 3 shows the test setup for applying power to both B1_VIN (J1) and B2_VIN (J2) on the TPS65291EVM from a single power supply and measuring the output voltage B2_VOUT (J6) when power is first applied.

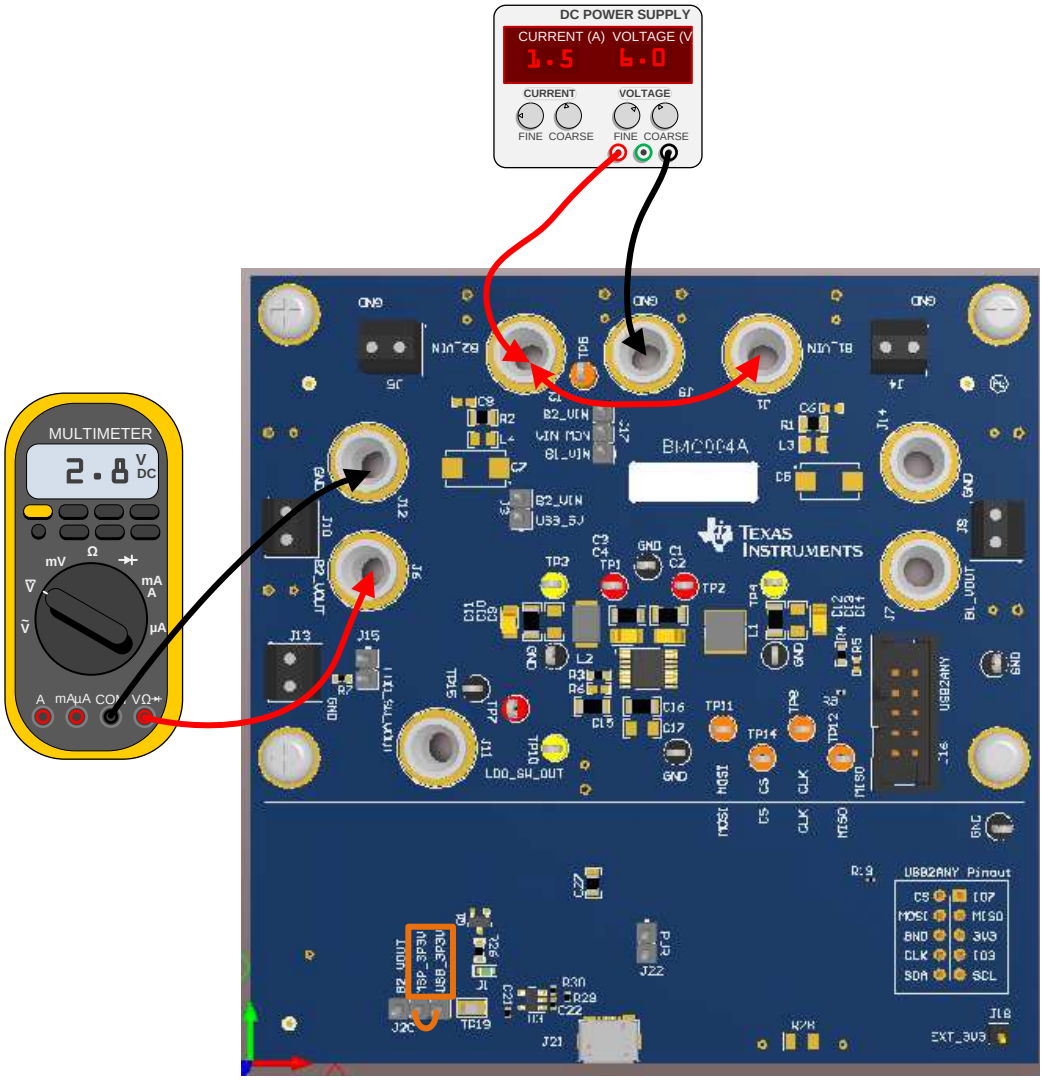

Figure 3. TPS65291 Test Setup: Power Supply and Multi-meter Connections

J1 (B1_VIN) and J9 (GND), or J4 (pin 2 = B1_VIN, pin 1 = GND) — TheJ1 and J9 banana jacks and the J4 screw terminal are for providing power to BUCK1 through the positive lead (+) of a power supply and a return path to ground through the negative lead (–).

J2 (B2_VIN) and J9 (GND), or J5 (pin 1 = B2_VIN, pin 2 = GND) — TheJ2 and J9 banana jacks and the J5 screw terminal are for providing power to BUCK2.

J6 (B2_VOUT) and J12 (GND), or J10 (pin 2 = B2_VOUT, pin 1 = GND) — TheJ6 and J12 banana jacks and the J10 screw terminal are for attaching a load to draw power from BUCK2.

J11 (LDO_SW_VOUT) and J12 (GND), or J13 (pin 1 = LDO_SW_VOUT, pin 1 = GND) — TheJ11 and J12 banana jacks and the J13 screw terminal are for attaching a load to draw power from LDO_SW.

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J7 (B1_VOUT) and J14 (GND), or J8 (pin 1 = LDO_SW_VOUT, pin 1 = GND) — TheJ7 and J14 banana jacks and the J8 screw terminal are for attaching a load to draw power from BUCK1.

2.2 Test Points

This section describes the test points located on the TPS65291EVM to measure the voltage of all pins of the TPS65291 device. Table 1 lists the test points.

Table 1. TPS65291EVM Test Point List

PCB Reference Designator	Color	Type	Net Name
TP1	Red	Input power	B2_VIN
TP2	Red	Input power	B1_VIN
TP3	Yellow	Output power	B2_VOUT
TP4	Yellow	Output power	B1_VOUT
TP5	Orange	Data output	VIN_MON
TP7	Red	Input power	LDO_SW_IN
TP8	Orange	Data input	CLK
TP10	Yellow	Output power	LDO_SW_OUT
TP11	Orange	Data input	MOSI
TP12	Orange	Data output	MISO
TP14	Orange	Data input	CS
TP6, TP9, TP13, TP15-TP18 (1)	Black	Ground	PGND, AGND, thermal pad
TP19	Metal (Surface Mount)	MSP430 power rail	USB_3P3V
J17 (2)	3-Pin Header	Input power	B1_VIN (pin 1)
		Data output	VIN_MON (pin 2)
		Input power	B2_VIN (pin 3)
J18 (2)	Header	MSP430 power output	EXT_3V3

(1) Ground test points are labeled GND (except for TP15) and do not show TPxx on the silk-screen of the PCB.
(2) Headers used as test points are tin or gold-plated tin but do not have colored plastic and are designated Jxx instead of TPxx.

CAUTION

J17 does not allow for the installation of a shunt to short two pins together. The center pin, VIN_MON, is an output that indicates a valid input supply on the B1_VIN or B2_VIN pin. The B1_VIN and B2_VIN pins have Kelvin connections routed to the J17 header and should be used for accurately measuring voltage with an oscilloscope.

2.3 Jumpers

This section describes the jumper headers located on the TPS65291EVM for connecting nets of the PCB together to perform various functions. Table 2 lists the jumpers.

Table 2. TPS65291EVM Jumper List

PCB Reference Designator	Pin	Net Name	Default Shunt Connection	Description
J20	1	USB_3P3V	Pins 1 and 2 Shorted	Required to deliver 3.3-V rail to MSP430 and turn on LED D1
	2	MSP_3P3V		
	3	B2_VOUT	—	Optional way to provide 3.3-V rail to MSP430 from TPS65291 BUCK2
J3	1	USB_5V	Not Installed	Optional way to provide 5-V VBUS rail to TPS65291 from USB
	2	B2_VIN		

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Table 2. TPS65291EVM Jumper List (continued)

PCB Reference Designator	Pin	Net Name	Default Shunt Connection	Description
J15	1	LDO_SW_OUT	Not Installed	Optional light load on LDO_SW
	2	GND		
J22	1	PUR	Not Installed	Short to re-flash firmware to MSP430
	2	VUSB		

Figure 3 shows the required jumper installation on J20. Figure 4 shows J20 installed correctly.

2.4 Cable Connections

When the PCB is first taken out of the box, the only cable connection required is a Standard-A to micro-B USB cable. Connect the micro-USB plug to J21 and the other end (standard-A plug) of the USB cable into a USB2or USB3 port of a computer.

If the PCB is split into two sections so that the lower half can be used as a stand-alone USB2ANY, a keyed 10-pin ribbon cable must be connected between J19 and J16 to control the TPS65291 device through SPI. Figure 4 shows these connections.

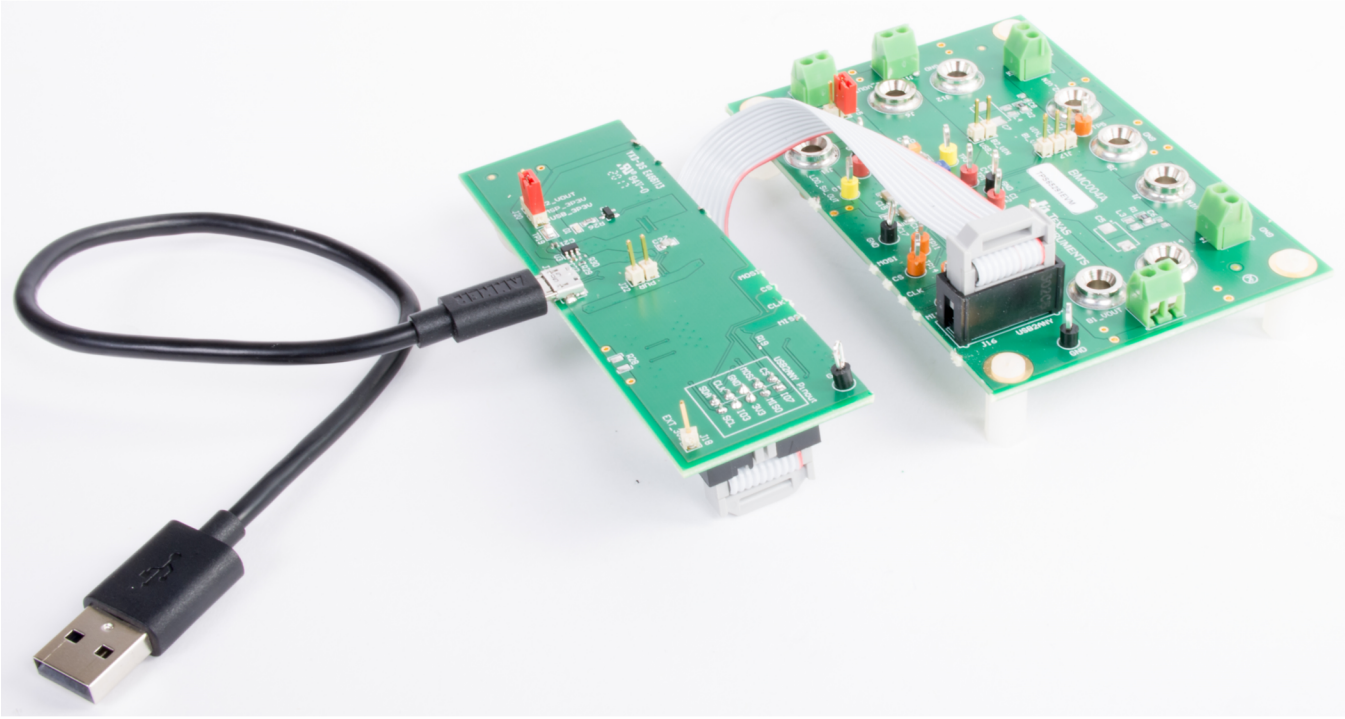

Figure 4. TPS65291EVM Split With Ribbon Cable Between USB2ANY and TPS65291 Sections

WARNING

Do not split the PCB into two sections without protection. Protective glasses and gloves should be worn. First, use wire cutters to partially sever the connections between the two sections on both top and bottom. Then, connect one end to a rigid surface with a vice grip. Finally, grab the other end of the PCB firmly with pliers and bend back and forth slowly until the two sections separate.

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2.5 EVM Operation

This section describes the power-on procedure and the software instructions to enable BUCK1 and LDO_SW. When these procedures are complete, a load can be applied in parallel to the multi-meter shown in Figure 3.Probes can be placed on any test point in Table 1 to evaluate the full performance of the TPS65291 device.

2.5.1 Power-On Procedure

After setting up the hardware to match the test setup shown in Figure 3, follow these instructions to verify the voltage on the always-on BUCK2 rail:

- Set the input supply voltage to 6V and ensure it is off before connecting to the EVM.
- Connect the power supply return lead (the black cable) to the J9 header.
- Apply the input power lead (the red cable) to J1 and a jumper cable from J1 to J2.
- Ensure that the current limit on the supply is 1.5 A.
- Connect the voltage lead of digital multi-meter (DMM) to B2_VOUT (J6) and connect the GND lead to J12.
- Turn the power supply on and observe the voltage on the DMM measuring J6 (B2_VOUT):
  - Measure (with the DMM) and verify the BUCK2 output voltage at J6 is approximately 2.8 V.
- Move the voltage lead of the DMM to J11 (LDO_SW_VOUT):
  - Measure (with the DMM) and confirm that LDO_SW is disabled.
- Move the voltage lead of the DMM to J7 (B1_VOUT):
  - Measure (with the DMM) and confirm that BUCK1 is disabled.

2.5.2 Software Instructions to Enable BUCK1 and LDO_SW

After verifying the operation of BUCK2, follow these instructions to enable BUCK1 and LDO_SW:

- Click the *Read All* button and verify that some values other than 0x00 (hexadecimal) appear in the **Register0** row of the register map table, as shown in Figure 5.
- Click the *Read All* button again and most blue highlighted '1's will turn white or gray, indicating that these bits have not changed since the last time they were read.

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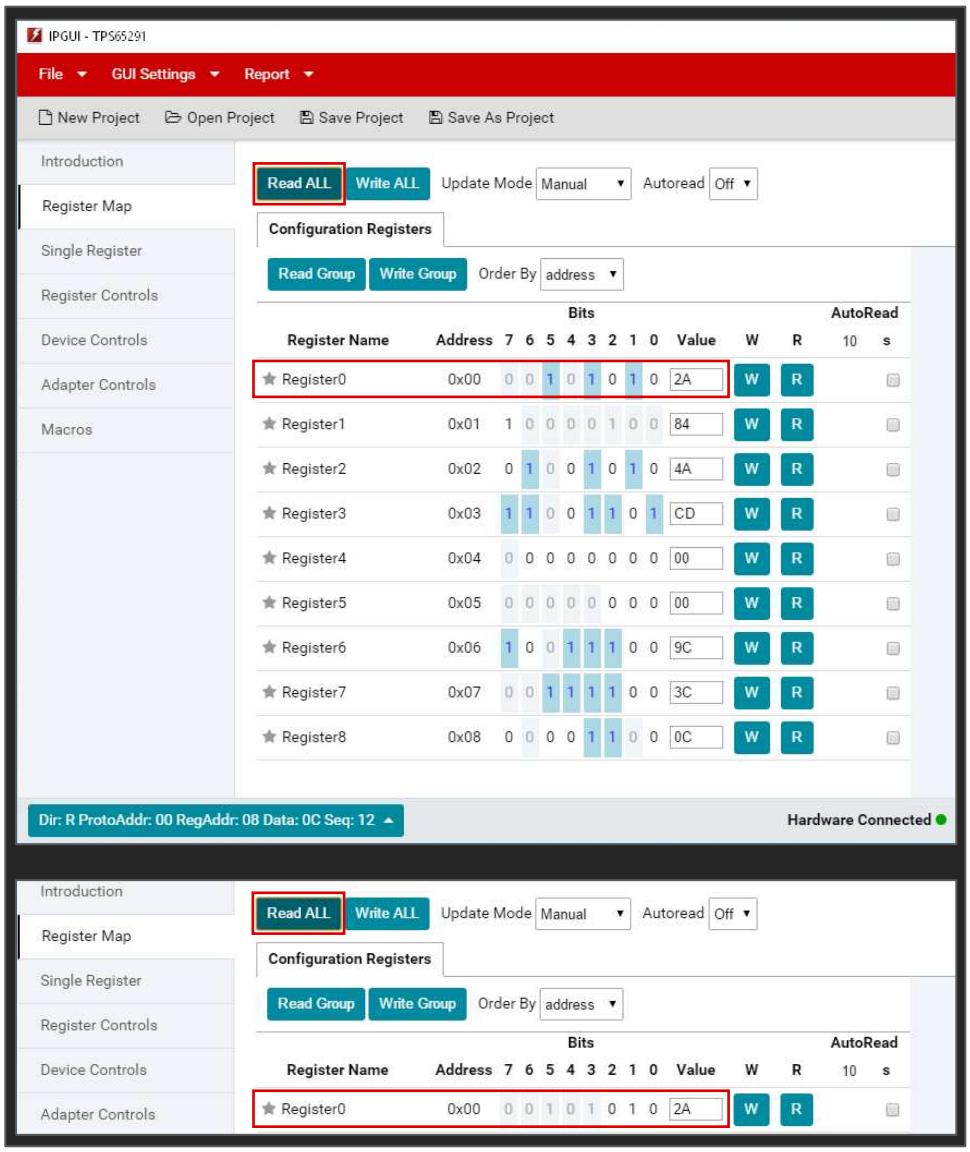

Figure 5. Successful Completion Read ALL Registers in IPG-UI

- Click the **Register0** row so that it is highlighted in gray and shows the **Register0** contents.
- Hover the mouse over Bit 1 to verify that **B2_Enreg** is *Enabled*, as shown in Figure 6.

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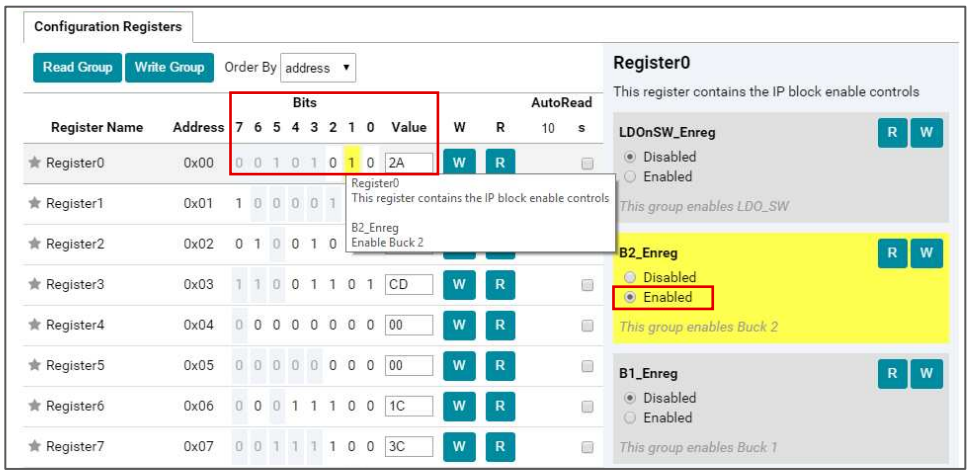

Figure 6. B2_Enreg is Enabled by Default in IPG-UI

- Change the **B1_Enreg** position from *Disabled* to *Enabled* while the red voltage lead of the DMM is still on J7 (B1_VOUT), and then click the *W* button in the **Register0** row to write new values to only this register. Figure 7 shows that bit 0 now has a value of 1b, **B1_Enreg** is *Enabled*, and that until the *W* button is clicked the changes made have not yet been written to the TPS65291 device.
  - Measure (with the DMM) and verify the voltage at J7 is approximately 3 V.

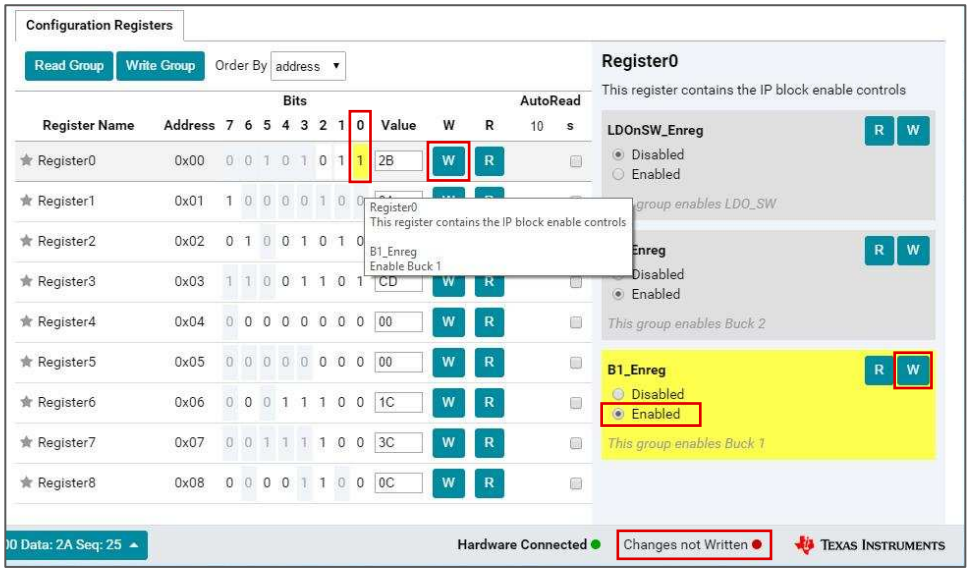

Figure 7. Enabling BUCK1 (B1_Enreg) in IPG-UI

- Move the red voltage lead of the DMM to J11 (LDO_SW_VOUT), change the **LDOnSW_Enreg** position from *Disabled* to *Enabled*, and then click the *W* button in the **Register0** row. Figure 8 shows that bit 2 now has a value of 1b, **LDOnSW_Enreg** is *Enabled*, and that after the *W* button is pressed all changes made by the user in the GUI have been written to the TPS65291 device. If more than one register is changed at a time, then the *Write All* function will be faster than writing to each register one at a time.
  - Measure (with the DMM) and verify the voltage at J11 is approximately 2.8 V, or 5 to 10 mV below B2_VOUT because LDO_SW is configured as a load switch by default.

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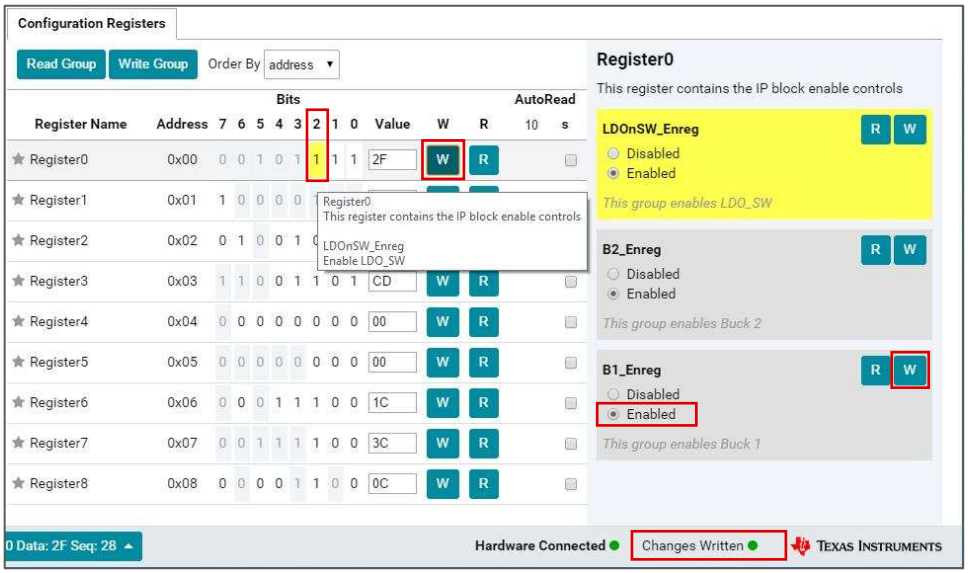

Figure 8. Enabling LDO_SW (LDOnSW_Enreg) in IPG-UI

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A.1 Layout

Figure 9 through Figure 14 show the board layout for the TPS65291EVM.

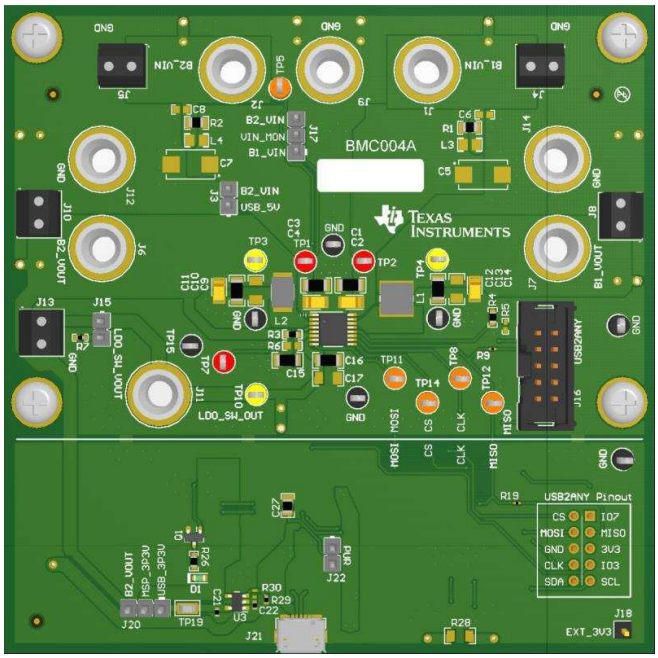

Figure 9. Component Placement—Top Assembly

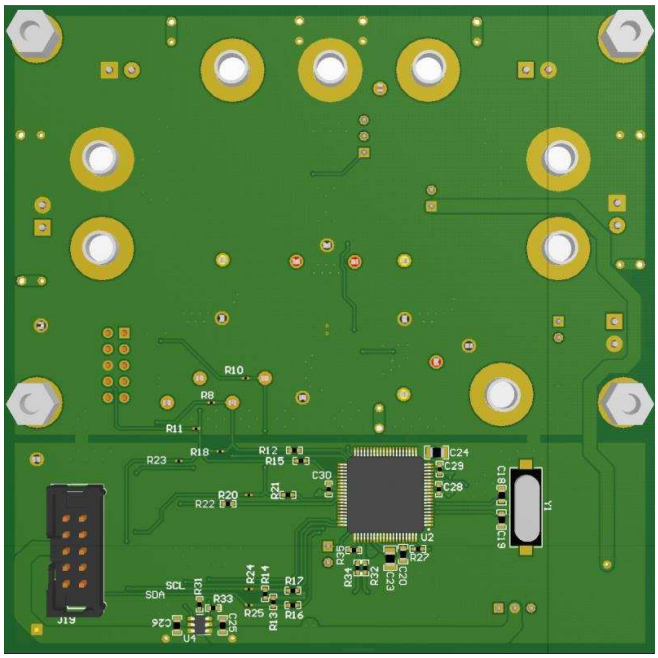

Figure 10. Component Placement—Bottom Assembly

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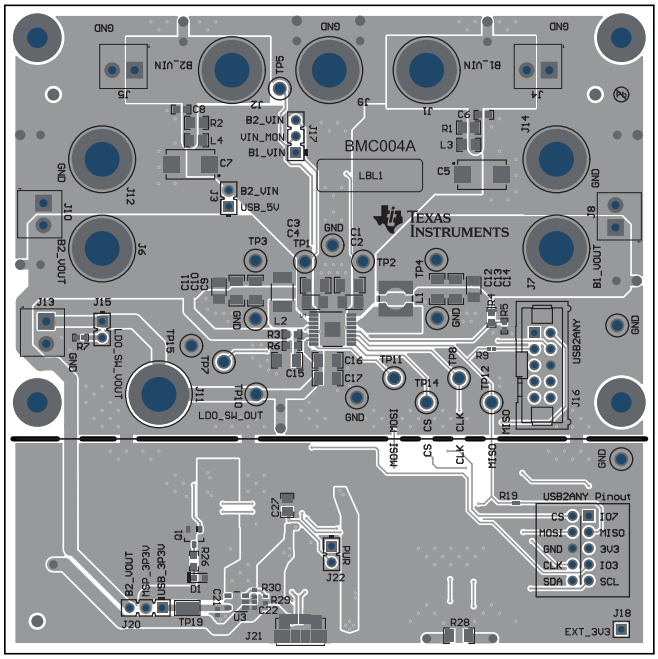

Figure 11. Layout—Top Composite

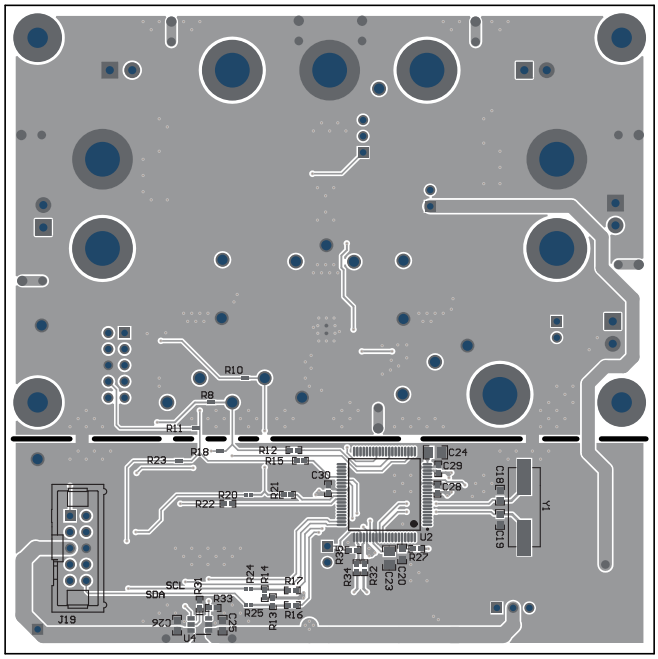

Figure 12. Layout—Bottom Composite

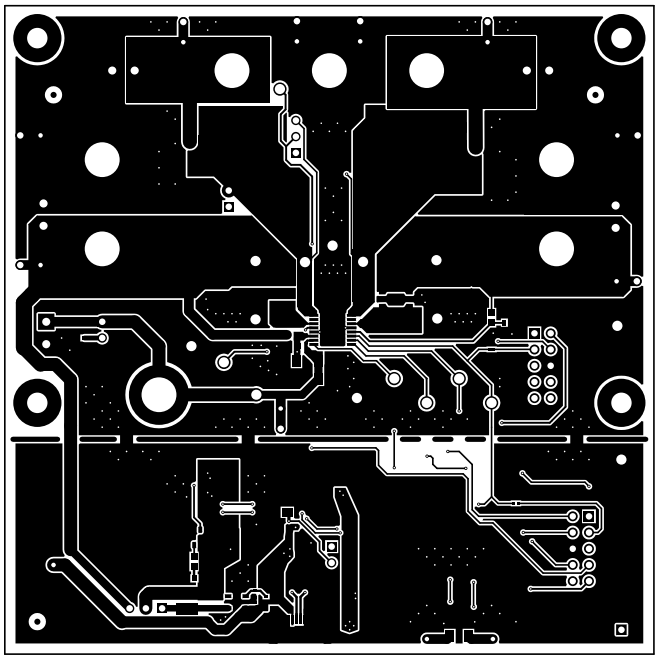

Figure 13. Top Layer

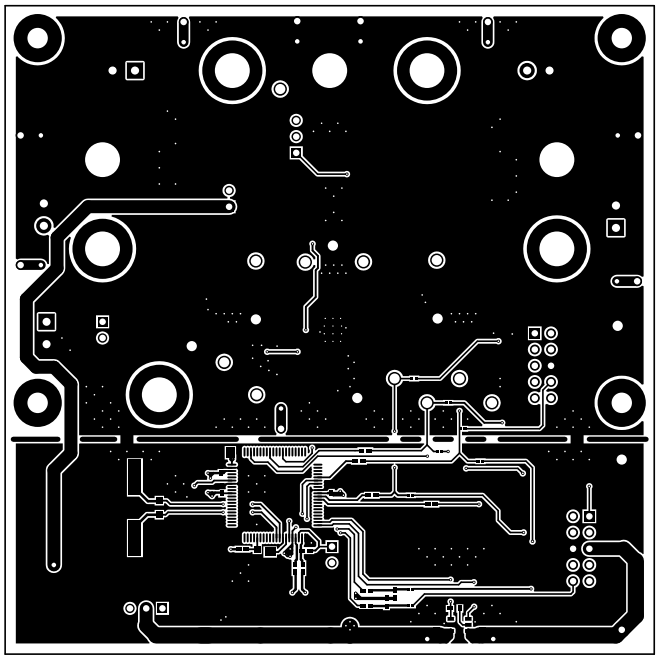

Figure 14. Bottom Layer (Top View)

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A.2 Schematic

Figure 15 shows the schematic of the TPS65291EVM.

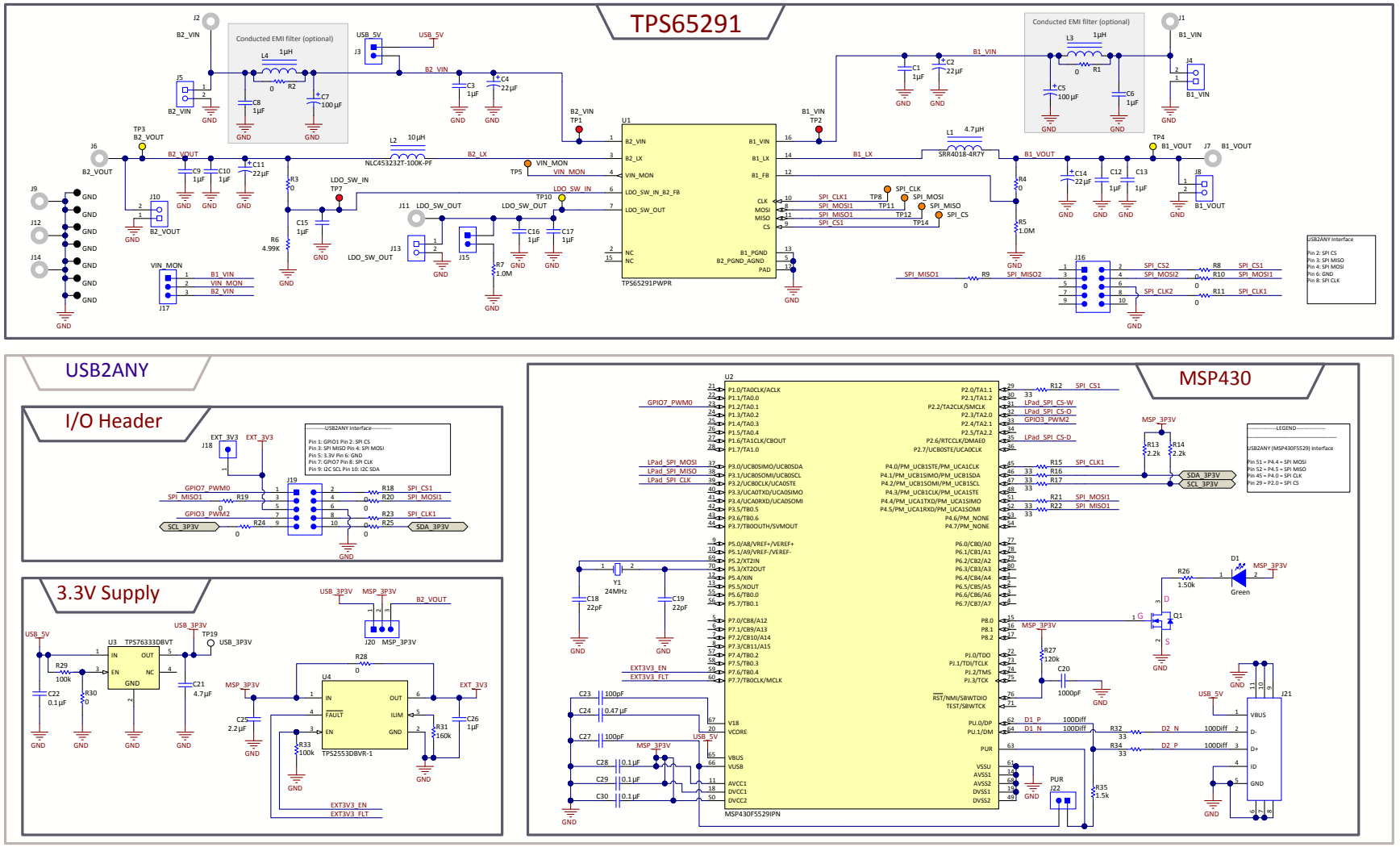

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Figure 15. TPS65291EVM Schematic

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A.3 Bill of Materials

Table 3 provides the bill of materials (BOM) for the TPS65291EVM.

Table 3. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		BMC004	Any
C1, C3, C10, C12, C15, C16	6	1uF	CAP, CERM, 1uF, 25V, +/-10%, X7R, 1206	1206	12063C105KAT2A	AVX
C2, C4, C11, C14	4	22uF	CAP, TA, 22 µF, 10 V, +/- 10%, 3 ohm, AEC-Q200 Grade 1, SMD	3216-18	TAJA226K010RNJ	AVX
C18, C19	2	22pF	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A220JAT2A	AVX
C20	1	1000pF	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	0603	C0603C102K5RACTU	Kemet
C21	1	4.7uF	CAP, CERM, 4.7 µF, 6.3 V, +/- 20%, X5R, 0402	0402	GRM155R60J475ME47D	MuRata
C22, C28, C29, C30	4	0.1uF	CAP, CERM, 0.1 µF, 10 V, +/- 10%, X5R, 0402	0402	GRM155R61A104KA01D	MuRata
C23, C27	2	100pF	CAP, CERM, 100 pF, 50 V, +/- 10%, C0G/NP0, 0805	0805	C0805C101K5GACTU	Kemet
C24	1	0.47uF	CAP, CERM, 0.47 µF, 16 V, +/- 5%, X7R, 0805	0805	0805YC474JAT2A	AVX
C25	1	2.2uF	CAP, CERM, 2.2 µF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata
C26	1	1uF	CAP, CERM, 1 µF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A105KA61D	MuRata
D1	1	Green	LED, Green, SMD	LED_0603	150060VS75000	Wurth Elektronik
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J2, J6, J7, J9, J11, J12, J14	8		Standard Banana Jack, Uninsulated, 8.9mm	Keystone575-8	575-8	Keystone
J3, J15, J22	3		Header, 2.54 mm, 2x1, Tin, TH	Header, 2.54 mm, 2x1, TH	TSW-102-07-T-S	Samtec
J4, J5, J8, J10, J13	5		Terminal Block, 3.5mm Pitch, 2x1, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology
J16, J19	2		Header (shrouded), 100mil, 5x2, High-Temperature, Gold, TH	5x2 Shrouded header	N2510-6002-RB	3M
J17, J20	2		Header, 2.54 mm, 3x1, Tin, TH	Header, 2.54 mm, 3x1, TH	TSW-103-07-T-S	Samtec
J18	1		Header, 100mil, 1pos, Gold, TH	Testpoint	TSW-101-07-G-S	Samtec
J21	1		Connector, Receptacle, Micro-USB Type B, R/A, Bottom Mount SMT	7.5x2.45x5mm	0473460001	Molex
L1	1	4.7uH	Inductor, Drum Core, Ferrite, 4.7 µH, 1.65 A, 0.082 ohm, SMD	Inductor, 4.8x1.8x4.8mm	SRR4018-4R7Y	Bourns
L2	1	10uH	Inductor, Wirewound, Ferrite, 10 µH, 0.55 A, 0.5 ohm, SMD	4.5x3.2x3.2mm	NLC453232T-100K-PF	TDK
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650"H x 0.200"W	THT-14-423-10	Brady
Q1	1	50V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R1, R2	2	0	RES, 0, 5%, 0.333 W, 0805	0805	CRCW08050000Z0EAHP	Vishay-Dale
R3	1	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R4	1	0	RES, 0, 5%, 0.1 W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R7	1	1.0Meg	RES, 1.0 M, 5%, 0.063 W, 0402	0402	CRCW04021M00JNED	Vishay-Dale
R8, R9, R10, R11, R18, R19, R20, R23, R24, R25	10	0	RES, 0, 5%, 0.05 W, 0201	0201	CRCW02010000Z0ED	Vishay-Dale
R12, R15, R16, R17, R21, R22, R32, R34	8	33	RES, 33, 5%, 0.063 W, 0402	0402	CRCW040233R0JNED	Vishay-Dale
R13, R14	2	2.2k	RES, 2.2 k, 5%, 0.063 W, 0402	0402	CRCW04022K20JNED	Vishay-Dale
R26	1	1.50k	RES, 1.50 k, 1%, 0.1 W, 0603	0603	CRCW06031K50FKEA	Vishay-Dale
R27	1	120k	RES, 120 k, 1%, 0.063 W, 0402	0402	CRCW0402120KFKED	Vishay-Dale
R29, R33	2	100k	RES, 100 k, 5%, 0.063 W, 0402	0402	CRCW0402100KJNED	Vishay-Dale
R31	1	160k	RES, 160 k, 5%, 0.063 W, 0402	0402	CRCW0402160KJNED	Vishay-Dale
R35	1	1.5k	RES, 1.5 k, 5%, 0.063 W, 0402	0402	CRCW04021K50JNED	Vishay-Dale
TP1, TP2, TP7	3		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone

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Table 3. Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
TP3, TP4, TP10	3		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint	5014	Keystone
TP5, TP8, TP11, TP12, TP14	5		Test Point, Multipurpose, Orange, TH	Orange Multipurpose Testpoint	5013	Keystone
TP6, TP9, TP13, TP15, TP16, TP17, TP18	7		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
TP19	1	SMT	Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	5015	Keystone
U1	1		High efficiency solution for multi-stacked batteries systems, PWP0016C (TSSOP-16)	PWP0016C	TPS65291PWPR	Texas Instruments
U2	1		Mixed Signal MicroController, PN0080A	PN0080A	MSP430F5529IPN	Texas Instruments
U3	1		Single Output LDO, 150 mA, Fixed 3.3 V Output, 2.7 to 10 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS & no Sb/Br)	DBV0005A	TPS76333DBVT	Texas Instruments
U4	1		Adjustable, Active High, Latch-off, Current-Limited Power-Distribution Switch, DBV0006A (SOT-23-6)	DBV0006A	TPS2553DBVR-1	Texas Instruments
Y1	1		Crystal, 24.000MHz, 20pF, SMD	Crystal, 11.4x4.3x3.8mm	ECS-240-20-5PX-TR	ECS Inc.
C5, C7	0	100uF	CAP, TA, 100uF, 16V, +/-20%, 0.125 ohm, SMD	7343-31	TPSD107M016R0125	AVX
C6, C8	0	1uF	CAP, CERM, 1 µF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A105KA61D	MuRata
C9, C13, C17	0	1µF	CAP, CERM, 1uF, 25V, +/-10%, X7R, 1206	1206	12063C105KAT2A	AVX
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A
L3	0	1uH	Inductor, Multilayer, Ferrite, 1 µH, 2 A, 0.08 ohm, SMD	2.0x1.0x1.2mm	LQM21PN1R0MGH	MuRata
L4	0	1uH	Inductor, Multilayer, Ferrite, 1 µH, 0.8 A, 0.19 ohm, SMD	0805	LQM21PN1R0MC0D	MuRata
R5	0	1.0Meg	RES, 1.0 M, 5%, 0.063 W, 0402	0402	CRCW04021M00JNED	Vishay-Dale
R6	0	4.99K	RES, 4.99k ohm, 1%, 0.1W, 0603	0603	CRCW06034K99FKEA	Vishay-Dale
R28	0	0	RES, 0, 5%, 0.25 W, 1206	1206	CRCW12060000Z0EA	Vishay-Dale
R30	0	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale

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Software Installation and Setup Instructions

B.1 IPG-UI Software Installation

The following instructions explain how to install the IPG-UI software on a computer. If this software is already installed, this section may be skipped.

To install the IPG-UI software, first download the IPG-UI software installation package from www.ti.com. Then unzip and install the IPG-UI software tool onto the computer.

B.2 IPG-UI Setup for TPS65291

The following instructions explain how to run, setup, and operate the IPG-UI software on a computer and connect it to the TPS65291EVM.

- Install a shunt on header J20, shorting pin 1 (USB_3P3V) and pin 2 (MSP_3P3V).
- Run the IPG-UI software by using the Windows *Start Menu* and navigating to the Texas Instruments folder, or by double-clicking the desktop icon, as shown in Figure 16.

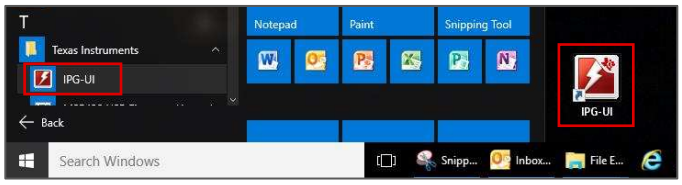

Figure 16. Run the IPG-UI Software

- Wait for the program to load.
- Plug in the micro-USB cable to J21 and connect the other end of the USB cable to an open USB2/3 port on the computer.
- Verify that the software is connected to the USB2ANY as shown in Figure 17.

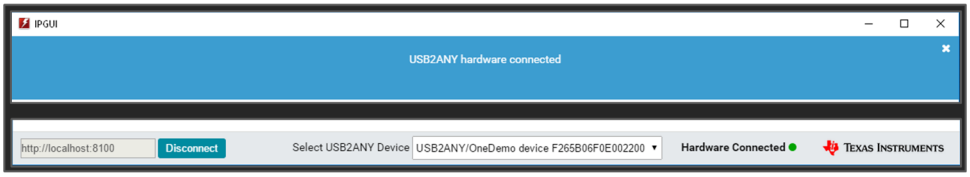

Figure 17. Successful Connection Between Computer and USB2ANY

- Click the drop-down menu in the *Create New Project* section and select *TPS65291-spi-1.x* as shown in Figure 18.

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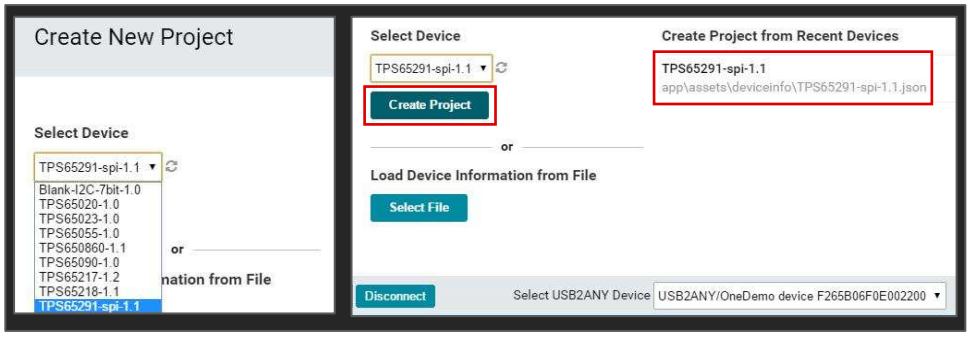

Figure 18. Creating New IPG-UI Project for the TPS65291

- Click the *Create Project* button.

NOTE: After a project is initially created, it is available in the *Create Projects from Recent Devices* menu. When a project is saved, it is available in the *Open Recent Projects* menu.

- Verify that a blue notification appears stating that register write access is enabled as shown in Figure 19.

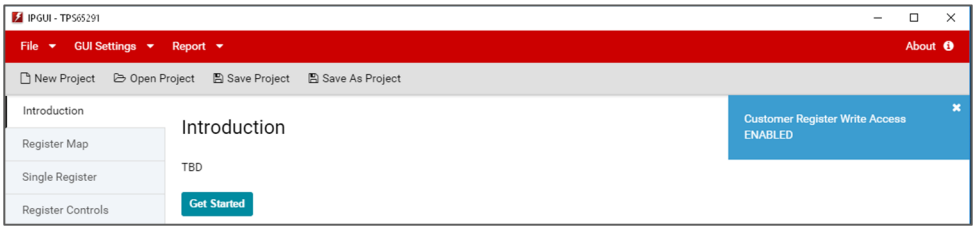

Figure 19. Successful Write Access to TPS65291 Notification

- The TPS65291 *Introduction* tab is now displayed. If a red notification appears (as in Figure 20), it indicates the computer can talk to the USB2ANY but cannot communicate with the TPS65291 device. The primary cause of this issue may be that the power supply is not turned on or a cable is unplugged. In case of either issue, the test setup of the EVM must be debugged before continuing.

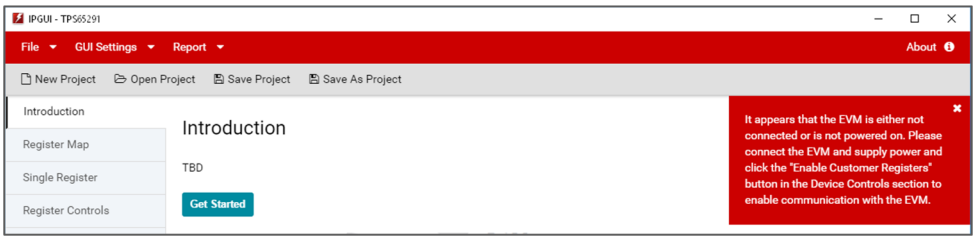

Figure 20. Failed GUI Communication to TPS65291 Notification

- Click the *Get Started* button or the *Register Map* tab shown in Figure 21 to begin reading from and writing to registers to evaluate the TPS65291 device.

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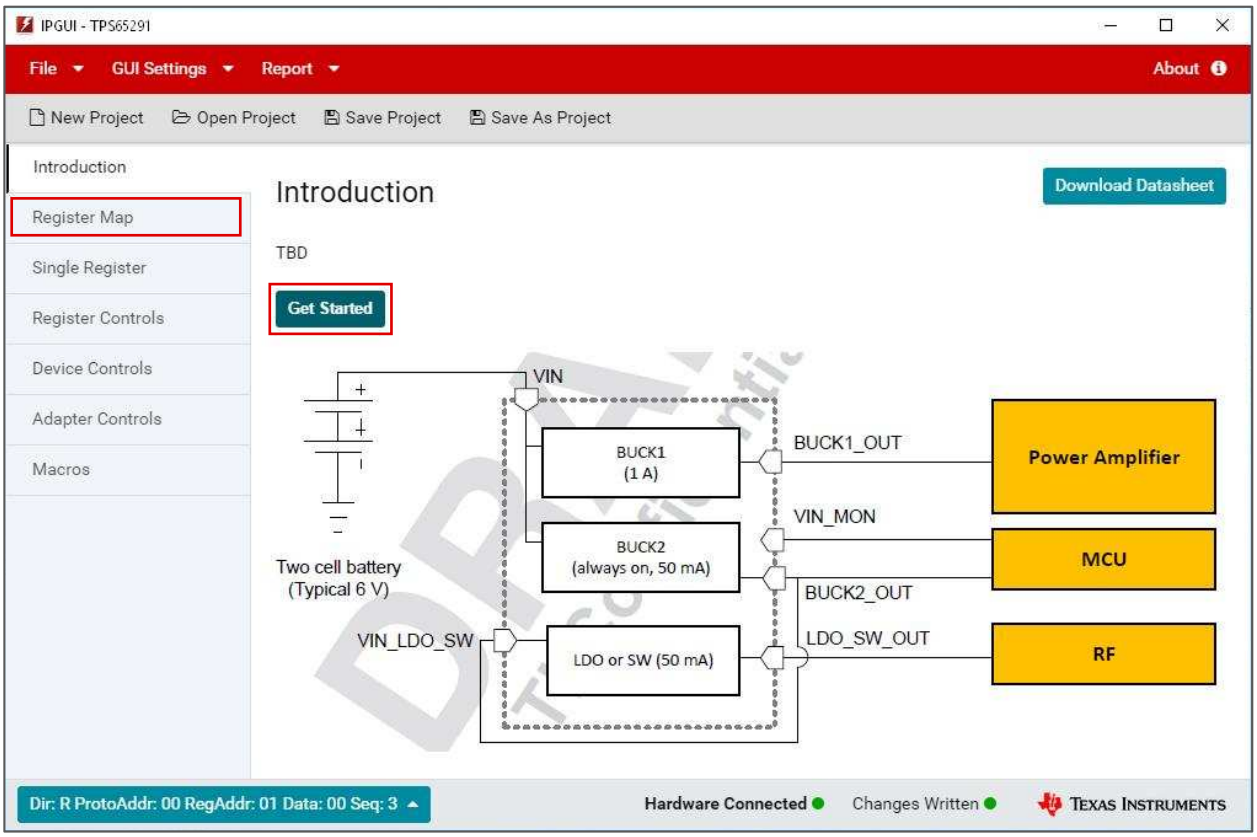

Figure 21. TPS65291 SPI Project Introduction Tab in IPG-UI

NOTE: At present, the IPG-UI software version is 2.5.0.3 and the TPS65291-SPI file version is 1.1.

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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      CAUTION

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FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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