TPS65987DDH and TPS65988DH Host Interface Technical Reference Manual

Technical Reference Manual

Literature Number: SLVUBH2B
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Introduction

1.1 Introduction

1.1.1 Purpose and Scope

This document describes the Host Interface for the TPS65987D and TPS65988 Type-C Port Switch / Power Delivery (PD) Controller devices.

1.1.2 Related Documents

- Universal Serial Bus Specification, Revision 2.0, April 27, 2000 plus ECN and Errata. http://www.usb.org/developers/docs/usb20_docs/
- Battery Charging Specification, Revision 1.2, December 7, 2010 plus Errata.
- Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013 and ECNs approved through August 11, 2014. www.usb.org/developers/docs
- USB Power Delivery Specification Revision 3.0, Version 1.0a www.usb.org/developers/docs
- USB Type-C Cable and Connector Specification Revision 1.2, March 25, 2016. www.usb.org/developers/docs
- VESA DisplayPort (DP) Standard, Version 1.3, September 17, 2014.
- Proposed DisplayPort Alt Mode on USB Type-C Standard, Version 1, Draft 5, September 6, 2014.

1.2 PD Controller Host Interface Description

1.2.1 Overview

The PD Controller provides a slave I2C port to interface to a host. The Host Interface provides general status information about the PD Controller, ability to control the PD Controller, status of USB Type-C Port and communications to/from a connected device and/or cable via USB PD messages.

The PD Controller supports a single I2C address for each USB-C port. A single port device will have a total of one unique I2C address, and a dual port device will have a total of two unique I2C addresses. This unique address for each USB-C port, defined as the Unique I2C address, is used for direct interaction with a specific USB-C port within the PD controller. All Host Interface communication that uses the Unique I2C address is referred to as Unique Address Interface.

The PD Controller supports a register-based Unique Address Interface. Section 1.3.1 lists the Unique Address Interface registers and Table 1-1 provides detailed Unique Address Interface register descriptions.

The key to the protocol diagrams is in the SMBus Specification, version 2.0 and is repeated here in part in Figure 1-1.

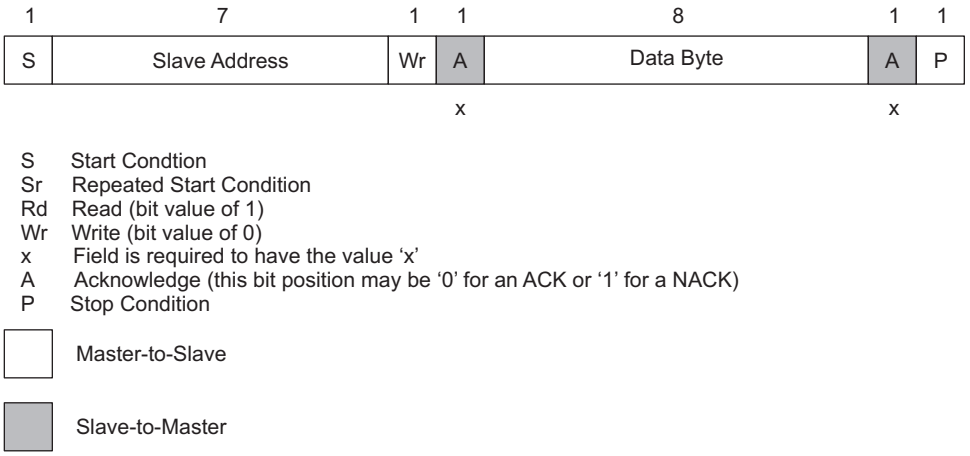

Figure 1-1. I2C Read/Write Protocol Key

1.2.2 Dual Port Addressing

The dual port PD Controller supports two identical ports in a single device. The Host, when present in the system, requires a method to address each port, Port 1 or Port 2, independently over each I2C interface.

For I2C1, Port1 and Port2 addresses are determined by the voltage sensed at the ADCIN2 terminal. The voltage at ADCIN2 is generated by a resistor divider from LDO_3V3 to ground. By changing the divider ratio, four pairs of slave addresses are possible. Each pair of slave addresses corresponds to Port 1 and Port 2 slave addresses. By default, I2C2 Port1 and Port2 addresses are unique but fixed. Refer to the TPS65988 Datasheet for further details. If TBTControllerType is set to 11b in the 0x27 Global System Configuration Register, then I2C2 Port1 and Port2 addresses are set to the same values as the I2C1 Port1 and Port2 addresses.

1.3 Unique Address Interface

1.3.1 Unique Address Interface Protocol

The Unique Address Interface allows for complex interactions between an I2C master and each PD Controller. The I2C Slave unique address is used to receive or respond to Host Interface protocol commands. Figure 1-2 and Figure 1-3 show the write and read protocols, respectively.

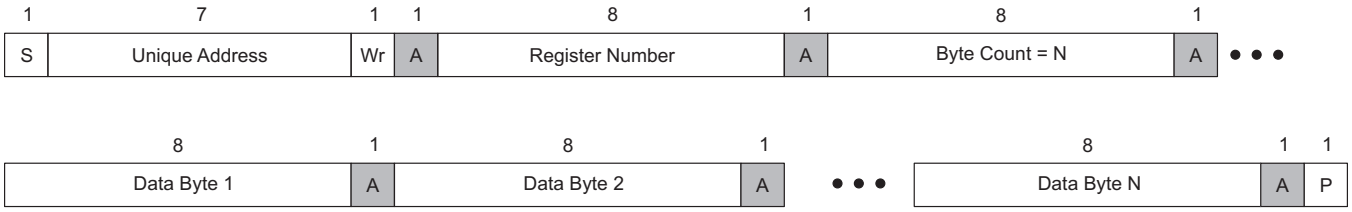

Figure 1-2. I2C Unique Address write register protocol

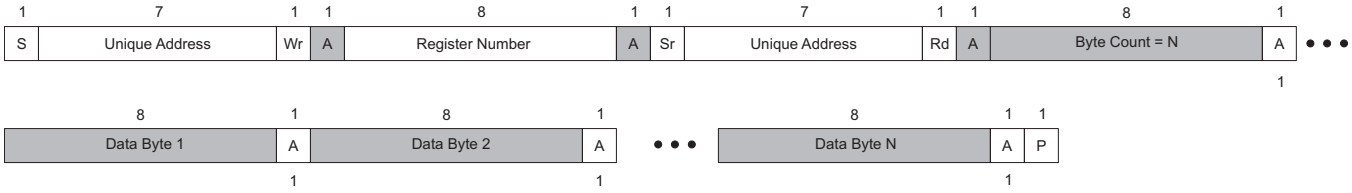

Figure 1-3. I2C Unique Address read register protocol

1.3.2 Unique Address Interface Registers

The PD Controller supports Unique Address Interface registers (Unique Address Registers) provided in Table 1-1. Unless otherwise indicated, registers are little endian (least significant byte in Data Byte 1). Registers that use four character codes (4CC) are defined where the first character corresponds to the ASCII value of Data Byte 1, the second character corresponds to the ASCII value of Data Byte 2, and so forth. Any 4CC codes that are less than 4 characters pad the tail with spaces (0x20). For a dual port PD controller, each port has its own independent set of Unique Address Registers, unless a Unique Address Register specifies that it is a register shared across both ports of the device.

Table 1-1. Unique Address Interface Registers

Register Number[(1)]	Register Name	Read/Write	# Data Bytes	Description
0x00	VID[(2)]	RO	4	Intel-assigned Thunderbolt™ Vendor ID, with the most significant 8 bits of the field padded with 0's. OTP boot loader will use TI's Vendor ID; application firmware may change to another vendor's VID.
0x01	DID[(2)]	RO	4	Vendor-specific Device ID. Boot loader will use Device ID specific to part (expected to be different per TI part number). Application firmware may change to a value specified by vendor.
0x02	ProtoVer[(2)]	RO	4	Thunderbolt™ Protocol Version. Required to return 1 per current specification.
0x03	Mode[(2)]	RO	4CC	Indicates the operational state of the port. 'APP ' = The PD Controller is fully functioning in the application firmware. 'BOOT' = Device booting in dead battery. 'PTCH' = Device in patch mode. Any other value indicates the PD Controller is functioning in a limited capacity.
0x04	Type[(2)]	RO	4CC	PD Controller default response is 'I2C ' (note space as 4th character).
0x05	UID[(2)]	RO	16	128-bit unique ID (unique for each PD Controller Port)
0x06	Customer Use	RO	8	These 8 bytes are allocated for customer use as needed. Initialized by Application Customization.
0x07	Reserved	RO	0	This register is not to be allocated and shall return a length of 0.

(1) Registers marked (Lock) may be write-protected unless the LOCK command is used to successfully unlock registers.
(2) On devices containing two ports, these registers are shared between the ports.

Table 1-1. Unique Address Interface Registers (continued)

Register Number[1]	Register Name	Read/Write	# Data Bytes	Description
0x08	Cmd1	RW	4CC	Command register used for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of “!CMD”.
0x09	Data1	RW	64	Data register used for the primary command interface.
0x0A-0x0E	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x0F	Version[2]	RO	4	Binary Coded Decimal version number, bootloader/application code version.Represented as VVVV.MM.RR with leading 0’s removed.e.g. 65794d (decimal) -> 0x00010102 -> 0001.01.02 -> 1.1.2 (version). The version information is returned in little Endian format i.e. byte 1 = RR, byte 2 = MM, etc.
0x10	Cmd2	RW	4CC	Command register used for the secondary command interface. Shall be cleared to 0x00000000 by PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register it shall be replaced by a 4CC value of “!CMD”.
0x11	Data2	RW	64	Data register used for the secondary command interface.
0x12-0x13	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x14	IntEvent1	RO	11	Interrupt event bit field for I2C_IRQ1 (output is low if any bit in this register is set). See Table 3-1.
0x15	IntEvent2	RO	11	Interrupt event bit field for I2C_IRQ2 (output is low if any bit in this register is set). See Table 3-1.
0x16	IntMask1	RW	11	Interrupt mask bit field corresponding to IntEvent1. A bit in IntEvent1 cannot be set if it is cleared in this register. See Table 3-1.
0x17	IntMask2	RW	11	Interrupt mask bit field corresponding to IntEvent2. A bit in IntEvent2 cannot be set if it is cleared in this register. See Table 3-1.
0x18	IntClear1	RW	11	Interrupt clear bit field for IntEvent1. Bits set in this register are cleared from IntEvent1. See Table 3-1.
0x19	IntClear2	RW	11	Interrupt clear bit field for IntEvent2. Bits set in this register are cleared from IntEvent2. See Table 3-1.
0x1A	Status	RO	8	Status bit field for non-interrupt events. See Table 3-3.
0x1B-0x1F	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x20	System Power State[3]	RW	1	System Power State 0x00 = S0, 0x03 = S3, 0x04 = S4, 0x05 = S5
0x21	Discovered SVIDs	RO	49	SVID information returned from Discover SVIDs messages
0x22-0x25	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x26	Power Path Status[3]	RO	8	Power Path Status. See Table 3-7.
0x27	Global System Configuration[3]	RW	14	Configuration bits that define hardware that is common to all ports and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. See Table 3-9. Initialized by Application Customization.
0x28	Port Configuration	RW	8	Configuration bits that define hardware that is specific to a the respective port and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. See Table 3-11. Initialized by Application Customization.

(3) On devices containing two ports, these registers are shared between the ports.

Table 1-1. Unique Address Interface Registers (continued)

Register Number[1]	Register Name	Read/Write	# Data Bytes	Description
0x29	Port Control	RW	4	Configuration bits affecting system policy. These bits may change during normal operation and are used for controlling the respective port. The PD Controller will not take immediate action upon writing. Changes made to this register will take effect the next time the appropriate policy is invoked. See Table 3-14. Initialized by Application Customization.
0x2A	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x2B	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x2C	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x2D	Boot Flags[3]	RO	12	Provides details on PD Controller boot flags and silicon revision. See Table 3-15.
0x2E	Build Identifier[3]	RO	49	ASCII string returns uniquely identifying custom build information.40 Hex Characters representing the build + 1 underscore character + MMDDYYYY (build date) + null terminator (0).Returns 0 length on released firmware.
0x2F	Device Info[3]	RO	47	ASCII string with hardware and firmware version information of the PD Controller.
0x30	RX Source Capabilities	RO	29	Stores latest Source Capabilities message received over BMC. See Table 3-17.
0x31	RX Sink Capabilities	RO	29	Stores latest Sink Capabilities message received over BMC. See Table 3-19.
0x32	TX Source Capabilities	RW	64	Stores PDOs and settings for outgoing Source Capabilities messages to send over BMC See Table 3-21 . Initialized by Application Customization.
0x33	TX Sink Capabilities	RW	57	Stores PDOs for outgoing Sink Capabilities messages to send over BMC. See Table 3-23. Initialized by Application Customization.
0x34	Active Contract PDO	RO	6	Stores PDOs data for the current contract. See Table 3-25.
0x35	Active Contract RDO	RO	4	Stores the RDO of the current contract, or all zeroes if no contract. See Table 3-27.
0x36	Sink Request RDO	RO	4	Most recent RDO sent by Sink, regardless of current PD Controller power role. May not be the current contract if an Accept has not yet been sent or if a Reject/Wait has been sent instead. Once it becomes active, it will be copied into register 0x35. See Table 3-29 .
0x37	Auto Negotiate Sink	RW	20	Defines the voltage range between which the system can function properly, allowing the PD Controller to negotiate its own contracts. Initialized by Application Customization. See Table 3-31.
0x38	Alternate Mode Entry Sequence	RW	16	Allows for selection of up to four alternate modes along with their sequence for auto entry attempt. A single mode will be entered automatically if valid. See Table 3-33. Initialized by Application Customization.
0x39-0x3E	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x3F	Power Status	RO	2	Status bit field for data consumed by the System Power Policy Manager. See Table 3-35.
0x40	PD Status	RO	4	Status bit field for PD messages and state machine. See Table 3-37.
0x41	PD3.0 Status	RO	4	Satus bit field for PD3.0 messages and state machine. See Table 3-39.
0x42	PD3.0 Configuration	RW	4	PD3.0 configuration settings. See Table 3-41.
0x43	Delay Configuration	RW	9	Delay configuration settings. See Section 3.22.
0x44-0x46	Reserved	RO	0	These registers are not allocated and return a length of 0.

Table 1-1. Unique Address Interface Registers (continued)

Register Number(1)	Register Name	Read/Write	# Data Bytes	Description
0x47	TX Identity	RW	49	Data to send over BMC as a response to Discover Identity. See Table 3-45. Initialized by Application Customization.
0x48	RX Identity SOP	RO	28	Latest Discover Identity response received over BMC from standard SOP. See Table 3-47.
0x49	RX Identity SOP'	RO	28	Latest Discover Identity response received over BMC from standard SOP'. See Table 3-49.
0x4A	User VID Configuration	RW	64	User VID Configuration. See Table 3-51. Initialized by Application Customization.
0x4B-0x4D	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x4E	RX Attention	RO	29	Latest Structured VDM Attention Initiator message received over BMC. NOTE: Only Structured VDM "Attention" messages get stored in this buffer. See register 0x4F for all other inbound VDMs:See Table 3-55.
0x4F	RX VDM	RO	29	Latest VDM message received over BMC except for Structured VDM Attention Initiator messages and SOP*_Debug messages). See Table 3-57.
0x50	Data Control	RW	6	Data provided by the Thunderbolt Controller. See .
0x51	DP SID Configuration	RW	6	DisplayPort Alternate Mode configuration. See Table 3-61. Initialized by Application Customization.
0x52	Intel VID Configuration	RW	7	Intel VID Thunderbolt Alternate Mode Configuration. See Table 3-63. Initialized by Application Customization.
0x53	Reserved	RO	0	Reserved.
0x54	Reserved	RO	0	Reserved.
0x55	Reserved	RO	0	Reserved.
0x56	Reserved	RO	0	Reserved.
0x57	User VID Status	RO	2	User VID Status. See Table 3-65.
0x58	DP SID Status	RO	37	DisplayPort Alternate Mode Status. See Table 3-67.
0x59	Intel VID Status	RO	9	Intel VID Thunderbolt Alternate Mode Status. See Table 3-69.
0x5A	Reserved	RO	0	Reserved.
0x5B	Reserved	RO	0	Reserved.
0x5C	GPIO Configuration(4)	RO	64	Application-specific GPIO Configurations. See Table 3-71.
0x5D	Retimer Debug Mode	RW	4	Holds data read from Retimer's Debug Mode Register
0x5E	Reserved	RO	0	Reserved.
0x5F	Data Status	RO	5	Status bit field of data consumed by the System Data Policy Manager. See Table 3-77.
0x60	RX User VID Attention VDM	RO	29	Latest Structured VDM Attention Initiator message received for User VID. See Table 3-80.
0x61	RX User VID Other VDM	RO	29	Latest Unstructured VDM or a non-Attention Structured VDM received for User VID. See Table 3-82.
0x62	Binary Indices	RW	12	See .
0x63	MIPI VID Status	RO	0	See Section 3.42

(4) These registers are used by the TPS6598x Application Customizer Tool to properly configure the device. Modifying these registers directly is not supported by TI.

Table 1-1. Unique Address Interface Registers (continued)

Register Number[1]	Register Name	Read/Write	# Data Bytes	Description
0x64	I2C Master Config	RW	16	See Section 3.43
0x66-0x68	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x69	CCn Pin States	RO	4	Contains current status of both CCn pins. See **Table 3-90.**
0x6A	Reserved	RO	0	This register is not allocated and returns a length of 0.
0x6B	HW Control	RW	9	Used to control various hardware peripherals on the device. See Table 3-92.
0x6C	App Config[4]	RO	60	Application-specific Configurations. See .
0x6D - 0x6F	Reserved	RO	0	These registers are not allocated and return a length of 0.
0x70	Sleep Configuration	RW	1	Sleep Configurations. Initialized by application firmware. See Table 3-96.
0x71	RX MIDB SOP	RO	26	Received Manufacturer Info Data Block SOP (MIDB). See Section 3.48.
0x72	GPIO Status[5]	RO	8	Captures status and settings of all GPIO pins. See Table 3-100.
0x73	TX MIDB SOP	RW	26	Transmit Manufacturer Info Data Block SOP (MIDB). See Section 3.50.
0x74	RX ADO	RO	4	Received Alert Message. See Section 3.51.
0x75	TX ADO	RW	4	Transmit Alert Message. See Section 3.52.
0x76	RX SCEDB	RO	24	Received Source Capabilities Extended Data Block (SCEDB). See Table 3-108.
0x77	TX SCEDB	RW	24	Transmit Source Capabilities Extended Data Block (SCEDB). See Table 3-110.
0x78	RX SDB	RO	7	Received Status Data Block (SDB), See Table 3-112.
0x79	TX SDB	RW	7	Transmit Status Data Block (SDB), See Table 3-114.
0x7A	RX BSDO	RO	32	Received Battery Status Data Objects (BSDO). See Table 3-116.
0x7B	TX BSDO	RW	32	Transmit Battery Status Data Objects (BSDO). See Section 3.58.
0x7C	RX BCDB	RO	9	Received Battery Capability Data Block (BCDB). See Table 3-120.
0x7D	TX BCDB	RW	63	Transmit Battery Capability Data Block (BCDB). See Section 3.60.
0x7E	RX MIDB SOP'	RO	26	Received Manufacturer Info Data Block SOP' (MIDB). See Section 3.61.
0x7F	TX MIDB SOP'	RW	26	Transmit Manufacturer Info Data Block SOP' (MIDB). See Section 3.62.
0x80-0xFF	Reserved	RO	0	These registers are not allocated and return a length of 0.

(5) On devices containing two ports, these registers are shared between the ports.

The PD Controller implements the Unique Address Interface Commands defined in Table 1-2.

Table 1-2. Unique Address Interface Commands

Command 4CC[1]	Command Summary	Reference
Gaid	Return to normal operation	See Table 4-2.
GAID	Cold reset request	See Table 4-3.
LOCK	Lock/Unlock writing to certain Unique Address registers	See Table 4-6.
DISC	Simulate port disconnect (Lock)	See Table 4-4.
ABRT	Abort current task	See Table 4-5.
SWSk	PD PR_Swap to Sink	See Table 4-7.
SWSr	PD PR_Swap to Source	See Table 4-8.
SWDF	PD DR_Swap to DFP	See Table 4-9.

(1) Commands marked (Lock) may be write-protected unless the LOCK command is used to successfully unlock the command.

Table 1-2. Unique Address Interface Commands (continued)

Command 4CC[1]	Command Summary	Reference
SWUF	PD DR_Swap to UFP	See Table 4-10.
SWVC	PD VCONN_Swap	See Table 4-11.
SRDY	System ready to sink power	See Table 4-22.
SRYR	SRDY reset	See Table 4-23.
DBfg	Clear Dead Battery Flag	See Table 4-41.
GSkC	PD Get Sink Capabilities	See Table 4-12.
GSrC	PD Get Source Capabilities	See Table 4-13.
HRST	PD issue Hard Reset	See Table 4-15.
CRST	PD issue Cable Reset	See Table 4-16.
VDMs	PD send VDM	See Table 4-17.
GO2M	PD send GotoMin	See .
ANeg	Auto-negotiate sink	See Table 4-40.
AMEn	PD send Enter Mode	See .
AMEx	PD send Exit Mode	See Table 4-19.
AMDs	Start discovery process	See Table 4-20.
GCdm	Get custom discovered modes	See Table 4-21.
SSrC	PD Send Source Capabilities	See .
FLrr	External Flash Load Read Regions (Lock)	See Table 4-29.
FLer	External Flash Erase Region Pointer (Lock)	See Table 4-30.
FLrd	External Flash Read (Lock)	See Table 4-31.
FLem	External Flash Erase Memory (Lock)	See Table 4-34.
FLad	External Flash Start Address (Lock)	See Table 4-32.
FLwd	External Flash Memory Write (Lock)	See Table 4-33.
FLvy	External Flash Verify (Lock)	See Table 4-35.
GPoe	GPIO Output Enable	See Table 4-36.
GPie	GPIO Input Enable	See Table 4-37.
GPsh	GPIO Set Output High	See Table 4-38.
GPsl	GPIO Set Output Low	See Table 4-39.
PTCs	Start Patch Download Sequence (Lock)	See Table 4-24.
PTCd	Patch Download (Lock)	See Table 4-25.
PTCc	Patch Download Complete (Lock)	SeeTable 4-26.
PTCq	Patch Query (Lock)	See Table 4-27.
PTCr	Patch Reset (Lock)	See Table 4-28.
GSCX	PD3.0 Get_Source_Cap_Extended	See Table 4-42.
GSSt	PD3.0 Get_Status	See Table 4-43.
GBaS	PD3.0 Get_Battery_Status	See Table 4-44.
GBaC	PD3.0 Get_Battery_Cap	See Table 4-45.
GMfi	PD3.0 Get_Manufacturer_Info	See Table 4-46.
MBWr	PD3.0 Message Buffer Write	See Table 4-47.
MBRd	PD3.0 Message Buffer Read	See Table 4-48.
FRSw	PD3.0 Send FR_Swap message	See .
SRrq	Security Request	See Table 4-49.
SRrs	Security Response	See Table 4-50.
ALRT	Send Alert message.	See Table 4-51.

PD Controller Policy Modes

2.1 Overview

The PD Controller implements modes for “SRC Policy” (handing out Source contracts), modes for “SNK Policy” (issuing Requests for Sink contracts), and modes for “AM Policy” (Alternate Mode negotiation).

2.2 Source Policy Modes

The SRC Policy modes supported are:

- SRCAutomaticMode (default)
- MultiPortSourcePolicyMode

In all SRC Policy modes, the PD Controller uses the *TX Source Capabilities* register to know what PDO(s) to advertise.

In SRCAutomaticMode, the PD Controller will automatically respond to Request messages as appropriate, and each port acts independently. Each port will advertise the PDO(s) contained in its respective *TX Source Capabilities* register. Explicit contracts made on one port will not affect the other port. This is the default SRC Policy Mode of the device, no specific bit needs to be set in the Unique Address Registers.

In MultiPortSourcePolicyMode, the PD Controller will automatically response to Request messages as appropriate, and each port will advertise the PDO(s) contained in its respective *TX Source Capabilities* register. However, once one port negotiates an explicit contract that is above the USB default power contract, the other port is limited to only negotiating USB default power contracts. MultiPortSourcePolicyMode is enabled by setting bit 7 to 1 in Byte13-14 of the *Global System Configuration* register. When bit 7 is set to 0 in Byte13-14 of the *Global System Configuration* register, SRCAutomaticMode is enabled.

2.3 Sink Policy

The SNK Policy modes supported are:

- SNKAutomaticMode (default)
- MultiPortSinkPolicyMode

In all Sink Policy modes, the PD controller will always prepare its own Request message based on the settings in the *Auto Negotiate Sink* register, and it will send its prepared Request message as soon as it is ready. The PD controller will insure that the timing needed for the Request message for USB-PD compliance are met automatically. For the dual port PD controller, in SNKAutomaticMode, each sink port behaves independently and once a source is connected to a port, that port will provide power to the system. For MultiportSinkPolicyMode, only one sink port will enable its sink path at a time to provide power to the system. If both ports are connected to a source, the port with the higher power contract will enable its sink path. MultiPortSinkPolicyMode is enabled by setting bits 1:0 to 01b in Byte13-14 of the *Global System Configuration* register. When bits 1:0 are set to 00b in Byte13-14 of the *Global System Configuration* register, SNKAutomaticMode is enabled.

NOTE: When the Auto Negotiate Sink register is inactive (first 4 bytes are 0), the PD Controller will only issue requests for vSafe5V @ 0mA.

2.4 Alternate Modes and Alternate Mode Policy

Power Delivery enables alternative modes of operation by providing the mechanisms to discover, enter, and exit Alternate Modes. The PD Specification defines mechanisms to discover, enter and exit Modes defined either by a standard or by a particular vendor. These Modes can be supported either by the Port Partner or by a cable connecting the two Port Partners.

The Alternate Mode Policy modes supported are:

- AMAutomaticMode (default)
- MultiPortAMPolicyMode

In all Alternate Mode Policy modes, the PD controller will discover/advertise Alternate Modes automatically and also to enter Alternate Modes automatically based on how its Unique Address Registers are configured. This policy applies both when the PD controller is a DFP and a UFP. For the dual port PD controller, when in AMAutomaticMode, each port operates independently and a specified Alternate Mode can be entered into on both ports simultaneously. For MultiPortAMPolicyMode, only one port may be in a specified Alternate Mode at a time, and Alternate Mode entry is handled on a first come first served basis. MultiPortAMPolicyMode is enabled by setting bits 3:2 to 01b in Byte13-14 of the *Global System Configuration* register. When bits 3:2 are set to 00b in Byte13-14 of the *Global System Configuration* register, AMAutomaticMode is enabled.

Unique Address Interface Register Detailed Descriptions

3.1 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Registers

Table 3-1. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Registers

Address	Name	Access	Length	Power-Up Default
0x14	IntEvent1	Read Only	11	0
0x15	IntEvent2	Read Only	11	0
0x16	IntMask1	Read/Write	11	1 (Initialized by Application Customization)
0x17	IntMask2	Read/Write	11	1 (Initialized by Application Customization)
0x18	IntClear1	Read/Write	11	0
0x19	IntClear2	Read/Write	11	0

Table 3-2. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Register Bit Field Definitions

Bits	Name	Description
Byte 11: Patch Status		
7:2	Reserved	Reserved.
1	ReadyForPatch	The device is ready to receive a patch bundle from the host.
0	PatchLoaded	Patch was loaded to the device.
Bytes 9-10:		
15	AlertMessageReceived	Alert Message received.
14	ChunkRequestReceived	Chunk Request message received.
13	ChunkResponseReceived	Chunk Response message received.
12	FRSsignalReceived	FRS swap signaling received.
11:7	Reserved	Reserved.
6	Ack_Timeout	Set whenever Ack_Timeout changes
5:3	Reserved	Reserved.
2	RXMemBufferFull	Receive memory buffer full.
1	TXMemBufferEmpty	Transmit memory buffer empty.
0	PD3StatusUpdate	Set whenever contents of PD3.0 Status register (0x41) change.
Byte 5-8:		
31	Intel_VID_StatusUpdate	Set when the contents of Intel VID Status register (0x59) change.
30	DP_SID_StatusUpdate	Set when the contents of DP SID Status register (0x58) change.
29	Reserved	Reserved.
28	Reserved	Reserved.
27	UserVIDAltModeOtherVDM	A User VID structured non-Attention VDM or unstructured VDM has been received.
26	UserVIDAltModeAttnVDM	A User VID structured Attention VDM has been received.
25	UserVIDAltModeExited	A User VID alternate mode has been exited.
24	UserVIDAltModeEntered	A User VID alternate mode has been entered.
23	Reserved	Reserved.

Table 3-2. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Register Bit Field Definitions (continued)

Bits	Name	Description
22	Reserved	Reserved.
21	Reserved	Reserved.
20	ExitModeComplete	Set when the Exit Mode process is complete.
19	DiscoverModesComplete	Set when the Discover Modes process has completed.
18	Vendor_Defined_Message_Sent	An interrupt to notify that a vendor defined message was sent
17	AMEnteredMode	Set when any alternate mode is entered
16	AMEntryFail	Set when any alternate mode attempted and failed. This can be used by a UFP to signal a Billboard event.
15	BISTMessageIgnored	Set when PD Controller receives a BIST message but ignored the message due to VBUS not a vSafe5V or unsupported BIST mode.
14	Error_UnableToSource	The Source was unable to increase the voltage to the negotiated voltage of the contract.
13	Reserved	Reserved.
12	ProcHot	A ProcHot event has occured. Clearing this interrupt also causes the ProcHot GPIO event to deassert.
11	Plug_Early_Notification	Interrupt for the Ice-Lake Platform
10	SNKtransitionComplete	This event occurs when the Sink Port State is in transition (PE_SNK_Select_Capability → PE_SNK_Transition_Sink). Note: Entering PE_SNK_Transition_Sink due to a GotoMin message does not trigger this event, it triggers GotoMinReceived instead.
9	Error_DischargeFailed	This bit is set whenever the PD Controller fails to discharge VBUS
8	Reserved	Reserved.
7	Error_MessageData	A message was received and the CRC failed or the data length in the header (“Number of Data Objects”) did not match the actual amount of data received or its signal level caused the message to be deemed invalid.
6	Error_ProtocolError	An unexpected message was received from the partner device.
5	Reserved	Reserved.
4	Error_MissingGetCapMessage	The partner device did not respond to the Get_Sink_Cap or Get_Source_Cap message that was sent.
3	Error_PowerEventOccurred	An OVP or short circuit event occurred on VBUS.
2	Error_CanProvideVoltageOrCurrentLater	The USB PD Source can provide acceptable voltage and current, but not at the present time. A “wait” message was sent or received.
1	Error_CannotProvideVoltageOrCurrent	The USB PD Source cannot provide an acceptable voltage and/or current. A Reject message was sent to the Sink or a Capability Mismatch was received from the Sink.
0	Error_DeviceIncompatible	When set to 1, a USB PD device with an incompatible specification version was connected. Or the partner device is not USB PD capable.
Bytes 1-4:		
31	Cmd2Complete	Set whenever a non-zero value in CMD2 register is set to zero or !CMD.
30	Cmd1Complete	Set whenever a non-zero value in CMD1 register is set to zero or !CMD.
29	VCONNSwapRequested	A VCONN swap was requested by the other device. Unless the PD Controller has been configured to swap automatically, then it is waiting for the host to tell it how to proceed with a SWVC (Swap VCONN) command. See Control Config.ProcessVconnSwap for configuring automatic PR swaps.
28	VCONNSwapComplete	A VCONN swap has completed.
27	PDStatusUpdate	Set whenever contents of PD Status register (0x40) change.
26	StatusUpdate	Set whenever contents of Status register (0x1A) change.
25	DataStatusUpdate	Set whenever contents of Data Status register (0x5F) change.
24	PowerStatusUpdate	Set whenever contents of Power Status register (0x3F) change.
23	PPswitchChanged	Set whenever Power Path Status registers (0x26) change.
22	HighVoltageWarning	Set when Status.HighVoltageWarning transitions from 0 to 1.
21	UsbHostPresentNoLonger	Set when Status.UsbHostPresent transitions to 11b..

Table 3-2. 0x14 - 0x19 IntEventX, IntMaskX, IntClearX Register Bit Field Definitions (continued)

Bits	Name	Description
20	UsbHostPresent	Set when Status.UsbHostPresent transitions to anything other than 11b.
19	GotoMinReceived	The PD Controller has received a GotoMin message while in a contract where the GiveBack flag in the RDO was set. The system needs to reduce power consumption down to the level specified in the Auto Negotiate Sink Register (0x37).
18	DRSwapRequested	A DR swap was requested by the other device. Unless the PD Controller has been configured to swap automatically, then it is waiting for the host to tell it how to proceed with a SWDF (Swap to DFP) or SWUF (Swap to UFP) command. See Port Control.ProcessSwapToDFP and Port Control.ProcessSwapToUFP for configuring automatic DR swaps.
17	PRSwapRequested	A PR swap was requested by the other device. Unless the PD Controller has been configured to swap automatically, then it is waiting for the host to tell it how to proceed with a SWSk (Swap to Sink) or SWSr (Swap to Source) command. See Control Config.ProcessSwapToSink and Control Config.ProcessSwapToSource for configuring automatic PR swaps.
16	LowVoltageWarning	Set when Status.LowVoltageWarning transitions from 0 to 1.
15	SinkCapMsgReady	Sink Capabilities has been updated by far-end device. See RX Sink Capabilities register for details.
14	SourceCapMsgReady	Source Capabilities has been updated by far-end device. See RX Source Capabilities register for details.
13	NewContractAsProv	An RDO from the far-end device has been accepted and the PD Controller is a Source. See Active Contract PDO & Active Contract RDO registers for details.
12	NewContractAsCons	An RDO from the far-end device has been accepted and the PD Controller is a Sink. See Active Contract PDO & Active Contract RDO registers for details.
11	VDMReceived	A Vendor Defined Message has been received. See RX VDM register for details.
10	AttentionReceived	An Attention Message has been received. See RX Attention register for details.
9	Overcurrent	Set whenever Status.Overcurrent changes.
8	BIST	Set whenever Status.BIST changes. See that bit for current status.
7	RdoReceivedFromSink	Set when Source receives RDO from Sink
6	FRSwapComplete	A Fast Role swap has completed.
5	DRSwapComplete	A Data Role swap has completed. See Status Register and PD Status Register for port state.
4	PRSwapComplete	A Power role swap has completed. See Status Register and PD Status Register for port state.
3	PlugInsertOrRemoval	USB Plug Status has Changed. See Status register for more plug details.
2	CableResetEvent	This event occurs when PD Controller sends Cable Reset signaling.
1	PDHardReset	A PD Hard Reset has been performed. See PD Status.HardResetDetails for more information.
0	PDSoftReset	A PD Soft Reset has been performed. See PD Status.SoftResetType for more information.

3.2 0x1A Status Register

Table 3-3. 0x1A Status Register

Address	Name	Access	Length	Power-Up Default
0x1A	Status	Read Only	8	0 (Never fully reset, though many bits change during connect or disconnect)

Table 3-4. 0x1A Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 7-8:			
15:0	Reserved	Reserved.	
Bytes 5-6:			
15:2	Reserved	Reserved.	
1:0	AMStatus	00b	No Alternate Modes attempted.
		01b	At least one Alternate Mode entry successful.
		10b	At least one Alternate Mode entry unsuccessful.
		11b	At least one Alternate Mode entry successful and at least one mode entry unsuccessful.
Bytes 1-4:			
31	Reserved	Reserved.	
30	Ack_Timeout	0b	SoC is responding timely
		1b	Soc has not responded to recent Data Status Update
29	LowVoltageWarning	0b	PD Controller operating as Sink or VBUS voltage is above limit specified by LowVoltageWarningLimit register or port is disconnected.
		1b	PD Controller operating as Source and VBUS voltage is below limit specified by LowVoltageWarningLimit register.
28	HighVoltageWarning	0b	PD Controller operating as Sink or VBUS voltage is below limit specified by HighVoltageWarningLimit register or port is disconnected.
		1b	PD Controller operating as Source and VBUS voltage is above limit specified by HighVoltageWarningLimit register.
27	BIST	0b	No BIST in progress.
		1b	BIST in progress (also indicated by Mode register, 0x03, reading ‘BIST’).
26	Reserved	Reserved.	
25:24	ActingAsLegacy	Indicates when PD Controller has gone into a mode where it is acting like a legacy (non PD) device.	
		00b	PD Controller is not in a legacy (non PD mode)
		01b	PD Controller is acting like a legacy sink. It will not respond to USB PD message traffic.
		10b	PD Controller is acting like a legacy source. It will not respond to USB PD message traffic.
		11b	Reserved.
23:22	UsbHostPresent	00b	No far-end device present providing VBUS or PD Controller power role is Source.
		01b	VBUS is being provided by a far-end device that is a PD device not capable of USB communications.
		10b	VBUS is being provided by a far-end device that is not a PD device.
		11b	VBUS is being provided by a far-end device that is a PD device capable of USB communications.
21:20	VbusStatus	00b	VBUS is at vSafe0V (less than 0.8V)
		01b	VBUS is at vSafe5V (4.75V to 5.5V).
		10b	VBUS is at other PD-negotiated power level and within expected limits.
		11b	VBUS is not within any of the above ranges.
19:7	Reserved	Reserved.	

Table 3-4. 0x1A Status Register Bit Field Definitions (continued)

Bits	Name	Description	
6	DataRole	Indicates current state of PD Controller Data Role once connected.	
		0b	PD Controller is UFP or port is disabled/disconnected.
		1b	PD Controller is DFP.
5	PortRole	Indicates current state of PD Controller C_CCx pulls, and therefore PD Controller Power Role, once connected. This bit does not toggle during Unattached.* state transitions.	
		0b	PD Controller is Sink (C_CCx pull-down active) or port is disabled/disconnected.
		1b	PD Controller is Source (C_CCx pull-up active).
4	PlugOrientation	Indicates port orientation when known (requires connection).	
		0b	Upside-up orientation (plug CC on C_CC1) or orientation unknown or port is disabled/disconnected.
		1b	Upside-down orientation (plug CC on C_CC2).
3:1	ConnState	000b	No connection
		001b	Port is disabled
		010b	Audio connection (Ra/Ra)
		011b	Debug connection (Rd/Rd)
		100b	No connection, Ra detected (Ra but no Rd)
		101b	Reserved (may be used for Rp/Rp Debug connection)
		110b	Connection present, no Ra detected (Rd but no Ra) or Rp detected with no previous Ra detection, includes PD Controller that connected in Attached.SNK.
		111b	Connection present, Ra detected (Rd and Ra detected) or Rp detected with previous Ra detection (assumes PD Controller started as Source and later swapped to Sink).
0	PlugPresent	0b	No plug present.
		1b	Plug present, see ConnState for details.

3.3 0x21 Discovered SVIDs Register

Table 3-5. 0x21 Discovered SVIDs Register

Address	Name	Access	Length	Power-Up Default
0x21	Discovered SVIDs	Read Only	49	0 (Never fully reset, though many bits change during connect or disconnect)

Table 3-6. 0x21 Discovered SVIDs Register Bit Field Definitions

Bits	Name	Description
Bytes 26-49:		
191:176	SvidsSOPPrime11	Twelfth SVID supported by SOP' cable plug
175:160	SvidsSOPPrime10	Eleventh SVID supported by SOP' cable plug
159:144	SvidsSOPPrime9	Tenth SVID supported by SOP' cable plug
143:128	SvidsSOPPrime8	Ninth SVID supported by SOP' cable plug
127:112	SvidsSOPPrime7	Eighth SVID supported by SOP' cable plug
111:96	SvidsSOPPrime6	Seventh SVID supported by SOP' cable plug
95:80	SvidsSOPPrime5	Sixth SVID supported by SOP' cable plug
79:64	SvidsSOPPrime4	Fifth SVID supported by SOP' cable plug
63:48	SvidsSOPPrime3	Fourth SVID supported by SOP' cable plug
47:32	SvidsSOPPrime2	Third SVID supported by SOP' cable plug
31:16	SvidsSOPPrime1	Second SVID supported by SOP' cable plug
15:0	SvidsSOPPrime0	First SVID supported by SOP' cable plug
Bytes 2-25:		
191:176	SvidsSOP11	Twelfth SVID supported by SOP port partner
175:160	SvidsSOP10	Eleventh SVID supported by SOP port partner
159:144	SvidsSOP9	Tenth SVID supported by SOP port partner
143:128	SvidsSOP8	Ninth SVID supported by SOP port partner
127:112	SvidsSOP7	Eighth SVID supported by SOP port partner
111:96	SvidsSOP6	Seventh SVID supported by SOP port partner
95:80	SvidsSOP5	Sixth SVID supported by SOP port partner
79:64	SvidsSOP4	Fifth SVID supported by SOP port partner
63:48	SvidsSOP3	Fourth SVID supported by SOP port partner
47:32	SvidsSOP2	Third SVID supported by SOP port partner
31:16	SvidsSOP1	Second SVID supported by SOP port partner
15:0	SvidsSOP0	First SVID supported by SOP port partner
Byte 1:		
7:4	NumberSVIDsSOPPrime	Number of SVIDs discovered on SOP'
3:0	NumberSVIDsSOP	Number of SVIDs discovered on SOP

3.4 0x26 Power Path Status Register

Table 3-7. 0x26 Power Path Status Register

Address	Name	Access	Length	Power-Up Default
0x26	Power Path Status	Read Only	8	0

Table 3-8. 0x26 Power Path Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 7-8:			
15:0	Reserved	Reserved.	
Bytes 4-6: PP and PP_CABLE overcurrent, RCP			
23:18	Reserved	Reserved.	
17	PP2_RCP	0b	No reverse current protection detected on PP2 switch
		1b	Reverse current protection detected on PP2 switch
16	PP1_RCP	0b	No reverse current protection detected on PP1 switch
		1b	Reverse current protection detected on PP1 switch
15:14	PowerSource	Indicates current PD Controller power source. NOTE: Since the Dead Battery flag forces PD Controller to be powered from VBUS, only 10b is valid when this flag is set. Any other setting indicates that the Dead Battery flag is not set.	
		00b	Reserved.
		01b	PD Controller is powered from VIN_3P3.
		10b	Dead Battery flag is set (PD Controller is powered from VBUS).
		11b	PD Controller is powered from VBUS and Dead Battery flag is not set.
13:12	Reserved	Reserved.	
11	PP2_CableOvercurrent	0b	No overcurrent condition exists on PP2_CABLE switch
		1b	PP2_CABLE a switch is in overcurrent condition
10	PP1_CableOvercurrent	0b	No overcurrent condition exists on PP1_CABLE switch
		1b	PP1_CABLE a switch is in overcurrent condition
9:6	Reserved	Reserved.	
5	PP2Overcurrent	0b	No overcurrent condition exists on PP2 switch.
		1b	PP2 switch is in overcurrent condition.
4	PP1Overcurrent	0b	No overcurrent condition exists on PP1 switch.
		1b	PP1 switch is in overcurrent condition.
3:2	Reserved	Reserved.	
1	PP2_CABLEenabled	Indicates current state of PP2_CABLE power.	
		0b	PP2_CABLE power not enabled.
		1b	PP2_CABLE power enabled.
0	PP1_CABLEenabled	Indicates current state of PP1_CABLE power.	
		0b	PP1_CABLE power not enabled.
		1b	PP1_CABLE power enabled.
Bytes 1-3: PP and PP_CABLE Switch Status			
23:18	Reserved	Reserved.	
17:15	PP4switch	Indicates current state of PP4 GPIO	
		000b	PP4 switch disabled. GPIO set logic low.
		001b	PP4 switch currently disabled due to fault (system output). GPIO set logic low.
		010b	PP4 switch enabled (system output). GPIO set logic high.
		011b	PP4 switch enabled (system input). GPIO set logic high.
		100b-111b	Reserved.

Table 3-8. 0x26 Power Path Status Register Bit Field Definitions (continued)

Bits	Name	Description	
14:12	PP3switch	Indicates current state of PP3 GPIO	
		000b	PP3 switch disabled. GPIO set logic low.
		001b	PP3 switch currently disabled due to fault (system output). GPIO set logic low.
		010b	PP3 switch enabled (system output). GPIO set logic high.
		011b	PP3 switch enabled (system input). GPIO set logic high.
		100b-111b	Reserved.
11:9	PP2switch	Indicates current state of PP2 switch.	
		000b	PP2 switch disabled.
		001b	PP2 switch currently disabled due to fault (system output).
		010b	PP2 switch enabled (system output).
		011b	PP2 switch enabled (system input).
		100b-111b	Reserved.
8:6	PP1switch	Indicates current state of PP1 switch.	
		000b	PP1 switch disabled.
		001b	PP1 switch currently disabled due to fault (system output).
		010b	PP1 switch enabled (system output).
		011b	PP1 switch enabled (system input).
		100b-111b	Reserved.
5:4	Reserved	Reserved.	
3:2	PP2_CABLEswitch	Indicates current state of PP2_CABLE switch.	
		00b	PP2_CABLE switch disabled.
		01b	PP2_CABLE switch currently disabled due to fault (system output).
		10b	PP2_CABLE switch CC1 enabled (system output).
		11b	PP2_CABLE switch CC2 enabled (system output).
1:0	PP1_CABLEswitch	Indicates current state of PP1_CABLE switch.	
		00b	PP1_CABLE switch disabled.
		01b	PP1_CABLE switch currently disabled due to fault (system output).
		10b	PP1_CABLE switch CC1 enabled (system output).
		11b	PP1_CABLE switch CC2 enabled (system output).

3.5 0x27 Global System Configuration

The register fields defined in the Global System Configuration register are for settings that are common to both ports of the device. In most usage cases, these settings will not change in normal operation or will not require immediate action if changed.
Note: Any modifications to this register will cause a port disconnect and reconnect with the new settings.

Table 3-9. 0x27 Global System Configuration Register

Address	Name	Access	Length	Power-Up Default
0x27[1]	Global System Configuration	Read/Write	14	0 (Initialized by application)

(1) This register is shared by all ports.

Table 3-10. 0x27 Global System Configuration Register Bit Field Definitions

Bits	Name	Description	
Bytes13-14:			
15	SPIReadOnly[1]	0b	PD Controller is allowed to attempt SPI flash updates.
		1b	SPI flash updates are not allowed (Setting will disable SPI flash update).
14:12	I2CTimeout[1]	Reset the I2C slave if the I2C timeout is exceeded.	
		000b	25 ms
		001b	50 ms (default)
		010b	75 ms
		011b	100 ms
		100b	125 ms
		101b	150 ms
		110b	175 ms
		111b	1 s
11	Reserved	Reserved (Write 0).	
10:9	MultiPortSinkNonOverlapTime	Controls the amount of time a new Sink input path closes after the old Sink input path opens. This forms a break-before-make condition when controlling Sink paths from both ports. This is only applicable when MultipPortSinkPolcy = 1 and applies to internal switch paths (PP1 or PP2), as well as, externally controlled switch paths (PP3 or PP4).	
		00b	1 ms
		01b	5 ms
		10b	10 ms
		11b	15 ms
8	Reserved	Reserved (Write 0).	
7	MultiPortSourcePolicy	Controls Source Power advertisement for two port operation	
		0b	Do not manage Source Power
		1b	Only one port may source more than USB default
6	MultiPortDRPolicy	Controls Data Role behavior for two port operation	
		0b	Do not manage Data Role
		1b	Only one UFP allowed
5:4	TBTControllerType	00b	Default
		01b	AR
		10b	TR
		11b	ICL

(1) Initialized by Application Customization.

Table 3-10. 0x27 Global System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
3:2	MultiPortAMPolicy	Controls Alternate Mode behavior for two port operation.	
		00b	Each port operates independently.
		01b	Limited Entry. Only one port may be in a specified Alternate Mode concurrently. Alternate Mode entry is handled on a first come first served basis.
		10b-11b	Reserved
1:0	MultiPortSinkPolicy	Controls input switches of each port when both ports are operating as a Sink.	
		00b	No Sink Management. Each Sink path behaves independently and do not consider the states of each other.
		01b	Highest Power. Only one Sink path is enabled at a time. If both ports are connected to a Source, the port with the higher power contract enables its Sink path.
		10b-11b	Reserved
Bytes 11-12:Reserved			
15:4	Reserved	Reserved (write 0).	
3:1	I2CMasterConfig	000b	All I2C masters are disabled
		001b	I2C1 is configured as an I2C master
		010b	I2C3 is configured as an I2C master
		011b	I2C1 and I2C3 are configured as I2C masters
		100b - 111b	Reserved
0	Reserved	Reserved (write 0).	
Bytes 9-10: PP1 and PP2 Over Current Clamp Timeout			
15:13	Reserved	Reserved (write 0).	
12	PP2_OCCTimeoutEnable[1]	Over Current Clamp timeout enable for PP2. This bit must be set to 1 to enable the over current clamp timeout.	
11:8	PP2_OCCTimeout[1]	Over Current Clamp timeout value for PP2. 0100b must be written to these bits to set the over current clamp timeout to 640 µs.	
7:5	Reserved	Reserved (write 0).	
4	PP1_OCCTimeoutEnable[2]	Over Current Clamp timeout enable for PP1. This bit must be set to 1 to enable the over current clamp timeout.	
3:0	PP1_OCCTimeout[2]	Over Current Clamp timeout value for PP1. 0100b must be written to these bits to set the over current clamp timeout to 640 µs.	
Byte 8: Power Path to VBUS Mapping			
7:0	PP_SW_MAP[2]	Maps each power switch to VBUS1 or VBUS2	
		xxxx_xxx0b	PP1 associated with VBUS1
		xxxx_xxx1b	PP1 associated with VBUS2
		xxxx_xx0xb	PP2 associated with VBUS1
		xxxx_xx1xb	PP2 associated with VBUS2
		xxxx_x0xxb	PP3 associated with VBUS1
		xxxx_x1xxb	PP3 associated with VBUS2
		xxxx_0xxxb	PP4 associated with VBUS1
		xxxx_1xxxb	PP4 associated with VBUS2
Byte 7: Reserved.			
7:0	Reserved	Reserved (write 0).	
Bytes 5-6: PP3 and PP4 Configuration			
15:6	Reserved	Reserved (write 0).	

(2) Initialized by Application Customization.

Table 3-10. 0x27 Global System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
5:3	PP4config[2]	Configuration for PP4 switch.	
		000b	PP4 not used and disabled (mapping of PP_SW_MAP for PP4 is do not care).
		001b	PP4 configured for Source (output)
		010b	PP4configured for Sink (input)
		011b	PP4 configured for Sink (input), but will wait for SYS_RDY command (SRDY) before closing the switch.
		100b	PP4 configured for Sink (input) and Source (output).
		101b	PP4 configured for Sink (input) and Source (output), but will wait for SYS_RDY command (SRDY) before closing the switch.
		110b - 111b	Reserved.
2:0	PP3config[2]	Configuration for PP3 switch.	
		000b	PP3 not used and disabled.(mapping of PP_SW_MAP for PP3 is do not care).
		001b	PP3 configured for Source (output)
		010b	PP3 configured for Sink (input)
		011b	PP3 configured for Sink (input), but will wait for SYS_RDY command (SRDY) before closing the switch.
		100b	PP3 configured for Sink (input) and Source (output).
		101b	PP3 configured for Sink (input) and Source (output), but will wait for SYS_RDY command (SRDY) before closing the switch.
		110b - 111b	Reserved.
Bytes 3-4: PP1 and PP2 Configuration			
15:6	Reserved	Reserved (write 0).	
5:3	PP2config[2]	Configuration for PP2 switch.	
		000b	PP2 not used and disabled. (mapping of PP_SW_MAP for PP2 is do not care).
		001b	PP2 configured for Source (output)
		010b	PP2 configured for Sink (input)
		011b	PP2 configured for Sink (input), but will wait for SYS_RDY command (SRDY) before closing the switch.
		100b	PP2 configured for Sink (input) and Source (output).
		101b	PP2 configured for Sink (input) and Source (output), but will wait for SYS_RDY command (SRDY) before closing the switch.
		110b - 111b	Reserved.
2:0	PP1config[3]	Configuration for PP1 switch.	
		000b	PP1 not used and disabled (mapping of PP_SW_MAP for PP1 is do not care).
		001b	PP1 configured for Source (output)
		010b	PP1 configured for Sink (input)
		011b	PP1 configured for Sink (input), but will wait for SYS_RDY command (SRDY) before closing the switch.
		100b	PP1 configured for Sink (input) and Source (output).
		101b	PP1 configured for Sink (input) and Source (output), but will wait for SYS_RDY command (SRDY) before closing the switch.
		110b - 111b	Reserved.
Bytes 1-2:PP_CABLE Configuration			
15:4	Reserved	Reserved (write 0).	

(3) Initialized by Application Customization.

Table 3-10. 0x27 Global System Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
3:2	PP2_CABLEconfig[3]	Configure for PP2_CABLE switches.	
		00b	PP2_CABLE switch not used (no VCONN support).
		01b	PP2_CABLE switch configured for output (current limited). USB spec is guaranteed by source (4.75V-5.5V output).
		10b	PP2_CABLE switch configured for output (current limited). USB spec is NOT guaranteed by source (2.7V-5.5V output). VCONN can only be provided in Powered.Accessory mode.
		11b	Reserved
1:0	PP1_CABLEconfig[3]	Configure for PP1_CABLE switches.	
		00b	PP1_CABLE switch not used (no VCONN support).
		01b	PP1_CABLE switch configured for output (current limited). USB spec is guaranteed by source (4.75V-5.5V output).
		10b	PP1_CABLE switch configured for output (current limited). USB spec is NOT guaranteed by source (2.7V-5.5V output). VCONN can only be provided in Powered.Accessory mode.
		11b	Reserved

3.6 0x28 Port Configuration

The register fields defined in the Port Configuration register are for settings of the hardware specific to the Type-C port used and, in most cases, will not change in normal operation or will not require immediate action if changed.
Note: Any modifications to this register will cause a port disconnect and reconnect with the new settings.

Table 3-11. 0x28 Port Configuration Register

Address	Name	Access	Length	Power-Up Default
0x28	Port Configuration	Read/Write	8	0 (Initialized by application)

Table 3-12. 0x28 Port Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 8:			
7:0	Reserved	Reserved.	
Byte 7: Source Contract Power Threshold GPIO Event			
7:0	PowerThresAsSourceContract	Power threshold setting for triggering GPIO output event indicating Source under contract with a power greater than or equal to the programmed threshold setting. Power threshold = (PowerThresAsSourceContract) * 500 mW.	
Byte 6: Sink Contract Voltage Threshold GPIO Event			
7:0	VoltageThresAsSinkContract	Voltage threshold setting for triggering GPIO output event indicating Sink under contract with a voltage greater than or equal to the programmed threshold setting. Voltage threshold = (VoltageThresSinkContractPort) * 200 mV. See Table 3-74 for GPIO event.	
Bytes 3-5: VBUS_UVP/OVP/SS			
23:21	Reserved	Reserved (Write 0).	
20	EnableUVPDebounce	0b	Disables an additional 40ms firmware debounce to PD Controller UVP
		1b	Enables an additional 40ms firmware debounce to PD Controller UVP
19	Reserved	Reserved (Write 0).	
18:17	SoftStart	Controls soft start on internal power path switch when configured as a Sink. Refer to the datasheet for all parametrics.	
		00b	0.41 V/ms typical
		01b	0.79 V/ms typical
		10b	1.57 V/ms typical
		11b	3.39 V/ms typical
16	VBUS_LowVoltageWarningLevel(1)	0b	When PD Controller is operating as a Source and the VBUS voltage dips below the nominal expected voltage by 10% Status.VBUS_LowVoltageWarning will be set to 1.
		1b	When PD Controller is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 20% Status.VBUS_LowVoltageWarning will be set to 1.
15	VBUS_HighVoltageWarningLevel(1)	0b	When PD Controller is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 10% Status.VBUS_HighVoltageWarning will be set to 1.
		1b	When PD Controller is operating as a Source and the VBUS voltage exceeds the nominal expected voltage by 20% Status.VBUS_HighVoltageWarning will be set to 1.
14:13	VBUS_OvpUsage(1)	00b	As a Sink, if VBUS voltage exceeds VBUS_OvpTripPoint it will be disconnected from the input rails to protect the system.
		01b	As a Sink, if VBUS voltage exceeds the expected maximum voltage on VBUS by more than 5% it will be disconnected from the input rails to protect the system.
		10b	As a Sink, if VBUS voltage exceeds the expected maximum voltage on VBUS by more than 10% it will be disconnected from the input rails to protect the system.
		11b	As a Sink, if VBUS voltage exceeds the expected maximum voltage on VBUS by more than 15% it will be disconnected from the input rails to protect the system.
12:7	VBUS_OvpTripPoint(1)	00h - 3Fh	As a Sink, if the voltage on VBUS exceeds this value and VBUS_OvpUsage is set to 00b, then VBUS1 will be disconnected from the input rails to protect the system. When set to 000000b, the OVP block is disabled if VBUS1_OvpUsage is set to 00b. The threshold in Volts is calculated as VBUS_OvpTripPoint*0.32V + 3.84V. The range is therefore 4.16V to 24V.

(1) Initialized by Application Customization.

Table 3-12. 0x28 Port Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
6:4	VBUS_UvpTripHV(1)	If VBUS voltage drops below the expected minimum voltage (while under a >5V PD contract) by more than the specified percentage as a Sink, the port will be considered disconnected and the VBUS discharge circuit will be enabled until vSafe0V is reached. NOTE: Percentage is calculated from nominal voltage if Fixed PDO, or minimum voltage for Variable and Battery PDOs. An extra -5% is added for Fixed PDOs. Cable voltage drop offset is also applied (operating current * 0.25Ω, maximum 0.75V).	
		000b	5%
		001b	10%
		010b	15%
		011b	20%
		100b	25%
		101b	30%
		110b	40%
		111b	50%
3:1	VBUS_UvpTripPoint5V(1)	If VBUS voltage drops below the specified voltage (while under a 5V PD contract or if no PD contract is in place) as a Sink, the port will be considered disconnected and the VBUS discharge circuit will be enabled until vSafe0V is reached.	
		000b	5%
		001b	10%
		010b	15%
		011b	20%
		100b	25%
		101b	30%
		110b	40%
		111b	50%
0	VBUS_SetUvpTo4P5V(2)	0b	VBUS_UVP is determined by VBSU_UvpTripPoint5V or VBUS_UvpTripHV settings.
		1b	VBUS_UVP is set to 4.5V (overrides VBUS_UvpTripPoint5V and VBUS_UvpTripHV settings).
Bytes 1-2: Port Configuration			
15	Reserved	Reserved (write 0).	
14:13	USB3rate(2)	00b	USB3 not supported
		01b	USB3 Gen1 signaling rate supported
		10b	USB3 Gen2 signaling rate supported
		11b	Reserved
12:11	VCONNsupported(2)	Configuration for VCONN switches.	
		00b	VCONN not supported (disabled).
		01b	Reserved.
		10b	VCONN supported as Source only (reject VCONN_Swap requests).
		11b	VCONN supported as Source/Sink (accept VCONN_Swap requests).
10	Reserved	Reserved (Write 0).	
9:8	SupportTypeCOptions	Controls whether optional Type-C state machine states are supported. NOTE: These states are mutually-exclusive and these options only exist when specific Type-C state machines are used.	
		00b	No Type-C optional states are supported.
		01b	Try.SRC state is supported as a DRP.
		10b	Try.SNK state is supported as a DRP.
		11b	PoweredAccessory state is supported as a SNK.
7	DebugAccessorySupport(2)	0b	Does not support Debug Accessory
		1b	Supports Debug Accessory

(2) Initialized by Application Customization.

Table 3-12. 0x28 Port Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
6	AudioAccessorySupport(2)	0b	Does not support Audio Accessory
		1b	Supports Audio Accessory
5:3	ReceptacleType(2)	Specifies USB-C connection	
		000b	Standard USB2-only USB-C receptacle.
		001b	Standard fully-featured USB-C receptacle.
		010b	Tethered USB2-only cable with USB-C plug.
		011b	Tethered fully-featured cable USB-C plug.
		100b-111b	Reserved
2	Reserved	Reserved (Write 0).	
1:0	TypeCStateMachine	Controls which form of Type-C state machine is active.	
		00b	SINK state machine selected.
		01b	SOURCE state machine selected.
		10b	DRP state machine selected.
		11b	Type-C state machine is disabled (CC neither pulled-up nor pulled-down).

3.7 0x29 Port Control

Table 3-13. 0x29 Port Control Register

Address	Name	Access	Length	Power-Up Default
0x29	Port Control	Read/Write	4	0 (Initialized by application)

Table 3-14. 0x29 Port Control Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4:			
31:30	ChargerDetectEnable(1)	00b	Charger Detect disabled
		01b	BC1.2 detection enabled
		10b	Proprietary charger detection enabled
		11b	BC1.2 and proprietary detection enabled
29	USBDisable	0b	USB not disabled
		1b	USB disabled
28:26	ChargerAdvertiseEnable	000b	Charger advertise disabled
		001b	BC 1.2 CDP advertisement only
		010b	BC 1.2 DCP advertisement only
		011b	DCP 1.2V advertisement only
		100b	DCP Divider3 advertisement only
		101b	DCP auto mode 1 (Divider3, BC1.2 short)
		110b	DCP auto mode 1 (Divider3, 1.2V, BC1.2 short)
		111b	Reserved
25	DCDEnable	0b	Data contact detect disabled
		1b	Data contact detect enabled
24	Resistor15kPresent	0b	15kOhm resistor not present (USB2.0 Host Phy pulldowns not enabled)
		1b	15kOhm resistor present (USB2.0 Host Phy pull-downs enabled)
23:22	Reserved	Reserved (Write 0).	
21	SinkControlBit	0b	Externally Powered bit does not affect sink switches
		1b	If Externally Power bit is also 1, port sink switch is opened
20	AutomaticSinkCapRequest	0b	PD Controller will not request Sink Capabilities from port partner after explicit contract is complete
		1b	PD Controller will request Sink Capabilities from port partner after explicit contract is complete
19	ExternallyPowered(1)	0b	No external power besides VBUS for this PD Controller .
		1b	The system is receiving external power from a source other than VBUS for this PD Controller .
18	ForceUSB3Gen1(1)	0b	Forced Gen1 operation. Data Status.USB3Speed register will always report full capabilities.
		1b	Forced Gen1 operation. Data Status.USB3Speed register will report USB3 Gen1-only.
17	Reserved	Reserved (Write 0).	
16	AutomaticIDRequest(1)	0b	PD Controller will not automatically issue Discover Identity VDM when DFP.
		1b	PD Controller will automatically issue Discover Identity VDM when DFP, to SOP', SOP'', SOP and SOP*_Debug when appropriate.
15	InitiateSwapToDFP(1)	0b	PD Controller does not automatically initiate and send swap to DFP requests to the far-end device.
		1b	PD Controller automatically initiates and sends DR_Swap requests to the far end device when appropriate if presently operating as UFP.

(1) Initialized by Application Customization.

Table 3-14. 0x29 Port Control Register Bit Field Definitions (continued)

Bits	Name	Description	
14	ProcessSwapToDFP(1)	0b	PD Controller does not automatically accept swap to DFP requests from the far-end device.
		1b	PD Controller automatically accepts DR_Swap requests from the far end device if presently operating as UFP.
13	InitiateSwapToUFP(1)	0b	PD Controller does not automatically initiate and send swap to UFP requests to the far-end device.
		1b	PD Controller automatically initiates and sends DR_Swap requests to the far end device when appropriate if presently operating as DFP.
12	ProcessSwapToUFP(1)	0b	PD Controller does not automatically accept swap to UFP requests from the far-end device.
		1b	PD Controller automatically initiates and sends DR_Swap requests to the far end device when appropriate if presently operating as UFP.
11	Reserved	Reserved (write 0)	
10	ProcessVconnSwap(1)	0b	PD Controller does not automatically accept VCONN_Swap requests from the far-end device.
		1b	PD Controller automatically accepts VCONN_Swap requests from the far end device.
9	Reserved	Reserved (write 0).	
8	Reserved	Reserved (write 0).	
7	InitiateSwapToSource(1)	0b	PD Controller does not automatically initiate and send swap to source requests to the far-end device.
		1b	PD Controller automatically initiates and sends PR_Swap requests to the far end device when appropriate if presently operating as C/P.
6	ProcessSwapToSource(1)	0b	PD Controller does not automatically accept swap to source requests from the far-end device.
		1b	PD Controller automatically accepts PR_Swap requests from the far end device if presently operating as C/P.
5	InitiateSwapToSink(1)	0b	PD Controller does not automatically initiate and send swap to sink requests to the far-end device.
		1b	PD Controller automatically initiates and sends PR_Swap requests to the far end device when appropriate if presently operating as P/C
4	ProcessSwapToSink(2)	0b	PD Controller does not automatically accept swap to sink requests from the far-end device.
		1b	PD Controller automatically accepts PR_Swap requests from the far end device if presently operating as P/C
3:2	DisablePD(2)	00b	Maintain normal USB PD behavior (default)
		01b	Stop USB PD activities and behave like a Legacy USB source. Present Power Role must be a Source.
		10b	Stop USB PD activities and behave like a Legacy USB sink. Present Power Role must be a Sink.
		11b	Reserved
1:0	TypeCCurrent(2)	Type-C Current advertisement. Setting is a do not care if a Source role is not enabled and active.	
		00b	Default Current
		01b	1.5A
		10b	3.0A
		11b	Reserved.

(2) Initialized by Application Customization.

3.8 0x2D Boot Flags Register

Table 3-15. 0x2D Boot Flags Register

Address	Name	Access	Length	Power-Up Default
0x2D[1]	Boot Flags	Read Only	12	Depends (Never reset)

(1) This register is shared by all ports.

Table 3-16. 0x2D Boot Flags Register Bit Field Definitions

Bits	Name	Description
Bytes 9-12: REV_ID_REG (treated as a 32-bit little endian value)		
31:8	Reserved	Reserved
7:4	REV_ID_Base	PD Controller Silicon (Base) revision, 0001b = A.
3:0	REV_ID_Metal	PD Controller Silicon (Metal) revision
Bytes 1-4: Boot Flags (treated as a 32-bit little endian value)		
31:21	Reserved	Reserved
20	PP4Switch	PP4 sink path enabled during dead-battery mode.
19	PP3Switch	PP3 sink path enabled during dead-battery mode.
18	PP2Switch	PP2 sink path enabled during dead-battery mode.
17	PP1Switch	PP1 sink path enabled during dead-battery mode.
16	Reserved	Reserved
15	Reserved	Reserved
14	CustomerOTPInvalid	If set the OTP Config bytes above are valid.
13	Region1CrcFail	CRC of read data from Region 1 of SPI memory failed.
12	Region0CrcFail	CRC of read data from Region 0 of SPI memory failed.
11	Reserved	Reserved
10	PatchDownloadErr	Patch bundle download error had occurred.
9	Region1FlashErr	An error occurred attempting to read Region 1 of SPI memory. A retry may have been successful.
8	Region0FlashErr	An error occurred attempting to read Region 0 of SPI memory. A retry may have been successful.
7	Region1Invalid	Region 1 header of the SPI memory was invalid.
6	Region0Invalid	Region 0 header of the SPI memory was invalid.
5	Region1	Region 1 of the SPI memory was attempted.
4	Region0	Region 0 of the SPI memory was attempted.
3	SpiFlashPresent	SPI_MISO pin was not grounded at boot, response received from SPI flash device. PD Controller is the primary device.
2	DeadBatteryFlag	PD Controller booted in dead-battery mode.
1	Reserved	Reserved
0	PatchHeaderErr	Patch bundle header error had occurred.

3.9 0x30 RX Source Capabilities Register

Table 3-17. 0x30 RX Source Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x30	RX Source Capabilities	Read Only	29	0 (Reset on disconnect and Hard Reset)

Table 3-18. 0x30 RX Source Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: PDO #7 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO7	Seventh Source Capabilities PDO received.
Bytes 22-25: PDO #6 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO6	Sixth Source Capabilities PDO received.
Bytes 18-21: PDO #5 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO5	Fifth Source Capabilities PDO received.
Bytes 14-17: PDO #4 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO4	Fourth Source Capabilities PDO received.
Bytes 10-13: PDO #3 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO3	Third Source Capabilities PDO received.
Bytes 6-9: PDO #2 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO2	Second Source Capabilities PDO received.
Bytes 2-5: PDO #1 (treated as a 32-bit little endian value)		
31:0	RXSourcePDO1	First Source Capabilities PDO received.
Byte 1: Header		
7:3	Reserved	Reserved.
2:0	RXSourceNumValidPDOs	Number of valid PDOs in this register (#bytes/4, 0-7).

3.10 0x31 RX Sink Capabilities Register

Table 3-19. 0x31 RX Sink Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x31	RX Sink Capabilities	Read Only	29	0 (Reset on disconnect and Hard Reset)

Table 3-20. 0x31 RX Sink Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: PDO #7 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO7	Seventh Sink Capabilities PDO received.
Bytes 22-25: PDO #6 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO6	Sixth Sink Capabilities PDO received.
Bytes 18-21: PDO #5 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO5	Fifth Sink Capabilities PDO received.
Bytes 14-17: PDO #4 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO4	Fourth Sink Capabilities PDO received.
Bytes 10-13: PDO #3 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO3	Third Sink Capabilities PDO received.
Bytes 6-9: PDO #2 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO2	Second Sink Capabilities PDO received.
Bytes 2-5: PDO #1 (treated as a 32-bit little endian value)		
31:0	RXSinkPDO1	First Sink Capabilities PDO received.
Byte 1: Header		
7:3	Reserved	Reserved.
2:0	RXSinkNumValidPDOs	Number of valid PDOs in this register (#bytes/4, 0-7).

3.11 0x32 TX Source Capabilities Register

Table 3-21. 0x32 TX Source Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x32	TX Source Capabilities	Read/Write	64	0 (Initialized by Application Customization, never reset)

Table 3-22. 0x32 TX Source Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 61-64 :PDO #7 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO7Bank1	Seventh Source Capabilities PDO contents Bank 01
Bytes 57-60: PDO #6 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO6Bank1	Sixth Source Capabilities PDO contents Bank 1.
Bytes 53-56: PDO #5 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO5Bank1	Fifth Source Capabilities PDO contents Bank 1.
Bytes 49-52: PDO #4 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO4Bank1	Fourth Source Capabilities PDO contents Bank 1.
Bytes 45-48: PDO #3 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO3Bank1	Third Source Capabilities PDO contents Bank 1.
Bytes 41-44: PDO #2 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO2Bank1	Second Source Capabilities PDO contents Bank 1.
Bytes 37-40: PDO #1 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO1Bank1	First Source Capabilities PDO contents Bank 1.
Bytes 33-36:PDO #7 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO7Bank0	Seventh Source Capabilities PDO contents Bank 0.
Bytes 29-32: PDO #6 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO6Bank0	Sixth Source Capabilities PDO contents Bank 0.
Bytes 25-28: PDO #5 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO5Bank0	Fifth Source Capabilities PDO contents Bank 0.
Bytes 21-24: PDO #4 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO4Bank0	Fourth Source Capabilities PDO contents Bank 0.
Bytes 17-20: PDO #3 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO3Bank0	Third Source Capabilities PDO contents Bank 0.
Bytes 13-16: PDO #2 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO2Bank0	Second Source Capabilities PDO contents Bank 0.
Bytes 9-12: PDO #1 (treated as a 32-bit little endian value)		
31:0	TXSourcePDO1Bank0	First Source Capabilities PDO contents Bank 0.
Bytes 7-8: Source Selection Bank 1.		
15:14	Reserved.	Reserved (write 0).
13:12	PDO7SourceBank1	Power Path Selection for PDO7 Bank 1.
11:10	PDO6SourceBank1	Power Path Selection for PDO6 Bank 1.
9:8	PDO5SourceBank1	Power Path Selection for PDO5 Bank 1.
7:6	PDO4SourceBank1	Power Path Selection for PDO4 Bank 1.
5:4	PDO3SourceBank1	Power Path Selection for PDO3 Bank 1.
3:2	PDO2SourceBank1	Power Path Selection for PDO2 Bank 1.

Table 3-22. 0x32 TX Source Capabilities Register Bit Field Definitions (continued)

Bits	Name	Description	
1:0	PDO1SourceBank1	Power Path Selection for PDO1 Bank 1.	
		00b	PP1 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
		01b	PP2 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
		10b	PP3 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
		11b	PP3 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
Bytes 5-6: Source Selection Bank 0.			
15:14	Reserved.	Reserved (write 0).	
13:12	PDO7SourceBank0	Power Path Selection for PDO7 Bank 0.	
11:10	PDO6SourceBank0	Power Path Selection for PDO6 Bank 0.	
9:8	PDO5SourceBank0	Power Path Selection for PDO5 Bank 0.	
7:6	PDO4SourceBank0	Power Path Selection for PDO4 Bank 0.	
5:4	PDO3SourceBank0	Power Path Selection for PDO3 Bank 0.	
3:2	PDO2SourceBank0	Power Path Selection for PDO2 Bank 0.	
1:0	PDO1SourceBank0	Power Path Selection for PDO1 Bank 0.	
		00b	PP1 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
		01b	PP2 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
		10b	PP3 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
		11b	PP4 sources the corresponding PDO (switch must be configured as output in Port Control Configuration registers).
Byte 4: Reserved			
7:0	Reserved	Reserved (write 0).	
Byte 3: PDO Bank Select			
7:2	Reserved	Reserved	
1	ActivePDOBankFollowsExternallyPowered	If set, ActivePDOBank is automatically changed based on the Externally Powered bit setting (Externally Powered 0->1 clears ActivePDOBank bit, Externally Powered 1->0 sets ActivePDOBank bit).	
0	ActivePDOBank	If clear, the PD Controller is using PDO bank 0. When set, the PD Controller is using PDO bank 1.).	
Byte 2: PDOs to advertise Bank 0			
7:2	AdvertisedPDOBank0	When bit is 1, corresponding PDO will be advertised for Bank 0. When bit is 0, corresponding PDO will only be advertised when Externally Powered bit is 1. The first 5V PDO (PDO1) is always advertised. Therefore these bits apply to PDO2 through PDO7.	
1:0	Reserved.	Reserved.	
Byte 1: Header Bank			
7:6	Reserved.	Reserved.	
5:3	TXSourceBank1NumPDOs	Number of valid PDOs (#bytes/4, 0-7) Bank 1.	
2:0	TXSourceBank0NumPDOs	Number of valid PDOs (#bytes/4, 0-7) Bank 0.	

3.12 0x33 TX Sink Capabilities Register

NOTE: Writes to this register have no immediate effect. The PD controller updates and uses this register each time it needs to send a *Sink Capabilities* message.

Table 3-23. 0x33 TX Sink Capabilities Register

Address	Name	Access	Length	Power-Up Default
0x33	TX Sink Capabilities	Read/Write	57	0 (Initialized by Application Customization, never reset)

Table 3-24. 0x33 TX Sink Capabilities Register Bit Field Definitions

Bits	Name	Description
Bytes 54-57: PDO #7 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 50-53: PDO #6 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 46-49: PDO #5 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 42-45: PDO #4 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 38-41: PDO #3 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 34-37: PDO #2 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
Bytes 30-33: PDO #1 Extension: These PDO extensions allow the user to configure a Maximum Operating Current or Power and a Minimum Operating Current or Power for each Sink PDO independently. Here the Maximum/Minimum Operating Current or Power are as defined by the PD specification for the request data object (RDO)		
31	Reserved	Reserved(Write 0).
30	AskForMax	When set to 1, the PD Controller will request the maximum current that the Source is able to provide that fits within the range of [Operating Current : MaxOperatingCurrentOrPower]. Example: If a Sink PDO is configured with (Fixed supply 20V, Operating Current = 1A, MaxOperatingCurrentOrPower=3A) without the *AskForMax* flag checked and the Source is capable of providing 20Vat2A, the Ssink will request an Operating Current = 1A, MaxOperatingCurrentOrPower=2A.If instead the Sink PDO is configured with (Fixed supply 20V, Operating Current = 1A, MaxOperatingCurrentOrPower = 3A) with the *AskForMax* flag checked and the Source is capable of providing 20V at 2A, the Sink will request an Operating Current = 2A, MaxOperatingCurrentOrPower = 2A.
29	Reserved	Reserved(Write 0).
19:10	MinOperatingCuorrentOrPower	Minimum Operational Current in 10 mA units or Minimum Operational Power in 250 mW units.
9:0	MaxOperatingCuorrentOrPower	Maximum Operational Current in 10 mA units or maximum Operational Power in 250 mW units.
Bytes 26-29: PDO #7 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO7	Seventh Sink Capabilities PDO contents.
Bytes 22-25: PDO #6 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO6	Sixth Sink Capabilities PDO contents.
Bytes 18-21: PDO #5 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO5	Fifth Sink Capabilities PDO contents.
Bytes 14-17: PDO #4 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO4	Fourth Sink Capabilities PDO contents.

Table 3-24. 0x33 TX Sink Capabilities Register Bit Field Definitions (continued)

Bits	Name	Description
Bytes 10-13: PDO #3 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO3	Third Sink Capabilities PDO contents.
Bytes 6-9: PDO #2 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO2	Second Sink Capabilities PDO contents.
Bytes 2-5: PDO #1 (treated as a 32-bit little endian value)		
31:0	TXSinkPDO1	First Sink Capabilities PDO contents.
Byte 1: Header		
7:3	Reserved	Reserved.
2:0	TXSinkNumValidPDOs	Number of valid PDOs in this register (#bytes/4, 0-7).

3.13 0x34 Active Contract PDO

Table 3-25. 0x34 Active Contract PDO Register

Address	Name	Access	Length	Power-Up Default
0x34	Active Contract PDO	Read Only	6	0 (reset on disconnect/connect/Hard Reset/PR_Swap)

Table 3-26. 0x34 Active Contract PDO Register Bit Field Definitions

Bits	Name	Description
Bytes 5-6: Source Properties		
15:10	Reserved	Reserved.
9:0	SourcePDOFlags	Contains bits 29:20 of the first PDO, regardless of which PDO is selected.
Bytes 1-4: Contract PDO (treated as 32-bit little endian value)		
31:0	ActiveContractPDO	Contents of PDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

3.14 0x35 Active Contract RDO

Table 3-27. 0x35 Active Contract RDO Register

Address	Name	Access	Length	Power-Up Default
0x35	Active Contract RDO	Read Only	4	0 (reset on disconnect/connect/Hard Reset/PR_Swap)

Table 3-28. 0x35 Active Contract RDO Register Bit Field Definitions

Bits	Name	Description
Bytes 1-4: Contract RDO (treated as 32-bit little endian value)		
31:0	ActiveContractRDO	Contents of RDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

3.15 0x36 Sink Request RDO

Table 3-29. 0x36 Sink Request RDO Register

Address	Name	Access	Length	Power-Up Default
0x36	Sink Request RDO	Read Only	4	0 (reset on disconnect/connect/Hard Reset/PR_Swap)

Table 3-30. 0x36 Sink Request RDO Register Bit Field Definitions

Bits	Name	Description
Bytes 1-4: Request RDO (treated as 32-bit little endian value)		
31:0	SinkRequestRDO	Contents of most recent Request RDO, sent by PD Controller as Sink or received by PD Controller as Source.

3.16 0x37 Auto Negotiate Sink

NOTE: Writing this register while a sink contract is in place will not cause an automatic renegotiation, changes will take effect the next time a contract is negotiated. The *ANeg* command forces a re-evaluation of this register and a new *Request* message will be issued if appropriate.

Table 3-31. 0x37 Auto Negotiate Sink Register

Address	Name	Access	Length	Power-Up Default
0x37	Auto Negotiate Sink	Read/Write	20	0 (Initialized by Application Customization)

Table 3-32. 0x37 Auto Negotiate Sink Register Bit Field Definitions

Bits	Name	Description	
Bytes 17-20: Non-Battery PDO Parameters			
31:22	Reserved	Reserved.	
21:20	PeakCurrent	Peak Current (See PD Spec)	
19:10	Reserved	Reserved.	
9:0	MaximumCurrent	Maximum Current (10 mA steps)	
Bytes 13-16: Battery PDO Parameters			
31:22	MinimumVoltage	Minimum Voltage (50 mV steps)	
21:20	Reserved	Reserved (Write 0).	
19:10	MaximumVoltage	Maximum Voltage (50 mV steps)	
9:0	MaximumPower	Maximum Power (250 mW steps)	
Bytes 9-12: RDO Current Parameters			
31:20	Reserved	Reserved (Write 0).	
19:10	MinOperatingCurrent	Min Operating Current (10 mA steps)	
9:0	OperatingCurrent	Operating Current (10 mA steps)	
Bytes 5-8: RDO Power Parameters			
31:20	Reserved	Reserved (Write 0).	
19:10	MinOperatingPower	Min Operating Power (250 mW steps)	
9:0	OperatingPower	Operating Power (250 mW steps)	
Bytes 3-4: Auto Negotiate Minimum Sink Required Operating Power			
15:10	Reserved	Reserved (Write 0).	
9:0	ANSinkMinRequiredPower	Minimum operating power required by the Sink in 250mW per LSB. Typically, this field is set to the maximum power across the PDOs defined in the TX Sink Capabilities Register (0x33). NOTE: If the TX Sink Capabilities Register includes Battery supply type PDO(s), then the maximum power of Battery PDOs should be considered even when Fixed supply and Variable supply PDOs of higher power are available.	
Byte 2: Auto-negotiate control			
7:1	Reserved	Reserved (Write 0).	
0	AutoComputeSinkMinPower	Decides if FW should compute minimum Sink operating power based on Sink Capability PDOs programmed in the TX Sink Capability register	
		0b	PD Controller uses the value stored in the ANSinkMinRequiredPower field as the minimum operating power required by the SInk.
		1b	PD Controller will automatically compute the minimum operating power required by the SInk based on the Sink PDOs stored in the TX Sink Capabilities Register (0x33) and store it in the ANSinkMinRequiredPower field. The ANSinkMInRequiredPower is updated during the negotiation of a new contract.
Byte 1: Auto-negotiate control and RDO flags			
7	RDOGiveBackFlag	RDO GiveBack Flag	

Table 3-32. 0x37 Auto Negotiate Sink Register Bit Field Definitions (continued)

Bits	Name	Description	
6	RDONoUsbSuspFlag	RDO NoUSBSusp Flag	
5:4	OfferPriority	Offer Priority when evaluating PDOs offered by source	
		00b	Higher current priority
		01b	Higher voltage priority
		10b	Higher power priority
		11b	Reserved.
3	RDOUsbCommCapable Flag	RDO USB Communicatoins Capable Flag	
2	AutoNgtSnkVariable	Auto Negotiate using Variable PDO	
1	AutoNgtSnkBattery	Auto Negotiate using Battery PDO.	
0	AutoNgt	Auto Negotiate Fixed PDO This bit must be set for AutoNgtSnkVariable/Battery.	

3.17 0x38 Alternate Mode Entry Sequence

Table 3-33. 0x38 Alternate Mode Entry Sequence Register

Address	Name	Access	Length	Power-Up Default
0x38	Alternate Mode Entry Sequence	Read/Write	16	0 (Initialized by Application Customization)

Table 3-34. 0x38 Alternate Mode Entry Sequence Register Bit Field Definitions

Bits	Name	Description
Bytes 13-16:SVID/Mode 4		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for fourth mode for entry attempt
Bytes 9-12:SVID/Mode 3		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for third mode for entry attempt
Bytes 5-8:SVID/Mode 2		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for second mode for entry attempt
Bytes 1-4:SVID/Mode 1		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for first mode for entry attempt

(1) Initialized by Application Customization.

3.18 0x3F Power Status

Table 3-35. 0x3F Power Status Register

Address	Name	Access	Length	Power-Up Default
0x3F	Power Status	Read Only	2	Depends, reset to 0 on disconnect.

Table 3-36. 0x3F Power Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-2:			
15:10	Reserved	Reserved (0)	
9:8	Charger Advertise Status	00b	Charger advertise disabled or not run
		01b	Charger advertisement in process
		10b	Charger advertisement complete
		11b	Reserved
7:4	Charger Detect Status	0000b	Charger detection disabled or not run
		0001b	Charger detection in progress
		0010b	Charger detection complete, none detected
		0011b	Charger detection complete, SDP detected
		0100b	Charger detection complete, BC 1.2 CDP detected
		0101b	Charger detection complete, BC 1.2 DCP detected
		0110b	Charger detection complete, Divider1 DCP detected
		0111b	Charger detection complete, Divider2 DCP detected
		1000b	Charger detection complete, Divider3 DCP detected
		1001b	Charger detection complete, 1.2V DCP detected
		1010b	Reserved
		1011b	Reserved
		1100b	Reserved
		1101b	Reserved
		1110b	Reserved
		1111b	Reserved
3:2	Type-C Current	00b	USB Default Current
		01b	1.5A Current
		10b	3A Current
		11b	PD contract negotiated (see other PD registers for more details).
1	SourceSink	0b	Connection requests power (PD Controller as source).
		1b	Connection provides power (PD Controller as sink).
0	PowerConnection	0b	No connection (rest of bits in this register are not valid).
		1b	Connection present (see other bits in register for more details).

3.19 0x40 PD Status

Table 3-37. 0x40 PD Status Register

Address	Name	Access	Length	Power-Up Default
0x40	PD Status	Read Only	4	Depends, reset on connect only.

Table 3-38. 0x40 PD Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4:			
31:22	Reserved	Reserved.	
21:16	HardResetDetails	000000b	Reset value, no hard reset.
		000001b	Required by the policy engine (signaling sent by far end).
		000010b	Requested by host.
		000011b	Invalid DR_Swap request during Active Mode
		000100b	Required by policy engine, DischargeFailed.
		000101b	Required by policy engine, NoResponseTimeOut.
		000110b	Required by policy engine, SendSoftReset.
		000111b	Required by policy engine, Sink_SelectCapability.
		001000b	Required by policy engine, Sink_TransitionSink.
		001001b	Required by policy engine, Sink_WaitForCapabilities.
		001010b	Required by policy engine, SoftReset.
		001011b	Required by policy engine, SourceOnTimeout.
		001100b	Required by policy engine, Source_CapabilityResponse.
		001101b	Required by policy engine, Source_SendCapabilities.
		001110b	Required by policy engine, SourcingFault.
		001111b	Required by policy engine, UnableToSource.
		010000b-111111b	Reserved
15:13	Reserved	Reserved	

Table 3-38. 0x40 PD Status Register Bit Field Definitions (continued)

Bits	Name	Description	
12:8	SoftResetType	00000b	Reset value, no soft reset.
		00001b	Soft reset received from far-end device.
		00010b	Reserved
		00011b	Soft reset sent, a GoodCRC was expected but something else was received.
		00100b	Soft reset sent because the received source capabilities message was invalid.
		00101b	Soft reset sent after retries were exhausted.
		00110b	Soft reset sent due to receiving an accept message unexpectedly.
		00111b	Reserved
		01000b	Soft reset sent due to receiving a GetSinkCap message unexpectedly.
		01001b	Soft reset sent due to receiving a GetSourceCap message unexpectedly.
		01010b	Soft reset sent due to receiving a GotoMin message unexpectedly.
		01011b	Soft reset sent due to receiving a PS_RDY message unexpectedly.
		01100b	Soft reset sent due to receiving a Ping message unexpectedly.
		01101b	Soft reset sent due to receiving a Reject message unexpectedly.
		01110b	Soft reset sent due to receiving a Request message unexpectedly.
		01111b	Soft reset sent due to receiving a Sink Capabilities message unexpectedly.
		10000b	Soft reset sent due to receiving a Source Capabilities message unexpectedly.
		10001b	Soft reset sent due to receiving a Swap message unexpectedly.
		10010b	Soft reset sent due to receiving a Wait Capabilities message unexpectedly.
		10011b	Soft reset sent due to receiving an unknown control message.
		10100b	Soft reset sent due to receiving an unknown data message.
		10101b	Soft reset sent to initialize SOP' controller in plug
		10110b	Soft reset sent to initialize SOP'' controller in plug
		10111-11111b	Reserved
7	Reserved	Reserved	
6	PresentRole	The PD source/sink role PD Controller is acting under.	
		0b	Sink
		1b	Source
5:4	PortType	The PD Sink/Source role PD Controller is acting under.	
		00b	Sink/Source
		01b	Sink
		10b	Source
		11b	Source/Sink
3:2	CCPullUp	CC Pull-up value detected by PD Controller when in CC Pull-down mode.	
		00b	Not in CC pull-down mode / no CC pull-up detected.
		01b	USB Default current
		10b	1.5A current
		11b	3A current
1:0	PlugDetails	Plug type.	
		00b	USB Type-C full-featured plug
		01b	USB 2.0 Type-C plug
		10b	Reserved
		11b	Reserved

3.20 0x41 PD3.0 Status

Table 3-39. 0x41 PD3.0 Status Register

Address	Name	Access	Length	Power-Up Default
0x41	PD3.0 Status	Read Only	4	Depends, reset on connect only.

Table 3-40. 0x41 PD3.0 Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4:			
31	UseUnchunkedMessages	Unchunked messages are supported.	
30:29	PlugPartnerNegSpecRev	Plug partner negotiated specification revision.	
		00b	PD Specification revision 1
		01b	PD Specification revision 2
		10b	PD Specification revision 3
		11b	Reserved
28:27	PortPartnerNegSpecRev	Port partner negotiated specification revision	
		00b	PD Specification revision 1
		01b	PD Specification revision 2
		10b	PD Specification revision 3
		11b	Reserved
26:25	PlugPartnerNegSpecSVDMRev	Plug partner negotiated SVDM specification revision.	
		00b	PD Specification revision 1
		01b	PD Specification revision 2
		10b	PD Specification revision 3
		11b	Reserved
24:23	PortPartnerNegSpecSVDMRev	Port partner negotiated SVDM specification revision.	
		00b	PD Specification revision 1
		01b	PD Specification revision 2
		10b	PD Specification revision 3
		11b	Reserved
22:5	Reserved	Reserved	
4	SecReqRcvd	Security Request Message received.	
3	SrcCapExtReqRcvd	Get Source Capabilities Extended Message received.	
2	SecRspRcvd	Security Response Message received	
1	SrcCapExtRcvd	Source Capabilities Extended Message received.	
0	NotSupportedRcvd	Not Supported Message received.	

3.21 0x42 PD3.0 Configuration Register

Table 3-41. 0x42 PD3.0 Configuration Register

Address	Name	Access	Length	Power-Up Default
0x42	PD3.0 Configuration	Read/Write	4	0

Table 3-42. 0x42 PD3.0 Configuration Register Bit Field Definitions

Bits	Name	Description	
Bytes 1-4:			
31:25	Reserved	Reserved (write 0)	
24	SupportCountyCodeInfo	0b	Country Code messages not supported
		1b	Country Code messages supported
23	SupportPPSStatusMsg	0b	PPS Status messages not supported
		1b	PPS Status messages supported
22	SupportFirmwareUpgradeMsg	0b	Firmware Upgrade messages not supported
		1b	Firmware Upgrade messages supported
21	SupportSecurityMsg	0b	Security messages not supported
		1b	Security messages supported
20	SupportManufactureInfoMsg	0b	Manufacturer Info messages not supported
		1b	Manufacturer Info messages supported
19	SupportBatteryStatusMsg	0b	Battery Status messages not supported
		1b	Battery Status messages supported
18	SupportBatteryCapMsg	0b	Battery Capabilities messages not supported
		1b	Battery Capabilities messages supported
17	SupportStatusMsg	0b	Status messages not supported
		1b	Status messages supported
16	SupportSourceCapExtMsg	0b	Source Capabilities Extended messages not supported
		1b	Source Capabilities messages supported
15:13	Reserved	Reserved (write 0)	
12	Reserved	Reserved (write 0)	
11:8	tFRSwapInit	FRS initiation timer in ms (1 LSB = 1 ms). This should be set to a value greater than 4ms but less than 15ms.	
7	Reserved	Reserved (write 0)	
6	FRSignalDisabledForUVP	0b	Fast Role Swap signaling from Source supported by UVP, GPIO, or 4CC Command events.
		1b	Fast Role Swap signaling from Source only supported by GPIO or 4CC Command events (no UVP).
5	FRSwapEnabled	0b	Fast Role Swap disabled.
		1b	Fast Role Swap enabled.
4	UnchunkedSupported	0b	Unchunked messages not supported
		1b	Unchunked messages supported
3:2	SOPPrimeRevision	00b	Revision 1.0
		01b	Revision 2.0
		10b	Revision 3.0
		11b	Reserved
1:0	SOPRevision	00b	Revision 1.0
		01b	Revision 2.0
		10b	Revision 3.0
		11b	Reserved

3.22 0x43 Delay Configuration Register

Table 3-43. 0x43 Delay Configuration Register

Address	Name	Access	Length	Power-Up Default
0x43	Delay Configuration	Read/Write	9	0

Table 3-44. 0x43 Delay Configuration Register Bit Field Definitions

Bits	Name	Description
Byte 9:		
7:0	Reserved	Reserved
Bytes 5-8:		
31:24	Reserved	Reserved
23:16	tRetimerForcePowerDelay	Configurable Delay between Retimer_PWR_EN GPIO and Retimer_Reset_N GPIO assertion (250us per LSB)
15:8	tConnectionDelay	Configurable Delay from initial connection configuration to start of PD negotiation (500us per LSB)
7:0	tAMConfigDelay	Configurable Delay from entering configuration to ACK response (500us per LSB)
Bytes 1-4:		
31:24	tHPDDelay	Configurable Delay after changing HPD state (500us per LSB)
23:16	tMuxDelay_DRS	Configurable Delay after changing mux data role (500us per LSB)
15:8	tMuxDelay_UFP	Configurable Delay from entering mode to ACK response (500us per LSB)
7:0	tMuxDelay_DFP	Configurable Delay from entering safe state to sending mode enter command (500us per LSB)

3.23 0x47 TX Identity

NOTE1: This register contains two “sets” of Discover Identity responses. Bytes 2-25 contain the “Primary” response, which goes to SOP on a host/device and SOP’ on a cable-only implementation. Bytes 26-49 contain the “Secondary” response, which goes to SOP’ on a device with a captive cable.

NOTE2: Writes to this register have no immediate effect. PD Controller will update and use the contents of this register each time a Discover Identity SVDM is received as a UFP.

Table 3-45. 0x47 TX Identity Register

Address	Name	Access	Length	Power-Up Default
0x47	TX Identity	Read/Write	49	0 (Initialized by Application Customization, never reset)

Table 3-46. 0x47 TX Identity Register Bit Field Definitions

Bits	Name	Description
Bytes 26-49: Secondary Primary Discovery Identity response.(1)		
Bytes 22-25: VDO #6 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO6(1)	Sixth Data Object for Primary Discover Identity response (context-specific)
Bytes 18-21: VDO #5 (treated as a 32-bit little endian value)		
31:0	TXIdentityDO5(1)	Fifth Data Object for Primary Discover Identity response (context-specific)
Bytes 14-17: VDO #4 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO4(1)	Fourth Data Object for SOP Discover Identity response
Bytes 10-13: VDO #3 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO3(1)	Third Data Object for Primary Discover Identity response
Bytes 6-9: VDO #2 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO2(1)	Second Data Object for Primary Discover Identity response (Cert Stat VDO).Note: Once initial Application Customization completes and whenever a Discover Identity response is sent, PD Controller will copy the contents of the Application Customization “USB-IF XID” to this field. Data written to this field by the Host will never be sent on USB-PD.
Bytes 2-5: VDO #1 (treated as a 32-bit little endian value)		
31:0	TXIdentityVDO1(1)	First Data Object for Discover Identity response (ID Header VDO).Note: USB_EP will use bits 15:0 of this field to get its USB Vendor ID (idVendor).
Byte 1		Number of valid PDOs in register
7	Reserved	Reserved (write 0)
6:4	NumValidIDOs in SOP’ Response(1)	Number of valid IDOs in register (0-7)When 0, the PD Controller will NAK USB PD Discover Identity message. When 1, the PD Controller will respond with BUSY message. 2-7 indicates valid (ACK) response.
3	Reserved	Reserved (write 0)
2:0	NumValidIDOs in SOP Response(1)	Number of valid IDOs in register (0-7)When 0, the PD Controller will NAK USB PD Discover Identity message. When 1, the PD Controller will respond with BUSY message. 2-7 indicates valid (ACK) response.

(1) Initialized by Application Customization.

3.24 0x48 RX Identity SOP

Table 3-47. 0x48 RX Identity SOP Register

Address	Name	Access	Length	Power-Up Default
0x48	RX Identity SOP	Read Only	28	0 (Reset on connect)

Table 3-48. 0x48 RX Identity SOP Register Bit Field Definitions

Bits	Name	Description	
Bytes 26-28: Reserved (write 0)			
Bytes 22-25: VDO #6 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO6	Sixth Data Object for SOP Discover Identity response (context-specific)	
Bytes 18-21: VDO #5 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO5	Fifth Data Object for SOP Discover Identity response (context-specific)	
Bytes 14-17: VDO #4 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO4	Fourth Data Object for SOP Discover Identity response (context-specific)	
Bytes 10-13: VDO #3 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO3	Third Data Object for SOP Discover Identity response (Product VDO).	
Bytes 6-9: VDO #2 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO2	Second Data Object for SOP Discover Identity response (Cert Stat VDO).	
Bytes 2-5: VDO #1 (treated as a 32-bit little endian value)			
31:0	RXIdSOPVDO1	First Data Object for SOP Discover Identity response (ID Header VDO).	
Byte 1: RX Identity SOP Status			
7:6	RXIdSOPResponse	00b	SOP Discover Identity request not sent or pending.
		01b	Responder ACK received.
		10b	Responder NAK received or response timeout.
		11b	Responder BUSY received (PD Controller will retry).
5:3	Reserved	Reserved.	
2:0	RXIdSOPNumValid	Number of valid VDOs in this register (#bytes/4, 0-6). Structured VDM Header is not captured in this register.	

3.25 0x49 RX Identity SOP'

Table 3-49. 0x49 RX Identity SOP' Register

Address	Name	Access	Length	Power-Up Default
0x49	RX Identity SOP'	Read Only	28	0 (Reset on connect)

Table 3-50. 0x49 RX Identity SOP' Register Bit Field Definitions

Bits	Name	Description	
Bytes 26-28: Reserved (write 0)			
Bytes 22-25: VDO #6 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO6	Sixth Data Object for SOP' Discover Identity response (context-specific)	
Bytes 18-21: VDO #5 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO5	Fifth Data Object for SOP' Discover Identity response (context-specific)	
Bytes 14-17: VDO #4 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO4	Fourth Data Object for SOP' Discover Identity response (context-specific)	
Bytes 10-13: VDO #3 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO3	Third Data Object for SOP' Discover Identity response (Product VDO).	
Bytes 6-9: VDO #2 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO2	Second Data Object for SOP' Discover Identity response (Cert Stat VDO).	
Bytes 2-5: VDO #1 (treated as a 32-bit little endian value)			
31:0	RXIdSOPpVDO1	First Data Object for SOP' Discover Identity response (ID Header VDO).	
Byte 1: RX Identity SOP' Status			
7:6	RXIdSOPpResponse	00b	SOP' Discover Identity request not sent or pending.
		01b	Responder ACK received.
		10b	Responder NAK received or response timeout.
		11b	Responder BUSY received (PD Controller will retry).
5:3	Reserved	Reserved.	
2:0	RXIdSOPpNumValid	Number of valid VDOs in this register (#bytes/4, 0-6). Structured VDM Header is not captured in this register.	

3.26 0x4A User VID Configuration

Table 3-51. 0x4A User VID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x4A	User VID Configuration	Read/Write	64	0 (Initialized by Application Customization)

Table 3-52. 0x4A User VID Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 64:			
7:0	Reserved	Reserved (Write 0)	
Byte 63:			
7:0	UserModeAutoSendVDOCount	If auto send unstructured VDM enabled, number of VDOs to send.	
Byte 61-62:			
15:14	Reserved	Reserved (Write 0)	
13:0	UserVIDAutoSendVendorData	If auto send unstructured VDM enabled, up to an additional 14 bits may be sent.	
Bytes 37-60			
191:0	UserVIDAutoSendVDOData	If auto send unstructured VDM enabled, up to 192 bits may be sent.	
Bytes 33-36:			
31:0	UserVIDmode4Name	User VID Mode 4 name	
Bytes 29-32:			
31:0	UserVIDmode3Name	User VID Mode 3 name	
Bytes 25-28:			
31:0	UserVIDmode2Name	User VID Mode 2 name	
Bytes 21-24:			
31:0	UserVIDmode1Name	User VID Mode 1 name	
Byte 20:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4LoadAppConfigData	0b	User VID Mode 4 load application configuration data on entry disabled
		1b	User VID Mode 4 load application configuration data on entry enabled
Byte 19:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode3LoadAppConfigData	0b	User VID Mode 3 load application configuration data on entry disabled
		1b	User VID Mode 3 load application configuration data on entry enabled
Byte 18:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2LoadAppConfigData	0b	User VID Mode 2 load application configuration data on entry disabled
		1b	User VID Mode 2 load application configuration data on entry enabled
Byte 17:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1LoadAppConfigData	0b	User VID Mode 1 load application configuration data on entry disabled
		1b	User VID Mode 1 load application configuration data on entry enabled
Byte 16:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4AutoSendUnstrVDM	0b	User VID Mode 4 auto send unstructured VDM on entry disabled
		1b	User VID Mode 4 auto send unstructured VDM on entry enabled
Byte 15:			
7:1	Reserved	Reserved (Write 0).	

Table 3-52. 0x4A User VID Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
0	UserVIDmode3AutoSendUnstrVDM	0b	User VID Mode 3 auto send unstructured VDM on entry disabled
		1b	User VID Mode 3 auto send unstructured VDM on entry enabled
Byte 14:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2AutoSendUnstrVDM	0b	User VID Mode 2 auto send unstructured VDM on entry disabled
		1b	User VID Mode 2 auto send unstructured VDM on entryenabled
Byte 13:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1AutoSendUnstrVDM	0b	User VID Mode 1 auto send unstructured VDM on entry disabled
		1b	User VID Mode 1 auto send unstructured VDM on entry enabled
Byte 12:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4AutoEntry	0b	User VID Mode 4 auto entry not supported
		1b	User VID Mode 4 auto entry supported
Byte 11:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode3AutoEntry	0b	User VID Mode 3 auto entry not supported
		1b	User VID Mode 3 auto entry supported
Byte 10:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2AutoEntry	0b	User VID Mode 2 auto entry not supported
		1b	User VID Mode 2 auto entry supported
Byte 9:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1AutoEntry	0b	User VID Mode 1 auto entry not supported
		1b	User VID Mode 1 auto entry supported
Byte 8:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode4Enabled	0b	User VID Mode 4 disabled
		1b	User VID Mode 4 enabled
Byte 7:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode3Enabled	0b	User VID Mode 3 disabled
		1b	User VID Mode 3 enabled
Byte 6:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode2Enabled	0b	User VID Mode 2 disabled
		1b	User VID Mode 2 enabled
Byte 5:			
7:1	Reserved	Reserved (Write 0).	
0	UserVIDmode1Enabled	0b	User VID Mode 1 disabled
		1b	User VID Mode 1 enabled
Bytes 3-4:			
15:0	UserVIDValue	User VID	
Byte 2:			
7:0	Reserved	Reserved	
Byte 1:			

Table 3-52. 0x4A User VID Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
7:1	Reserved	Reserved (Write 0).	
0	UserVidEnabled	0b	User VID disabled
	UserVidEnabled	1b	User VID enabled

3.27 0x4B MIPI VID Configuration

Table 3-53. 0x4B MIPI VID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x4B	MIPI VID Configuration	Read Only	4	0 (Reset on connect)

Table 3-54. 0x4B – MIPI VID Configuration Register Bit Field Definitions

Bits	Name	Description	
Bytes 3-4:			
15	OverlayMode15Supported	0b	Overlay Mode 15 not supported
		1b	Overlay Mode 15 supported
14	OverlayMode14Supported	0b	Overlay Mode 14 not supported
		1b	Overlay Mode 14 supported
13	OverlayMode13Supported	0b	Overlay Mode 13 not supported
		1b	Overlay Mode 13 supported
12	OverlayMode12Supported	0b	Overlay Mode 12 not supported
		1b	Overlay Mode 12 supported
11	OverlayMode11Supported	0b	Overlay Mode 11 not supported
		1b	Overlay Mode 11 supported
10	OverlayMode10Supported	0b	Overlay Mode 10 not supported
		1b	Overlay Mode 10 supported
9	OverlayMode9Supported	0b	Overlay Mode 9 not supported
		1b	Overlay Mode 9 supported
8	OverlayMode8Supported	0b	Overlay Mode 8 not supported
		1b	Overlay Mode 8 supported
7	OverlayMode7Supported	0b	Overlay Mode 7 not supported
		1b	Overlay Mode 7 supported
6	OverlayMode6Supported	0b	Overlay Mode 6 not supported
		1b	Overlay Mode 6 supported
5	OverlayMode5Supported	0b	Overlay Mode 5 not supported
		1b	Overlay Mode 5 supported
4	OverlayMode4Supported	0b	Overlay Mode 4 not supported
		1b	Overlay Mode 4 supported
3	OverlayMode3Supported	0b	Overlay Mode 3 not supported
		1b	Overlay Mode 3 supported
2	OverlayMode2Supported	0b	Overlay Mode 2 not supported
		1b	Overlay Mode 2 supported
1	OverlayMode1Supported	0b	Overlay Mode 1 not supported
		1b	Overlay Mode 1 supported
0	OverlayMode0Supported	0b	Overlay Mode 0 not supported
		1b	Overlay Mode 0 supported
Byte 2:			
7:2	Reserved	Reserved	
1	DebugModeAutoEntryAllowed	0b	MIPI Debug mode Auto Entry not supported
		1b	MIPI Debug mode Auto Entry supported
0	Reserved	Reserved	
Byte 1:			

Table 3-54. 0x4B – MIPI VID Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
7:2	Reserved	Reserved	
1	MIPIDebugModeEnabled	0b	Debug mode disabled
		1b	Debug mode enabled
0	MIPIVidEnabled	0b	MIPI VID disabled
		1b	MIPI VID enabled

3.28 0x4E RX Attention

NOTE: Only Structured VDM messages with Command Type = Initiator (00b) and Command = Attention (6) get stored in this buffer. See register 0x4F for all other inbound VDMs.

Table 3-55. 0x4E RX Attention Register

Address	Name	Access	Length	Power-Up Default
0x4E	RX Attention	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-56. 0x4E RX Attention Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO7	Seventh Data Object of most recently received Attention SVDM.
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO6	Sixth Data Object of most recently received Attention SVDM.
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO5	Fifth Data Object of most recently received Attention SVDM.
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO4	Fourth Data Object of most recently received Attention SVDM.
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO3	Third Data Object of most recently received Attention SVDM.
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO2	Second Data Object of most recently received Attention SVDM.
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO1	First Data Object of most recently received Attention SVDM.
Byte 1: RX Attention Status		
7:5	RXAttentionSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.
4:3	Reserved	Reserved.
2:0	RXAttentionNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).

3.29 0x4F RX VDM

NOTE: Structured VDM “Attention” Initiator messages are only stored in register 0x4E, not this register.

Table 3-57. 0x4F RX VDM Register

Address	Name	Access	Length	Power-Up Default
0x4F	RX VDM	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-58. 0x4F RX VDM Register Bit Field Definitions

Bits	Name	Description	
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)			
31:0	RXVDMDO7	Seventh Data Object of most recently received VDM.	
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)			
31:0	RXVDMDO6	Sixth Data Object of most recently received VDM.	
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)			
31:0	RXVDMDO5	Fifth Data Object of most recently received VDM.	
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)			
31:0	RXVDMDO4	Fourth Data Object of most recently received VDM.	
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)			
31:0	RXVDMDO3	Third Data Object of most recently received VDM.	
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)			
31:0	RXVDMDO2	Second Data Object of most recently received VDM.	
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)			
31:0	RXVDMDO1	First Data Object of most recently received VDM.	
Byte 1: RX VDM Status			
7:5	RXVDMSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.	
4:3	RXVDMSource	SOP* of message source.	
		00b	VDM came from SOP.
		01b	VDM came from SOP’.
		10b	VDM came from SOP’’.
		11b	VDM came from SOP*_Debug.
2:0	RXVDMNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).	

3.30 0x50 Data Control

This register provides *shortcuts* that set other bits in the System Control or Command register, for convenience of the Thunderbolt Controller or other host. It also holds data that the TBT controller wants to write to the Debug Mode Register of the Retimer through the PD controller. The TBT Controller initiates the PD controller's write to the Debug Mode Register of the Retimer using the Data Control Register as well.

Table 3-59. 0x50 Data Control Register

Address	Name	Access	Length	Power-Up Default
0x50	Data Control	Read-Write	6	0 (Managed by Thunderbolt Controller)

Table 3-60. 0x50 Data Control Register Bit Field Definitions

Bits	Name	Description	
Bytes 3-6: Retimer Debug Mode Register			
Bytes 1-2: Data Control (treated as 32-bit little endian value)			
15	HPDlevel	HPD level from DP Sink connection to Titan Ridge to PD Controller. Used only for TBT devices. Not used for TBT hosts.	
		0b	HPD low
		1b	HPD high
14	HPD_IRQsticky	HPD IRQ from DP Sink connection to Titan Ridge to PD Controller. Cleared when Data_Status.HPD_IRQ_Sticky. Used only for TBT devices. Not used for TBT hosts.	
		0b	No HPD IRQ
		1b	HPD IRQ
13	HPD_IRQ_ACK	0b	No HPD_IRQ_ACK
		1b	HPD_IRQ_ACK
12	WriteToRetimer	0b	No action. Ignore Bytes 3-6
		1b	Write Bytes 3-6 to Retimer
11:6	Reserved	Reserved (write 0).	
5	DPhostConnected	0b	No DP host connected upstream. Only applicable TBT devices.
		1b	DP host connected upstream. Only applicable TBT devices.
4	USBhostConnected	0b	No USB host connected upstream. Only applicable TBT devices.
		1b	USB host connected upstream. Only applicable TBT devices.
3	StatusNak	Reserved (Host may write 0 or 1, no action to be taken).	
2	InterruptAck	When set, causes all bits in the IntEvent2 register to be cleared (clearing all interrupt events).	
1	SoftReset	When set, causes a soft-reset of PD Controller. Equivalent to Gaid 4CC.	
0	HostConnected	0b	No TBT host connected. NOTE: The Thunderbolt Controller will also set bit 1 (SoftReset) when transitioning this bit from 1->0 to force a port disconnect/reconnect.
		1b	TBT host connected.

3.31 0x51 DP SID Configuration

Table 3-61. 0x51 DP SID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x51	DP SID Configuration	Read/Write	6	0 (Initialized by Application Customization)

Table 3-62. 0x51 DP SID Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 6:			
7:2	Reserved	Reserved (write 0).	
1	DP_AutoEntryAllowed	0b	DP Alternate Mode auto-entry disabled.
		1b	DP Alternate Mode auto-entry enabled.
0	Reserved	Reserved (write 0).	
Byte 5:			
7:1	Reserved	Reserved (Write 0).	
0	MultifunctionPreferred	0b	Multifunction not preferred.
		1b	Multifunction preferred.
Byte 4:			
7:0	UFP_D Pin Assignments Supported	Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed.	
		00000000b	UFP pin assignments are not supported.
		xxxxxxx1b	Pin assignment A is supported
		xxxxxx1xb	Pin assignment B is supported
		xxxxx1xxb	Pin assignment C is supported
		xxxx1xxxb	Pin assignment D is supported
		xxx1xxxxb	Pin assignment E is supported
		xx1xxxxxb	Reserved
		x1xxxxxxb	Reserved
		1xxxxxxxb	Reserved
Byte 3:			
7:0	DFP_D Pin Assignments Supported	Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed.	
		00000000b	DFP pin assignments are not supported.
		xxxxxxx1b	Pin assignment A is supported
		xxxxxx1xb	Pin assignment B is supported
		xxxxx1xxb	Pin assignment C is supported
		xxxx1xxxb	Pin assignment D is supported
		xxx1xxxxb	Pin assignment E is supported
		xx1xxxxxb	Pin assignment F is supported
		x1xxxxxxb	Reserved
		1xxxxxxxb	Reserved
Byte 2:			
7	USB 2.0 Signaling Not Used	0b	USB r2.0 signaling may be required on A6 - A7 or B6 - B7 (D+/D-) while in DP configuration
		1b	USB r2.0 signaling is not required on A6 - A7 or B6 - B7 (D+/D-) while in DP configuration
6	DP Receptacle Indication	0b	DisplayPort interface is presented on a USB Type-C Plug
		1b	DisplayPort interface is presented on a USB Type-C Receptacle

Table 3-62. 0x51 DP SID Configuration Register Bit Field Definitions (continued)

Bits	Name	Description	
5:2	Signaling for Transport of DisplayPort Protocol	Each bit may be set and corresponds to a particular signaling rate and electrical spec. For example, this can be set to xx11b is that it supports both DP 1.3 rates and USB Gen 2 rates.	
		xxx1b	Supports DP v1.3 signaling rates and electrical specification
		xx1xb	Supports USB Gen 2 signaling rate and electrical specification
		x1xxb	Reserved
		1xxxb	Reserved
1:0	DP Port Capability	00b	Reserved
		01b	UFP_D-capable (including Branch device)
		10b	DFP_D-capable (including Branch device)
		11b	Both DFP_D and UFP_D-capable
Byte 1:			
7:2	Reserved	Reserved (Write 0).	
1	DP Mode	0b	DP Mode Disabled
		1b	DP Mode EnabledNote: DP must be enabled, bit[0], for this bit to enable DP. Note: DP only has one mode for now so this bit is redundant. However, other modes may be added in the future so providing the structure here for this. If other modes are added in the future, then bits 31:24 of the DP capabilities message (bits[39:32] of this register) will be non-zero.
0	Enable DP SID	0b	DP SVID disabled
		1b	DP SVID Enabled (at least one mode from bits 7:1 must also be enabled for DP to be enabled)

3.32 0x52 Intel VID Configuration

Table 3-63. 0x52 Intel VID Configuration Register

Address	Name	Access	Length	Power-Up Default
0x52	Intel VID Configuration	Read/Write	7	0 (Initialized by Application Customization)

Table 3-64. 0x52 Intel VID Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 7:			
7:2	Reserved	Reserved (write 0).	
1	TBT_AutoEntryAllowed	0b	TBT Alternate Mode auto-entry disabled.
		1b	TBT Alternate Mode auto-entry enabled.
0	Reserved	Reserved (write 0).	
Bytes 5-6: TBT Mode SOP' Data (treated as 16-bit little endian value)			
15:0	TBTModeDataTXSOPp	Upper 16 bits of data to be sent on Intel VID SVDM Discover Modes (SOP') response (UFP) or used to drive TBT AM policy (DFP). This field can be left all 0's when TBT device has a receptacle or captive active cable instead of a captive passive cable.	
Bytes 3-4: TBT Mode SOP Data (treated as 16-bit little endian value)			
15:0	TBTModeDataTXSOP	Upper 16 bits of data to be sent on Intel VID SVDM Discover Modes (SOP) response (UFP) or used to drive TBT AM policy (DFP).	
Byte 2: Intel VID Mode Configuration			
7:4	Reserved	Reserved (write 0)	
3	vPro_Capable	0b	vPro is not supported
		1b	vPro is supported
2	ANMinPowerRequired	0b	TBT Mode can be configured regardless of power contract. CapabilityMismatch field in Data Status will always be 0.
		1b	PD Controller will enter TBT Mode regardless of power contract, but will not set Data Status to indicate TBT Connected until ANMinimumPower limit has been met. Until sufficient power is available, Billboard will be presented and TBT Attention message will be sent to request USB connection instead of TBT. Note that once sufficient power is available, the Billboard will not be re-enabled even if a later contract does not provide sufficient power, however the CapabilityMismatch field in Data Status always reflects active contract when PD Controller is a Sink.
1	TBT_eMarker_Override	0b	If the PD Controller does not receive a response on SOP' it will assume a Cable VDO b2:0 value of 000b, which prevents Thunderbolt Mode entry.
		1b	If the PD Controller does not receive a response on SOP' it will assume a Cable VDO b2:0 value of 001b, which allows Thunderbolt Mode entry (will treat cable as 10Gb/s passive).
0	TBT_VOUT_3V3_Required	0b	VOUT_3V3 not required for Thunderbolt Mode support.
		1b	VOUT_3V3 is required for Thunderbolt Mode support.
Byte 1: Intel Mode Enables			
7:2	Reserved	Reserved (write 0)	
1	ThunderboltMode	0b	Thunderbolt Mode disabled.
		1b	Thunderbolt Mode enabled. The PD Controller as UFP will advertise Thunderbolt Mode. The PD Controller as DFP will negotiate Thunderbolt Mode.
0	Enable_Intel_VID	0b	Intel VID disabled.
		1b	Intel VID enabled.

3.33 0x57 User VID Status

Table 3-65. 0x57 User VID Status Register

Address	Name	Access	Length	Power-Up Default
0x57	User VID Status	Read Only	2	0 (Cleared on disconnect or Hard Reset)

Table 3-66. 0x57 User VID Status Register Bit Field Definitions

Bits	Name	Description	
Byte 2:			
7:5	Reserved	Reserved (0).	
4	UserMode4Status	0b	User Mode 4 not entered.
		1b	User Mode 4 entered.
3	UserMode3Status	0b	User Mode 3 not entered.
		1b	User Mode 3 entered.
2	UserMode2Status	0b	User Mode 2 not entered.
		1b	User Mode 2 entered.
1	UserMode1Status	0b	User Mode 1 not entered.
		1b	User Mode 1 entered.
0	Reserved	Reserved.	
Byte 1:			
7:5	Reserved	Reserved.	
4:2	ErrorCode		
1	VID Active	0b	VID not active
		1b	VID active
0	VID_Detected	0b	VID not detected.
		1b	VID detected.

3.34 0x58 DP SID Status

Table 3-67. 0x58 DP SID Status Register

Address	Name	Access	Length	Power-Up Default
0x58	DP SID Status	Read Only	37	0 (Cleared on disconnect or Hard Reset)

Table 3-68. 0x58 DP SID Status Register Bit Field Definitions

Bits	Name	Description		
Bytes 34-37: DP Mode Data RX SOP' (treated as 32-bit little endian value)				
31:0	DPModeDataSOPp	Contents of DP Discover Mode response from Cable Plug		
Bytes 30-33: DP Configure RX SOP' (treated as 32-bit little endian value)				
31:0	DPConfigFromPlug	Contents of DP Configure message received from Cable Plug		
Bytes 26-29: DP Configure TX SOP' (treated as 32-bit little endian value)				
31:0	DPConfigToPlug	Contents of DP Configure message sent to Cable Plug		
Bytes 22-25: DP Status RX SOP' (treated as 32-bit little endian value)				
31:0	DPStatusACKFrom Plug	Most recently received DP Status Acknowledgment from Cable Plug		
Bytes 18-21: DP Status TX SOP' (treated as 32-bit little endian value)				
31:0	DPStatusToPlug	Current Outgoing DP Status message contents to Cable Plug		
Bytes 14-17: DP Mode Data TX/RX (treated as 32-bit little endian value)				
31:0	DPModeData	Contents of DP Discover Mode response when received (DFP_U) or sent (UFP_U).		
Bytes 10-13: DP Configure TX/RX (treated as 32-bit little endian value)				
31:0	DPConfigure	Contents of DP Configure message when sent (DFP_U) or received (UFP_U).		
Bytes 6-9: DP Status RX (treated as 32-bit little endian value)				
31:0	DPStatusRX	Most recently received DP Status message contents.		
Bytes 2-5: DP Status TX (treated as 32-bit little endian value)				
31:0	DPStatusTX	Current Outgoing DP Status message contents.		
Byte 1: DP Mode Status				
7:5	Reserved	Reserved (0).		
4:2	ErrorCode	Error Code.		
1	DPModeActive	DFP_U	0b	DP Mode not active
			1b	PD Controller has entered DisplayPort Mode with attached UFP_U.
		UFP_U	0b	DP Mode not active
			1b	Attached DFP_U has entered DisplayPort Mode.
0	DP_SID_Detected	DFP_U	0b	DP SID not detected.
			1b	UFP_U returned DP SID in Discover SVIDs response or responded with ACK to DP SID SVDM Commands.
		UFP_U	0b	DP SID not detected.
			1b	DFP_U has issued DP SID SVDM (Discover Modes, Enter Mode, etc).

3.35 0x59 Intel VID Status

Table 3-69. 0x59 Intel VID Status Register

Address	Name	Access	Length	Power-Up Default
0x59	Intel VID Status	Read Only	9	0 (Cleared on disconnect or Hard Reset)

Table 3-70. 0x59 Intel VID Status Register Bit Field Definitions

Bits	Name	Description	
Bytes 8-9: TBT Discover Modes Response SOP (treated as 16-bit little endian value)			
15:0	TBTDiscoverModeDataSOP	Upper 16 bits of SOP Discover Modes response for TBT Mode when received (DFP) or sent (UFP). Lower 16 bits of the response are always 0x0001 NOTE: In the UFP role, this register simply copies the contents of the Intel VID Configuration register bits 23:8 at the time the Discover Modes response is generated.	
Bytes 6-7: TBT Enter Mode TX/RX (treated as 16-bit little endian value)			
15:0	TBTEnterModeData	Upper 16 bits of second VDO to Thunderbolt Enter Mode command when sent (DFP) or received (UFP).	
Bytes 2-5: TBT Attention TX/RX (treated as 32-bit little endian value)			
31:0	TBTAttentionData	Contents of Attention VDO in Thunderbolt Mode when sent (UFP) or received (DFP).	
Byte 1: Intel Mode Status			
7:5	Reserved	Reserved (0).	
4:2	ErrorCode	Error Code.	
1	ThunderboltModeActive	DFP	PD Controller has entered Thunderbolt Mode with attached UFP.
		UFP	Attached DFP has entered Thunderbolt Mode.
0	Intel_VID_Detected	DFP	UFP returned Intel VID in Discover SVIDs response or responded with ACK to Intel VID SVDM Commands.
		UFP	DFP has issued Intel VID SVDM (Discover Modes, Enter Mode, etc).

3.36 0x5C GPIO Configuration

Table 3-71. 0x5C GPIO Configuration Register

Address	Name	Access	Length	Power-Up Default
0x5C	GPIO Configuration	Read Only	64	0 (Initialized by Application Customization)

Table 3-72. 0x5C GPIO Configuration Register Bit Field Definitions

Bits	Description Name	
Bytes 61-64: GPIO Event Polarity		
31:23	Reserved	Reserved (write 0).
22:0	GPIO_EVENT_POL	Controls polarity of a selected event for each GPIO Setting bit to 0, does not alter the polarity of the event mapped to the corresponding GPIO. Setting bit to 1, inverts the polarity of the event mapped to the corresponding GPIO.
Bytes 56-60: Reserved for additional GPIO		
7:0	Reserved	Reserved (write 0).
Byte 55: GPIO22 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO22_EVENT	Event table mapping for GPIO22. See Table 3-74.
Byte 54: GPIO21 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO21_EVENT	Event table mapping for GPIO21. See Table 3-74.
Byte 53: GPIO20 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO20_EVENT	Event table mapping for GPIO20. See Table 3-74.
Byte 52: GPIO19 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO19_EVENT	Event table mapping for GPIO19. See Table 3-74.
Byte 51: GPIO18 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO18_EVENT	Event table mapping for GPIO18. See Table 3-74.
Byte 50: GPIO17 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO17_EVENT	Event table mapping for GPIO17. See Table 3-74.
Byte 49: GPIO16 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO16_EVENT	Event table mapping for GPIO16. See Table 3-74.
Byte 48: GPIO15 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO15_EVENT	Event table mapping for GPIO15. See Table 3-74.
Byte 47: GPIO14 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO14_EVENT	Event table mapping for GPIO14. See Table 3-74.
Byte 46: GPIO13 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO13_EVENT	Event table mapping for GPIO13. See Table 3-74.
Byte 45: GPIO12 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO12_EVENT	Event table mapping for GPIO12. See Table 3-74.
Byte 44: GPIO11 Configuration		

Table 3-72. 0x5C GPIO Configuration Register Bit Field Definitions (continued)

Bits	Description Name	
7	Reserved	Reserved (write 0).
6:0	GPIO11_EVENT	Event table mapping for GPIO11. See Table 3-74.
Byte 43: GPIO10 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO10_EVENT	Event table mapping for GPIO10. See Table 3-74.
Byte 42: GPIO9 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO9_EVENT	Event table mapping for GPIO9. See Table 3-74.
Byte 41: GPIO8 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO8_EVENT	Event table mapping for GPIO8. See Table 3-74.
Byte 40: GPIO7 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO7_EVENT	Event table mapping for GPIO7. See Table 3-74.
Byte 39: GPIO6 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO6_EVENT	Event table mapping for GPIO6. See Table 3-74.
Byte 38: GPIO5 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO5_EVENT	Event table mapping for GPIO5. See Table 3-74.
Byte 37: GPIO4 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO4_EVENT	Event table mapping for GPIO4. See Table 3-74.
Byte 36: GPIO3 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO3_EVENT	Event table mapping for GPIO3. See Table 3-74.
Byte 35: GPIO2 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO2_EVENT	Event table mapping for GPIO2. See Table 3-74.
Byte 34: GPIO1 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO1_EVENT	Event table mapping for GPIO1. See Table 3-74.
Byte 33: GPIO0 Configuration		
7	Reserved	Reserved (write 0).
6:0	GPIO0_EVENT	Event table mapping for GPIO0. See Table 3-74.
Bytes 29-32: Reserved		
31:0	Reserved	Reserved (write 0).
Bytes 25-28: GPIO Weak Pull-Up Control (treated as 32-bit little endian)		
31:22	Reserved	Reserved (write 0).
21:0	GPIO_PU_CFG	Controls weak pull-up setting for each configurable GPIO (1=Enabled, 0=Disabled).
Bytes 21-24: GPIO Weak Pull-Down Control (treated as 32-bit little endian)		
31:22	Reserved	Reserved (write 0).
21:0	GPIO_PD_CFG	Controls weak pull-down setting for each configurable GPIO (1=Enabled, 0=Disabled).
Bytes 17-20: GPIO_MUX_CFG (treated as 32-bit little endian)		
31:18	Reserved	Reserved (write 0).
17:0	GPIO_MUX_SEL	GPIO (0) vs. Secondary Function (1). See Table 3-73.
Bytes 13-16: GPIO Open-Drain Output Control (treated as 32-bit little endian)		

Table 3-72. 0x5C GPIO Configuration Register Bit Field Definitions (continued)

Bits	Description Name	
31:22	Reserved	Reserved (write 0).
21:0	GPIO_OD_EN	Controls push-pull (0) vs. open-drain (1) setting for each configurable GPIO.
Bytes 9-12: GPIO Output Control (treated as 32-bit little endian)		
31:22	Reserved	Reserved (write 0).
21:0	GPIO_DATA	Controls output level for each GPIO enabled as output (0=Drive Low, 1=Drive High)
Bytes 5-8: GPIO Interrupt Control (treated as 32-bit little endian)		
31:22	Reserved	Reserved (write 0).
21:0	GPIO_INT_EN	Controls interrupt enable for each GPIO (1=Interrupt Enabled, 0=Interrupt Disabled).
Bytes 1-4: GPIO OE Control (treated as 32-bit little endian)		
31:22	Reserved	Reserved (write 0).
21:0	GPIO_OE	Controls output enable for each GPIO (1=Output Enabled, 0=Hi-Z).

3.36.1 GPIO Multiplexor

Table 3-73 defines the GPIO Secondary Functions supported used in bytes 17-20 of the I/O Configuration Register.

Table 3-73. GPIO Secondary Functions

GPIOn	Secondary Function Name	Input Output	Secondary Function Description
0:2	Reserved	NA	Reserved. No muxing of secondary functions onto GPIOs associated with these bits
3	HPD1	Input/Output	DisplayPort HPD1 (TX and RX).
4	HPD2	Input/Output	DisplayPort HPD2 (TX and RX).
5:7	Reserved	NA	Reserved. No muxing of secondary functions onto GPIOs associated with these bits
8	SPI_MISO	Input	SPI Master input data, Slave output data. GPIO8 is always SPI_MISO whether this bit is 0 or 1
9	SPI_MOSI	Output	SPI Master output data, Slave input data
10	SPI_CLK	Output	SPI Master clock
11	SPI_SS	Output	SPI slave select
12	SWD_CLK	Input	SWD clock
13	SWD_DAT	Input/Output	SWD data
14	DSM_PWM1	Output	Pulse width modulated output
15	DSM_PWM2	Output	Pulse width modulated output
16	PP3 (PP_EXT1)	Output	PP3 (PP_EXT1) output
17	PP4 (PP_EXT2)	Output	PP4 (PP_EXT2) output
18	I2C3_SCL (GPIO5), I2C3_SDA (GPIO6)	Input/Output	I2C3 Master is active on GPIO5 and GPIO6 when this bit is set to 1. GPIO5 and GPIO6 are normal GPIOs when this bit is set to 0
31:19	Reserved	NA	Reserved. No muxing of secondary functions onto GPIOs associated with these bits

3.36.2 GPIO Events

Table 3-74 defines the GPIO Events supported used in bytes 33-64 of the GPIO Configuration Register.

Table 3-74. GPIO Events

Event#	Secondary Function Name	Input Output	Description
0	NullEvent	NA	No event associated with this GPIO.
1	PlugEvent_Port1	Output	Output (push-pull): Asserted high when plug event (attached state) has occurred on Port 1, otherwise low.
2	PlugEvent_Port2	Output	Output (push-pull): Asserted high when plug event has occurred on Port 2, otherwise low.
3	Cable_Orientation_Event_Port1	Output	Output (push-pull): Indicates the plug orientation on Port 1. Low when the plug is connected upside-up or disconnected. High when plug is connected upside-down.
4	Cable_Orientation_Event_Port2	Output	Output (push-pull): Indicates the plug orientation on Port 2. Low when the plug is connected upside-up or disconnected. High when plug is connected upside-down.
5	AMSEL_Event_Port1	Output	Output (push-pull): Used to configure external super-speed multiplexors for the DisplayPort Alternate Mode on Port 1. Set high when DisplayPort alternate mode is entered and pin assignment A/C/E. Set low when DisplayPort alternate mode is entered and pin assignment B/D/F. Set Hi-Z when DisplayPort alternate mode is not entered.
6	AMSEL_Event_Port2	Output	Output (push-pull): Used to configure external super-speed multiplexors for the DisplayPort Alternate Mode on Port 2. Set high when DisplayPort alternate mode is entered and pin assignment A/C/E. Set low when DisplayPort alternate mode is entered and pin assignment B/D/F. Set Hi-Z when DisplayPort alternate mode is not entered.
7	SourcePDO0Contract_Port1	Output	Output (push-pull): Asserted high when Source PDO0 on Port 1 has been negotiated, otherwise low.
8	SourcePDO1Contract_Port1	Output	Output (push-pull): Asserted high when Source PDO1 on Port 1 has been negotiated, otherwise low.
9	SourcePDO2Contract_Port1	Output	Output (push-pull): Asserted high when Source PDO2 on Port 1 has been negotiated, otherwise low.
10	SourcePDO3Contract_Port1	Output	Output (push-pull): Asserted high when Source PDO3 on Port 1 has been negotiated, otherwise low.
11	SourcePDO0ContractBit0_Port1	Output	Output (push-pull): Bit0 of binary encoded outputs indicating when Source PDO0 through PDO7 on Port 1have been negotiated.
12	SourcePDO1ContractBit1_Port1	Output	Output (push-pull): Bit1 of binary encoded outputs indicating when Source PDO0 through PDO7 on Port 1 have been negotiated.
13	SourcePDO2ContractBit2_Port1	Output	Output (push-pull): Bit2 of binary encoded outputs indicating when Source PDO0 through PDO7 on Port 1have been negotiated.
14	SourcePDO0Contract_Port2	Output	Output (push-pull): Asserted high when Source PDO0 on Port 1 has been negotiated, otherwise low.
15	SourcePDO1Contract_Port2	Output	Output (push-pull): Asserted high when Source PDO1 on Port 1 has been negotiated, otherwise low.
16	SourcePDO2Contract_Port2	Output	Output (push-pull): Asserted high when Source PDO2 on Port 1 has been negotiated, otherwise low.
17	SourcePDO3Contract_Port2	Output	Output (push-pull): Asserted high when Source PDO3 on Port 1 has been negotiated, otherwise low.
18	SourcePDO0ContractBit0_Port2	Output	Output (push-pull): Bit0 of binary encoded outputs indicating when Source PDO0 through PDO7 on Port 1have been negotiated.
19	SourcePDO1ContractBit1_Port2	Output	Output (push-pull): Bit1 of binary encoded outputs indicating when Source PDO0 through PDO7 on Port 1 have been negotiated.
20	SourcePDO2ContractBit2_Port2	Output	Output (push-pull): Bit2 of binary encoded outputs indicating when Source PDO0 through PDO7 on Port 1have been negotiated.
21	Reserved	N/A	Reserved.
22	Reserved	N/A	Reserved.
23	Reserved	N/A	Reserved.
24	Reserved	N/A	Reserved.

Table 3-74. GPIO Events (continued)

Event#	Secondary Function Name	Input Output	Description
25	Reserved	N/A	Reserved.
26	Reserved	N/A	Reserved.
27	Reserved	N/A	Reserved.
28	Reserved	N/A	Reserved.
29	Reserved	N/A	Reserved.
30	Reserved	N/A	Reserved.
31	Reserved	N/A	Reserved.
32	Reserved	N/A	Reserved.
33	Reserved	N/A	Reserved.
34	Reserved	N/A	Reserved.
35	Reserved	N/A	Reserved.
36	Reserved	N/A	Reserved.
37	Reserved	N/A	Reserved.
38	Reserved	N/A	Reserved.
39	USB3_Event_Port1	Output	Output (NMOS open-drain): High-Z when data connection is USB3 on Port 1, low in all other cases.
40	USB3_Event_Port2	Output	Output (NMOS open-drain): High-Z when data connection is USB3 on Port 2, low in all other cases.
41	DP_Mode_Selection_Event_Port1	Output	Output (push-pull): Asserted high when data connection is DP, otherwise low.
42	DP_Mode_Selection_Event_Port2	Output	Output (push-pull): Asserted high when data connection is DP, otherwise low.
43	User_SVID_Active_Event_Port1	Output	The User Alternate Mode event GPIO Identifies when a port has entered an Alternate Mode using the User Defined SVID. Asserted high when port is in User SVID Alternate Mode..
44	User_SVID_Active_Event_Port2	Output	The User Alternate Mode event GPIO Identifies when a port has entered an Alternate Mode using the User Defined SVID. Asserted high when port is in User SVID Alternate Mode..
45	Source_Sink_Event_Port1	Output	Asserted high when port is operating as a Source. Asserted low when port is operating as a Sink.
46	Source_Sink_Event_Port2	Output	Asserted high when port is operating as a Source. Asserted low when port is operating as a Sink.
47	DP_or_USB3_Event_Port1	Output	Asserted high when data connection is DisplayPort or USB3; Low if neither data mode is active or port is disconnected.
48	DP_or_USB3_Event_Port2	Output	Asserted high when data connection is DisplayPort or USB3; Low if neither data mode is active or port is disconnected.
49	UFP_DFP_Event_Port1	Output	Asserted high when port is operating as UFP. Asserted low when port is operating as DFP.
50	UFP_DFP_Event_Port2	Output	Asserted high when port is operating as UFP. Asserted low when port is operating as DFP.
51	TBT_Mode_Selection_Event_Port1	Output	Output (push-pull): Asserted high when data connection is TBT, otherwise low.
52	TBT_Mode_Selection_Event_Port2	Output	Output (push-pull): Asserted high when data connection is TBT, otherwise low.
53	Billboard_Event_Port1	Output	Output (push-pull): Asserted high when Billboard must be presented.
54	Billboard_Event_Port2	Output	Output (push-pull): Asserted high when Billboard must be presented.
55	Fault_Input_Event_Port1	Input	Used to allow external devices to enable error recovery on a given port. There is one fault condition input per port. When set low port enters Error Recovery State. When set high, no action.
56	Fault_Input_Event_Port2	Input	Used to allow external devices to enable error recovery on a given port. There is one fault condition input per port. When set low port enters Error Recovery State. When set high, no action.

Table 3-74. GPIO Events (continued)

Event#	Secondary Function Name	Input Output	Description
57	FastRoleSwap_Event_Port1	Input	On the falling edge of input event, a device configured as a Source will enable the FRS pull-down on the CC pin and start the FRS process. No action on rising edge of input event.
58	FastRoleSwap_Event_Port2	Input	On the falling edge of input event, a device configured as a Source will enable the FRS pull-down on the CC pin and start the FRS process. No action on rising edge of input event.
59	Fault_Condition_Active_Low_Event_Port1	Output	Asserts low on an overcurrent event.
60	Fault_Condition_Active_Low_Event_Port2	Output	Asserts low on an overcurrent event.
61	Input_Load_Appconfig_Set1_Event_Port1	Input	Upon Rising Edge: App Config Set for GPIO = High will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional). Upon Falling Edge: App Config Set for GPIO = Low will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional).
62	Input_Load_Appconfig_Set1_Event_Port2	Input	Upon Rising Edge: App Config Set for GPIO = High will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional). Upon Falling Edge: App Config Set for GPIO = Low will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional).
63	Input_Load_Appconfig_Set2_Event_Port1	Input	Upon Rising Edge: App Config Set for GPIO = High will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional). Upon Falling Edge: App Config Set for GPIO = Low will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional).
64	Input_Load_Appconfig_Set2_Event_Port2	Input	Upon Rising Edge: App Config Set for GPIO = High will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional). Upon Falling Edge: App Config Set for GPIO = Low will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional).
65	Input_Load_Appconfig_Set3_Event_Port1	Input	Upon Rising Edge: App Config Set for GPIO = High will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional). Upon Falling Edge: App Config Set for GPIO = Low will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional).
66	Input_Load_Appconfig_Set3_Event_Port2	Input	Upon Rising Edge: App Config Set for GPIO = High will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional). Upon Falling Edge: App Config Set for GPIO = Low will be loaded as the active configuration. 1st 4CC Data and Command is written to selected CMDX register (optional). 2nd 4CC Data and Command (or PD Task) is written to selected CMDx register (optional).
67	Sink_Greater_Than_Threshold_Event_Port1	Output	Asserted high when in an active PD contract and Sinking less than threshold setting.. Asserted low when any other Sink or Source PD contract is active, no PD contract is active, or port is disconnected

Table 3-74. GPIO Events (continued)

Event#	Secondary Function Name	Input Output	Description
68	Sink_Greater_Than_Threshold_Event_Port2	Output	Asserted high when in an active PD contract and Sinking less than threshold setting. Asserted low when any other sink or source PD contract is active, no PD contract is active, or port is disconnected
69	Retimer_PWR_EN_Event_Port1	Output	Power Control for external retimer attached to port 1. Asserted high when USB Type-C connection is present, or when the "Retimer_SoC_Force_PWR_Event" is asserted high. Otherwise, this event is asserted low
70	Retimer_PWR_EN_Event_Port2	Output	Power control for external retimer attached to port 2. Asserted high when USB Type-C connection is present, or when the "Retimer_SoC_Force_PWR_Event" is asserted high. Otherwise, this event is asserted low
71	Retimer_Reset_N_Event_Port1	Output	Reset signal for external retimer attached to port 1. Asserted high when a USB Type-C connection is present and asserted low when there is no USB Type-C connection present. Upon a USB Type-C connection, first the "Retimer_PWR_EN_Event_Portx" event will occur, and then this event will occur tRetimerForcePowerDelay later. When a USB Type-C connection is removed, first this event will go low, and then "Retimer_PWR_EN_Event_Portx" event will happen tRetimerForcePowerDelay later. tRetimerForcePowerDelay is set in the 0x43 Delay Configuration Register
72	Retimer_Reset_N_Event_Port2	Output	Reset signal for external retimer attached to port 2. Asserted high when a USB Type-C connection is present and asserted low when there is no USB Type-C connection present. Upon a USB Type-C connection, first the "Retimer_PWR_EN_Event_Portx" event will occur, and then this event will occur tRetimerForcePowerDelay later. When a USB Type-C connection is removed, first this event will go low, and then "Retimer_PWR_EN_Event_Portx" event will happen tRetimerForcePowerDelay later. tRetimerForcePowerDelay is set in the 0x43 Delay Configuration Register
73	ProcHot_N_Event_Port1	Output	A signal to the main SOC to notify it of any changes in power capabilities. When this event is asserted, typically the main SOC will reduce its power consumption until it has re-evaluated the new power capabilities of the system. This event is asserted high when the device enters Unattached.SRC, Unattached.SNK, when sending a Request message, sending an Accept message to a PR_SWAP request, or when a PD3.0 Fast Role Swap occurs. This event is asserted low when the ProcHot interrupt in the IntEventX register (0x14 for port 1, 0x15 for port 2) is cleared
74	ProcHot_N_Event_Port2	Output	A signal to the main SOC to notify it of any changes in power capabilities. When this event is asserted, typically the main SOC will reduce its power consumption until it has re-evaluated the new power capabilities of the system. This event is asserted high when the device enters Unattached.SRC, Unattached.SNK, when sending a Request message, sending an Accept message to a PR_SWAP request, or when a PD3.0 Fast Role Swap occurs. This event is asserted low when the ProcHot interrupt in the IntEventX register (0x14 for port 1, 0x15 for port 2) is cleared
75	Retimer_SoC_OVR_Force_PWR_Event	Input	When this input is asserted (high), the PD controller (through the Retimer_PWR_EN_Event_Portx GPIO event) will instruct the external retimers to power on always, even when no USB Type-C connection is present. When this input is deasserted (low), the PD controller will only instruct the external retimers to power on when a USB Type-C connection is present
76	Barrel_Jack_Event	Input	An input GPIO event to indicate to the PD controller that a barrel jack power source has been connected to the system. Upon a rising edge of this event, the dead battery flag will be cleared, the ExternallyPowered bit in the 0x29 Port Control register will be set to 1, and the PD controller will attempt to become the power Source if it is currently the power Sink through a PR_SWAP request. Upon a falling edge of this event, the ExternallyPowered bit will be set to 0, and the PD controller will attempt to become the power Sink if it is currently the power Source through a PR_SWAP request.
77	UFP_Indicator_Event	Output	Asserted high when at least one port has a data role of UFP
78	Prevent_DRSwap_To_UFP_Event	Input	When high DR_Swap requests that would result in the target port changing to the UFP role will be rejected

Table 3-74. GPIO Events (continued)

Event#	Secondary Function Name	Input Output	Description
79	High_Current_Contract_Active_Event	Output	Asserted high when at least one port has negotiated a contract exceeding 5V@0.9A
80	Prevent_High_Current_Contract_Event	Input	When high source capabilities are reduced to only 5V@0.9A
81	Reserved	N/A	Reserved
82	Reserved	N/A	Reserved
83	Reserved	N/A	Reserved
84	Reserved	N/A	Reserved
85	Audio_Mode_Event_Port1	Output	This event is asserted when an Audio Accessory (Ra/Ra) is attached on Port 1
86	Audio_Mode_Event_Port2	Output	This event is asserted when an Audio Accessory (Ra/Ra) is attached on Port 2
87	SRC_PWR_Greater_Than_Threshold_Event_Port1	Output	This event is asserted high when the USB Type-C implicit contract of the explicit USB PD contract currently negotiated is allowing the sourcing of power greater than the threshold value programmed in the PowerThresAsSourceContract Byte 7 in the Port Configuration Register (0x28). This event is asserted low when the currently negotiated contract is less than the programmed threshold
88	SRC_PWR_Greater_Than_Threshold_Event_Port2	Output	This event is asserted high when the USB Type-C implicit contract of the explicit USB PD contract currently negotiated is allowing the sourcing of power greater than the threshold value programmed in the PowerThresAsSourceContract Byte 7 in the Port Configuration Register (0x28). This event is asserted low when the currently negotiated contract is less than the programmed threshold
89	Debug_Accessory_Event_Port1	Output	This event is asserted when a Debug Accessory (Rp/Rp) is attached on Port 1
90	Debug_Accessory_Event_Port2	Output	This event is asserted when a Debug Accessory (Rp/Rp) is attached on Port 2
91	Sink_PDO0_Negotiated_Port1	Output	This event is asserted when the TXSinkPDO1 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
92	Sink_PDO1_Negotiated_Port1	Output	This event is asserted when the TXSinkPDO2 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
93	Sink_PDO2_Negotiated_Port1	Output	This event is asserted when the TXSinkPDO3 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
94	Sink_PDO3_Negotiated_Port1	Output	This event is asserted when the TXSinkPDO4 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
95	Sink_PDO_Negotiated_TT_1_Port1	Output	These 3 events combine to form a 3-bit truth table to allow digital outputs indicating the active state of up to 7 PDOs. TT 3 is the most-significant bit (MSB) and TT 1 is the least significant bit (LSB)
96	Sink_PDO_Negotiated_TT_2_Port1	Output	
97	Sink_PDO_Negotiated_TT_3_Port1	Output	
98	Sink_PDO0_Negotiated_Port2	Output	This event is asserted when the TXSinkPDO1 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
99	Sink_PDO1_Negotiated_Port2	Output	This event is asserted when the TXSinkPDO2 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
100	Sink_PDO2_Negotiated_Port2	Output	This event is asserted when the TXSinkPDO3 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
101	Sink_PDO3_Negotiated_Port2	Output	This event is asserted when the TXSinkPDO4 from the TX Sink Capabilities Register (0x33) has been negotiated. Otherwise, this event is deasserted
102	Sink_PDO_Negotiated_TT_1_Port2	Output	These 3 events combine to form a 3-bit truth table to allow digital outputs indicating the active state of up to 7 PDOs. TT 3 is the most-significant bit (MSB) and TT 1 is the least significant bit (LSB)
103	Sink_PDO_Negotiated_TT_2_Port2	Output	
104	Sink_PDO_Negotiated_TT_3_Port2	Output	
105	VCONN_On_Event_Port1	Output	This event is asserted when PP_CABLE1 is enabled to source VCONN on port 1

Table 3-74. GPIO Events (continued)

Event#	Secondary Function Name	Input Output	Description
106	VCONN_On_Event_Port2	Output	This GPIO is asserted when PP_CABLE2 is enabled to source VCONN on port 2
107	Reserved	N/A	Reserved
108	Reserved	N/A	Reserved
109	Reserved	N/A	Reserved
110	Reserved	N/A	Reserved
111	PR_Swap_Ext_Vbus_Dsch_Port1	Output	This event causes the mapped GPIO to be pulled low after a PR_Swap to enable an external V_{BUS} discharge circuit during a power-role swap on port 1
112	PR_Swap_Ext_Vbus_Dsch_Port2	Output	This event causes the mapped GPIO to be pulled low after a PR_Swap to enable an external V_{BUS} discharge circuit during a power-role swap on port 2
113	PP1_SW_Event	Output	This event is asserted whenever the PP1 internal power path switch is closed. It is deasserted whenever the PP1 switch is opened
114	PP2_SW_Event	Output	This event is asserted whenever the PP2 internal power path switch is closed. It is deasserted whenever the PP2 switch is opened
115	I2C1_Master_IRQ_Event_Port1	Input	When this input is asserted, it generates an interrupt to the I2C1 master so it can properly respond to an external retimer
116	I2C1_Master_IRQ_Event_Port2	Input	When this input is asserted, it generates an interrupt to the I2C1 master so it can properly respond to an external retimer
117	I2C3_Master_IRQ_Event_Port1	Input	When this input is asserted, it generates an interrupt to the I2C3 master so it can properly respond to an external retimer
118	I2C3_Master_IRQ_Event_Port2	Input	When this input is asserted, it generates an interrupt to the I2C3 master so it can properly respond to an external retimer
119	Reserved	N/A	Reserved
120	Reserved	N/A	Reserved
121	USB2_On_HS_Mux_Event_Port1	Output	This event is asserted high when USB2.0 is active, otherwise, it is deasserted
122	USB2_On_HS_Mux_Event_Port2	Output	This event is asserted high when USB2.0 is active, otherwise, it is deasserted
123	BC1.2_Host_Pull_Down_Enable_Event_Port1	Output	This event is set low when BC1.2 ChargerAdvertiseEnable bits are set to one of the DCP modes in the Port Control Register (0x29) to disable the USB2.0 Host Pull-downs (Hi-Z them), if the USB Host needs an external signal to disable its pull-downs, so the BC1.2 DCP modes can function properly. This event is also asserted low when there is no USB Type-C connection. Otherwise, it is asserted high.
124	BC1.2_Host_Pull_Down_Enable_Event_Port2	Output	This event is set low when BC1.2 ChargerAdvertiseEnable bits are set to one of the DCP modes in the Port Control Register (0x29) to disable the USB2.0 Host Pull-downs (Hi-Z them), if the USB Host needs an external signal to disable its pull-downs, so the BC1.2 DCP modes can function properly. This event is also asserted low when there is no USB Type-C connection. Otherwise, it is asserted high.
125	Sink_Arbitration_Output	Output	Works in conjunction with Sink_Arbitration_Input to ensure only one sinking path in the system is turned on.
126	Sink_Arbitration_Input	Input	On a falling edge of this GPIO, the PD controller will evaluate the policy engine state and context for each port. If appropriate, the PD controller will enable the sink paths for one or both ports. Before enabling the sink paths, the Sink_Arbitration_Output will be driven high, and the PD controller will wait for the MultiPortSinkNonOverlapTime which is set in the Global System Configuration register (0x27). On a rising edge of this GPIO, the PD controller disables the sink paths for the ports that are connected to a USB PD source The PD controller also drives the Sink_Arbitration_Output low.

3.37 0x5D Retimer Debug Mode

After the PD controller writes data from Bytes 3-6 of the 0x50 Data Control register to the Retimer, the PD controller will read back the data it wrote to the Retimer and store that data in this register.

Table 3-75. 0x5D Retimer Debug Mode Register

Address	Name	Access	Length	Power-Up Default
0x5D	Retimer Debug Mode	Read-Write	4	0

Table 3-76. 0x5D Retimer Debug Mode Register Bit Field Definitions

Bits	Name	Description
Bytes 1-4: Retimer Debug Mode Register		

3.38 0x5F Data Status

Table 3-77. 0x5F Data Status Register

Address	Name	Access	Length	Power-Up Default
0x5F	Data Status	Read Only	5	0 (cleared on disconnect)

Table 3-78. 0x5F Data Status Register Bit Field Definitions

Bits	Name	Description	
Byte 5:			
7:0	Debug_Alternate_Mode_ID	NIDnT Overlay Number	
Bytes 1-4: Data Status (treated as 32-bit little endian value)			
31	Reserved	Reserved (0)	
30	Retimer_Data_Valid	0b	Bytes 6-9 are not valid
		1b	Bytes 6-9 are valid
29:28	TBTCableGen	00b	3rd generation TBT (10.3125 and 20.625 Gb/s)
		01b	4th generation TBT (10.0, 10.3125, 20.0 and 20.625 Gb/s)
		10b-11b	Reserved
27:25	TBTCableSpeedSupport	000b	Reserved
		001b	USB3.1 gen1 cable (10Gb/s Thunderbolt support)
		010b	10Gb/s only
		011b	10Gb/s & 20Gb/s only
		100b-111b	Reserved
24	S0_power_negotiated	0b	Active contract does not have a power mismatch or PD Controller is not a Sink.
		1b	Active contract (as a Sink) has a power mismatch. Not enough power for S0.
23	ForceLSX	0b	Normal operation.
		1b	Force LSX connection active, regardless of TBT operation.
22	Debug_Alternate_Mode_Type	0b	NIDnT
		1b	IDO
21	Debug_Alternate_Mode_Connection	0b	Debug alternate mode not entered
		1b	Debug alternate mode entered
20	ActiveLinkTraining	0b	Active with bi-directional LSRX communication (also used for passive cables)
		1b	Active with uni-directional LSRX communication
19	vPro_Dock_detected	0b	No vPro Dock detected
		1b	vPro Dock detected
18	CableType	0b	Non-Optical Cable
		1b	Optical Cable
17	TBTType	0b	Type-C to Type-C Cable
		1b	Legacy Adapter
16	TBTConnection	0b	No Thunderbolt connection. This value is also used if TBT Mode is active but an Attention SVDM has been sent/received enabling USB2 instead of TBT.
		1b	Thunderbolt connection (see above bits for more details).
15	HPDlevel[1]	HPD level from PD Controller to TBT Controller to DP Source for connection. Used only for TBT hosts. Not used for TBT devices.	
		0b	HPD low
		1b	HPD high

(1) Titan Ridge only.

Table 3-78. 0x5F Data Status Register Bit Field Definitions (continued)

Bits	Name	Description	
14	HPD_IRQsticky[1]	HPD IRQ from PD Controller to TBT Controller to DP Source for connection. Used only for TBT hosts. Not used for TBT devices.	
		0b	No HPD IRQ
		1b	HPD IRQ
13	HPD_IRQ_ACK[1]	0b	No HPD_IRQ_ACK.
		1b	HPD_IRQ_ACK.
12	Debug_Accessory_Mode	0b	No Debug Accessory Present
		1b	Debug Accessory Present
11:10	DPPinAssignment	00b	'Legacy' DP, USB-C to DP cable (spec pin assignments E-F, if supported).
		01b	'Legacy' DP, USB-C to USB-C cable (spec pin assignments C-D, if supported).
		10b	'New' DP, USB-C to USB-C cable (spec pin assignments A-B, if supported).
		11b	Reserved
9	DPSourceSink	0b	DP Source (DFP_D) connection requested (if supported by configuration).
		1b	DP Sink (UFP_D) connection requested (if supported by configuration).
8	DPConnection	0b	No DisplayPort connection.
		1b	DisplayPort connection (see above bits for more details).
7	USBDataRole	0b	DFP
		1b	UFP
6	USB3Speed	0b	USB3 limited to Gen 1 speed (5Gbps).
		1b	USB3 allowed to Gen 2 speed (10Gbps).
5	USB3Connection	0b	No USB3 connection.
		1b	USB3 connection on SSTx1/Rx1 if upside-up, SSTx2/Rx2 if upside-down.
4	USB2Connection	0b	No USB2 connection to USB_RP.
		1b	USB2 connection to USB_RP on 'Mission' D+/D- pair.
3	OvercurrentOrTemperature	0b	No over-current or over-temperature condition
		1b	Over-current or over-temperature condition has occurred.
2	ActiveCable	0b	Cable is passive.
		1b	Cable is active.
1	DataOrientation	0b	Plug is oriented on CC1 (upside-up) or no data connection.
		1b	Plug is oriented on CC2 (upside-down) with a valid data connection.
0	DataConnection	0b	No data connection (rest of bits in this register are cleared).
		1b	Data connection present (at least one other bit in this register is non-zero).

Equivalent DisplayPort spec pin assignment mapping:

Table 3-79. 0x5F Data Status (Equivalent DP Specification Pin Assignment Mapping)

DPPinAssignment	USB3Connection	DPSourceSink = 0	DPSourceSink = 1
00	0	DP Source Pin Assignment "E"	DP Sink Pin Assignment "E"
00	1	DP Source Pin Assignment "F"	INVALID
01	0	DP Source Pin Assignment "C"	DP Sink Pin Assignment "C"
01	1	DP Source Pin Assignment "D"	DP Sink Pin Assignment "D"
10	0	DP Source Pin Assignment "A"	DP Sink Pin Assignment "A"
10	1	DP Source Pin Assignment "B"	DP Sink Pin Assignment "B"

Table 3-79. 0x5F Data Status (Equivalent DP Specification Pin Assignment Mapping) (continued)

11	0	INVALID	INVALID
11	1	INVALID	INVALID

3.39 0x60 RX User VID Attention VDM

NOTE: Only Structured VDM messages for User SVID with Command Type = Initiator (00b) and Command = Attention (6) get stored in this buffer. See register 0x61 (Section 3.40) for all other inbound VDMs.

Table 3-80. 0x60 RX User VID Attention VDM Register

Address	Name	Access	Length	Power-Up Default
0x60	RX User VID Attention VDM	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-81. 0x60 RX User VID Attention VDM Register Bit Field Definitions

Bits	Name	Description
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO7	Seventh Data Object of most recently received Attention SVDM.
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO6	Sixth Data Object of most recently received Attention SVDM.
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO5	Fifth Data Object of most recently received Attention SVDM.
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO4	Fourth Data Object of most recently received Attention SVDM.
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO3	Third Data Object of most recently received Attention SVDM.
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO2	Second Data Object of most recently received Attention SVDM.
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)		
31:0	RXAttentionDO1	First Data Object of most recently received Attention SVDM.
Byte 1: RX Attention Status		
7:5	RXAttentionSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.
4:3	Reserved	Reserved.
2:0	RXAttentionNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).

3.40 0x61 RX User VID Other VDM

Table 3-82. 0x61 RX User VID Other VDM Register

Address	Name	Access	Length	Power-Up Default
0x61	RX User VID Other VDM	Read Only	29	0 (Reset on disconnect/connect/Hard Reset)

Table 3-83. 0x61 RX User VID Other VDM Register Bit Field Definitions

Bits	Name	Description	
Bytes 26-29: DO #7 (treated as a 32-bit little endian value)			
31:0	RXVDMDO7	Seventh Data Object of most recently received VDM.	
Bytes 22-25: DO #6 (treated as a 32-bit little endian value)			
31:0	RXVDMDO6	Sixth Data Object of most recently received VDM.	
Bytes 18-21: DO #5 (treated as a 32-bit little endian value)			
31:0	RXVDMDO5	Fifth Data Object of most recently received VDM.	
Bytes 14-17: DO #4 (treated as a 32-bit little endian value)			
31:0	RXVDMDO4	Fourth Data Object of most recently received VDM.	
Bytes 10-13: DO #3 (treated as a 32-bit little endian value)			
31:0	RXVDMDO3	Third Data Object of most recently received VDM.	
Bytes 6-9: DO #2 (treated as a 32-bit little endian value)			
31:0	RXVDMDO2	Second Data Object of most recently received VDM.	
Bytes 2-5: DO #1 (treated as a 32-bit little endian value)			
31:0	RXVDMDO1	First Data Object of most recently received VDM.	
Byte 1: RX VDM Status			
7:5	RXVDMSequenceNum	Increments by one every time this register is updated, rolls over upon reflow.	
4:3	RXVDMSource	SOP* of message source.	
		00b	VDM came from SOP.
		01b	VDM came from SOP'.
		10b	VDM came from SOP''.
		11b	VDM came from SOP*_Debug.
2:0	RXVDMNumValid	Number of valid VDOs in this register (#bytes/4, 0-7).	

3.41 0x62 Binary Data Indices

Table 3-84. 0x62 Binary Data Indices Register

Address	Name	Access	Length	Power-Up Default
0x62	Binary Data Indicies	Read/Write	12	0 (Initialized by Application Customization)

Table 3-85. 0x62 Binary Data Indices Register Bit Field Definitions

Bits	Name	Description
Bytes 11-12: Reserved		
Bytes 9-10: Reserved		
Bytes 3-8: I2C Master Data		
47:40	NumberofI2CEvent_Port 2	Number of I2C Events associated with port 2
39:32	I2CEventStartIndex_Port 2	Start index of the I2C Event offsets associated with port 2
31:24	NumberofI2CEvent_Port 1	Number of I2C Events associated with port 1
23:16	I2CEventStartIndex_Port 1	Start index of the I2C Event offsets associated with port 1
15:8	NumberofI2CEvents_Common	Number of I2C Events associated with both ports
7:0	I2CEventStartIndex_Common	Start index of the I2C Event offsets associated with both ports
Bytes 1-2: Country Codes Data		
15:8	NumberofCountryCodes	Number of Country Codes supported
7:0	CountryCodesStartIndex	Start index of the Country Codes offsets in the Application customization binary buffer

3.42 0x63 MIPI VID Status

Table 3-86. 0x63 MIPI VID Status Register

Address	Name	Access	Length	Power-Up Default
0x63	MIPI VID Status	Read Only	1	0 (Cleared on disconnect or Hard Reset)

Table 3-87. 0x63 MIPI VID Status Register Bit Field Definitions

Bits	Name	Description	
Byte 1: MIPI Mode Status			
7:5	Reserved	Reserved (0).	
4:2	ErrorCode	Error Code.	
1	DebugModeStatus	0b	Debug Mode not entered.
		1b	Debug Mode entered.
0	MIPI_VIDStatus	0b	MIPI VID not entered.
		1b	MIPI VID entered.

3.43 0x64 I2C Master Config

Table 3-88. 0x64 I2C Master Configuration Register

Address	Name	Access	Length	Power-Up Default
0x64	I2C Master Configuration	Read/Write	16	0 (Initialized by Application Customization)

Table 3-89. 0x64 I2C Master Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 16: Index 8 I2C Module mapping			
Byte 15: Index 7 I2C Module mapping			
Byte 14: Index 6 I2C Module mapping			
Byte 13: Index 5 I2C Module mapping			
Byte 12: Index 4 I2C Module mapping			
Byte 11: Index 3 I2C Module mapping			
Byte10: Index 2 I2C Module mapping			
Byte 9: Index 1 I2C Module mapping			
Byte 8: Index 8 Slave Address Mapping - Sets I2C address associated with events for index 8 (Bit definition matches Byte 1)			
Byte 7: Index 7 Slave Address Mapping - Sets I2C address associated with events for index 7 (Bit definition matches Byte 1)			
Byte 6: Index 6 Slave Address Mapping - Sets I2C address associated with events for index 6 (Bit definition matches Byte 1)			
Byte 5: Index 5 Slave Address Mapping - Sets I2C address associated with events for index 5 (Bit definition matches Byte 1)			
Byte 4: Index 4 Slave Address Mapping - Sets I2C address associated with events for index 4 (Bit definition matches Byte 1)			
Byte 3: Index 3 Slave Address Mapping - Sets I2C address associated with events for index 3 (Bit definition matches Byte 1)			
Byte 2: Index 2 Slave Address Mapping - Sets I2C address associated with events for index 2 (Bit definition matches Byte 1)			
7:0	Reserved	Reserved (Write 0).	
Byte 1: Index 1 Slave Address Mapping - Sets I2C address associated with events for index 1			
7:1	SlaveAddr	7-bit I2C slave address	
0	SlaveEnable	Enable/Disable of I2C Master for this slave.	
		0b	Disabled
		1b	Enabled

3.44 0x69 TypeC State Register

Table 3-90. 0x69 TypeC State Register

Address	Name	Access	Length	Power-Up Default
0x69	TypeC State	Read	4	0

Table 3-91. 0x69 TypeC State Register Bit Field Definitions

Bits	Name	Description	
Byte 4: Type C Port State			
7:0	TypeCPortState	00h	Disabled
		01h-04h	Reserved.
		05h	ErrorRecovery
		06h-23h	Reserved.
		24h	Unattached.Accessory
		25h-2Ah	Reserved.
		2Bh	AttachWait.Accessory
		2Ch-44h	Reserved.
		45h	Try.SRC
		46h-4Dh	Reserved.
		4Eh	TryWait.SNK
		4Fh	Try.SNK
		50h	TryWait.SRC
		51-5Fh	Reserved.
		60h	Attached.SRC
		61h	Attached.SNK
		62h	AudioAccessory
		63h	DebugAccessory
		64h	AttachWait.SRC
		65h	AttachWait.SNK
		66h	Unattached.SNK
		67h	Unattached.SRC
		68h-FFh	Reserved.
Byte 3: CC2 Pin State			
7:0	CC2PinState	00h	Not connected
		01h	Ra detected (Source only)
		02h	Rd detected (Source only)
		03h	STD Advertisement detected (SInk only)
		04h	1.5A Advertisement detected (Sink Only)
		05h	3.0A Advertisement detected (Sink Only)
		06h - FFh	Reserved
Byte 2: CC1 Pin State			
7:0	CC1PinState	00h	Not connected
		01h	Ra detected (Source only)
		02h	Rd detected (Source only)
		03h	STD Advertisement detected (SInk only)
		04h	1.5A Advertisement detected (Sink Only)
		05h	3.0A Advertisement detected (Sink Only)
		06h - FFh	Reserved
Byte1: CC Pin for PD			

Table 3-91. 0x69 TypeC State Register Bit Field Definitions (continued)

Bits	Name	Description	
7:0	CCpinForPD	00h	Not connected
		01h	C_CC1 is CC pin for PD communication
		02h	C_CC2 is CC pin for PD communication
		03h - FFh	Reserved

3.45 0x6B HW Control

Table 3-92. 0x6B HW Control Register

Address	Name	Access	Length	Power-Up Default
0x6B	HW Control	Read/Write	9	0 (Initialized by Application Customization)

Table 3-93. 0x6B HW Control Register Bit Field Definitions

Bits	Name	Description	
Byte 9: Reserved (must write 0)			
Bytes 5-8: PWM2 (1)			
31:24	Reserved	Reserved (write 0).	
23:16	PWM2width	PWM2 pulse width.	
15:12	Reserved	Reserved (write 0).	
11:8	PWM2period	PWM2 clock period	
7:2	Reserved	Reserved (write 0).	
1	PWM2clockSource	PWM2 clock source	
		0b	100kHz
		1b	24 MHz
0	PWM2enable	Enable/Disable of PWM2	
		0b	Disabled
		1b	Enabled
Bytes 1-4: PWM1 (1)			
31:24	Reserved	Reserved (write 0).	
23:16	PWM1width	PWM1 pulse width.	
15:12	Reserved	Reserved (write 0).	
11:8	PWM1period	PWM`1clock period	
7:2	Reserved	Reserved (write 0).	
1	PWM1clockSource	PWM1 clock source	
		0b	100kHz
		1b	24 MHz
0	PWM1enable	Enable/Disable of PWM1	
		0b	Disabled
		1b	Enabled

(1) The PWM must be configured by the MCU in the system; the PD state machine in the TPS65987/88 does not control the PWM duty cycle.

3.46 0x6C App Configuration

Table 3-94. 0x6C App Configuration Register

Address	Name	Access	Length	Power-Up Default
0x6C	App Configuration	Read Only	60	0 (Initialized by Application Customization)

Table 3-95. 0x6C App Configuration Register Bit Field Definitions

Bits	Name	Description	
Bytes 57-60: Second 4CC Command Exit Group 3. Refer to Group 1 details.			
Bytes 53-56: First 4CC Command Exit Group 3. Refer to Group 1 details.			
Bytes 49-52: Second 4CC Command Enter Group 3. Refer to Group 1 details.			
Bytes 45-48: First 4CC Command Enter Group 3. Refer to Group 1 details.			
Byte 44: Application Configuration Second 4CC Command Interface Group 2. Refer to Group 1 details.			
Byte 43: Application Configuration First 4CC Command Interface Group 2. Refer to Group 1 details.			
Bytes 41-42: Application Configuration Indexes Group 3. Refer to Group 1 details.			
Bytes 37-40: Second 4CC Command Exit Group 2. Refer to Group 1 details.			
Bytes 33-36: First 4CC Command Exit Group 2. Refer to Group 1 details.			
Bytes 29-32: Second 4CC Command Enter Group 2. Refer to Group 1 details.			
Bytes 25-28: First 4CC Command Enter Group 2. Refer to Group 1 details.			
Byte 24: Application Configuration Second 4CC Command Interface Group 2. Refer to Group 1 details.			
Byte 23: Application Configuration First 4CC Command Interface Group 2. Refer to Group 1 details.			
Bytes 21-22: Application Configuration Indexes Group 2. Refer to Group 1 details.			
Bytes 17-20: Second 4CC Command Exit Group 1			
31:0	Command2ExitGroup	Second 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command may be a Task Command.	
Bytes 13-16: First 4CC Command Exit Group 1			
31:0	Command1ExitGroup	First 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command cannot be a Task Command.	
Bytes 9-12: Second 4CC Command Enter Group 1			
31:0	Command2EnterGroup	Second 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This may be a Task Command.	
Bytes 5-8: First 4CC Command Enter Group 1			
31:0	Command1EnterGroup	First 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This command cannot be a Task Command.	
Byte 4: Application Configuration Second 4CC Command Interface Group 1			
7:1	Reserved	Reserved	
0	Command2Interface	0b	CMD1
		1b	CMD2
Byte 3: Application Configuration First 4CC Command Interface Group 1			
7:1	Reserved	Reserved	
0	Command1Interface	0b	CMD1
		1b	CMD2
Bytes 1-2: Application Configuration Indexes Group 1			
15:8	AppConfigIndexExit	Index pointing to application configuration to use upon GPIO asserted low or Alternate Mode exit events.	
7:0	AppConfigIndexEnter	Index pointing to application configuration to use upon GPIO asserted high or Alternate Mode entered events.	

3.47 0x70 Sleep Configuration Register

Table 3-96. 0x70 Sleep Configuration Register

Address	Name	Access	Length	Power-Up Default
0x70	Sleep Configuration	Read/Write	1	0 (Initialized by Application Customization)

Table 3-97. 0x70 Sleep Configuration Register Bit Field Definitions

Bits	Name	Description	
Byte 1:			
7:3	Reserved	Reserved (Write 0).	
2:1	SleepTime	00b	Reserved
		01b	Wait for at least 100ms before entering sleep mode
		10b	Wait for at least 1000ms before entering sleep mode
		11b	Reserved
0	Sleep Mode Allowed	0b	Device will never enter sleep modes
		1b	Device will enter sleep modes after device is idle for Sleep Time

3.48 0x71 Received Manufacturer Info Data Block SOP (MIDB)

Table 3-98. 0x71 Received Manufacturer Info Data Block SOP (MIDB) Register

Address	Name	Access	Length	Power-Up Default
0x71	RX MIDB SOP	Read Only	4 to 26	0

Table 3-99. 0x71 Received Manufacturer Info Data Block SOP (MIDB)

Bits	Name	Description
Bytes 5-26:Manufacturer String		
Bytes 3-4: PID		
Bytes 1-2: VID		

3.49 0x72 GPIO Status Register

Check the device-specific datasheet for the available GPIO because it may vary by device type.

Table 3-100. 0x72 GPIO Status Register

Address	Name	Access	Length	Power-Up Default
0x72	GPIO Status	Read	8	0

Table 3-101. 0x72 GPIO Status Register Bit Field Definitions

Bits	Name	Description	
Byte 8: Reserved			
Byte 7: GPIO[21:16] Direction Register - same format as Byte 1, respectively for each GPIO. Unused bits are reserved.			
Byte 6: GPIO[15:8] Direction Register - same format as Byte 1, respectively for each GPIO.			
Byte 5: GPIO[7:0] Direction Register			
7	GPIO7Dir	0b	Configured as Input
		1b	Configured as output
6	GPIO6Dir	0b	Configured as Input
		1b	Configured as output
5	GPIO5Dir	0b	Configured as Input
		1b	Configured as output
4	GPIO4Dir	0b	Configured as Input
		1b	Configured as output
3	GPIO3Dir	0b	Configured as Input
		1b	Configured as output
2	GPIO2Dir	0b	Configured as Input
		1b	Configured as output
1	GPIO1Dir	0b	Configured as Input
		1b	Configured as output
0	GPIO0Dir	0b	Configured as Input
		1b	Configured as output
Byte 4: Reserved			
Byte 3: GPIO[21:16] Data Register - same format as Byte 1, respectively for each GPIO. Unused bits are reserved.			
Byte 2: GPIO[15:8] Data Register - same format as Byte 1, respectively for each GPIO.			
Byte 1: GPIO[7:0] Data Register			
7	GPIO7Data	0b	Logic low at GPIO[7]
		1b	Logic high at GPIO[7]

Table 3-101. 0x72 GPIO Status Register Bit Field Definitions (continued)

Bits	Name	Description	
6	GPIO6Data	0b	Logic low at GPIO[6]
		1b	Logic high at GPIO[6].
5	GPIO5Data	0b	Logic low at GPIO[5]
		1b	Logic high at GPIO[5]
4	GPIO4Data	0b	Logic low at GPIO[4]
		1b	Logic high at GPIO[4]
3	GPIO3Data	0b	Logic low at GPIO[3]
		1b	Logic high at GPIO[3]
2	GPIO2Data	0b	Logic low at GPIO[2]
		1b	Logic high at GPIO[2]
1	GPIO1Data	0b	Logic low at GPIO[1]
		1b	Logic high at GPIO[1]
0	GPIO0Data	0b	Logic low at GPIO[0]
		1b	Logic high at GPIO[0[

3.50 0x73 Transmit Manufacturer Info Data Block SOP (MIDB)

Table 3-102. 0x73 Transmit Manufacturer Info Data Block SOP (MIDB) Register

Address	Name	Access	Length	Power-Up Default
0x73	TX MIDB SOP	Read Only	4 to 26	0

Table 3-103. 0x73 Transmit Manufacturer Info Data Block SOP (MIDB)

Bits	Name	Description
Bytes 5-26:	Manufacturer String	
Bytes 3-4:	PID	
Bytes 1-2:	VID	

3.51 0x74 Received Alert Data Object (ADO)

Table 3-104. 0x74 Received Alert Data Object (ADO) Register

Address	Name	Access	Length	Power-Up Default
0x74	RX ADO	Read Only	4	0

Table 3-105. 0x74 Received Alert Data Object (ADO)

Bits	Name	Description
Bytes 1-4: Latest ADO		
31:24	AlertType	Type of alert
23:20	FixedBatteries	Status change of fixed batteries when selected by AlertType.
19:16	HotSwapBatteries	Status change of hot swappable batteries when selected by AlertType.
15:0	Reserved	Shall be set to zero.

3.52 0x75 Transmit Alert Data Object (ADO)

Table 3-106. 0x75 Transmit Alert Data Object (ADO) Register

Address	Name	Access	Length	Power-Up Default
0x75	TX ADO	Read/Write	4	0

Table 3-107. 0x75 Transmit Alert Data Object (ADO)

Bits	Name	Description
Bytes 1-4: ADO to be transmitted.		
31:24	AlertType	Type of alert
23:20	FixedBatteries	Status change of fixed batteries when selected by AlertType.
19:16	HotSwapBatteries	Status change of hot swappable batteries when selected by AlertType.
15:0	Reserved	Shall be set to zero.

3.53 0x76 Received Source Capabilities Extended Data Block (SCEDB)

Table 3-108. 0x76 Received Source Capabilities Extended Data Block (SCEDB) Register

Address	Name	Access	Length	Power-Up Default
0x76	RX SCEDB	Read Only	24	0

Table 3-109. 0x76 Received Source Capabilities Extended Data Block (SCEDB)

Bits	Name	Description
Byte 24: Source PDP		
Byte 23: Batteries		
Byte 22: Source Inputs		
Byte 21: Touch Temperature		
Bytes 19-20: Peak Current 3		
Bytes 17-18: Peak Current 2		
Bytes 15-16: Peak Current 1		
Byte 14: Touch Current		
Byte 13: Compliance		
Byte 12: Holdup Time		
Byte 11: Voltage Regulation		
Byte 10: HW Version		
Byte 9: FW Version		
Bytes 5-8: XID		
Bytes 3-4: PID		
Bytes 1-2: VID		

3.54 0x77 Transmit Source Capabilities Extended Data Block (SCEDB)

Table 3-110. 0x77 Transmit Source Capabilities Extended Data Block (SCEDB) Register

Address	Name	Access	Length	Power-Up Default
0x77	TX SCEDB	Read/Write	24	0

Table 3-111. 0x77 Transmit Source Capabilities Extended Data Block (SCEDB)

Bits	Name	Description
Byte 24: Source PDP		
Byte 23: Batteries		
Byte 22: Source Inputs		
Byte 21: Touch Temperature		
Bytes 19-20: Peak Current 3		
Bytes 17-18: Peak Current 2		
Bytes 15-16: Peak Current 1		
Byte 14: Touch Current		
Byte 13: Compliance		
Byte 12: Holdup Time		
Byte 11: Voltage Regulation		
Byte 10: HW Version		
Byte 9: FW Version		
Bytes 5-8: XID		
Bytes 3-4: PID		
Bytes 1-2: VID		

3.55 0x78 Received Status Data Block (SDB)

Table 3-112. 0x78 Received Status Data Block (SDB) Register

Address	Name	Access	Length	Power-Up Default
0x78	RX SDB	Read Only	7	0

Table 3-113. 0x78 Received Status Data Block (SDB)

Bits	Name	Description
Bytes 6-7: SOP' SDB		
Byte 7: Flags		
Byte 6: Internal Temperature		
Bytes 1-5: SOP SDB		
Byte 5: Temperature Status		
Byte 4: Event Flags		
Byte 3: Present Battery Input		
Byte 2: Present Input		
Byte 1: Internal Temperature		

3.56 0x79 Transmit Status Data Block (SDB)

Table 3-114. 0x79 Transmit Status Data Block (SDB) Register

Address	Name	Access	Length	Power-Up Default
0x79	TX SDB	Read/Write	7	0

Table 3-115. 0x79 Transmit Source Data Block (SDB)

Bits	Name	Description
Bytes 6-7: SOP' SDB		
Byte 7: Flags		
Byte 6: Internal Temperature		
Bytes 1-5: SOP SDB		
Byte 5: Temperature Status		
Byte 4: Event Flags		
Byte 3: Present Battery Input		
Byte 2: Present Input		
Byte 1: Internal Temperature		

3.57 0x7A Received Battery Status Data Objects (BSDO)

Table 3-116. 0x7A Received Battery Status Data Objects (BSDO) Register

Address	Name	Access	Length	Power-Up Default
0x7A	RX BSDO	Read Only	32	0

Table 3-117. 0x7A Received Battery Status Data Objects (BSDO)

Bits	Name	Description
Bytes 29-32: Latest BSDO Hot-Swappable Battery 3		
Bytes 25-28: Latest BSDO Hot-Swappable Battery 2		
Bytes 21-24: Latest BSDO Hot-Swappable Battery 1		
Bytes 17-20: Latest BSDO Hot-Swappable Battery 0		
Bytes 13-16: Latest BSDO Fixed Battery 3		
Bytes 9-12: Latest BSDO Fixed Battery 2		
Bytes 5-8: Latest BSDO Fixed Battery 1		
Bytes 1-4: Latest BSDO Fixed Battery 0		
31:16	BatteryPC	Battery's State of Charge (SOC)
15:8	BatteryInfo	Battery State
7:0	Reserved	Shall be set to zero.

3.58 0x7B Transmit Battery Status Data Objects (BSDO)

Table 3-118. 0x7B Transmit Battery Status Data Objects (BSDO) Register

Address	Name	Access	Length	Power-Up Default
0x7B	TX BSDO	Read/Write	32	0

Table 3-119. 0x7B Transmit Battery Status Data Objects (BSDO)

Bits	Name	Description
Bytes 29-32: Latest BSDO Hot-Swappable Battery 3		
Bytes 25-28: Latest BSDO Hot-Swappable Battery 2		
Bytes 21-24: Latest BSDO Hot-Swappable Battery 1		
Bytes 17-20: Latest BSDO Hot-Swappable Battery 0		
Bytes 13-16: Latest BSDO Fixed Battery 3		
Bytes 9-12: Latest BSDO Fixed Battery 2		
Bytes 5-8: Latest BSDO Fixed Battery 1		
Bytes 1-4: Latest BSDO Fixed Battery 0		
31:16	BatteryPC	Battery's State of Charge (SOC)
15:8	BatteryInfo	Battery State
7:0	Reserved	Shall be set to zero.

3.59 0x7C Received Battery Capability Data Block (BCDB)

Table 3-120. 0x7C Received Battery Capability Data Block (BCDB) Register

Address	Name	Access	Length	Power-Up Default
0x7C	RX BCDB	Read Only	9	0

Table 3-121. 0x7C Received Battery Capability Data Block (BCDB)

Bits	Name	Description
Byte 9: Battery Type		
Bytes 7-8: Battery Last Full Charge Capacity		
Bytes 5-6: Battery Design Capacity		
Bytes 3-4: PID		
Bytes 1-2: VID		

3.60 0x7D Transmit Battery Capability Data Block (BCDB)

Table 3-122. 0x7D Transmit Battery Capability Data Block (BCDB) Register

Address	Name	Access	Length	Power-Up Default
0x7D	TX BCDB	Read/Write	63	0

Table 3-123. 0x7D Transmit Battery Capability Data Block (BCDB)

Bits	Name	Description
Bytes 54-63: Battery 6 BCDB: Same fields as described in Battery 0.		
Bytes 46-54: Battery 5 BCDB : Same fields as described in Battery 0.		
Bytes 37-45: Battery 4 BCDB : Same fields as described in Battery 0.		
Bytes 28-36: Battery 3 BCDB : Same fields as described in Battery 0.		
Bytes 19-27: Battery 2 BCDB: Same fields as described in Battery 0.		
Bytes 10-18: Battery 1 BCDB : Same fields as described in Battery 0.		
Bytes 1-9: Battery 0 BCDB		
Byte 9: Battery Type		
Bytes 7-8: Battery Last Full Charge Capacity		
Bytes 5-6: Battery Design Capacity		
Bytes 3-4: Battery PID		
Bytes 1-2: Battery VID		

3.61 0x7E Received Manufacturer Info Data Block SOP' (MIDB)

Table 3-124. 0x7E Received Manufacturer Info Data Block SOP' (MIDB) Register

Address	Name	Access	Length	Power-Up Default
0x7E	RX MIDB SOP'	Read Only	4 to 26	0

Table 3-125. 0x7E Received Manufacturer Info Data Block SOP' (MIDB)

Bits	Name	Description
Bytes 5-26:	Manufacturer String	
Bytes 3-4:	PID	
Bytes 1-2:	VID	

3.62 0x7F Transmit Manufacturer Info Data Block SOP' (MIDB)

Table 3-126. 0x7F Transmit Manufacturer Info Data Block SOP' (MIDB) Register

Address	Name	Access	Length	Power-Up Default
0x7F	TX MIDB SOP'	Read Only	4 to 26	0

Table 3-127. 0x7F Transmit Manufacturer Info Data Block (MIDB)

Bits	Name	Description
Bytes 5-26:	Manufacturer String	
Bytes 3-4:	PID	
Bytes 1-2:	VID	

One-PD Controller Command and Task Detailed Descriptions

4.1 Overview

This section describes the One-PD Controller Commands and Tasks defined by the PD Controller Host Interface. Commands are categorized into various sub-groups in this section. All Commands and Tasks that return data using the DataX/ExtDataX registers will always ensure the proper output data is loaded into those registers before setting the CmdX register to 0 to indicate Command/Task completion. DataX/ExtDataX must never be modified by PD Controller once CmdX has been changed to 0, to ensure the Host can retrieve data from the previously-executed Command or Task, and to ensure the Host can load these registers for a future Command or Task without risk of overwriting. Note that other registers may continue to be updated after a Command or Task completes, as commands may have additional side effects.

4.2 Tasks

Tasks are a special form of Commands that return a status code in the first byte of the DataX register. The standard Task response byte is defined in Table 4-1. The remaining DataX bytes may be used at each Task's discretion.

Table 4-1. Standard Task Response

Description	**Tasks are a special form of Commands that return a status code in the first byte of the DataX register.**			
Output DataX	Bit	Name	Description	
	Byte 1: Task Return Code			
	7:4	Reserved	Reserved for standard Tasks. May be used by certain Tasks for Task-specific return codes. Successful return codes may use this byte provided TaskResult is 0x0.	
	3:0	TaskResult	Standard Task return codes.	
			0x0	Task completed successfully.
			0x1	Task timed-out or aborted by 'ABRT' Request.
			0x2	Reserved.
			0x3	Task rejected.
			0x4-0xF	Reserved for standard Tasks. May be used by certain Tasks for Task-specific error codes. Treated as an error when encountered.

4.3 Commands

Many commands also return as their output the Standard Task Response(see Table 4-1) code in the first byte of the DataX register. Each specific command description will inform whether or not the Standard Task Response is used for the command output in the DataX register.

4.4 CPU Control

4.4.1 'Gaid' – Return to normal operation

Table 4-2. 'Gaid' – Return to normal operation

Description	**The 'Gaid' Command causes a warm restart of the PD Controller processor.**
Input DataX	None
Output DataX	None
Command Completion	Technically this command never completes since the processor restarts. However, since all HI registers return to their default state upon reboot, all CmdX/DataX/ExtDataX registers will return to 0, which will mark this command as complete.
The 'Gaid' Command causes a warm restart of the PD Controller processor.	PD Controller may momentarily NAK I2C transactions while rebooting.
Add'l Information	None

4.4.2 'GAID' – Cold reset request

Table 4-3. GAID' – Cold reset request

Description	The 'GAID Command causes a cold restart of the PD Controller processor.
Input DataX	None
Output DataX	None
Command Completion	Technically this command never completes since the processor restarts. However, since all HI registers return to their default state upon reboot, all CmdX/DataX/ExtDataX registers will return to 0, which will mark this command as complete. This command forces the PD Controller to reboot its OTP bootloader.
The 'Gaid' Command causes a warm restart of the PD Controller processor.	PD Controller may momentarily NAK I2C transactions while rebooting.
Add'l Information	None

4.5 Modal Tasks

The following Tasks are considered “Modal” for PD Controller . Only one Modal Task can be active at a time, if the Mode register (0x03) reports any value other than ‘APP ‘ when a Modal Task is issued the Task will be Rejected unless this Modal Task is considered a higher-priority, in which case it may cancel other Modal Tasks. Modal Tasks change the value of the Mode register as described below, and this value remains unless the Task defines its own mechanism for disabling the mode, or if a ‘Gaid’/’GAID’ Command is issued to reboot PD Controller and clear the Mode.

4.5.1 ‘DISC’ – Simulate port disconnect

Table 4-4. ‘DISC’ – Simulate port disconnect

Description	**The ‘DISC’ Modal Task causes the PD Controller to act as if the USB-C port is disconnected, with an optional Host-specified delay to restoring normal port operation. If currently there is no USB-C connection on the port, then this task will be rejected. The port that will be disconnected when writing the 'DISC' command will correspond to whichever I2C address you wrote the 'DISC' command to (port 1 I2C address or port 2 I2C address).**		
Input DataX	**Bit**	**Name**	**Description**
	Byte 1: Reconnect Delay		
	7:0	DISCdelay	8-bit value in seconds for disconnect time. If 0, there is no automatic reconnect.
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The ‘DISC’ Modal Task This command always completes successfully, it has no reason to be rejected or timed-out. If another Modal Task was already active the ‘DISC’ Modal Task will cancel that Modal Task and take its place. The ‘DISC’ Modal Task completes immediately, it does not wait for the re-connect delay		
Side Effects	Effectively the action of this Modal Task is to force the Type-C state machine into the Disabled state, which disables the CC pull-up/downs. Any power switch that was enabled as input or output will be disabled either as a direct result of this Modal Task or an indirect result due to the disconnect event. This causes any existing connection to be lost, and the HI registers will be updated as appropriate for a disconnect event. No new connections will be detected because the port is in the Disabled state. The Type-C state machine does not return to normal operation unless DISCdelay is non-zero and the specified delay passes or a ‘Gaid’/’GAID’ Command is issued to reboot PD Controller .The Mode register (0x03) is changed to ‘DIS#’(# being the port number that is currently being disconnected) while this Modal Task is active to indicate that PD Controller is not in its normal operating state. If DISCdelay is non-zero when the specified delay expires the Mode register will return to ‘APP ‘. If another Modal Task is enabled that cancels this one then the port shall be re-enabled at that time, regardless of DISCdelay and even if the timer had not yet expired. NOTE: If a hot-VBUS Source is attached VBUS may still be present at the input to PD Controller even though it is in the Disabled state. Some VBUS-related registers may report this voltage presence as usual, however PD Controller will keep its power switches disabled until normal operation is restored.		
Add’ l Information	None		

4.6 Special Tasks

4.6.1 'ABRT' – Abort current Task

Table 4-5. 'ABRT' – Abort current Task

Description	**The 'ABRT' Request is not exactly a Task of its own, it is a value that when written to a CmdX register can affect a long-running Command/Task that is currently running on that CmdX interface. Normally a Host is not allowed to write anything to CmdX if it reads back as anything other than 0 or '!CMD', but the 'ABRT' value can always be written to CmdX.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 If PD Controller is busy processing a Command or Task on CmdX when it sees an 'ABRT' Request, it will cause that Command/Task (the assumption is that a Command/Task will only look when it is safe to abort). Tasks will return a TaskResult of 01b (Aborted). If a Command/Task manages complete since the last time it checked CmdX, it will complete normally, updating DataX as it normally would and setting CmdX to 0 (PD Controller will not notice that 'ABRT' had even been written to CmdX, it will simply overwrite that value with 0 upon completion of the Command/Task). If the top-level CmdX processor sees 'ABRT' in a CmdX register (i.e. no Command/Task is being processed, or CmdX was written just after the command completed) then DataX will be left unmodified and CmdX will simply return to 0 so that the results of the just-finished Command/Task will still be accessible (NOTE: Since only Tasks provide a well-defined return code, the results of any Command after writing 'ABRT' cannot be trusted. As such it is preferred that any long-running Command be implemented as a Task instead).		
Command Completion	As the 'ABRT' Request is not actually a task it is difficult to say when it completes. If no Command/Task was active the top-level command processing loop will simply ignore it and clear CmdX. If a Command/Task is running then 'ABRT' will remain in CmdX until the Command/Task completes (either because it completed normally or because it detected the 'ABRT' and aborted).		
Side Effects	Writing 'ABRT' to a CmdX register should have no side effects other than canceling the active Command/Task. The aborted Command/Task should perform any necessary cleanup.		
Add' l Information	None		

4.6.2 'LOCK' – Lock/Unlock Host Interface

Table 4-6. LOCK' – Lock/Unlock Host Interface

Description	**The 'LOCK' Task manages write access to certain One-PD Controller registers and access to certain 4CC Commands/Tasks (designed elsewhere in this spec as locked). One-PD Controller registers can be implemented as read-only, always-writable, or writable-when-unlocked. The latter is the only time the LOCK status needs to be checked during One-PD Controller register write operations. A 4CC may be designated as locked, and a locked 4CC will return '!CMD' in CmdX when the Host Interface is locked, and will function normally then the HI is unlocked.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Host Key (treated as 32-bit little endian value)		
	31:0	HostKey	Copied to internal Key location provided Key==UnlockCode OR Key==0, ignored otherwise.
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'LOCK' Task shall be considered rejected if: • Previous Key value was not 0 or did not match UnlockCode (Key was already locked). • Key was updated but new value is not 0 and does not match UnlockCode (Key is now locked). The 'LOCK' Task shall be considered successful if: • Key was updated and matches UnlockCode or is 0 (requires that previous Key value also either matched UnlockCode or was 0).		
Command Completion	The 'LOCK' Task completes as soon as Key is updated or the Task fails.		
Side Effects	The only side effect to the 'LOCK' Task is the locking/unlocking of certain One-PD Controller registers and 4CCs.		
Add' l Information	The implementation of the locking concept is meant to be very simple. The "UnlockCode" is a 32-bit value that is never changed after Application Customization (default value if not customized is 0x00000000). PD Controller will keep track of the UnlockCode as well as the last "Key" value entered by the Host, this value also defaults to 0x00000000. When these two values match (UnlockCode == Key) the Host Interface is considered unlocked. When the values do not match (UnlockCode != Key) the Host Interface is considered locked. As a result of the power-up defaults, if Application Customization does not change the UnlockCode then the Host Interface starts out unlocked, if Application Customization changes the UnlockCode to a non-zero value then the Host Interface starts out locked. The 'LOCK' Task is used to change the Key, note that once written to an incorrect (and non-zero) value the Key itself becomes locked and can no longer be changed via the 'LOCK' Task (PD Controller must be rebooted to reset the Key to 0). Note that if UnlockCode is 0 and any non-zero value is written using the 'LOCK' Task, the Host Interface becomes locked and the Key cannot be changed as it is now locked.		

4.7 PD Message Tasks

4.7.1 'SWSk' – PD PR_Swap to Sink

Table 4-7. 'SWSk' – PD PR_Swap to Sink

Description	**The 'SWSk' Task instructs PD Controller to attempt to become a Sink via PR_Swap at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'SWSk' Task shall be considered rejected if: • The Source indicated via Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSk' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSk' Task shall be considered successful if: • PD Controller is already in the Sink power role. • The PR_Swap is Accepted and completes normally.		
Command Completion	The 'SWSk' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the Source.		
Side Effects	When the 'SWSk' Task completes successfully PD Controller will have transitioned to the Sink power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Add' l Information	None		

4.7.2 'SWSr' – PD PR_Swap to Source

Table 4-8. 'SWSr' – PD PR_Swap to Source

Description	**The 'SWSr' Task instructs PD Controller to attempt to become a Source via PR_Swap at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'SWSr' Task shall be considered rejected if: • The Sink previously indicated via Sink or Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSr' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSr' Task shall be considered successful if: • PD Controller is already in the Source power role. • The PR_Swap is Accepted and completes normally.		
Command Completion	The 'SWSr' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the Sink.		
Side Effects	When the 'SWSr' Task completes successfully PD Controller will have transitioned to the Source power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Add' l Information	None		

4.7.3 'SWDF' – PD DR_Swap to DFP

Table 4-9. 'SWDF' – PD DR_Swap to DFP

Description	**The 'SWDF' Task instructs PD Controller to attempt to become a DFP via DR_Swap at the first opportunity while maintaining policy engine compliance. If there are any active Alternate Modes as a UFP PD Controller will attempt to exit those Modes first before sending the DR_Swap.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'SWDF' Task shall be considered rejected if: • The UFP indicated via Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWDF' Task shall be considered successful if: • PD Controller is already in the DFP data role. • The DR_Swap is Accepted and completes normally.		
Command Completion	The 'SWDF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the DFP.		
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the DFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Add' l Information	None		

4.7.4 'SWUF' – PD DR_Swap to UFP

Table 4-10. 'SWUF' – PD DR_Swap to UFP

Description	**The 'SWUF' Task instructs PD Controller to attempt to become a UFP via DR_Swap at the first opportunity while maintaining policy engine compliance. If there are any active Alternate Modes as a DFP PD Controller will exit those Modes first before attempting the DR_Swap.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'SWUF' Task shall be considered rejected if: • The DFP indicated via Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWUF' Task shall be considered successful if: • PD Controller is already in the UFP data role. • The DR_Swap is Accepted and completes normally.		
Command Completion	The 'SWUF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task may continue to run because of Wait messages being sent by the UFP.		
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the UFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Add' l Information	None		

4.7.5 'SWVC' – PD VCONN_Swap

Table 4-11. 'SWVC' – PD VCONN_Swap

Description	**The 'SWVC' Task instructs PD Controller to attempt a VCONN_Swap at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'SWVC' Task shall be considered rejected if: • The VCONN_Swap is Rejected. The 'SWVC' Task shall be considered timed-out if: • The VCONN _Swap is Accepted but failed to complete per the PD spec. The 'SWVC' Task shall be considered successful if: • The VCONN_Swap is Accepted and completes normally.		
Command Completion	The 'SWVC' Task completes either when the VCONN_Swap is finished or it otherwise fails. The Task may continue to run because of Wait messages being sent by the port partner.		
Side Effects	When the 'SWVC' Task completes successfully PD Controller will have swapped VCONN provider responsibilities, which impacts other registers. If the VCONN_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.		
Add' l Information	None		

4.7.6 'GSkC' – PD Get Sink Capabilities

Table 4-12. GSkC' – PD Get Sink Capabilities

Description	**The 'GSkC' Task instructs PD Controller to issue a Get_Sink_Cap message to the far-end device at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 • The far-end device is a Source and indicated it was not Dual-Role Power. • The far-end device Rejects the Get_Sink_Cap message. The 'GSkC' Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD spec. The 'GSkC' Task shall be considered successful if: • The Get_Sink_Cap message is sent, GoodCRC'ed and a Sink Capabilities response is received and processed.		
Command Completion	The 'GSkC' Task completes either when the Sink Capabilities message is received or the Task otherwise fails.		
Side Effects	When the 'GSkC' Task completes successfully the *RX Sink Capabilities* register (0x31) will have been updated.		
Add' l Information	None		

4.7.7 'GSrC' – PD Get Source Capabilities

Table 4-13. 'GSrC' – PD Get Source Capabilities

Description	**The 'GSrC' Task instructs PD Controller to issue a Get_Source_Cap message to the far-end device at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'GSrC' Task shall be considered rejected if: • The far-end device is a Sink and indicated (via previous Source or Sink Capabilities) it was not Dual-Role Power or Rejects the Get_Source_Cap message. The 'GSrC' Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD spec. The 'GSrC' Task shall be considered successful if: • The Get_Source_Cap message is sent, GoodCRC'ed and a Source Capabilities response is received and processed.		
Command Completion	The 'GSrC' Task completes either when the Source Capabilities message is received or the Task otherwise fails.		
Side Effects	When the 'GSrC' Task completes successfully the *RX Source Capabilities* register (0x30) will have been updated.		
Add' l Information	None		

4.7.8 'SSrC' – PD Send Source Capabilities

Table 4-14. 'SSrC' – PD Send Source Capabilities

Description	**The 'SSrC' Task instructs PD Controller to send a Source Capabilities message at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'SSrC' Task shall be considered rejected if: • PD Controller is not in a Source role. The 'SSrC' Task shall be considered timed-out if: • The Source Capabilities message was sent but no GoodCRC was received. The 'SSrC' Task shall be considered successful if: • The Source Capabilities message was sent and a GoodCRC is received.		
Command Completion	The 'SSrC' Task completes either when the Sink Capabilities message GoodCRC is received or the Task otherwise fails.		
Side Effects	Unique Address Interface Registers may change as a result of the contract negotiation that begins with the new Source Capabilities message.		
Add' l Information	None		

4.7.9 'HRST' – PD issue Hard Reset

Table 4-15. 'HRST' – PD issue Hard Reset

Description			
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'HRST' Task shall be considered timed-out if: • PD Controller is unable to produce Hard Reset Signaling before tHardResetComplete expires. The 'HRST' Task shall be considered successful if: • The Hard Reset Signaling is produced.		
Command Completion	The 'HRST' Task completes either when the Hard Reset Signaling is produced or the timer expires.		
Side Effects	A PD Hard Reset has many side effects to both power and data operation, too numerous to list here.		
Add' l Information	None		

4.7.10 'CRST' – PD issue Cable Reset

Table 4-16. 'CRST' – PD issue Cable Reset

Description	**The 'CRST' Task instructs PD Controller to issue Cable Reset Signaling at the first opportunity while maintaining policy engine compliance. If PD Controller is the DFP but is not currently providing VCONN power then this Task will also attempt to power VCONN (see the 'VCOn' Task).**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'CRST' Task shall be considered rejected if: • PD policy does not allow Cable Reset Signaling to be sent (e.g. PD Controller is a UFP/Sink). • PD Controller is DFP but is unable to provide VCONN (equivalent to the 'VCOn' Task reject conditions). The 'CRST' Task shall be considered successful if: • The Cable Reset Signaling is produced.		
Command Completion	The 'CRST' Task completes either when the Cable Reset Signaling is produced or the Task otherwise fails.		
Side Effects	A PD Cable Reset has many side effects to both power and data operation, too numerous to list here.		
Add' l Information	None		

4.7.11 'VDMs' – PD send VDM

Table 4-17. 'VDMs' – PD send VDM

Description	**The 'VDMs' Task instructs PD Controller to send a Vendor Defined Message (VDM) at the first opportunity while maintaining policy engine compliance.**				
Input DataX	**Bit**	**Name**	**Description**		
	Bytes 26-29: VDO #7 (treated as 32-bit little endian value)				
	31:0	VDO7	Contents of seventh VDO, if applicable.		
	Bytes 22-25: VDO #6 (treated as 32-bit little endian value)				
	31:0	VDO6	Contents of sixth VDO, if applicable.		
	Bytes 18-21: VDO #5 (treated as 32-bit little endian value)				
	31:0	VDO5	Contents of fifth VDO, if applicable.		
	Bytes 14-17: VDO #4 (treated as 32-bit little endian value)				
	31:0	VDO4	Contents of fourth VDO, if applicable.		
	Bytes 10-13: VDO #3 (treated as 32-bit little endian value)				
	31:0	VDO3	Contents of third VDO, if applicable.		
	Bytes 6-9: VDO #2 (treated as 32-bit little endian value)				
	31:0	VDO2	Contents of second VDO, if applicable.		
	Bytes 2-5: VDO #1 (treated as 32-bit little endian value)				
	31:0	VDO1	Contents of first VDO (VDM Header if SVDM).		
	Byte 1: VDMs Task Header				
	7:6	Reserved	Reserved (write 0).		
	5:4	SOPTarget	Ordered Set to send VDM to.		
			00b	SOP.	
			01b	SOP'.	
			10b	SOP''.	
			11b	SOP*_Debug (SOP'_Debug for Source, SOP''_Debug for Sink).	
	3	Reserved	Reserved (write 0).		
	2:0	NumDOs	Number of VDOs to transmit (1-7), includes VDM Header for SVDMs.		
	Bit	**Name**	**Description**		
	Byte 1: Standard Task Return Code				
Output DataX	Table 4-1 The 'VDMs' Task shall be considered rejected if: • NumDOs is set to 0. • PD policy does not allow a VDM to be sent at this time. • DFP/UFP is instructed to send to SOP' when not appropriate (e.g. DFP during Implicit Contract following a PR_Swap) or a UFP is instructed to send to SOP''. The 'VDMs' Task shall be considered timed-out if: • The VDM was sent but no GoodCRC was received. The 'VDMs' Task shall be considered successful if: • The VDM was sent and a GoodCRC was received.				
Command Completion	The 'VDMs' Task completes when the VDMs is delivered and a GoodCRC is received or the appropriate number of retries have been attempted without a GoodCRC, or the Task is rejected. This Task does not wait for a VDM response since there is no guarantee of a response especially for Unstructured VDMs.				
Side Effects	If the 'VDMs' Task succeeds in sending the requested VDM, PD Controller is not aware of the VDM it sent, so it will not be expecting a response. All incoming VDMs that are not Initiator Attention messages will be stored in the *RX VDM* register (0x4F) regardless of PD Controller 's current state so the response can be processed by the Host, but it will not otherwise be processed by PD Controller . For example, if VDMs is used to send a Discover Identity SVDM Command to SOP', the *RX Identity SOP'* register does not get updated since PD Controller 's PD state machine was not in the proper state to receive this response.				
Add' l Information	None				

4.8 Alternate Mode Tasks

4.8.1 'AMEn' – PD send Enter Mode

Table 4-18. 'AMEn' – PD send Enter Mode

Description	**The PD controller will automatically send the Enter Mode command for appropriate Alternate Modes discovered based in its configuration settings. For the normal PD state machine process of entering Alternate Modes, the Host does not need to interact. However, if the Host ever needs to manually exit an Alternate Mode, and then at a later time wants to re-enter an Alternate Mode, then this 4CC command must be used. If the Alternate Mode trying to be re-entered requires any cable negotiation (SOP', SOP'') in addition to negotiation with the the other USB-C port (SOP), then the 'AMEn' command will automatically negotiate the Alternate Mode with all the required SOP* targets.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 2-3: AMEn SVID (treated as 16-bit little endian value)		
	15:0	SVIDTarget	SVID to use for Enter Mode SVDM Command.
	Byte 1: AMEn Task Header		
	7:5	ObjPos	Object Position of Mode to enter. If 000b PD Controller will enter the Mode as it would have in the initial PD negotiation process. 111b is Reserved and the 'AMEn' Task will be rejected if used. Any other value will cause the PD Controller to send an Enter Mode SVDM Command.
	4:0	Reserved	Reserved (write 0).
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'AMEn' Task shall be considered rejected if: • PD Controller is not in a DFP data role (includes no present Type-C connection). • SVIDTarget is not supported by PD Controller. • The Mode selected by ObjPos is not a valid mode or not a mode supported by the PD controller. • The Enter Mode SVDM Command was sent and GoodCRC'ed and a NAK Response was received. • The requested Alternate Mode has already been entered. The 'AMEn' Task shall be considered timed-out if: • The Enter Mode SVDM Command was sent but no GoodCRC was received, or a GoodCRC was received and no SVDM Response was received in the required time. The 'AMEn' Task shall be considered successful if:The Enter Mode SVDM Command was sent and GoodCRC'ed and an ACK Response was received.		
Command Completion	The 'AMEn' Task completes when the Enter Mode SVDM Command is delivered and a GoodCRC is received and an ACK Response is received, or the Task is otherwise rejected or times-out. If PD policy does not currently allow an SVDM to be sent (for example no Explicit Contract has been achieved) this Task will wait until PD policy allows the SVDM to be sent. The PD spec currently does not allow a BUSY response to an Enter Mode SVDM Command, however if PD Controller receives a BUSY Response the 'AMEn' Task will remain active and continue to retry the Enter Mode SVDM Command.		
Side Effects	Assuming the 'AMEn' Task succeeds in sending the Enter Mode SVDM Command and receives a SVDM Response, PD Controller will update the *Status* register (0x1A) to indicate that a Mode is active. For SVIDs and Modes that PD Controller supports it will also update the appropriate VID/SID Status and *Data Status* registers (for example the DPModeActive field in *DP SID Status* when a SVDM ACK is received to the DP SID Enter Mode Command for the DisplayPort Object Position). As each SVDM Response is received it will be stored in the *RX VDM* register (0x4F) as usual, allowing the Host to perform any additional processing of the SVDM Response. Note that if ObjPos is set to a valid Mode, Enter Mode SVDM Commands may be sent to multiple SOP* Ordered Sets, meaning multiple Enter Mode SVDM Responses may be received, only the final response (most likely SOP since cable mode entry is generally done first) will remain in the *RX VDM* register.		
Add' l Information	None		

4.8.2 'AMEx' – PD send Exit Mode

Table 4-19. 'AMEx' – PD send Exit Mode

Description	**The PD Controller will automatically discover and enter into Alternate Modes according to its configuration settings. It will also exit Alternate Modes on its own whenever needed to maintain PD compliance. However, if in an Alternate Mode the Host ever needs the PD controller to exit the Alternate Mode manually, the AMEx command should be used. Once an Alternate Mode has been exited, if the Alternate Mode needs to be re-entered, then the Host will need to manually re-enter the Alternate Mode using the AMEn command; once a manual exit is done with the AMEx command, to re-enter the Alternate Mode, a manual AMEn enter is required. When using the 'AMEx" command to exit an Alternate Mode, all SOP* targets that require an Exit Mode SVDM message to properly exit the Alternate Mode will be sent an Exit Mode SVDM message.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 2-3: AMEx SVID (treated as 16-bit little endian value)		
	15:0	SVIDTarget	SVID to use for Exit Mode SVDM Command.
	Byte 1: AMEx Task Header		
	7:5	ObjPos	Object Position of Mode to exit. If 111b PD Controller will use 111b in its Exit Mode SVDM Command to exit all Modes associated with the SVID. 000b is Reserved and the 'AMEx' Task will be rejected if used.
	4:0	Reserved	Reserved (write 0).
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'AMEx' Task shall be considered rejected if: • PD Controller is not in a DFP data role (includes no present Type-C connection). • The Exit Mode SVDM Command was sent and GoodCRC'ed and a NAK Response was received. • The device is not currently in the Alternate Mode trying to be exited. • The SVIDTarget is not supported by the PD controller. • The Mode corresponding to the ObjPos is not valid. The 'AMEx' Task shall be considered timed-out if: • The Exit Mode SVDM Command was sent but no GoodCRC was received, or a GoodCRC was received and no SVDM Response was received in the required time. The 'AMEx' Task shall be considered successful if: • The Exit Mode SVDM Command was sent and GoodCRC'ed and an ACK Response was received.		
Command Completion	The 'AMEx' Task completes when the Exit Mode SVDM Command(s) are delivered and a GoodCRC is received and an ACK Response is received, or the Task is otherwise rejected or times-out. There should be no reason for PD policy to prevent the SVDM to be sent or else a Mode should not have been able to be entered in the first place. The PD spec currently does not allow a BUSY response to an Exit Mode SVDM Command, however if PD Controller receives a BUSY Response the 'AMEx' Task will remain active and continue to retry the Exit Mode SVDM Command.		
Side Effects	Assuming the 'AMEx' Task succeeds in sending the Exit Mode SVDM Command(s) and receives a SVDM Response PD Controller will take the appropriate action for exiting the Mode. The PD Controller will also update the appropriate VID/SID Status and *Data Status* registers (for example the DPModeActive field in *DP SID Status* when a SVDM ACK is received to the DP SID Exit Mode Command for the DisplayPort Object Position). As each SVDM Response is received it will be stored in the *RX VDM* register (0x4F) as usual, allowing the Host to perform any additional processing of the SVDM Response. Note that because the PD controller will send Exit Modes messages on all SOP targets as appropriate, the SOP' and SOP'' Exit Mode SVDM Responses may be overwritten by additional Exit Mode SVDM Responses, since the last Exit Mode is sent to SOP, its SVDM Response will be the final value in the *RX VDM* register.		
Add' l Information	None		

4.8.3 'AMDs' – PD Start Alternate Mode Discovery

Table 4-20. 'AMDs' – PD Start Alternate Mode Discovery

Description	**The 'AMDs' Task instructs PD Controller to start the Alternate Mode Discovery process**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'AMDs' Task shall be considered rejected if: • Not a DFP for PD2.0 Operation. • The Discover Identity message was sent and GoodCRC'ed and a NAK response was received. • The Discover SVIDs message was sent and GoodCRC'ed and a NAK response was received. The 'AMDs' Task shall be considered successful if: • Both the Discover Identity and the Discover SVIDs messages were sent and GoodCRC'ed, and ACK Responses were returned for both of them.		
Command Completion	This task will complete after the PD controller has sent the Discover Identity, Discover SVIDs, and Discover Modes messages that take place during that Alternate Mode Discovery process, or when the task is otherwise rejected.		
Side Effects	As a part of the Alternate Mode Discovery process, the Discovered SVIDS register (0x21), RX Identity SOP register (0x48), RX Identity SOP' register (0x49), User VID Status register (0x57), DP SID Status register (0x58), and Intel VID Status register (0x59) could be updated. Which registers get up dated will depend on how many of the Alternate Mode Discovery process PD message successfully get responses, which also influences whether or not the command returns it completed successfully or not in the Output DataX register.		
Add' l Information	None		

4.9 'GCdm' – Get Custom Discovered Modes

Table 4-21. 'GCdm' – Get Custom Discovered Modes

Description	**After a successful 'GCdm' command, PD Controller returns a list of VDOs along with their respective object position.**		
Input DataX	**Bit**	**Name**	**Description**
	Byte 1	Reserved (Write 0)	
	Bytes 2-3	SVID	SVID of Alternate Mode
Output DataX	**Bit**	**Name**	**Description**
	Bytes 1-4	VDOMode1	VDO for Mode 1
	Byte 5	VDOMode1Pos	Object Position for Mode 1
	Bytes 6-9	VDOMode2	VDO for Mode 2
	Byte 10	VDOMode2Pos	Object Position for Mode 2
	Bytes 11-14	VDOMode3	VDO for Mode 3
	Byte 15	VDOMode3Pos	Object Position for Mode 3
	Bytes 16-19	VDOMode4	VDO for Mode 4
	Byte 20	VDOMode4Pos	Object Position for Mode 4
	Bytes 21-24	VDOMode5	VDO for Mode 5
	Byte 25	VDOMode5Pos	Object Position for Mode 5
	Bytes 26-29	VDOMode6	VDO for Mode 6
	Byte 30	VDOMode6Pos	Object Position for Mode 6
	Bytes 31-34	VDOMode7	VDO for Mode 7
	Byte 35	VDOMode7Pos	Object Position for Mode 7
Command Completion	The 'GCdm' Task completes when Output is updated with VDO modes and positions.		
Side Effects	None		
Add' l Information	None		

4.10 Power Switch Tasks

4.10.1 'SRDY' – System ready to sink power

Table 4-22. 'SRDY' – System ready to sink power

Description	**The 'SRDY' Task instructs PD Controller to enable a power switch configured as a Sink so it can start allowing the system to sink power.**				
Input DataX	**Bit**	**Name**	**Description**		
	Byte 1: SRDY Input				
	7:3	Reserved	Reserved (write 0).		
	2:0	SwitchSelect	Specifies which switch will be enabled. Switches must be configured as Sink (input) switches that wait for SYS_RDY command (SRDY).		
			000b	PP1	
			001b	PP2	
			010b	PP3	
			011b	PP4	
			100b - 111b	Reserved (Write 0).	
		Name	**Description**		
Output DataX	Byte 1: Standard Task Return Code Table 4-1 The 'SRDY' Task shall be considered rejected if: • PD Controller is not in a Sink role. • SwitchSelect == 000b through 011b and the specified switch is not configured for input. • The selected switch cannot be enabled for some reason (UVP/OVP or some other fault). The 'SRDY' Task shall be considered successful if: • PD Controller is able to determine the switch to enable, it is configured as an input and it is enabled successfully.				
Command Completion	The 'SRDY' Task completes when the selected input switch is successfully enabled or the Task otherwise fails.				
Side Effects	When 'SRDY' completes power switches may have been re-configured, which will affect the Status register.				
Add' l Information	None				

4.10.2 'SRYR' – SRDY reset

Table 4-23. 'SRYR' – SRDY reset

Description	**The 'SRYR' Task instructs PD Controller to disable the currently-enabled input switch, if there is one.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The 'SRYR' Task completes as soon as all input switches are disabled. This command will be rejected if the port is not in the USB-C Sink state.		
Side Effects	When 'SRYR' completes an active input switch will be disabled, which will affect the Status register. PD Controller will remember the switch that was just disabled, if the 'SRDY' Task is issued with SwitchSelect == 01b the previously-enabled switch will be enabled once again.		
Add' l Information	None		

4.11 Patch Bundle Update Tasks

The following tasks are used for updating a Patch Bundle.

4.11.1 'PTCs' – Start Patch Download Sequence

Table 4-24. 'PTCs' – Start Patch Load Sequence

Description	**The 'PTCs' Task starts the patch loading sequence. This command initializes the firmware in preparation for a patch bundle load sequence and indicates what the patch bundle will contain.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: Patch Bundle Content Selection			
	7:2	Reserved	Reserved (write 0).	
	1	DevicePatch	If set to 1, the device patch will be included in the patch bundle. If set to 0, the device patch will not be included in the patch bundle.	
	0	AppConfig	If set to 1, application configuration data will be included in the patch bundle. If set to 0, application configuration data will not be included in the patch bundle.	
Output DataX	**Bit**	**Name**	**Description**	
	Byte 4	AppConfigStartStatus	0x00	Application Configuration Patch start success
			0x20	Application Configuration Patch already loaded
			0x40	Application Configuration Patch process already started
	Byte 3	DevicePatchStartStatus	0x00	Device Patch start success
			0x20	Device Patch already loaded
			0x40	Device Patch process already started
	Byte 2	PatchStartStatus	0x00	Patch start success
			0x40	Patch start warning, see Byte 3 - DevicePatchStartStatus and Byte 4 - AppConfigStartStatus
			0x80	Patch start failure
	Byte 1	Reserved		
Command Completion	The 'PTCs' Task completes once output has a valid PatchStartStatus.			
Side Effects	None			
Add' l Information	None			

4.11.2 'PTCd' – Patch Download

Table 4-25. 'PTCd' – Patch Download

Description	**After a successful "PTCs" command, patch binary data can be transferred 64 bytes at a time using this task command.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 1-64	PatchData	Binary data for patch at 64 bytes at a time. Last data can be less than 64 bytes.	
Output DataX	**Bit**	**Name**	**Description**	
	Byte 9-10	ApplicationConfigurationDataTransferred	Size of Application Configuration sent	
	Byte 7-8	DevicePatchDataTransferred	Size of Device Patch sent	
	Byte 5-6	TotalDataTransferred	Size of total patch sent, including Application Configuration and the Device Patch	
	Byte 4	Reserved		
	Byte 3	PatchLoadingState	0x00	Not Started
			0x01	Application Configuration Header Phase 1
			0x02	Application Configuration Header Phase 2
			0x03	Waiting for Application Configuration Data
			0x04	Application Configuration Data Loading
			0x05	Waiting for Device Patch Data
			0x06	Device Patch Header Loading
			0x07	Device Patch Data Loading
			0x08	Device Patch Loading Done
			0x09	Error
			0x0A	Patching Processes Completed Successfully
	Byte 2	TransferStatus	0x00	Successful download
			0x40	Patch length exceeded
			0x80	Not expecting patch.
	Byte 1	Reserved		
Command Completion	The 'PTCd' Task completes once output has a valid TransferStatus.			
Side Effects	None			
Add' l Information	Before sending the next set of patch bytes, poll on command register for 0. Check the Output DataX Byte 1 TransferStatus.			

4.11.3 'PTCc' – Patch Download Complete

Table 4-26. 'PTCc' – Patch Data Transfer Complete

Description	**The 'PTCc' Task ends the patch loading sequence. Send this command after all patch data has been transferred via the PTCd command. This command will initiate the checksum check on the binary patch data that has been transferred, and if the checksum is successful, the patch_init function contained within the patch will be executed. If this command is sent prior to a 'PTCs' start command, it indicates to the PD Controller that no patch is available and bypass the patch process.**			
Input DataX	**Bit**	**Name**	**Description**	
	None			
Output DataX	**Bit**	**Name**	**Description**	
	Byte 4	AppConfigPatchCompleteStatus	0x00	Success
			0x40	Warning
			0x80	Failure
	Byte 3	DevicePatchCompleteStatus	0x00	Success
			0x20	Not ready
			0x40	Not a patch
			0x41	Patch header checksum mismatch
			0x42	Patch not compatible with this version of ROM
			0x43	Patch code checksum mismatch
			0x44	Null patch received
			0x45	Error patch received
	Byte 2	Reserved		
	Byte 1	Reserved		
Command Completion	The 'PTCc' Task completes as output has a valid DevicePatchCompleteStatus and AppConfigPatchCompleteStatus.			
Side Effects	None			
Add' l Information	When command register goes to 0 check the Output DataX register for status.			

4.11.4 'PTCq' – Patch Query

Table 4-27. 'PTCq' – Patch Query

Description	**The 'PTCq' Task can be used to query the status of the patch process.**			
Input DataX	**Bit**	**Name**	**Description**	
	None			
Output DataX	**Bit**	**Name**	**Description**	
	Byte 14	ApplicationConfigurationPatchSource	0x00	None
			0x01	Application Configuration Patch Loaded from SRAM
			0x02	Application Configuration Patch Loaded from Flash
			0x03	Application Configuration Patch Loaded from I2C
			0x04	Application Configuration Patch Loaded from Default Configuration
	Byte 13	ApplicationConfigurationPatchState	0x00	No Application Configuration Patch
			0x01	Application Configuration Patch Loading from SRAM
			0x02	Application Configuration Patch Loading from Flash
			0x03	Application Configuration Patch Loading from I2C
			0x04	Application Configuration Patch Loading from Default Configuration
			0x05	Application Configuration Patch Loading Done
			0x06	Application Configuration Patch Loading First
			0x07	Application Configuration Patch Loading Last
			0x08	Application Configuration Patch Error
			0x09	Application Configuration Patch Completed Successfully
			0x0A	Application Configuration Patch Loading Failed
	Byte 12	DevicePatchSource	0x00	None
			0x01	Device Patch Loaded from SRAM
			0x02	Device Patch Loaded from Flash
			0x03	Device Patch Loaded from I2C
			0x04	Default
	Byte 11	DevicePatchState	0x00	No Device Patch
			0x01	Device Patch Loading
			0x02	Device Patch Loading Done
			0x03	Device Patch Running
			0x04	Reserved
			0x05	Reserved
			0x06	Device Patch Error

Table 4-27. 'PTCq' – Patch Query (continued)

Description	The 'PTCq' Task can be used to query the status of the patch process.			
Output DataX	Byte 9-10	ApplicationConfigurationDataTransferred	Size of Application Configuration sent	
	Byte 7-8	DevicePatchDataTransferred	Size of Device Patch sent	
	Byte 5-6	TotalDataTransferred	Size of total patch sent, including Application Configuration and the Device Patch	
	Byte 4	Reserved		
	Byte 3	PatchLoadingState	0x00	Not Started
			0x01	Application Configuration Header Phase 1
			0x02	Application Configuration Header Phase 2
			0x03	Waiting for Application Configuration Data
			0x04	Application Configuration Data Loading
			0x05	Waiting for Device Patch Data
			0x06	Device Patch Header Loading
			0x07	Device Patch Data Loading
			0x08	Device Patch Loading Done
			0x09	Error
			0x0A	Patching Processes Completed Successfully
	Byte 2	PatchReturnCode	0x00	Success
			0x40	Warning
			0x80	Failure
	Byte 1			
	7	noDevicePatch	If set to 1, there is currently noDevicePatch	
	6:4	Reserved	Reserved	
	3	noApplicationConfigPatch	If set to 1, there is currently noApplicationConfigPatch	
	2:0	Reserved	Reserved	
Command Completion	The 'PTCq' Task completes as output has valid information loaded.			
Side Effects	None			
Add' l Information	None			

4.11.5 'PTCr' – Patch Reset

Table 4-28. 'PTCr' – Patch Reset

Description	**The 'PTCq' Task command will reset the patch firmware to the no patch state.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 4: Application Configuration Reset Key			
	7:0	AppConfigResetKey	0xEFh	Required to reset the Application Configuration currently running. If no Application Configuration is running, the AppConfigResetKey is not required, and 0x00 should be written to AppConfigResetKey.
	Byte 3: Device Patch Reset Key			
	7:0	DevicePatchResetKey	0xBEh	Required to reset a Device Patch that is currently running. If no Device Patch is running, the DevicePatchResetKey is not required, and no specific value is required to be written.
	Byte 2: Reserved (Write 0)			
	Byte 1: Reset Control			
	7:2	Reserved (Write 0)		
	1	DevicePatchReset	0b	The Device Patch will not be reset.
			1b	The Device Patch will be reset if the Device Patch Reset Key input into DataX before running the 'PTCr' command matches the secret key in the memory of the device.
	0	AppConfigReset	0b	Application Configuration will not be reset.
			1b	Application Configuration will be reset if the AppConfig Reset Key input into DataX before running the 'PTCr' command matches the secret key in the memory of the device.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1:			
	7:4	DevicePatchReturn	0x00	Device Patch reset successful
			0x04	A Device Patch is currently running, and the Device Patch reset key did not match, so the Device Patch did not get reset
	3:0	AppConfigReturn	0x00	Application Configuration reset successful
			0x04	Application Configuration reset key did not match, Application Configuration did not get reset
Command Completion	The 'PTCr' Task completes as output has a valid AppConfigReturn and DevicePatchReturn.			
Side Effects	None			
Add' l Information	None			

4.11.6 'FLrr' – Flash Load Read Regions

Table 4-29. 'FLrr' – Set Flash Read Region

Description	**The 'FLrr' Command loads the address of the flash memory for the selected region into Output DataX.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: Region Number			
	7:1	Reserved	Reserved.	
	0	RegionNum	Region Number	
			0b	Region 0
			1b	Region 1
Output DataX	**Bytes**	**Name**	**Description**	
	1-4	ReadRegionAddr	Read Region Address (treated as 32-bit little-endian value).	
Command Completion	The 'FLrr' Command completes once the address is loaded.			
Side Effects	None			
Add' l Information	None			

4.11.7 'FLer' – Flash Erase Region Pointer

Table 4-30. 'FLer' –Flash Erase Region Pointer

Description	**The 'FLer' Command erases the selected region pointer.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: Region Number			
	7:1	Reserved	Reserved.	
	0	RegionNum	Region Number	
			0b	Region 0
			1b	Region 1
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Return Code			
	7:0	ReturnCode	0x00h	Region pointer erase successful
			0xFFh	Error, flash is busy
			0xFEh	Error, invalid pointer address, cannot erase
Command Completion	The 'FLer' Command completes once selected pointer is erased.			
Side Effects	None			
Add' l Information	None			

4.11.8 'FLrd' – Flash Memory Read

Table 4-31. 'FLrd' – Flash Memory Read

Description	**The 'FLrd' Command reads the flash at the specified address.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Flash address (treated as 32-bit little-endian value).		
Output DataX	**Bytes**	**Name**	**Description**
	Bytes 1-16: Memory contents (little-endian).		
Command Completion	The 'FLrd' Command completes once selected memory locations are loaded.		
Side Effects	None		
Add' l Information	None		

4.11.9 'FLad' – Flash Memory Write Start Address

Table 4-32. 'FLad' – Flash Memory Write Start Address

Description	**The 'FLad' Command sets start address in preparation the flash write.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 1-4: Flash address (treated as 32-bit little-endian value).		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1		
Command Completion	The 'FLad' Command completes once selected memory address is loaded.		
Side Effects	None		
Add' l Information	None		

4.11.10 'FLwd' – Flash Memory Write

Table 4-33. 'FLwd' – Flash Memory Write

Description	**The 'FLwd' Command writes data beginning at the flash start address defined by the 'FLad' Command. The address is auto-incremented.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 1-64: Up to 64 bytes of flash data			
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Return Code			
	7:0	ReturnCode	0x00h	Flash memory write successful
			0xFFh	Error, flash is busy
Command Completion	The 'FLwd' Command completes once selected the flash is written.			
Side Effects	None			
Add' l Information	None			

4.11.11 'FLem' – Flash Memory Erase

Table 4-34. 'FLem' – Flash Memory Erase

Description	**The 'FLem' Command erases the number of segments specified.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 1-4: Flash address (treated as 32-bit little-endian value) of first sector.			
	Byte 5: Number of 4KB sectors to erase.			
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Return Code			
	7:0	ReturnCode	0x00h	Region pointer erase successful
			0xFFh	Error, flash is busy
			0xFEh	Error, invalid pointer address, cannot erase
Command Completion	The 'FLem' Command completes once selected memory address is loaded.			
Side Effects	None			
Add' l Information	None			

4.11.12 'FLvy' – Flash Memory Verify

Table 4-35. 'FLvy' – Flash Memory Verify

Description	**The 'FLvy' Command verifies if the patch/configuration is valid.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 1-4: Flash address (treated as 32-bit little-endian value) of header location.			
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Return Code			
	7:0	ReturnCode	0x00h	The patch/configuration is valid.
			0x01h	The patch/configuration is not valid.
Command Completion	The 'FLvy' Command completes once header is checked and validated.			
Side Effects	None			
Add' l Information	None			

4.12 I/O Commands

4.12.1 'GPoe' – GPIO Output Enable

Table 4-36. 'GPoe' – GPIO Output Enable

Description	**The 'GPoe' Command enables the specified output.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 15h	GPIO0 through GPIO21.
			16h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code Table 4-1			
Command Completion	The 'GPoe' Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller 's GPIOs manually. GPIOs that are connected to PD Controller Events may not behave properly if they are modified by the 'GPIO' Command. Extreme care must be taken with the use of this Command.			
Add' l Information	None			

4.12.2 'GPie' – GPIO Input Enable

Table 4-37. 'GPie' – GPIO Input Enable

Description	**The 'GPie' Command enables the specified input**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 15h	GPIO0 through GPIO21.
			16h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code Table 4-1			
Command Completion	The 'GPie' Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller 's GPIOs manually. GPIOs that are connected to PD Controller Events may not behave properly if they are modified by the 'GPIO' Command. Extreme care must be taken with the use of this Command.			
Add' l Information	None			

4.12.3 'GPsh' – GPIO Set Output High

Table 4-38. GPsh' – GPIO Set Output High

Description	**The 'GPsh' Command sets the specified output logic high**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 15h	GPIO0 through GPIO21.
			16h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code Table 4-1			
Command Completion	The 'GPsh' Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller 's GPIOs manually. GPIOs that are connected to PD Controller Events may not behave properly if they are modified by the 'GPIO' Command. Extreme care must be taken with the use of this Command.			
Add' l Information	None			

4.12.4 'GPsl' – GPIO Set Output Low

Table 4-39. GPsl' – GPIO Set Output Low

Description	**The 'GPsl' Command sets the specified output logic low**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: GPIO number			
	7:0	GPIOnum	GPIO number	
			00h - 15h	GPIO0 through GPIO21.
			16h - FFh	Reserved.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code Table 4-1			
Command Completion	The 'GPsl' Command completes once the GPIO new values are committed to the GPIO registers.			
Side Effects	There are many possible expected or unexpected side effects of changing PD Controller 's GPIOs manually. GPIOs that are connected to PD Controller Events may not behave properly if they are modified by the 'GPIO' Command. Extreme care must be taken with the use of this Command.			
Add' l Information	None			

4.13 Miscellaneous Commands

4.13.1 'ANeg' – Auto Negotiate Sink Update

Table 4-40. 'ANeg' – Auto Negotiate Sink Update

Description	**The 'ANeg' Command instructs PD Controller to re-evaluate the *Auto Negotiate Sink* register (0x37). If the re-evaluation produces a different RDO than the Active Contract RDO then a new Request message is sent.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code Table 4-1		
Command Completion	The 'ANeg' Command completes once the new RDO is calculated and PD Controller either decides to send a new Request message (and that message is sent and the GoodCRC received) or determines that no Request is necessary.		
Side Effects	The side effects include a new PD contract negotiation and updates to the associated registers.		
Add' l Information	None		

4.13.2 'DBfg – Clear Dead Battery Flag

Table 4-41. 'DBfg' – Clear Dead Battery Flag

Description	**The 'DBfg' Command is used to clear the dead battery flag. This command does not disable the PP_EXT input switch that may have been enabled during dead battery operation.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code Table 4-1		
Command Completion	The 'DBfg' Command completes once the effects of clearing the Dead Battery Flag are complete. If the Dead Battery Flag is already cleared, and the 'DBfg' Command is ran, then the 'Task rejected(0x3)' Standard Task Return Code will be returned in Output DataX. If the Dead Battery Flag has not yet been cleared, then the 'DBfg' Command will return the Standard Task Return Code 'Task completed successfully(0x0)' in Output DataX.		
Side Effects	The Dead Battery Flag causes the PD Controller to take specific actions, so clearing this flag will have side effects. PD Controller 's power input is forced to VBUS until the Dead Battery Flag is cleared, so executing this command will change PD Controller 's power input.		
Add' l Information	None		

4.14 PD3.0 Specific 4CC Commands

These commands support the PD3.0 release. In general for these commands, if PD3.0 revision has not been negotiated in the explicit PD contract between the two USB Type-C ports, then these PD3.0 4CC commands will be rejected by the Host Interface.

4.14.1 GSCX – PD Get_Source_Cap_Extended

Table 4-42. GSCX – PD Get Source Capabilities Extended

Description	**The GSCX Task instructs the PD Controller to issue a Get_Source_Cap_Extended message to the far-end device at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The GSCX Task shall be considered rejected if: • The far-end device is a Sink and indicated (via previous Source or Sink Capabilities) it was not Dual-Role Power or Rejects the Get_Source_Cap_Extended message. The GSCX Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD specification. The 'GSCX Task shall be considered successful if: • The Get_Source_Cap_Extended message is sent, GoodCRC'ed and a Source Extended Capabilities response is received and processed.		
Command Completion	The GSCX Task completes either when the Source_Capabilities_Extended message is received or the Task otherwise fails.		
Side Effects	When the GSCX Task completes successfully the *RX Source Capabilities Extended* register (0xTBD) will have been updated.		
Additional Information	None		

4.14.2 GSSt – PD Get_Status

Table 4-43. GSSt – PD Get Status

Description	**The GSSt Task instructs the PD Controller to issue a Get_Status message to the far-end device at the first opportunity while maintaining policy engine compliance.**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'GSSt' Task shall be considered rejected if: • The far-end device is a Sink and indicated (via previous Source or Sink Capabilities) it was not Dual-Role Power or Rejects the Get_Source_Status message. The GSSt Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD specification. The 'GSSt Task shall be considered successful if: • The Get_Source_Status message is sent, GoodCRC'ed and a Source Extended Capabilities response is received and processed.		
Command Completion	The GSSt Task completes either when the Source_Status message is received or the Task otherwise fails.		
Side Effects	When the GSSt Task completes successfully the *RX_Source_Status* register (0xTBD) will have been updated.		
Additional Information	None		

4.14.3 GBaS – PD Get_Battery_Status

Table 4-44. GBaS – PD Get Battery Status

Description	**The GBaS Task instructs the PD Controller to issue a Get_Battery_Status message to the far-end device at the first opportunity while maintaining policy engine compliance.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: Battery Status Reference			
	7:0	BatteryRef	00h - 03h	Represent the Fixed Batteries.
			04h - 07h	Represent the Hot Swappable Batteries.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1 The 'GBaS' Task shall be considered rejected if: • A Not_Supported message is received in response to the Get_Battery_Status message. The GBaS Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD specification. The 'GBaS' Task shall be considered successful if: • The Get_Battery_Status message is sent, GoodCRC'ed and a Battery_Status message is received and processed.			
Command Completion	The GBaS Task completes either when the Battery_Status message is received or the Task otherwise fails.			
Side Effects	When the 'GBaS'' Task completes successfully the *Received Battery Status Data Objects (BSDO)* register (0x7A) will have been updated.			
Additional Information	None			

4.14.4 GBaC – PD Get_Battery_Cap

Table 4-45. GBaC – PD Get Battery Capabilities

Description	**The GBaC Task instructs the PD Controller to issue a Get_Battery_Cap message to the far-end device at the first opportunity while maintaining policy engine compliance.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 1: Battery Status Reference			
	7:0	BatteryRef	00h - 03h	Represent the Fixed Batteries.
			04h - 07h	Represent the Hot Swappable Batteries.
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1 The 'GBaC' Task shall be considered rejected if: • A Not_Supported message is received in response to the Get_Battery_Cap message. The GBaC Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD specification. The 'GBaC' Task shall be considered successful if: • The Get_Battery_Cap message is sent, GoodCRC'ed and a Battery_Capabilities message is received and processed.			
Command Completion	The GBaC Task completes either when the Battery_Capabilities message is received or the Task otherwise fails.			
Side Effects	When the 'GBaC'' Task completes successfully the *Received Battery Capability Data Block (BCDB)* register (0x7C) will have been updated.			
Additional Information	None			

4.14.5 GMfI – PD Get_Manufacturer_Info

Table 4-46. GMfI – PD Get Manufacturer Info

Description	**The GMfI Task instructs the PD Controller to issue a Get_Manufacturer_Info message to the far-end device at the first opportunity while maintaining policy engine compliance.**			
Input DataX	**Bit**	**Name**	**Description**	
	Byte 3: Battery Status Reference			
	7:0	ManufInfoRef	Manufacture Info Reference. If ManufInfoTarget == 01h, otherwise reserved (write 0).	
			00h - 03h	Represent the Fixed Batteries.
			04h - 07h	Represent the Hot Swappable Batteries.
	Byte 2: Manufacturer Info Target			
	7:0	ManufInfoTarget	Manufacturer Info Target	
			00h	Port/Cable Plug
			01h	Battery
			02h - FFh	Reserved.
	Byte 1: SOP Target			
	7:2	Reserved	Reserved	
	1:0	SOPTarget	SOP* to send.	
			00b	SOP
			01b	SOP’
			10b	SOP''
			11b	Reserved
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1 The ‘GMfI' Task shall be considered rejected if: • SOPTarget is set to SOP' or SOP'', but cable communication is currently not allowed (for example, you are not the VCONN provider and VCONN Swaps are not allowed). • A Not_Supported message is received in response to the Get_Manufacturer_Info message. The 'GMfI' Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD specification. The ‘GMfI' Task shall be considered successful if: • The Get_Manufacturer_Info message is sent, GoodCRC’ed and a Manufacturer_Info response is received and processed.			
Command Completion	The GMfI Task completes either when the Manufacturer_Info message is received or the Task otherwise fails.			
Side Effects	When the ‘GMfI'' Task completes successfully the *Received Manufacturer Info Data Block SOP (MIDB)* register (0x71) or the *Received Manufacturer Info Data Block SOP' (MIDB)'* register (0x7E) will have been updated. If SOPTarget is set to SOP'' and the command completes successfully, then the 'MBRd' 4CC command will need to be ran to extract the data from extended message buffer received from SOP''.			
Additional Information	None			

4.14.6 MBWr – Message Buffer Write

Table 4-47. MBWr – Message Buffer Write

Description	**The MBWr command instructs the PD Controller to write data into the extended message buffer local to the PD Controller in preparation for sending an extended message to the far-end device.**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 7 - 64 : Data Byte 2 through Data Byte 58.		
	Byte 6: Data Byte 1		
	7:0	DataByte1	First Byte of data to be written at BuffOffset. Does not wrap beyond buffer size.
	Byte 5: Data Size		
	7:6	Reserved	Reserved (Write as 0).
	5:0	DataSize	Number of data bytes to be stored in the message buffer. Up to 59 bytes can be stored at once.
	Bytes 3-4: Buffer Offset		
	15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible.
	Bytes 1-2: Message Size		
	15:0	MessageSize	Size of message in bytes.
Output DataX	**Bit**	**Name**	**Description**
	None. Note: Possibly make this a Task Response.		
Command Completion	The MBWr Command completes once buffer data of DataSize at BuffOffset has been written to the message buffer. This 4CC command will be rejected if the MessageSize is larger than 260 bytes, or if the DataSize goes over 260 bytes when accounting for the BuffOffset input.		
Side Effects	None		
Additional Information	None		

4.14.7 MBRd – Message Buffer Read

Table 4-48. MBRd – Message Buffer Read

Description	**The MBRd command instructs the PD Controller to read data from the extended message buffer previously received from the far-end device.**		
Input DataX	**Bit**	**Name**	**Description**
	Byte 3: Data Size		
	7:6	Reserved	Reserved (Write as 0).
	5:0	DataSize	Number of data bytes to be read in from the message buffer. Up to 62 bytes can be read at once.
	Bytes 1-2: Buffer Offset		
	15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible.
Output DataX	**Bit**	**Name**	**Description**
	Bytes 4 - 64: Data Bytes 2 through Data Byte 62		
	Byte 3: Data Byte 1		
	7:0	DataByte1	First Byte of data read at BuffOffset.
	Bytes 1-2: Message Size		
	15:0	MessageSize	Size of message in bytes.
Command Completion	The MBRd Command completes once buffer data of DataSize at BuffOffset has been read from the message buffer. This 4CC command will be rejected if the DataSize is larger than 62 bytes, or if the DataSize goes over 260 bytes when accounting for the BuffOffset input.		
Side Effects	None		
Additional Information	None		

4.14.8 SRrq– Security Request

Table 4-49. SRrq – Security Request

Description	**The SRrq Task instructs the PD Controller to issue a Security Request message to the far-end device at the first opportunity while maintaining policy engine compliance. The memory buffer for storing the information of the command must first be written using a sequence of MBWr commands by the host. Once transferred to the far-end device, a Security_Request_Event is asserted and the message can be retrieved using a sequence of MBRd commands.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 4-5: Data Size			
	15:0	DataSize	Number of data bytes to be transferred from the message buffer. Up to 260 bytes can be transferred at a time.	
	Bytes 2-3: Buffer Offset			
	15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible. Normally set to 0, the beginning of the memory buffer.	
	Byte 1: SOP Target			
	7:2	Reserved	Reserved	
	1:0	SOPTarget	SOP* to send.	
			00b	SOP
			01b	SOP'
			10b	SOP''
			11b	Reserved
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1			
Command Completion	The 'SRrq' command will complete when the Security_Request message has been sent and has been GoodCRC'ed.			
Side Effects				
Additional Information	None			

4.14.9 SRrs– Security Response

Table 4-50. SRrs - Security Response

Description	**The SRrs Task instructs the PD Controller to send a Security Response message to the far-end device at the first opportunity while maintaining policy engine compliance. The memory buffer for storing the information of the command must first be written using a sequence of MBWr commands by the host. Once transferred to the far-end device, a Security_Response_Event is asserted and the message can be retrieved using a sequence of MBRd commands.**			
Input DataX	**Bit**	**Name**	**Description**	
	Bytes 4-5: Data Size			
	15:0	DataSize	Number of data bytes to be transferred from the message buffer. Up to 260 bytes can be transferred at a time.	
	Bytes 2-3: Buffer Offset			
	15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible. Normally set to 0, the beginning of the memory buffer.	
	Byte 1: SOP Target			
	7:2	Reserved	Reserved	
	1:0	SOPTarget	SOP* to send.	
			00b	SOP
			01b	SOP'
			10b	SOP''
			11b	Reserved
Output DataX	**Bit**	**Name**	**Description**	
	Byte 1: Standard Task Return Code			
	Table 4-1			
Command Completion	The 'SRrs' command will complete when the Security_Response message has been sent and has been GoodCRC'ed.			
Side Effects				
Additional Information	None			

4.14.10 ALRT – Send Alert Message

Table 4-51. ALRT – Send Alert Message

Description	**The ALRT Task instructs the PD Controller to issue a Alert message to the far-end device at the first opportunity while maintaining policy engine compliance. Contents of the Alert message sent come from the data input into the *Transmit Alert Data Object (ADO)* register (0x75).**		
Input DataX	**Bit**	**Name**	**Description**
	None		
Output DataX	**Bit**	**Name**	**Description**
	Byte 1: Standard Task Return Code		
	Table 4-1 The 'ALRT' Task shall be considered rejected if: • A Not_Supported message is received in response to the Alert message. The 'ALRT' Task shall be considered timed-out if: • The far-end fails to respond within the time required by the PD specification. The 'ALRT' Task shall be considered successful if: • The Alert message is sent and GoodCRC'ed.		
Command Completion	The command will complete when the Alert message is sent and GoodCRC'ed or the command is otherwise rejected.		
Side Effects	None		
Additional Information	None		

4.15 UCSI 4CC Commands

The following commands are for UCSI implementation.

4.15.1 'UCSI' - UCSI Commands

The 'UCSI' command is used to pass a UCSI command from the PPM to the LPM. The input and output data are dependent on the command passed. The supported commands and their associated data structures are outlined below:

Table 4-52. UCSI - PPM_RESET

Description	**CONNECTOR_RESET - This command is used to reset the Platform Policy Manager**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:7	Reserved	Reserved
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x01h (PPM_RESET)
Output DataX	**Bit**	**Name**	**Description**
	Byte 1		
	7:0	Task Response	Standard task return code and additional error flags
Command Completion	This command will always return a successful task return code.		
Side Effects	None		
Additional Information	None		

Table 4-53. UCSI - CONNECTOR_RESET

Description	**CONNECTOR_RESET - This command is used to reset the Type-C Port**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:7	Reserved	Reserved
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x03h (CONNECTOR_RESET)
Output DataX	**Bit**	**Name**	**Description**
	Byte 1		
	7:0	Task Response	Standard task return code and additional error flags
			0x04 - Connector reset failed
Command Completion	This command is successful if the device is not in Dead battery state or the port is not the Dead Battery Power Provider. Command failure reasons are indicated in error code in Byte 1.		
Side Effects	None		

Table 4-53. UCSI - CONNECTOR_RESET (continued)

Description	CONNECTOR_RESET - This command is used to reset the Type-C Port
Additional Information	None

Table 4-54. UCSI - GET_CAPABILITY

Description	GET_CAPABILITY - This command is used to get the capabilities of the device		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:7	Reserved	Reserved
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x06h (GET_CAPABILITY)
Output DataX	**Bit**	**Name**	**Description**
	Bytes 16-17		
	15:0	bcdTypeCVersion	Type-C Version Supported (0x130)
	Bytes 14-15		
	15:0	bcPDVersion	PD Version Supported (0x030)
	Bytes 12-13		
	15:0	bcdBCVersion	BC version supported (0x120)
	Byte 11		
	7:0	Reserved	
	Byte 10		
	7:0	Number of Alternate Modes	Not Populated by TPS6598x
	Bytes 7-9:		
	23:7	Reserved	
	6	External supply notification supported	
	5	Cable details supported	
	4	PDO Details supported	
	3	Alternate mode override supported	
	2	Alternate mode details supported	
	1	Reserved	
	0	SET_UOM Supported	
	Byte 6		
	7	Reserved	
	6:0	bNumConnectors	Not Populated by TPS6598x
	Bytes 2-5: bmAttributes		
	31:16	Reserved	
	15:8	bmPowerSource	
	7	Reserved	
	6	USB Type-C Current	
	5:3	Reserved	
	2	USB Power Delivery	
	1	Battery Charging	
	0	Disabled State Support	
	Byte 1		
	7:0	Task Response	Standard task return code

Table 4-54. UCSI - GET_CAPABILITY (continued)

Description	GET_CAPABILITY - This command is used to get the capabilities of the device
Command Completion	This command will always return a successful task return code.
Side Effects	None
Additional Information	None

Table 4-55. UCSI - GET_CONNECTOR_CAPABILITY

Description	**GET_CONNECTOR_CAPABILITY - This command is used to get the capabilities of the port**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	7	Reserved	
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x07h (GET_CONNECTOR_CAPABILITY)
Output DataX	**Bit**	**Name**	**Description**
	Byte 3:		
	7:6	Reserved	
	5	Swap to SNK	
	4	Swap to SRC	
	3	Swap to UFP	
	2	Swap to DFP	
	1	Consumer	
	0	Provider	
	Byte 2: Operation Mode		
	7	Alternate Mode	
	6	USB3	
	5	USB2	
	4	Debug Accessory	
	3	Analog Audio Accessory	
	2	DRP (Rp/Rd)	
	1	Rd Only	
	0	Rp Only	
	Byte 1		
	7:0	Task Response	Standard task return code
Command Completion	This command will always return a successful task return code.		
Side Effects	None		
Additional Information	None		

Table 4-56. UCSI - SET_UOR

Description	**SET_UOR - This command is used to set the USB operation role that the OPM wants the connector to operate at for the current connection**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:10	Reserved	
	9:7	USB Operation Role	xx1b - If this bit is set the connector shall initiate swap to DFP if not already in teh DFP role
			x1xb - If this bit is set the connector shall initiate swap to UFP if not already in the UFP role
			1xxb - If this bit is set then the connector shall accept role swap change requests from the port partner. If this bit is cleared then the connector shall reject role swap change requests from the port partner
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x09h (SET_UOR)
Output DataX	**Bit**	**Name**	**Description**
	Byte 1		
	7:0	Task Response	Standard task return code and error flags
			0x04 - Not in Active Contract
			0x05 - Not supporting the role which has been requested
			0x06 - Unsuccessful completion of the Data Role Swap message
			0x07 - Rejected by port partner
			0x08 - Hard reset during Data Role Swap message
Command Completion	This command is successful if port is already in the role it is requested for or after successful completion of Data Role Swap Message if not in role requested for. Command failure reasons are indicated in error code in Byte 1		
Side Effects	None		
Additional Information	None		

Table 4-57. UCSI - SET_PDR

Description	**SET_PDR - This command is used to set the power direction that the OPM wants the connector to operate at for the current connection**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:10	Reserved	
	9:7	Power Direction Role	xx1b - If this bit is set the connector shall initiate swap to Source if not already in the Source role
			x1xb - If this bit is set the connector shall initiate swap to Sink if not already in the Sink role
			1xxb - If this bit is set then the connector shall accept power swap change requests from the port partner. If this bit is cleared then the connector shall reject power swap change requests from the port partner
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x0Bh (SET_PDR)
Output DataX	**Bit**	**Name**	**Description**
	Byte 1		
	7:0	Task Response	Standard task return code and error flags
			0x04 - Not in Active Contract
			0x05 - Not supporting the role which has been requested
			0x06 - Unsuccessful completion of the Power Role Swap message
			0x07 - Rejected by port partner
			0x08 - Hard reset during Power Role Swap message
Command Completion	This command is successful if port is already in the role it is requested for or after successful completion of Power Role Swap Message if not in role requested for. Command failure reasons are indicated in error code in Byte 1		
Side Effects	None		
Additional Information	None		

Table 4-58. UCSI - GET_CONNECTOR_STATUS

Description	GET_CONNECTOR_STATUS - This command is used to get the capabilities of the device		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:7	Reserved	Reserved
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x12h (GET_CONNECTOR_STATUS)
Output DataX	**Bit**	**Name**	**Description**
	Byte 10		
	7:4	Reserved	
	3:2	Provider Capabilities Limited Reason	00b - Power Budget Lowered
			01b - Reaching Power Budget Limit
			10b - Reserved
			11b - Reserved
	1:0	Battery Charging Capability Status	00b - No Charging
			01b - Nominal Charging Rate
			10b - Slow Charging Rate
			11b - Very Slow Charging Rate
	Bytes 6-9:		
	31:0	Request Data Object (RDO)	This field is only valid when the Connect Status field is set to one and the Power Operation Mode field is set to PD
	Bytes 4-5:		
	15:13	Connector Partner Type	000b - Reserved
			001b - DFP Attached
			010b - UFP Attached
			011b - Powered cable/No UFP Attached
			100b - Powered cable/ UFP Attached
			101b - Debug Accessory Attached
			110b - Audio Adapter Accessory attached
			111b - Reserved
	12:5	Connector Partner Flags	xxxxxxx1b - USB Mode
			xxxxxx1xb - Alternate Mode
	4	Power Direction	0b - Connector is operating as a SINK
			1b - Connector is operating as a SOURCE
	3	Connect Status	Set to 1 when a device is connected
	2:0	Power Operation Mode	000b - Reserved
			001b - USB Default Operation
			010b - Battery Charging
			011b - Power Delivery
			100b - USB Type-C Current (1.5A)
			101b - USB Type-C Current (3.0A)
			110b - Reserved
			111b - Reserved

Table 4-58. UCSI - GET_CONNECTOR_STATUS (continued)

Description	GET_CONNECTOR_STATUS - This command is used to get the capabilities of the device		
Output DataX	Bytes 2-3: Connector Status Change		
	15	Error	
	14	Connect Change	
	13	Reserved	
	12	Power Direction Change	
	11	Connector Partner Status Change	
	10	Reserved	
	9	Battery Charging Status Change	
	8	Supported CAM Change	
	7	PD Reset Complete	
	6	Negotiated Power Level Change	
	5	Supported Provider Capabilities Change	
	4	Reserved	
	3	Reserved	
	2	Power Operation Mode Change	
	1	External Supply Change	
	0	Reserved	
	Byte 1		
	7:0	Task Response	Standard task return code
Command Completion	This command will always return a successful task return code.		
Side Effects	None		
Additional Information	None		

Table 4-59. UCSI - GET_ALTERNATE_MODES

Description	**GET_ALTERNATE_MODES - This command is used to get the Alternate Modes that the Connector/Cable/Attached Device is capable of supporting**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:26	Reserved	
	25:24	Number of Alternate Modes	Number of Alternate Modes to return starting from the Alternate Mode Offset. The number of Alternate Modes to return is the value in this field plus 1. The maximum value of this field is 1.
	23:16	Alternate Mode Offset	Starting offset of the first alternate mode to be returned
	15	Reserved	
	14:8	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	7:3	Reserved (Write 0)	
	2:0	Recipient	00b - Port (Connector)
			01b - SOP
			10b - SOP'
			11b - SOP"
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x0Ch (GET_ALTERNATE_MODES)
Output DataX	**Bit**	**Name**	**Description**
	Byte 11-14		
	31:0	MID[1]	Mode ID associated with the below SVID
	Bytes 9-10		
	15:0	SVID[1]	Standard or Vendor ID
	Bytes 5-8		
	31:0	MID[0]	Mode ID associated with the below SVID
	Bytes 3-4		
	15:0	SVID[0]	Standard or Vendor ID
	Byte 2		
	7:0	Data Length	Number of Data Bytes returned
	Byte 1		
	7:0	Task Response	Standard task return code and error flags
Command Completion	If a value greater than 11b is written to Recipient in Input DataX, if Number of Alternate Modes is greater than 1 in Input DataX, or the Alternate Mode Offset is greater than the maximum allowed number of total modes allowed by the USB-PD spec in Input DataX, then this task will be rejected. Otherwise, this command will complete successfully.		
Side Effects	None		
Additional Information	None		

Table 4-60. UCSI - GET_CAM_SUPPORTED

Description	**GET_CAM_SUPPORTED - This command is used to get the list of Alternate Modes that are currently supported on the connector**		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:7	Reserved	Reserved
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x0Dh (GET_CAM_SUPPORTED)
Output DataX	**Bit**	**Name**	**Description**
	Byte 2		
	7:0	SupportedAlternateModes	
	Byte 1		
	7:0	Task Response	Standard task return code and additional error flags
Command Completion	This command will always return a successful task return code.		
Side Effects	None		
Additional Information	None		

Table 4-61. UCSI - GET_PDOS

Description	GET_PDOS - This command is used to get the Sink or Source PDOs associated with the identified connector		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:21	Reserved	Reserved
	20:19	Source Capabilities Type	00b - Current Supported Source Capabilites
			01b - Advertised Capabilities
			10b - Maximum Supported Source Capabilities
			11b - Not Used
	18	Source or Sink PDOs	This field shall be set to one if the OPM wants to retrieve the Source PDOs otherwise it wants to retrieve the Sink PDOs.
	17:16	Number of PDOs	Number of PDOs to return starting from the PDO Offset. The number of PDOs to return is the value in this field plus 1.
	15:8	PDO Offset	Starting offset of the first PDO to be returned
	7	Partner PDO	This field shall be set to one if the OPM wants to retrieve the PDOS of the device attached to the connector
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x10h (GET_PDOS)
Output DataX	**Bit**	**Name**	**Description**
	Bytes 14 - 17		
	31:0	PDO[3]	
	Bytes 10 - 13		
	31:0	PDO[2]	
	Bytes 6-9		
	31:0	PDO[1]	
	Bytes 2-5		
	31:0	PDO[0]	
	Byte 1		
	7:0	Task Response	Standard task return code and additional error flags
Command Completion	If Partner PDO is set to 1, then this task will either be successful, timed out, or rejected based on the same criteria as the 'GSrC' PD Get Source Capabilities or as the 'GSkC' Get Sink Capabilities, depending on the Source or Sink PDOs bit, which determines what type of PDOs you are requesting. Please see those 4CC command descriptions for more details. If Partner PDO is set to 0 and Source Capabilities Type is set to 11b, then this task will be rejected. Other than the previous mentioned cases occurring, if this task is ran, it will complete successfully.		
Side Effects	None		
Additional Information	None		

Table 4-62. UCSI - GET_ERROR_STATUS

Description	GET_ERROR_STATUS - This command is used to get details about an error, if one is reported by the PPM		
Input DataX	**Bit**	**Name**	**Description**
	Bytes 3-8:		
	47:7	Reserved	Reserved
	6:0	Connector Number	This field indicates the connector whose capabilities are to be retrieved. Write a 0x1h for connector/port 1 and write a 0x2h for connector/port 2. The connector number needs to correspond with the port I2C address the 'UCSI' 4CC command is written to. A value of zero in this field is illegal.
	Byte 2		
	7:0	DataLength	0x00h
	Byte 1		
	7:0	Command	0x13h (GET_ERROR_STATUS)
Output DataX	**Bit**	**Name**	**Description**
	Bytes 15 -18		
	31:0	Reserved	
	Bytes 11 - 14		
	31:0	Reserved	
	Bytes 7-10		
	31:0	Reserved	
	Bytes 3-6 : Error Information		
	31:15	Reserved	
	14	Reserved	
	13	Reserved	
	12	Swap rejected	
	11	PPM Policy Conflict	
	10	Hard Reset	
	9	Port Partner rejected swap	
	8	Undefined	
	7	Overcurrent	
	6	Contract negotiation failure	
	5	Command unsuccessful due to dead battery condition	
	4	CC Communication Error	
	3	Incompatible Connector Partner	
	2	Invalid Command Specific Parameters	
	1	Non Existent Connector	
	0	Unrecognized Command	
	Bytes 2		
	7:0	Data Length	
	Byte 1		
	7:0	Task Response	Standard task return code and additional error flags
Command Completion	This command will always return a successful task return code.		
Side Effects	None		

Table 4-62. UCSI - GET_ERROR_STATUS (continued)

Description	GET_ERROR_STATUS - This command is used to get details about an error, if one is reported by the PPM
Additional Information	None

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