The TPS61022EVM-034 evaluates the performance of the TPS61022, which is a 8-A boost converter with 0.5-V ultra-low input voltage. This user's guide describes the input and output ranges, EVM setup, bill of materials (BOM), schematic, and the PCB layout.

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1 Introduction

1.1 Performance

Table 1 provides a summary of the TPS61022EVM performance characteristics, tested at 25°C ambient temperature.

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>3.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output voltage (TPS61022EVM)</td>
<td>5.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output current</td>
<td></td>
<td>3</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1.2 Modification

The EVM is designed to support some modifications by the user. The external component can be changed according to the real application.

1.3 Input Capacitor

A 150-µF tantalum capacitor, C1, is added as the input capacitor in the EVM. The ESR of the tantalum capacitor is 0.1 Ω, to damp the ringing of the input voltage when the EVM is powered by a power supply with a long cable. The capacitor is not required for proper operation and can be removed in a real application.

1.4 Feedforward Capacitor

A feedforward capacitor C8 in parallel with R1 induces a pair of zero and pole in the loop transfer function. By setting the proper zero frequency, the feedforward capacitor can increase the phase margin to improve the loop stability. The C8 is not populated in the TPS61022EVM. The phase margin of the TPS61022EVM is good enough when the input voltage is from 2.5 V to 4.4 V. In the applications that input voltage is below 2 V or output effective capacitance is larger than 40 µF, TI suggests to add the feedforward capacitor. The calculation of the feedforward capacitor can be found in the TPS61022 data sheet and in TI application report Feedforward Capacitor Makes Boost Converter Fast and Stable.

For example, TI suggests a 10-pF feedforward capacitor for C8 if input voltage of the EVM is 1.8 V. Figure 1 is the Bode plot with and without the feedforward capacitor. The phase margin is 63° with the feedforward capacitor, while the phase margin is only 44° without feedforward capacitor. Test conditions are VIN = 1.8 V, VOUT = 5 V, and IOUT = 1 A.

![Figure 1. Bode Plot Comparison With and Without Feedforward Capacitor](bodevin1.8.xlsm.grf)
2 Setup

This section describes the setup of the TPS61022EVM-034.

2.1 Input/Output Connector Descriptions

See the following:

- **J1-VIN**: Positive input connection from the input supply for the EVM
- **J2-VOUT**: Positive connection for the output voltage
- **J3-GND**: Return connection from the input supply for the EVM
- **J4-GND**: Return connection for the output voltage
- **J5-MODE**: MODE pin input jumper. Place a jumper across MODE and pin 1 (GND) to set in auto PFM mode, place a jumper across MODE and pin 3 (VIN) to set in forced PWM mode
- **J6-EN**: EN pin input jumper. Place a jumper across EN and pin 3 (VIN) to turn on the IC, place a jumper across EN and pin 1 (GND) to turn off the IC
- **J7-VIN_S**: Input voltage sensing for measuring efficiency. VIN_S+ is for positive input and VIN_S- is for negative input.
- **J8-VOUT_S**: Output voltage sensing for measuring efficiency. VOUT_S+ is for output positive node and VOUT_S- is for output negative node
3 Schematic and Bill of Materials

This section provides the TPS61022EVM-034 schematic, bill of materials (BOM), and board layout.

3.1 Schematic

Figure 2 is the EVM schematic.

Figure 2. TPS61022EVM-034 Schematic
### 3.2 Bill of Materials

Table 2 displays the EVM bill of materials.

<table>
<thead>
<tr>
<th>Designator</th>
<th>Qty</th>
<th>Value</th>
<th>Description</th>
<th>PackageReference</th>
<th>PartNumber</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>150uF</td>
<td>CAP, TA, 150 uF, 10 V, +/- 10%, 0.1 ohm, SMD</td>
<td>7343-31</td>
<td>T495D157K010ATE100</td>
<td>Kemet</td>
</tr>
<tr>
<td>C2, C4, C5, C6</td>
<td>4</td>
<td>22uF</td>
<td>CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805</td>
<td>0805</td>
<td>GRM21BR61A226ME44L</td>
<td>Murata</td>
</tr>
<tr>
<td>C3</td>
<td>1</td>
<td>0.1uF</td>
<td>CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402</td>
<td>0402</td>
<td>GRM155R61A104KA01D</td>
<td>Murata</td>
</tr>
<tr>
<td>C10</td>
<td>0</td>
<td>100pF</td>
<td>CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603</td>
<td>0603</td>
<td>GRM1885CH101JA01D</td>
<td>Murata</td>
</tr>
<tr>
<td>C7</td>
<td>0</td>
<td>47uF</td>
<td>CAP, CERM, 47 uF, 10 V, +/- 10%, X5R, 1206</td>
<td>1206</td>
<td>GRM31CR61A476KE1SL</td>
<td>Murata</td>
</tr>
<tr>
<td>C9</td>
<td>0</td>
<td>1000uF</td>
<td>CAP, AL, 1000 uF, 10 V, +/- 20%, 0.15 ohm, SMD</td>
<td>SMT Radial G</td>
<td>EEE-FCA102P</td>
<td>Panasonic</td>
</tr>
<tr>
<td>C8</td>
<td>0</td>
<td>10pF</td>
<td>CAP, CERM, 10 pF, 10 V, +/- 10%, X7R, 0603</td>
<td>0603</td>
<td>06032C100K72A</td>
<td>AVX</td>
</tr>
<tr>
<td>R4</td>
<td>0</td>
<td>10.0</td>
<td>RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603</td>
<td>0603</td>
<td>CRCW060310R0FKEA</td>
<td>Vishay-Dale</td>
</tr>
</tbody>
</table>

**Table 2. TPS61022EVM-034 Bill of Materials**
4 Board Layout

The PCB of the TPS61022EVM has four layers. Figure 3 and Figure 4 show the top side and bottom side of the PCB layout, respectively. The two internal layers are ground panels helping to improve the thermal performance.
Figure 4. TPS61022EVM-034 Bottom-Side Layout
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