User's Guide
TPS629210EVM User's Guide

TEXAS INSTRUMENTS

ABSTRACT

The TPS629210EVM is designed to help user easily evaluate the performance of TPS629210. The user's guide includes the following:

- Performance characteristics
- EVM configuration
- Test setup
- Test results
- PCB layout
- Schematic diagram
- Bill of materials

Table of Contents

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1 Introduction

The TPS629210 is a high efficiency and highly flexible synchronous step-down buck converter in a small 1.6-mm × 2.1-mm SOT583 package. The TPS629210 can be configured to run 2.5 MHz or 1 MHz in either forced PWM mode or auto PFM/PWM mode. In 2.5-MHz auto PFM/PWM mode, automatic efficiency enhancement mode automatically adjusts the switching frequency based on both input and output voltage to hold a high efficiency through the whole operation range without the need of using different inductors. The device includes a smart-Config/mode input to select the following:

- Different combinations of external and internal feedback
- Maximum switching frequency
- Output discharge enable and disable
- Auto PFM/PWM
- Forced PWM operations

The TPS629210EVM(BSR131-005) uses 1-A TPS629210 to produce a 3.3-V output from a 12-V input.

2 Performance Specification

Table 2-1 provides a summary of the TPS629210EVM performance specifications. All the specifications are given at an ambient temperature of 25°C.

Table 2-1. TPS629210EVM Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	UNIT
Input voltage		5	12	17	V
Output voltage			3.3		V
Output current		0		1	A
Input current	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, forced PWM, 2.5 MHz, 3.3-µH inductor		5.7		mA
	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, forced PWM, 2.5 MHz, 3.3-µH inductor		0.302		A
Switching frequency	Set by Mode/S-CONF pin		2.5		MHz
Line regulation	V_{IN} = 5 V–17 V, V_{OUT}= 3.3 V, I_{OUT} = 1 A, forced PWM, 2.5 MHz, VSET, 3.3-µH inductor		±0.15		%
Load regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A–1 A, forced PWM and auto PFM/PWM with AEE, 2.5 MHz, VSET, 3.3-µH inductor		±0.15		%
Output ripple	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, forced PWM, 2.5 MHz, 3.3-µH inductor		10		mV
Peak efficiency	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A–1 A, forced PWM, 2.5 MHz, 3.3-µH inductor		90.43		%
	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A–1 A, auto PFM/PWM with AEE, 2.5 MHz, 3.3-µH inductor		90.77		%
	V_{IN} = 12 V, V_{OUT} = 3.3 V,I_{OUT} = 10 mA, auto PFM/PWM with AEE, 2.5 MHz, 3.3-µH inductor		84.66		%
Output rise time	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, forced PWM, 2.5 MHz, 3.3-µH inductor		500		µs
Load transient	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0.5 A–1 A, Slew rate: 1 A/µs, forced PWM, VSET, 2.5 MHz, 3.3-µH inductor		±58		mV
Loop bandwidth	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, forced PWM, VSET, 2.5 MHz, 3.3-µH inductor		95.89		kHz
Phase margin	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, forced PWM, VSET, 2.5 MHz, 3.3-µH inductor		84.4		°
IC case temperature	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, forced PWM, 2.5 MHz, 3.3-µH inductor, 10 minutes soaking		34.6		°C

3 EVM Configuration and Modification

The EVM is designed to provide access to features of the TPS629210. The EVM also provides jumpers for different configurations. Jumper selections must be made prior to enabling the TPS629210. Additional input and output capacitors can be added. The input voltage at which the IC turns on can be programmed with a voltage divider. The TPS629210EVM allows multiple MODE/S-CONF pin configurations for switching frequency, auto PFM/PWM with AEE, forced PWM and output discharge setting, as well as internal and external feedback options. The loop response can also be measured.

3.1 Input and Output Capacitors

C2 is provided for additional input capacitance. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple. C6, C7, C8, and C9 are provided for additional output capacitors. These capacitors are not required for proper operation but can be used to reduce the output voltage ripple. The total output capacitance must remain within the recommended range for the TPS629210.

3.2 Configurable Enable Threshold Voltage

JP1 is provided as an option for the Enable pin with precise threshold voltage. R4 and R5 can be adjusted to set a user-selectable input voltage at which the IC turns on. The EVM pre-configured R4 and R5 to have 6.5-V rising and 5.85-V falling threshold voltage.

3.3 MODE/S-CONF Setting

JP2 is used to set different MODE/S-CONF configurations. MODE/S-CONF can be connected to VIN and GND as a traditional HIGH or LOW level. R6 and R7 select the other device configurations including the following:

* Internal/external feedback
* Switching frequency
* Output discharge
* Auto PFM/PWM or forced PWM options

The values of R6 and R7 can be changed per the user's requirement.

* While using the internal feedback (VSET) configuration for the output voltage setting, either float the FB pin by cutting the net tie (NT1) included on the back of the board or remove both R1 and R2 for 3.3-V output voltage. Other output voltage can be programmed by removing R1 and changing the value of R2. Ensure the JP2 jumper is placed correctly for proper operation with internal feedback.

> **WARNING**
> Do not set the MODE pin for external feedback if either the net tie (NT1) is cut or R1 and R2 are removed. This can cause damage to the device due to lack of external feedback control.

* Dynamic mode option is an advanced feature that allows the MODE pin to actively switch between forced PWM and auto PFM/PWM during operation, but this is only possible by driving the mode pin between VIN and GND. This feature provides the user with the option of controlling if and when the device enters power save mode (DCM).

3.4 Power Good

JP3 is provided as an option for power-good test point. If power good is not used, it is recommended to tie to GND or leave open.

3.5 Power-Good Pullup Voltage

JP4 is provided as an option for power-good pullup voltage. Either V_{IN} or V_{OUT} with a 100-kΩ pullup resistor.

3.6 Feedforward Capacitor Option

C10 is provided as an optional of feedforward capacitor (Cff) to help improve the loop stability if needed. A more detailed discussion on the optimization for stability versus transient response can be found in *Optimizing Transient Response of Internally Compensated dc-dc Converter With Feedforward Capacitor* and *Feedforward Capacitor to Improve Stability and Bandwidth With the TPS621-Family and TPS821-Family* application reports.

3.7 Output Voltage Setting

The TPS629210EVM is configured for external feedback as default with an output voltage of 3.3 V set by R1 and R2. Additionally, if the internal feedback (VSET) configuration is used, the user can cut net tie NT1 located on the back of the board. This modification is shown in Figure 3-1. This floats the FB pin, resulting in a 3.3-V output voltage using the internal VSET. Resistors R1 and R2 can also be changed to set the output voltage between 0.6 V and 5.5 V. See the *TPS629210 3-V to 17-V, 1-A Low IQ Buck Converter in SOT583 Package* data sheet for recommended values. R2 was populated with 34 k such that if the internal (VSET) is chosen while R1 is removed, the device regulates to 1.8-V output voltage.

> **WARNING**
> If the output voltage is increased, make sure the voltage rating of output capacitor C5 is sized appropriately.
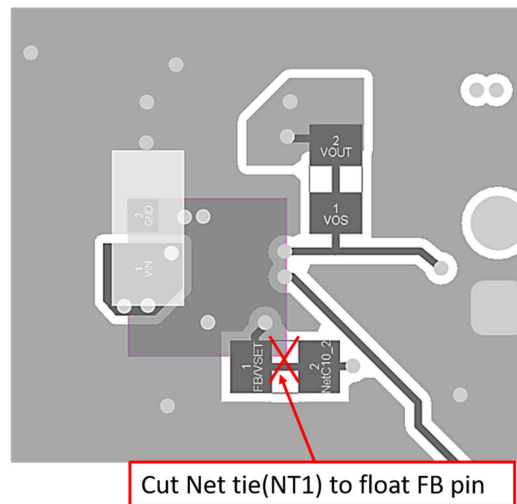
Figure 3-1. Internal Feedback (VSET) Configuration Board Modification

3.8 Loop Response Measurement

The loop response can be measured after simply changing to the board. First, cut net tie (NT2) and install a 10-Ω 0603 resistor on the bottom of board. Figure 3-2 shows this change. An AC signal (10-mV, peak-to-peak amplitude is recommended) can be injected into the control loop across the added 10-Ω resistor.
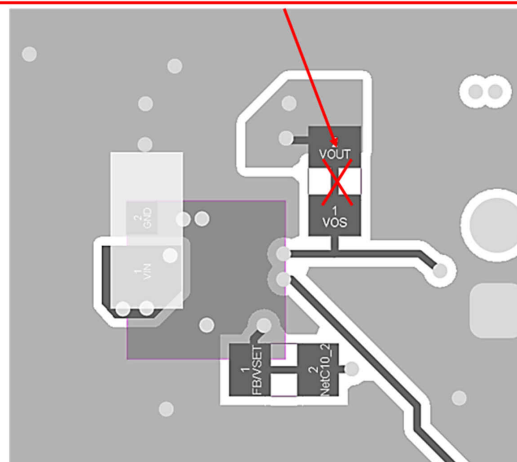
Figure 3-2. Bode Plot Measurement Board Modification

4 EVM Test Set Up

This section describes how to properly test the EVM

4.1 Input and Output Connectors

Table 4-1. Input and Output Connector

Connector	Pins	Description
J1	Pin1 and Pin2	V_{IN} positive input for input supply
	Pin3 and Pin4	S+ and S– input voltage sense. Input voltage measure points
	Pin5 and Pin6	GND return for input supply
J2	Pin1 and Pin2	V_{OUT} output voltage connection
	Pin3 and Pin4	S+ and S– output voltage sense. Output voltage measure points
	Pin5 and Pin6	GND output return connection

4.2 Jumper Configuration

4.2.1 JP1 Enable

Table 4-2. Enable Pin Configuration

Jumper Short Location	Description
Pin2 and Pin3	Turn on the device as default.
Pin3 and Pin4	Turn off device.
Pin1 and Pin2, Pin3 and Pin4	Set programmable Enable threshold voltage with R4 and R5.
Pin3 and Pin4	Pin1 can be used for external supply voltage with R4 and R5 resistor divider.

4.2.2 JP2 MODE/S-CONF

Table 4-3. MODE/S-CONF Pin Configuration

Jumper Short Location	Description
Pin1 and Pin3	Forced PWM, 2.5 MHz, external FB, output discharge enabled
Pin3 and Pin5	Auto PFM/PWM with AEE, 2.5 MHz. external FB, output discharge enabled
Pin2 and Pin4	124 k to GND, forced PWM, 1 MHz, internal FB(VSET), output discharge disabled
Pin4 and Pin6	64.9 k to GND, auto PFM/PWM, 1 MHz, internal FB(VSET), output discharge enabled

4.2.3 JP3 Power Good

The PGOOD output is on pin 1 of this header with a convenient ground on pin 2. If PG is not used, short pin1 and pin2 by a jumper.

4.2.4 JP4 PG Pullup Voltage

Table 4-4. PG Pullup Voltage Option

Jumper Short Location	Description
Pin1 and Pin2	PG pulls up to output voltage.
Pin2 and Pin3	PG pulls up to input voltage.
No jumper	JP4 pin2 can pull up to different external voltage. This external voltage must remain below 18 V.

5 Test Results

This section provides the test results of the TPS629210EVM.
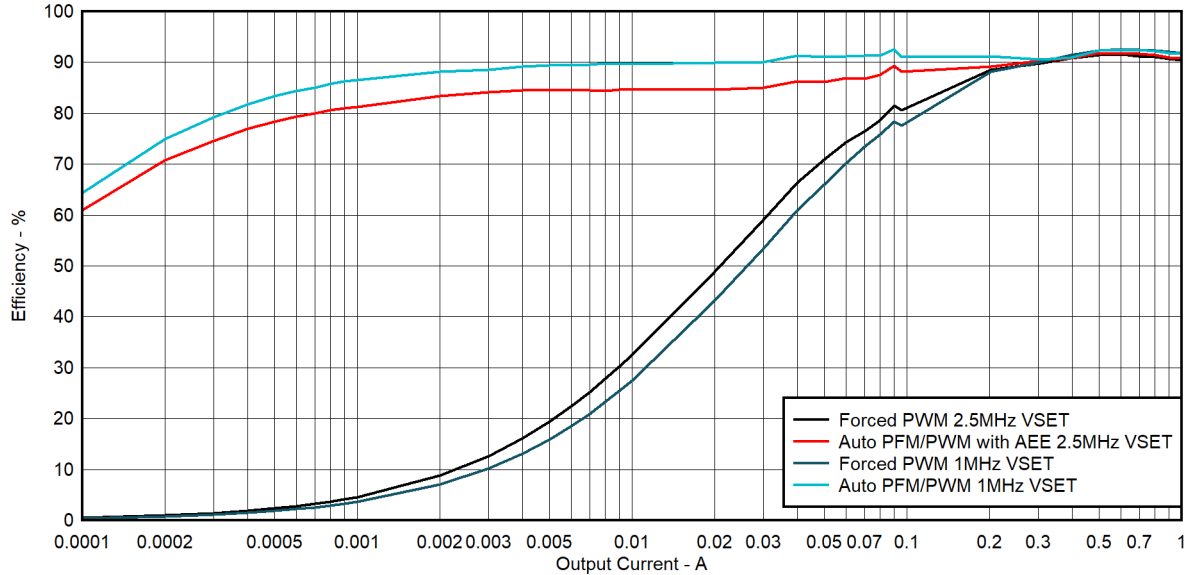
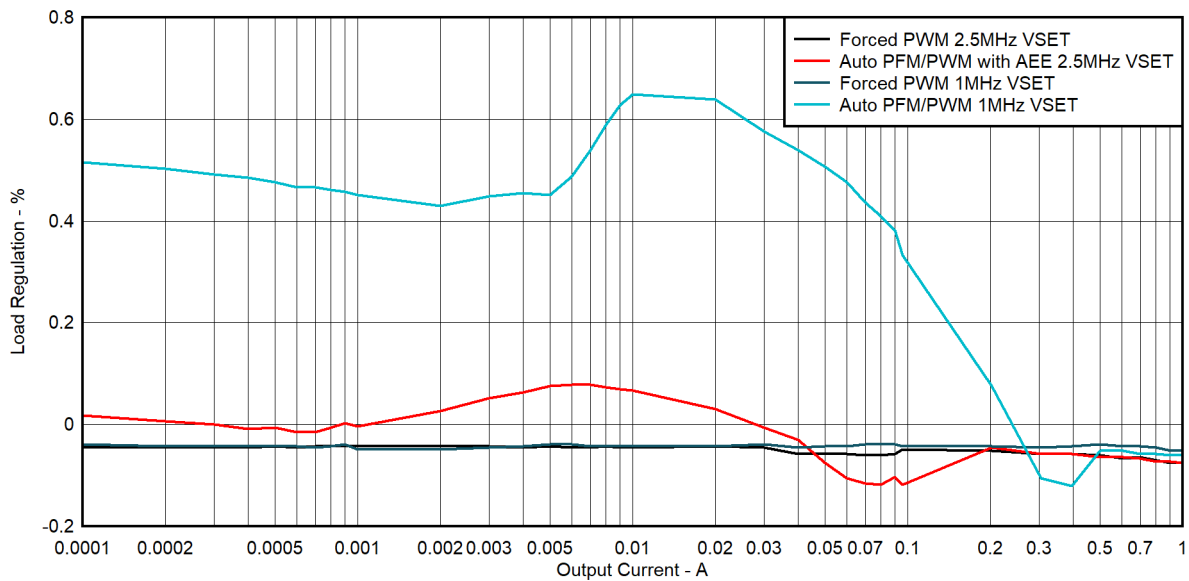**Figure 5-1. Efficiency, V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 2.5 MHz and 1 MHz**

Figure 5-2. Load Regulation, V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 2.5 MHz and 1 MHz
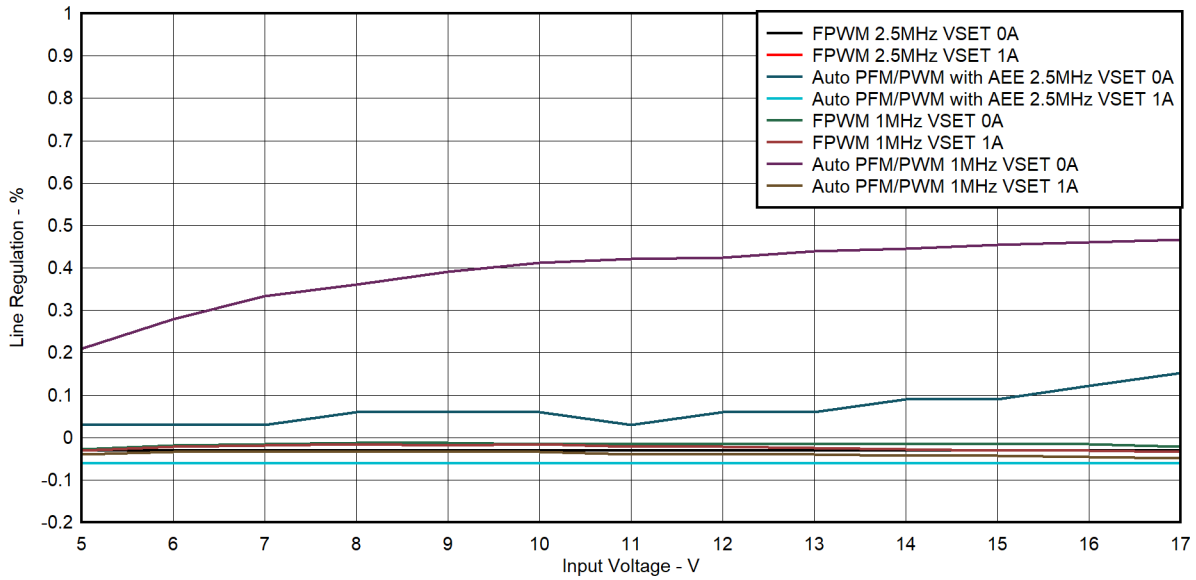
Figure 5-3. Line Regulation, V_{IN} = 5 V–17 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A and 1 A, F_{SW} = 2.5 MHz and 1 MHz
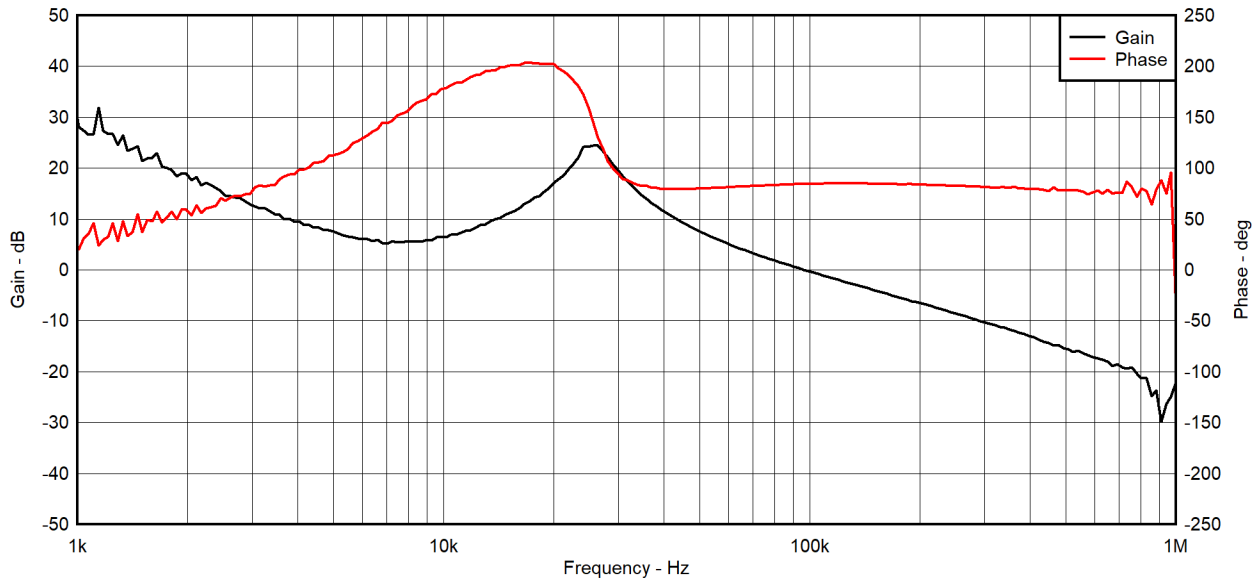
Figure 5-4. Loop Response Forced PWM VSET, V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A
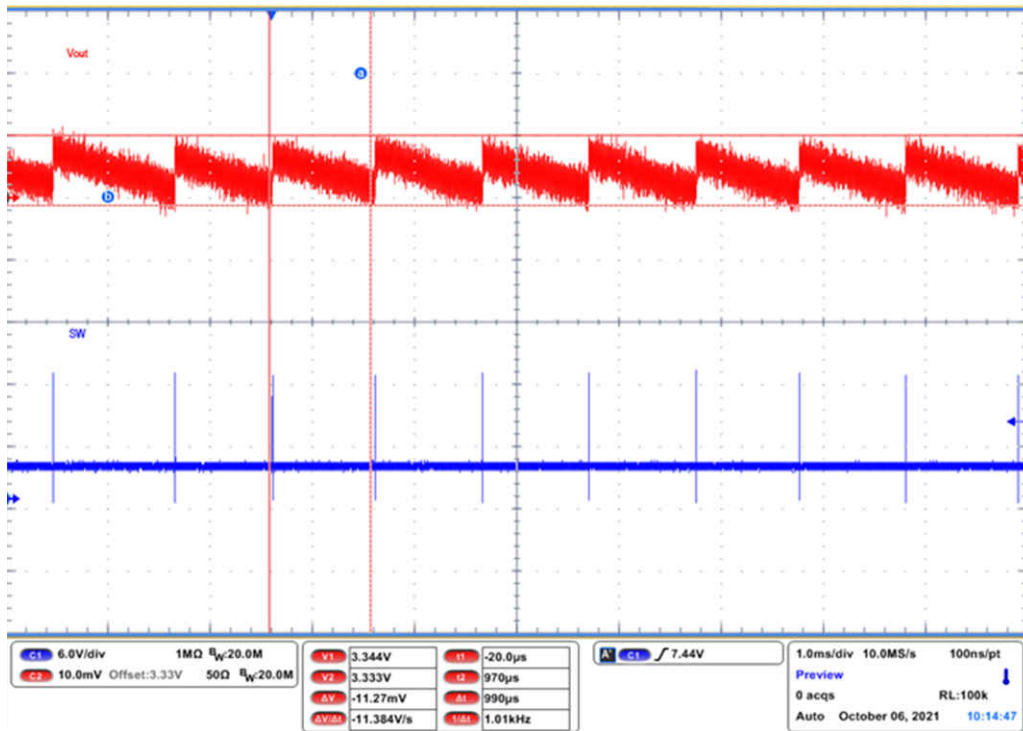
Figure 5-5. Output Voltage Ripple Auto PFM/PWM, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$ = 0 A
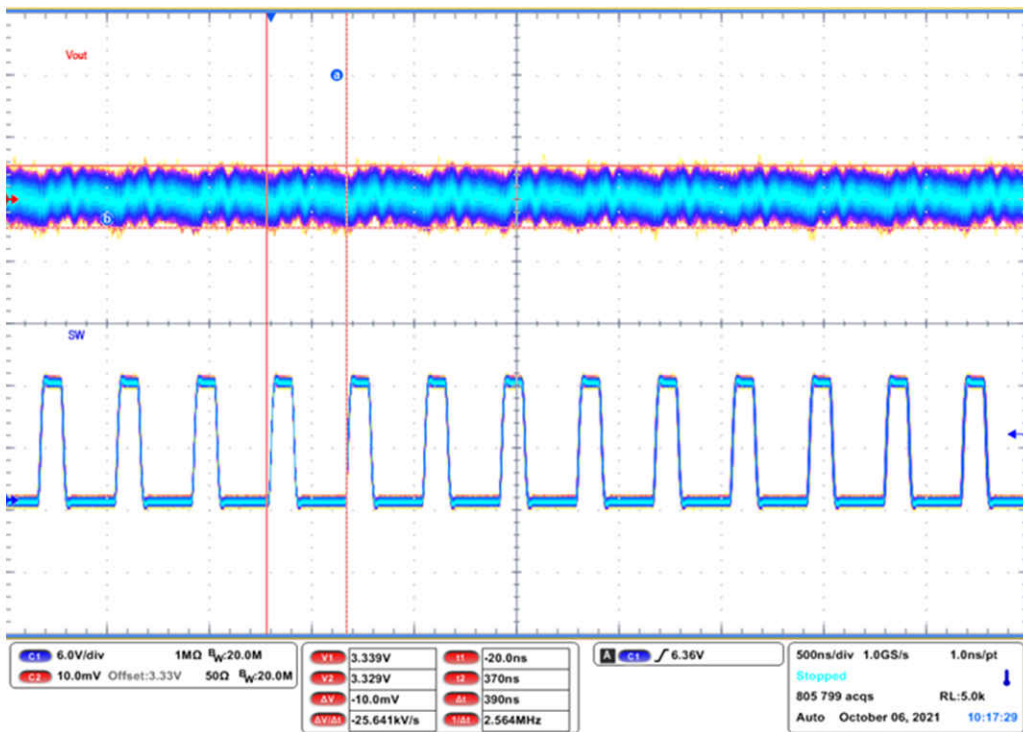
Figure 5-6. Output Voltage Ripple Forced PWM, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$ = 1 A
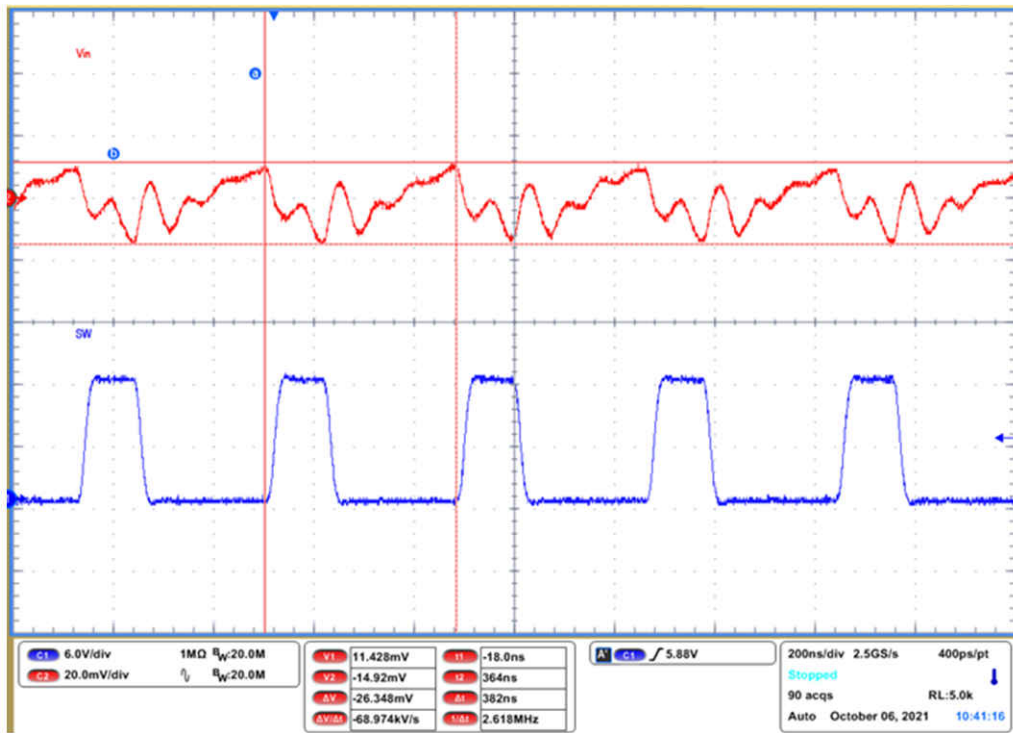
Figure 5-7. Input Voltage Ripple Forced PWM, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$ = 1 A
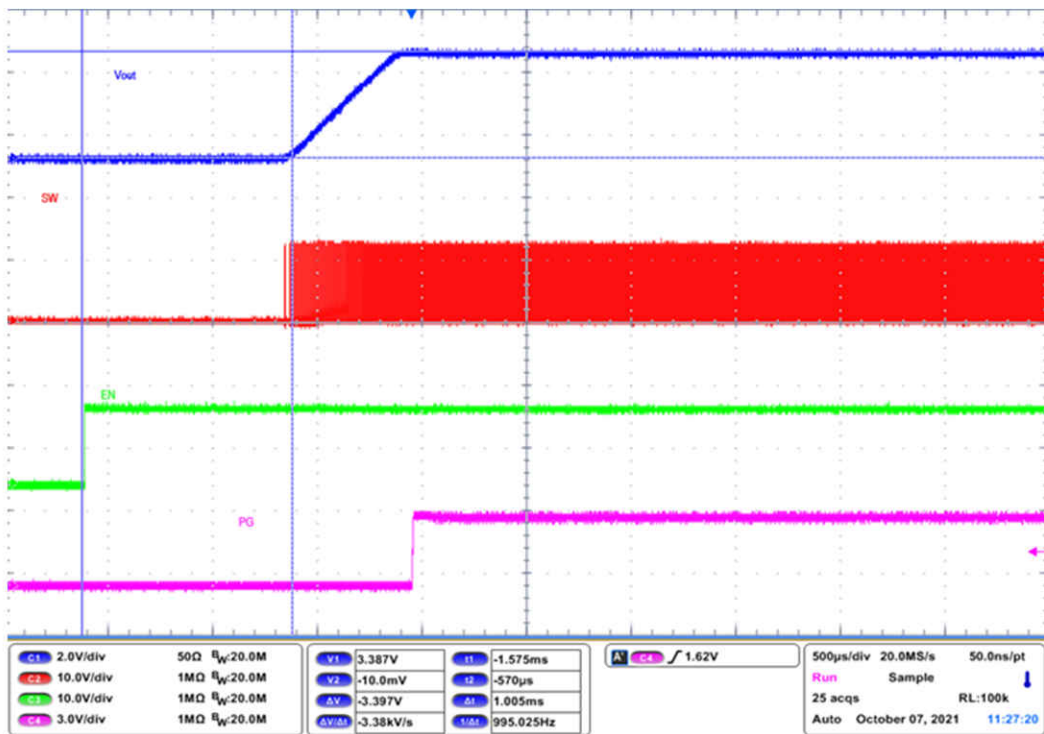
Figure 5-8. Enable Start-Up Forced PWM, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$ = 1 A
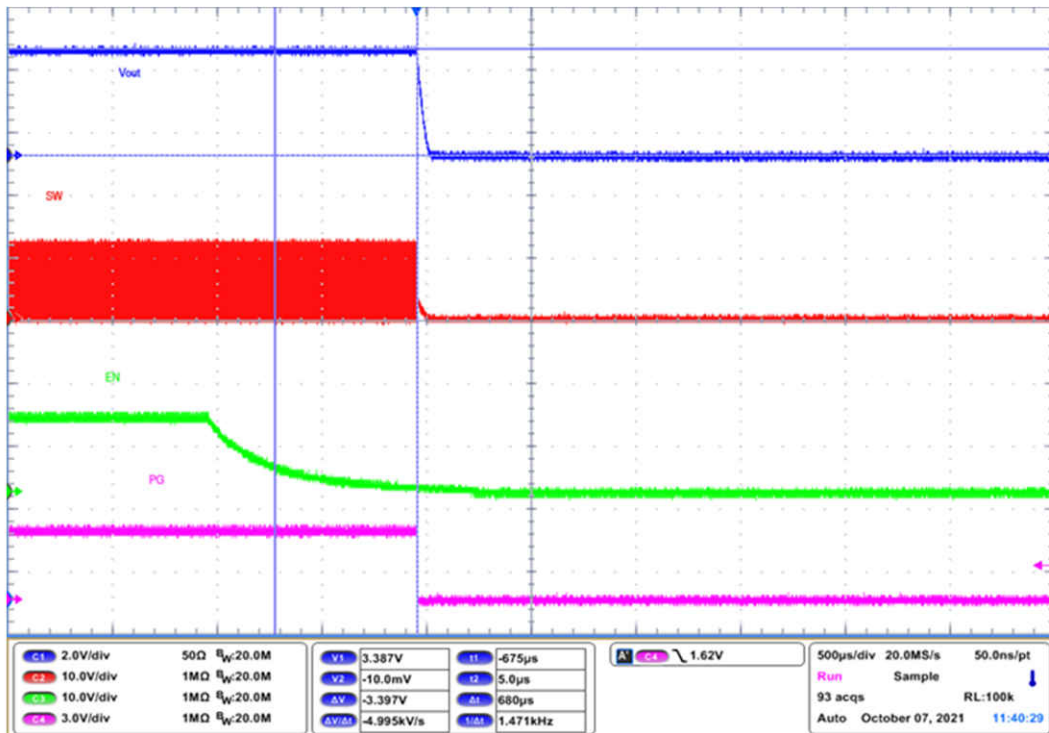
Figure 5-9. Enable Shutdown Forced PWM, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$ = 1 A
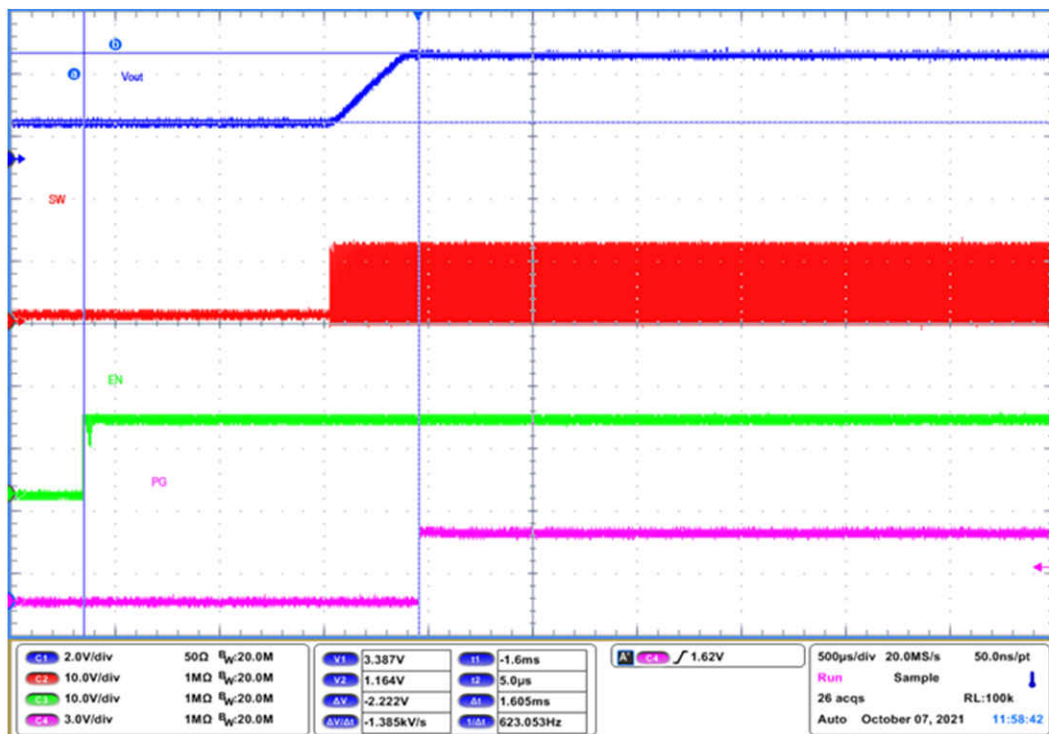
Figure 5-10. Enable Pre-Bias Start-Up Forced PWM, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$ = 0 A
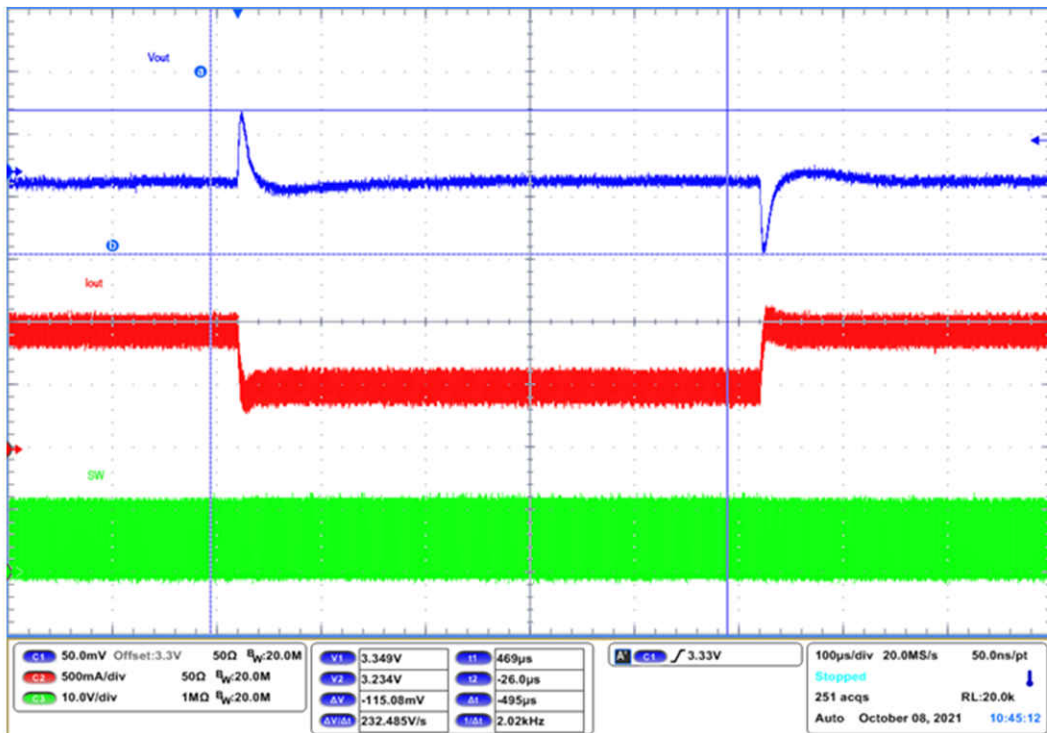
Figure 5-11. Load Transient Forced PWM VSET, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$= 0.5 A–1 A, Slew Rate = 1 A/us
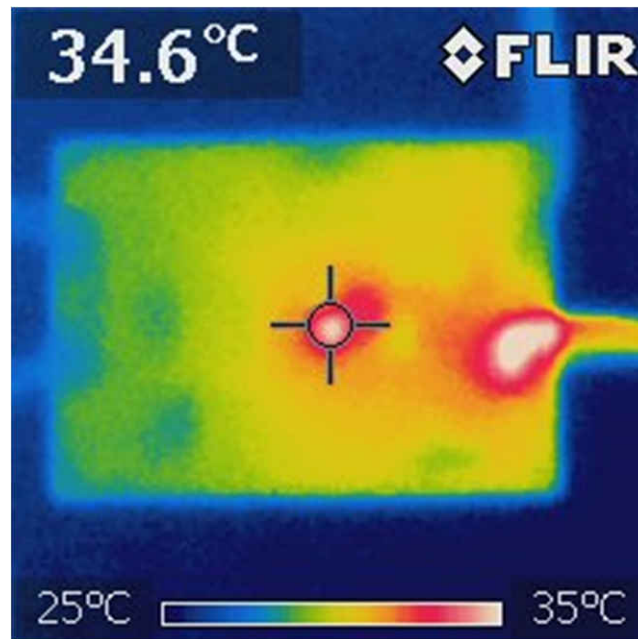
Figure 5-12. Thermal Performance Forced PWM, V$_{IN}$ = 12 V, V$_{OUT}$ = 3.3 V, I$_{OUT}$ = 1 A F$_{SW}$ = 2.5 MHz

6 Board Layout
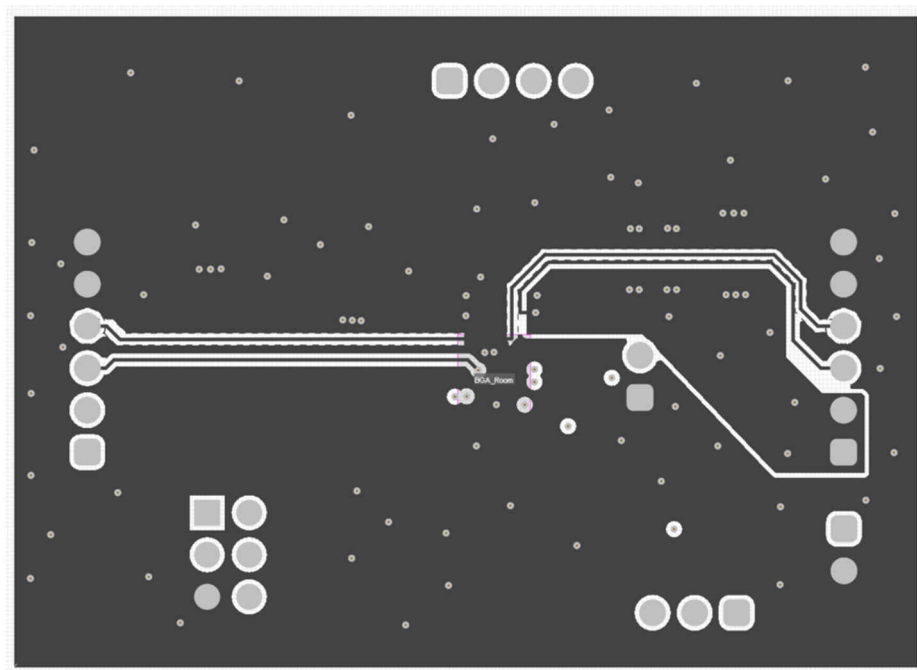
This section provides the EVM board layout and illustrations.
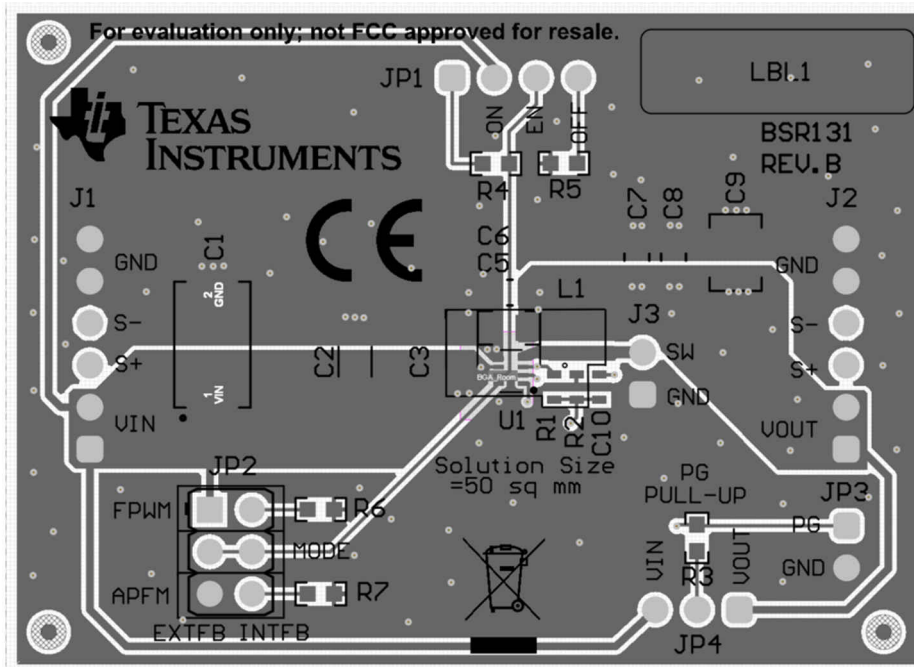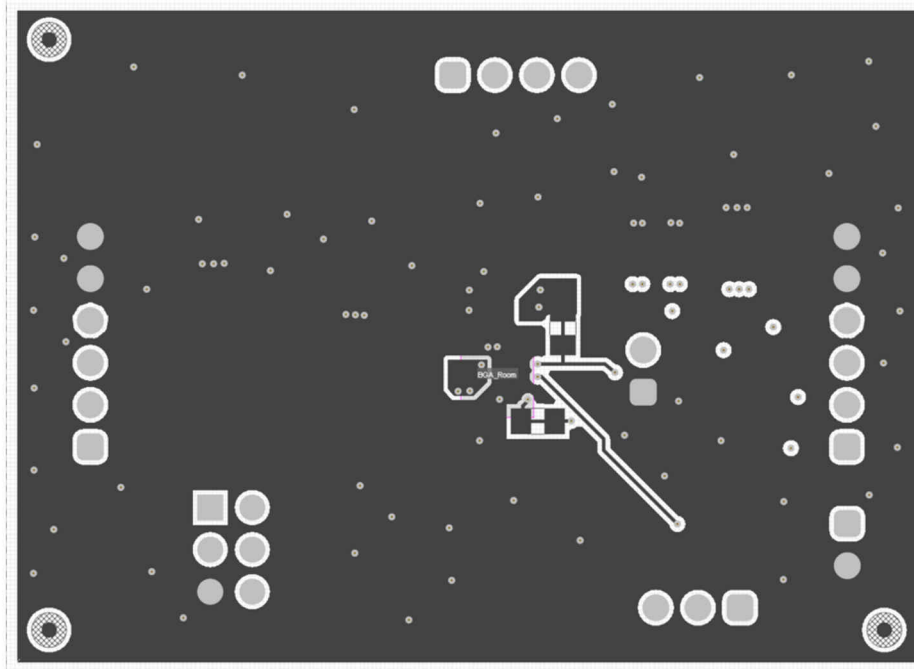

Figure 6-1. Top Assembly
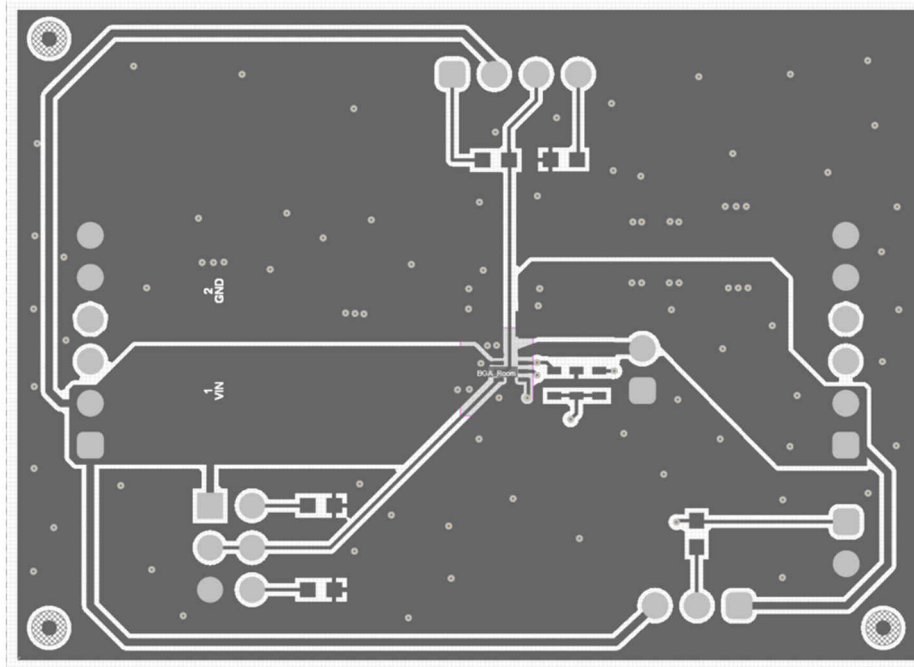
Figure 6-2. Top Layer
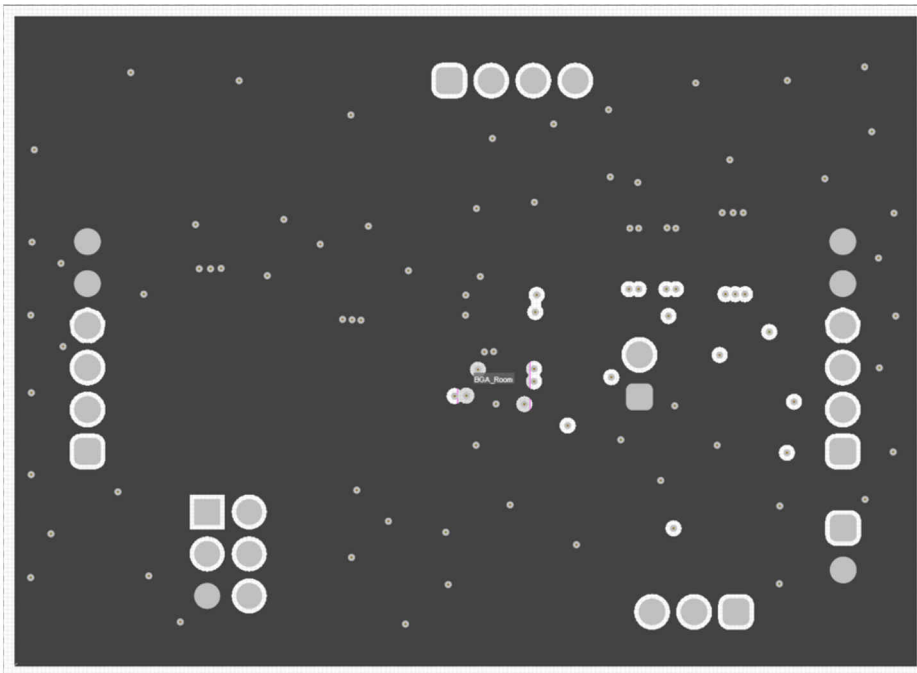
Figure 6-3. Internal Layer 1

Figure 6-4. Internal Layer 2

Figure 6-5. Bottom Layer

7 Schematic and Bill of Materials

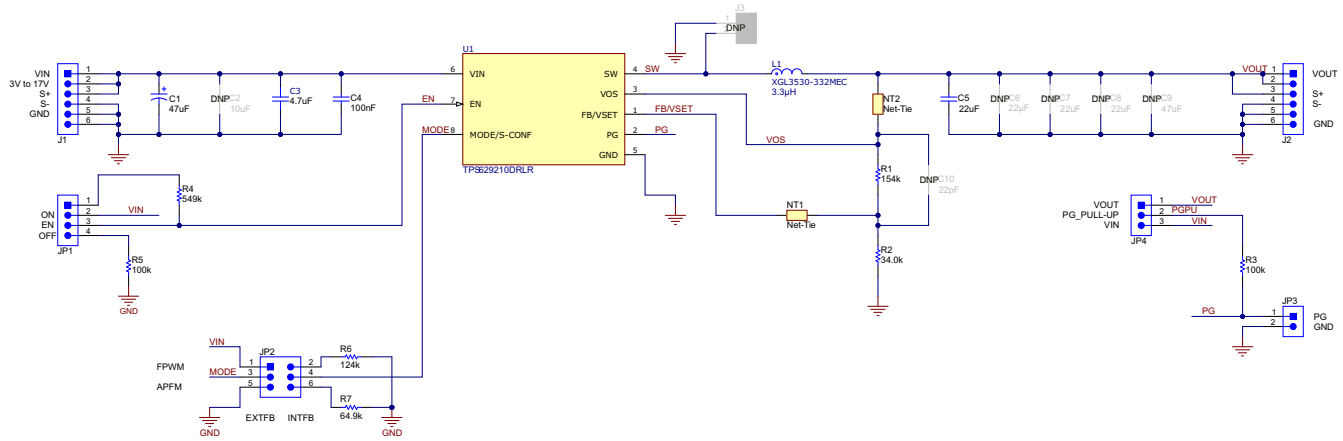This section provides the EVM schematic and bill of materials (BOM).

7.1 Schematic

Figure 7-1. TPS629210EVM Schematic

7.2 Bill of Materials

Table 7-1. TPS629210EVM Bill of Materials

Designator	Qty	Value	Description	Package	Part Number	Manufacturer
C1	1	47 µF	CAP, TA, 47 µF, 35 V, ±10%, 0.3 Ω, SMD	7343-43	T495X476K035ATE300	Kemet
C3	1	4.7µF	Cap Ceramic 4.7 µF 25 V X7R 10% Pad SMD 1206 +125°C Automotive T/R	1206	CGA5L1X7R1E475K160AC	TDK
C4	1	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ±10%, X7R, 0603	0603	C0603C104K3RACTU	Kemet
C5	1	22 µF	CAP, CERM, 22 µF, 6.3 V, ±20%, X7T, AEC-Q200 Grade 1, 0805	0805	GCM21BD70J226ME36L	MuRata
J1, J2	2		Header, 2.54 mm, 6 × 1, Gold, TH	Header, 2.54 mm, 6 × 1, TH	61300611121	Wurth Elektronik
JP1	1		Header, 2.54 mm, 4 × 1, Gold, TH	Header, 2.54 mm, 4 × 1, TH	61300411121	Wurth Elektronik
JP2	1		Header, 2.54 mm, 3 × 2, Gold, TH	Header, 2.54 mm, 3 × 2, Gold, TH	61300621121	Wurth Elektronik
JP3	1		Header, 2.54 mm, 2 × 1, Gold, TH	Header, 2.54 mm, 2 × 1, TH	61300211121	Wurth Elektronik
JP4	1		Header, 2.54 mm, 3 × 1, Gold, TH	Header, 2.54 mm, 2 × 1, TH	61300311121	Wurth Elektronik
L1	1	3.3 µH	Molded Power Inductor, Shielded, 3.3 µH 20%, 5.4A, 37.4-mΩ DCR max, AEC-Q200, T/R	SMT_IND_3MM2_3MM5	XGL3530-332MEC	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll	PCB Label 0.650 × 0.200 inch	THT-14-423-10	Brady
R1	1	154 k	RES, 154 k, 1%, 0.1 W, 0603	0603	RC0603FR-07154KL	Yageo
R2	1	34.0 k	RES, 34.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0734KL	Yageo
R3, R5	2	100 k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo
R4	1	549 k	RES, 549 k, 1%, 0.1 W, 0603	0603	RC0603FR-07549KL	Yageo
R6	1	124 k	RES, 124 k, 1%, 0.1 W, 0603	0603	RC0603FR-07124KL	Yageo
R7	1	64.9 k	RES, 64.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0764K9L	Yageo

Table 7-1. TPS629210EVM Bill of Materials (continued)

Designator	Qty	Value	Description	Package	Part Number	Manufacturer
U1	1		3-V to 17-V, Synchronous Buck Converters in 1.6 mm x 2.1 mm SOT583 Package	SOT583	TPS629210DRLR	Texas Instruments
C2	0	10 µF	CAP, CERM, 10 µF, 25 V, ±20%, X7R, 1206_190	1206_190	C3216X7R1E106M160AE	TDK
C6	0	22 µF	CAP, CERM, 22 µF, 6.3 V, ±20%, X7T, AEC-Q200 Grade 1, 0805	0805	CGA4J1X7T0J226M	TDK
C7, C8	0	22 µF	CAP, CERM, 22 µF, 10 V, ±20%, X7S, 0805	0805	C2012X7S1A226M125AC	TDK
C9	0	47 µF	CAP, CERM, 47 µF, 6.3 V, ±20%, X7R, 1210	1210	GRM32ER70J476ME20L	MuRata
C10	0	22 pF	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H220JA01D	MuRata
J3	0		Header, 2.54 mm, 2 × 1, Gold, TH	Header, 2.54 mm, 2 × 1, TH	61300211121	Wurth Elektronik

8 References

TPS629210 3 V to 17 V, 1-A Low Iq Buck Converter in SOT583 Package Data Sheet

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