ABSTRACT
This user’s guide describes the TPS36Q1EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing and top and bottom board layouts.

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1 Trademarks
All trademarks are the property of their respective owners.
2 Introduction

The TPS36Q1EVM is an evaluation module (EVM) for the TPS3435-Q1, TPS3436-Q1, TPS35-Q1, and TPS36-Q1 voltage supervisors. These families are automotive-grade devices with support for undervoltage supervisor and watchdog functionality. Please see Table 2-1 for specific functions supported by each family. The TPS36Q1EVM is shipped pre-installed with the TPS3436CCCBGDDFRQ1 device, but can be used with any TPS3435-Q1, TPS3436-Q1, TPS35-Q1, or TPS36-Q1 device variant. The TPS3435-Q1, TPS3436-Q1, TPS35-Q1, and TPS36-Q1 families offer multiple pinout options. The TPS36Q1EVM offers connections to all input and output pins supported by various pinouts. Test points are provided to give the user access to an extra ground connection if needed for oscilloscope or multimeter measurements.

Table 2-1. Voltage Supervisors

<table>
<thead>
<tr>
<th>Family</th>
<th>Voltage Supervision</th>
<th>Watchdog</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS3435-Q1</td>
<td>None</td>
<td>Timeout</td>
</tr>
<tr>
<td>TPS3436-Q1</td>
<td>None</td>
<td>Window</td>
</tr>
<tr>
<td>TPS35-Q1</td>
<td>Undervoltage</td>
<td>Timeout</td>
</tr>
<tr>
<td>TPS36-Q1</td>
<td>Undervoltage</td>
<td>Window</td>
</tr>
</tbody>
</table>

Figure 2-1. TPS36Q1EVM Board Top

Figure 2-2. TPS36Q1EVM Board Bottom
2.1 Related Documentation

TPS3435-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet
TPS3436-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet
TPS35-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet
TPS36-Q1 Automotive Nano IQ Precision Watchdog Timer data sheet
3 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TPS36Q1EVM schematic, bill of materials (BOM), and layout.
Figure 3-1. TPS36Q1EVM Schematic
## 3.2 TPS36Q1EVM Bill of Materials

Table 3-1. BOM

<table>
<thead>
<tr>
<th>DESIGNATOR</th>
<th>QUANTITY</th>
<th>VALUE</th>
<th>DESCRIPTION</th>
<th>PACKAGE REFERENCE</th>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB</td>
<td>1</td>
<td></td>
<td>Printed Circuit Board</td>
<td>LP064</td>
<td>0603</td>
<td>Any</td>
</tr>
<tr>
<td>C1</td>
<td>1</td>
<td>0.1 µF</td>
<td>CAP, CERM, 0.1 µF, 16 V, ± 5%, X7R, 0603</td>
<td>C0603C104J4RACTU</td>
<td>Kemet</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>3</td>
<td>0.01 µF</td>
<td>CAP, CERM, 0.01 µF, 25 V, ± 1%, C0G/NP0, 0603</td>
<td>C0603C103F3GACTU</td>
<td>Kemet</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>3</td>
<td>0.01 µF</td>
<td>CAP, CERM, 1 µF, 25 V, ± 10%, X7R, 0603</td>
<td>C0603C105K3RACTU</td>
<td>Kemet</td>
<td></td>
</tr>
<tr>
<td>H1, H2, H3, H4</td>
<td>4</td>
<td></td>
<td>Machine Screw, Round, #4-40 x 1/4, Nylon, Philips Panhead</td>
<td>1002C</td>
<td>NY PMS 440 0025 PH</td>
<td>B&amp;F Fastner Supply</td>
</tr>
<tr>
<td>H5, H6, H7, H8</td>
<td>4</td>
<td></td>
<td>Standoff, Hex, 0.5&quot;L #4-40 Nylon</td>
<td>1002C</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>J1, J2, J3, J5</td>
<td>4</td>
<td>Header, 2.54 mm, 4x2, Tin, SMT</td>
<td>Molex_0015912080</td>
<td>1902C</td>
<td>Molex</td>
<td></td>
</tr>
<tr>
<td>J4</td>
<td>1</td>
<td></td>
<td>Header, 100mil, 3x1, Tin, TH</td>
<td>CONN_PEC03SAAN</td>
<td>PEC03SAAN</td>
<td>Sullins Connector Solutions</td>
</tr>
<tr>
<td>J6</td>
<td>1</td>
<td></td>
<td>Header, 2.54 mm, 2x1, Gold, R/A, SMT</td>
<td>Molex_87898-0204</td>
<td>878980204</td>
<td>Molex</td>
</tr>
<tr>
<td>LBL1</td>
<td>1</td>
<td></td>
<td>Thermal Transfer Printable Labels, 0.650&quot; W x 0.200&quot; H - 10,000 per roll</td>
<td>Label_650x200</td>
<td>THT-14-423-10</td>
<td>Brady</td>
</tr>
<tr>
<td>R1, R2</td>
<td>2</td>
<td>100k</td>
<td>RES, 100 k, 1%, 0.1 W, 0603</td>
<td>0603</td>
<td>RC0603FR-07100KL</td>
<td>Yageo</td>
</tr>
<tr>
<td>TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11</td>
<td>11</td>
<td></td>
<td>Test Point, Compact, SMT</td>
<td>Testpoint_Keystone_Compact</td>
<td>5016</td>
<td>Keystone Electronics</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td></td>
<td>Automotive Nano IQ Precision Watchdog Timer SOT-23-8</td>
<td>DDF0008A-MFG</td>
<td>TPS3436CCCBGDDFR_Q1</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>FID1, FID2, FID3</td>
<td>0</td>
<td></td>
<td>Fiducial mark. There is nothing to buy or mount.</td>
<td>Fiducial10-30</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>
3.3 Layout and Component Placement

Figure 3-2 and Figure 3-3 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 3-4 and Figure 3-5 show the top and bottom layouts, Figure 3-6 and Figure 3-7 show the top and bottom layers, and Figure 3-8 shows the top solder mask of the EVM.
Figure 3-8. Top Solder Mask
4 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM.

4.1 EVM Jumpers

Tables 4-1, 4-2, 4-3, and 4-4 list the default jumper connections and functional descriptions for each device configuration. Each pinout configuration detailed in this section applies to all TPS3435-Q1, TPS3436-Q1, TPS35-Q1, and TPS36-Q1 device families. Please note that for pinouts A, B and C, Pin 7 refers to RESET for the TPS35-Q1 and TPS36-Q1 devices and WDO for the TPS3435-Q1 and TPS3436-Q1 devices.

Table 4-1. Pinout A Onboard Jumpers

<table>
<thead>
<tr>
<th>PIN NUMBER / NAME</th>
<th>JUMPER CONNECTION</th>
<th>DEFAULT CONNECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1 / MR</td>
<td>J1</td>
<td>Closed (pin 7, pin 8)</td>
<td>Jumper J1 configures the MR pin. Connect a shunt jumper to pins 7-8 of jumper J1 to enable the device (logic high) or to pins 5-6 to disable the device (logic low).</td>
</tr>
<tr>
<td>Pin 2 / CWD</td>
<td>J2</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J2 configures the CWD pin. Connect a shunt jumper to pins 7-8 to connect to V_{DD}, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.8 CWD and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.</td>
</tr>
<tr>
<td>Pin 3 / CRST</td>
<td>J3</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J3 configures the CRST pin. Connect a shunt jumper to pins 7-8 to connect to V_{DD}, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.7 CRST and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.</td>
</tr>
<tr>
<td>Pin 5 / SET0</td>
<td>J4</td>
<td>Closed (pin 2, pin 3)</td>
<td>Jumper J4 configures the SET0 pin. Connect a shunt jumper to pins 1-2 of jumper J3 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.</td>
</tr>
<tr>
<td>Pin 6 / WDI</td>
<td>J5</td>
<td>Closed (pin 3, pin 4)</td>
<td>Jumper J5 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for RESET/WDO to not assert.</td>
</tr>
<tr>
<td>Pin 7 / RESET / WDO</td>
<td>J6</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the RESET output high. Disconnect pins 1-2 if using a push-pull variant.</td>
</tr>
</tbody>
</table>
### Table 4-2. Pinout B Onboard Jumpers

<table>
<thead>
<tr>
<th>PIN NUMBER / NAME</th>
<th>JUMPER CONNECTION</th>
<th>DEFAULT CONNECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1 / SET0</td>
<td>J1</td>
<td>Closed (pin 5, pin 6)</td>
<td>Jumper J1 configures the SET0 pin. Connect a shunt jumper to pins 5-6 of jumper J1 to input a logic high or to pins 7-8 to input a logic low. Please refer to the data sheet for SETx functionality.</td>
</tr>
<tr>
<td>Pin 2 / CWD</td>
<td>J2</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J2 configures the CWD pin. Connect a shunt jumper to pins 7-8 to connect to $V_{DD}$, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.8 CWD and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.</td>
</tr>
<tr>
<td>Pin 3 / CRST</td>
<td>J3</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J3 configures the CRST pin. Connect a shunt jumper to pins 7-8 to connect to $V_{DD}$, pins 3-4 to connect to C6, and pins 1-2 to connect to C7. Refer to 5.7 CRST and the data sheet for more details on watchdog timeout periods. Do not connect to pins 5-6 in this configuration.</td>
</tr>
<tr>
<td>Pin 5 / SET1</td>
<td>J4</td>
<td>Closed (pin 2, pin 3)</td>
<td>Jumper J4 configures the SET1 pin. Connect a shunt jumper to pins 1-2 of jumper J4 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.</td>
</tr>
<tr>
<td>Pin 6 / WDI</td>
<td>J5</td>
<td>Closed (pin 3, pin 4)</td>
<td>Jumper J5 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for $RESET/WDO$ to not assert.</td>
</tr>
<tr>
<td>Pin 7 / $RESET/WDO$</td>
<td>J6</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the $RESET$ output high. Disconnect pins 1-2 if using a push-pull variant.</td>
</tr>
</tbody>
</table>

### Table 4-3. Pinout C Onboard Jumpers

<table>
<thead>
<tr>
<th>PIN NUMBER / NAME</th>
<th>JUMPER CONNECTION</th>
<th>DEFAULT CONNECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1 / SET0</td>
<td>J1</td>
<td>Closed (pin 5, pin 6)</td>
<td>Jumper J1 configures the SET0 pin. Connect a shunt jumper to pins 5-6 of jumper J1 to input a logic high or to pins 7-8 to input a logic low. Please refer to the data sheet for SETx functionality.</td>
</tr>
<tr>
<td>Pin 2 / MR</td>
<td>J2</td>
<td>Closed (pin 7, pin 8)</td>
<td>Jumper J2 configures the MR pin. Connect a shunt jumper to pins 5-6 of jumper J2 to input a logic high or to pins 7-8 to input a logic high.</td>
</tr>
<tr>
<td>Pin 3 / WDI</td>
<td>J3</td>
<td>Closed (pin 7, pin 8)</td>
<td>Jumper J3 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for $RESET/WDO$ to not assert.</td>
</tr>
<tr>
<td>Pin 5 / SET1</td>
<td>J4</td>
<td>Closed (pin 2, pin 3)</td>
<td>Jumper J4 configures the SET1 pin. Connect a shunt jumper to pins 1-2 of jumper J4 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.</td>
</tr>
<tr>
<td>Pin 6 / WD-EN</td>
<td>J5</td>
<td>Closed (pin 5, pin 6)</td>
<td>Jumper J5 configures the WD-EN pin. Connect a shunt jumper to pins 5-6 of jumper J5 to enable the watchdog timer (logic high) and pins 7-8 to disable the watchdog timer (logic low).</td>
</tr>
<tr>
<td>Pin 7 / $RESET/WDO$</td>
<td>J6</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the $RESET$ output high. Disconnect pins 1-2 if using a push-pull variant.</td>
</tr>
</tbody>
</table>
## Table 4-4. Pinout D Onboard Jumpers (TPS35-Q1/TPS36-Q1 Only)

<table>
<thead>
<tr>
<th>PIN NUMBER / NAME</th>
<th>JUMPER CONNECTION</th>
<th>DEFAULT CONNECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1 / SET0</td>
<td>J1</td>
<td>Closed (pin 5, pin 6)</td>
<td>Jumper J1 configures the SET0 pin. Connect a shunt jumper to pins 5-6 of jumper J1 to input a logic high or to pins 7-8 to input a logic low. Please refer to the data sheet for SETx functionality.</td>
</tr>
<tr>
<td>Pin 2 / WD-EN</td>
<td>J2</td>
<td>Closed (pin 7, pin 8)</td>
<td>Jumper J2 configures the WD-EN pin. Connect a shunt jumper to pins 5-6 of jumper J5 to enable the watchdog timer (logic high) and pins 7-8 to disable the watchdog timer (logic low).</td>
</tr>
<tr>
<td>Pin 3 / WDI</td>
<td>J3</td>
<td>Closed (pin 7, pin 8)</td>
<td>Jumper J3 configures the WDI pin. Connect a shunt jumper to pins 7-8 to input a WDI signal through TP3. A rising edge must be occur at this pin during the open window in order for \texttt{RESET/WDO} to not assert.</td>
</tr>
<tr>
<td>Pin 5 / SET1</td>
<td>J4</td>
<td>Closed (pin 2, pin 3)</td>
<td>Jumper J4 configures the SET1 pin. Connect a shunt jumper to pins 1-2 of jumper J4 to input a logic high or to pins 2-3 to input a logic low. Please refer to the data sheet for SETx functionality.</td>
</tr>
<tr>
<td>Pin 6 / WDO</td>
<td>J5</td>
<td>Closed (pin 3, pin 4)</td>
<td>Jumper J5 configures the WDO pin. Connect a shunt jumper to pins 1-2 if using an open-drain variant to activate pull-up resistor R1 and pull the WDO output high. Connect pins 3-4 if using a push-pull variant.</td>
</tr>
<tr>
<td>Pin 7 / RESET</td>
<td>J6</td>
<td>Closed (pin 1, pin 2)</td>
<td>Jumper J6 is used if there is an open-drain variant being evaluated. Connect a shunt jumper to pins 1-2 to activate pull-up resistor R2 and pull the \texttt{RESET} output high. Disconnect pins 1-2 if using a push-pull variant.</td>
</tr>
</tbody>
</table>

### 4.2 EVM Test Points

Test points are placed throughout the board and are used to verify pin functionality. Each device configuration option letter has different pinouts, so each test point can serve different purposes depending on the chosen IC. For example, test point 1 (TP1) is used to monitor pin 1, but the functionality of pin 1 varies between \texttt{MR}, \texttt{SET0}, and \texttt{CWD} as seen in Figure 4-1. Jumpers can be used with shunt jumpers to connect two pins together in order to serve multiple testing purposes. For example, connecting pins 7-8 of jumper J1 connects pin 1 to \texttt{VDD}, a logic high, and connecting pins 5-6 of jumper J1 connects pin 1 to \texttt{GND}, a logic low. Pins can also be connected to delay capacitors via the jumpers, and these connections can be used to adjust programmable timeout periods.
Figure 4-1. Schematic Closeup
5 EVM Setup and Operation

This section describes the functionality and operation of the TPS36Q1EVM. Even though this EVM comes with the TPS3436CCCBGDFRQ1 variant, this section will cover the EVM utilization with the TPS36-Q1, TPS35-Q1, and TPS3435-Q1 installed on the board. All timing based parameters of this device are located in the respective device’s datasheet.

5.1 Input Power (V_DD)

The input voltage (V_DD) is connected through TP8 on the board. The input voltage range is 1.04V to 6.0 V. The TPS35-Q1 and the TPS36-Q1 families offer voltage supervision on the V_DD pin and supervisor output on the RESET pin. The voltage threshold of the supervisor is dependent on the specific device used. Please refer to the datasheet for additional details.

5.2 RESET

For the TPS35-Q1 and TPS36-Q1 options A, B, and C, the RESET pin will assert on either V_DD going below the supervisor threshold, the MR pin being pulled low, or the watchdog detecting a fault. To access the RESET output, a probe can be attached to TP7. For pinout option D devices, supervisor faults are mapped to the RESET pin and watchdog faults are mapped to the WDO pin.

Please note that if using a push-pull output variant, the shunt jumper on J6 must be removed as a pull-up is not needed.

5.3 Manual Reset (MR)

Pinout options A and C support MR functionality. The Manual Reset (MR) can be utilized by either J2 (option C) or J1 (option A) headers. By installing a shunt jumper on pins 5-6 of J1 or J2, the MR pin is connected to ground. Moving the shunt jumper to pins 7-8 will connect the MR pin to V_DD. For the TPS35-Q1 and TPS36-Q1 devices, pulling the MR pin LOW will assert the RESET signal and deassert the WDO signal. For the TPS3435-Q1 and TPS3436-Q1 devices, pulling the MR pin LOW will assert the WDO signal. Pulling the MR pin HIGH will return the RESET and WDO outputs to their deasserted states after the tD time delay.

5.4 SET0 and SET1

The function of the SETx pins will vary based on the device used in the EVM. Please refer to the device data sheet for the functionality. Drive SETx pins to logic 1 (connect to V_DD) or logic 0 (connect to GND) as per the device pinout and functionality requirements. Refer to Tables 4-1, 4-2, 4-3, and 4-4 for suggested jumper connections.

5.5 Watchdog Enable (WD_EN)

The WD_EN pin is only available in option C and D devices. This pin is used to ENABLE (logic 1) or disable (logic 0) the watchdog functionality of the device. To utilize this pin, configure J5, for option C devices, or J2 for option D devices. Refer to Table 4-3 and Table 4-4 for suggested jumper connections.

5.6 Watchdog Input (WDI)

WDI is a falling edge triggered watchdog input. TPS35-Q1 and TPS3435-Q1 devices support timeout watchdog monitor operation, while the TPS36-Q1 and TPS3436-Q1 devices support window watchdog monitor operation. Refer respective data sheet for timing related requirements. Refer to Tables 4-1, 4-2, 4-3, and 4-4 for suggested jumper connections.

5.7 Watchdog Output (WDO)

The WDO output is asserted in the event of a watchdog error. For TPS35-Q1 and TPS36-Q1 devices, the WDO pin is offered in pinout option D. For TPS3435-Q1 and TPS3436-Q1 devices, the WDO pin is offered in options A, B, and C. Refer to Tables 4-1, 4-2, 4-3, and 4-4 for suggested jumper connections.

5.8 CRST

A capacitor between the CRST pin and GND sets the output assert time tD. The TPS36Q1EVM offers two pre-installed options: 0.01µF and 1µF. These capacitors correspond to 49.5ms and 4.95s tD time delays, respectively. Refer to Table 4-1 and Table 4-2 for suggested jumper settings. If other timing option is needed,
the capacitor may be replaced. Refer to the respective device data sheet to determine the capacitor value for required timing.

5.9 CWD

A capacitor between the CWD pin and GND sets the watchdog timeout period \( t_{WD} \) for TPS35-Q1 and TPS3435-Q1 devices or the watchdog close window period \( t_{WC} \) for TPS36-Q1 and TPS3436-Q1 devices. The TPS36Q1EVM offers two pre-installed options: 0.01\( \mu \)F and 1\( \mu \). These capacitors correspond to 49.5ms and 4.95s \( t_{WD} \) time delays for the TPS35-Q1 and TPS3435-Q1 devices, respectively. The \( t_{WD} \) values are determined by the SET0 and SET1 pins; please refer to Table 5-1 for a list of the values and the data sheet for the \( t_{WD} \) calculation. Refer to Table 4-1 and Table 4-2 for suggested jumper settings. If other timing option is needed, the capacitor can be replaced. Refer to the respective device data sheet to determine the capacitor value for required timing.

Table 5-1. Typical \( t_{WC} \) Values for TPS36-Q1 and TPS3436-Q1

<table>
<thead>
<tr>
<th>SET0</th>
<th>SET1</th>
<th>0.01( \mu )F</th>
<th>1( \mu )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0.792s</td>
<td>79.2s</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0.396s</td>
<td>39.6s</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Disabled/&quot;00&quot; if using Pinouts C or D</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0.099s</td>
<td>9.9s</td>
</tr>
</tbody>
</table>
6 EVM Performance Results

The following measurements are taken using the TPS3436CCCBGDDFRQ1 with SET0=0 and SET1=0.

Figure 6-1. Early Fault

Figure 6-2. Late Fault
Figure 6-3. Valid Pulse

Figure 6-4. Startup Delay
### 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>October 2022</td>
<td>*</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>
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3.1 United States

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FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.
Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan.
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 Safety-Related Warnings and Restrictions:

4.3.1 User shall operate the EVM within TI’s recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designers. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designers.

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