

## ABSTRACT

The TPS65219 family of power management integrated circuits (PMICs) includes a configurable non-volatile memory (NVM) space. This programmer's guide details the step by step instructions to define the PMIC default configuration and how to reprogram the NVM.

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The configuration process described in this document writes to the NVM space and is intended to be used in a production line or prototype board. This mechanism is not intended to be used in final applications because the process impacts the regulator outputs and the function of digital pins. The TPS6521905 is an orderable part number, part of the TPS65219 family, created specifically to support custom NVM configuration. Table 1-1 shows the user-programmable variants and the supported package size, temperature, and switching mode. Figure 1-1 describes the supply options for pre-configured and custom NVMs based on volume. Design resources are available not only for pre-configured and high volume NVMs, but also for low volume custom NVMs. These resources can include application notes, user's guides, technical reference manuals, and NVM configuration files ready to be loaded into the PMIC NVM. Visit the TPS6521905 product page on ti.com or use our PMIC E2E forum to ask about available resources.

Note

To support NVM programming, TI offers two socketed EVMs, one for each package size. **TPS65219EVM-SKT** is the orderable part number for the 5x5 socketed EVM and **TPS65219EVM-RSM** is the orderable part number for the 4x4 socketed EVM.

OPN	Package	Temperature	Switching Frequency Supported
TPS6521905RHBR	RHB - 5x5 (0.5mm pitch)	Ta = -40C to 105C Tj = -40C to 125C	Quasi-Fixed Frequency (auto-PFM and forced-PWM)
TPS6521905RSMR	RSM - 4x4 (0.4mm pitch)	Ta = -40C to 105C Tj = -40C to 125C	Quasi-Fixed Frequency (auto-PFM and forced-PWM)
TPS6521905WRHBRQ1	RHB - 5x5 (0.5mm pitch) Wettable Flank	Ta = -40C to 125C Tj = -40C to 150C	Quasi-Fixed Frequency (auto-PFM and forced-PWM)
Available Upon Request	RHB - 5x5 (0.5mm pitch) Wettable Flank	Ta = -40C to 125C Tj = -40C to 150C	Fixed Frequency (recommended for applications that require best EMI control. Spread spectrum and out-of-phase switching are available)

#### Table 1-1. TPS65219 User-Programmable variants









## 2 Hardware Requirements for NVM Programming

The PMIC has two memory spaces, the register map space and the NVM space. Re-programming the NVM is done by first writing to the register map through the serial interface (I2C) and then saving the register settings into the NVM. Because the configuration first involves writing to the register map, which controls the regulator and digital pins, there must be no dependency or need to use the PMIC resources. For example, an external power supply must be used to supply the pull-up resistors of the I2C pins instead of using one of the PMIC power resources while reprogramming the NVM. Table 2-1 and Figure 2-1 show the minimum hardware requirements for the hardware setup between the PMIC and the programming device.

Note

Other external components like inductors, capacitors, and so on are not needed to re-program the NVM in Initialize state. However, those components are needed for the PMIC operation in Active state and to validate NVM settings.

Device pin	Required Connections							
VSYS	VSYS voltage must be 3.3V or higher without exceeding the maximum recommended voltage in the spec.							
	VSYS must have a minimum of 2.2uF capacitance.							
VDD1P8	VDD1P8 must have a 2.2uF capacitance							
I2C pins	Pull-up resistors on I2C pins (SDA/SCL) must be supplied by external 3.3V supply.							
	I2C pins of the PMIC must be driven by an external I2C device that can communicate with the PMIC and write to the registers.							
EN/PB/VSENSE	EN/PB/VSENSE pin must be connected to VSYS with a pull-up resistor.							
AGND	AGND (pin# 15) must be connected to the PCB ground planes through a VIA . Keep the trace from the AGDN pin to the VIA short.							
Thermal Pad	The package thermal pad must be connected to the PCB ground plane with a minimum of nine VIAS.							

Table 2	-1	Minimum	Hardware	Roa	uiromonte	for	NVM	Programmi	na
		wiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiiii	Ilaluwale	NEY	unements	101		FIUgrammi	пy



Figure 2-1. Hardware Setup for NVM Programming



## **3 Typical NVM Flow**

This section describes the typical NVM definition flow which consists of the following steps: System requirements, Hardware setup, NVM programming and Test/Validation.

### 1. System Requirements

Identify the system requirements and build a power distribution network (PDN). Voltage/Current, power-up/ power-down sequence, low power modes, and load transient are typical requirements from processors, SoCs and peripherals.

### 2. Hardware Setup

The TPS65219 can be programmed using the PMIC socketed EVM, a customer prototype board (in-circuit programming), or production line.

 Socketed EVM: The PMIC socketed EVM comes with an onboard MSP340 that can communicate with the PMIC through I2C to re-program the NVM memory. This hardware also integrates a discrete 3.3V LDO that can supply the I2C pull-up resistors while the PMIC rails are OFF in Initialize state.



### Figure 3-1. Socketed EVM

Prototype board: The user-programmable TPS6521905 NVM comes with all the power resources inactive by default and the EN/PB/VSENSE pin configured as push-button with without FSD (PU\_ON\_FSD = 0x0). If this pin is pulled up to VSYS, PMIC stays OFF (Initialize state) when a valid supply is connected to VSYS. This configuration allows the reprogramming of the NVM before the power-up sequence is executed. Figure 3-2 shows what customers need to include in the prototype board to re-program the PMIC NVM. The components required include three test points on GND, SCL, SDA, and a 1x3 single row header connector that selects the pull-up supply between the external 3.3V and the PMIC rail that supplies the I2C pins in the normal application. The USB2ANY (available at ti.com) can be used to communicate with the PMIC and re-program the NVM settings.





Figure 3-2. Prototype Example

### Note

See section "Specifications" and "Detailed Design Procedure" in the data sheet for information about recommended external components like inductors, output capacitance, and so on.

 Production line: PMIC NVM can also be re-programmed in a production line following the Figure 2-1 before soldering the device into the final PCB.

### 3. NVM Programming

Follow the programming instructions in Section 4 to change the register settings and save the new values into the NVM memory. The TPS65219-GUI can be used with the socketed EVM (or a prototype board plus an external USB2ANY). Alternatively, customers can use their preferred I2C debugger tool to write to each of the NVM registers without using the TPS65219-GUI. Once the NVM is re-programmed, it is recommended to perform a power cycle to confirm the new register settings were saved into the NVM memory.

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	File	Opt	ions Ioois Heip						
	A	፰ Configuration - NVM fields							
Full Register Map	٥	READ	ALL REGISTERS Note: Ch	hanging the value in a drop	down menu will cause	an immed	liate I2C write to th		
(includes NVM and non-NVM bits)	/		PMIC Status	Power R	Resources		Digital Pins		
NVM register fields	-	B	Bucks Switching Mode		Buck1				
	ŗ	C	Switching Mode Qua Note: Default Switching M should not be changed.	asi-fixed frequency 🛩	Buck1_EN BUCK1_STBY_EN	Enable Enable	ed in Active state ed in Standby stal		
Programming steps	~	s	Spread Spectrum Disa Note: Spread Spectrum se when Bucks configured fo	abled  v etting has no effect or quasi-fixed frequency	Output Voltage UV monitor Bandwidth	0.750\ -5% U high b	V V andwidth		
		L	LDO1			LDO2			
		0 s	LDO1_EN E LDO1_STBY_EN E	Enabled in Active state V		LDO2_EI	N E TBY_EN E		
			UV monitor _ LDO1_LSW_CONFIG _	-5% UV	is Load-Switch 🗸	UV monit	tor _t SW_CONFIG 0		
			Referen	1 - LDO1 configured as Byp	002 Configuratio	n	YP_CONFIG 0		
			LDOx_LSW_CONFIG	LDC	Dx_BYP_CONFIG		Configuration		
			0		0		LDO		
			0		1		Bypass		
			1		X		Load-Switch		

### Figure 3-3. TPS65219-GUI

#### 4. NVM Testing

NVM settings must be tested to confirm expected PMIC behavior. The list below shows the minimum recommended tests. These tests can be performed in the socketed EVM or prototype board. If the socketed EVM was used to re-program the PMIC, the devices can be soldered down into the customer prototype board to test and validate system level functionality. Alternatively, the PMIC on the soldered down TPS65219EVM can be replaced to test a custom NVM configuration.

- · Measure all output voltages
- Collect scope waveform for power-up sequence (include GPIOs if enabled and nRSTOUT)
- Collect scope waveform for power-down sequence (include GPIOs if enabled and nRSTOUT)
- Test EN/PB/VSENSE pin function and polarity to trigger ON and OFF request.
- Test each multi-function pin (VSEL, MODE/STBY, MODE/RESET) configuration and polarity. Pull this pin high or low and verify if PMIC behavior changes according to the configured pin function.

#### Note

The socketed EVM can be used for re-programming and basic tests (For example: measuring output voltages, colleting power-up sequence waveforms, and so on) but must not be used to test specific performance parameters like load transient and efficiency because the socket pogo pins and layout placement introduce higher parasitic that do not represent the design of a real application.



## **4 Programming Instructions**

This section describes the steps required to program the PMIC NVM. The programming process consists of two primarily steps; changing the register settings and saving the new values into the NVM memory. TI recommends programming the NVM in Initialize state, where VSYS is supplied but all of the PMIC outputs and monitors are OFF.

Figure 4-1 shows the steps to reprogram the device. The first command consists of an I2C OFF request to send the device to Initialize state. This command is only needed if the device is not in Initialize state. The second I2C command enables an internal oscillator for I2C communication and disables the rails discharge. The third step requires updating register settings to match specific application requirements following the programming instructions. After the register settings are updated, the new values can be saved into the NVM by writing 0x0A to register address 0x34. The last step "Validation" is optional and consists of an I2C command that compares register settings with NVM content.

#### Note

The first I2C command (I2C OFF request) is only needed if the PMIC is not in Initialize state. The user programmable OPN TPS6521905 comes with the EN/PB/VSENSE pin configured as "push-button" with the FSD feature disabled by default. When configured as PB, the device detects an ON-request when the pin is pulled low. If this pin has a pull-up to VSYS, then PMIC stays in Initialize state after VSYS is supplied. To verify if I2C communication is available in Initialize state, it is recommended to read the NVM ID register on address 0x01. The read back matches the two digits after the "TPS65219" in the part number. For example, when using TPS6521905, register 0x01 reads 05.

1 Send I2C OFF Request	Register Address: 0x29 Data: 0x01 (I2C_OFF_REQ)
2 Enable I2C Communication	Register Address: 0x34 Data: 0x09 (EN_OSC_DIY)
3 Update register settings	This step requires updating the correct register settings to match specific application regquirements
4 NVM Programming	Register Address: 0x34 Data: 0x0A (EN_OSC_DIY)
5 NVM Validation	Register Address: 0x34 Data: 0x07 (EN_OSC_DIY)

### Figure 4-1. NVM Programming

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## 4.1 Configuring Enable Settings

The PMIC has an Active and Standby state where rails can be enabled or disabled. The state change can be triggered by the MODE/STBY pin when configured as STBY.

- Figure 4-2 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-1 show the register fields to be written when NOT using the TPS65219-GUI.

<b>f</b>	=	Configuration - NVM fi	elds														
۵	READ ALL REGISTERS Note: Changing the value in a dropdown menu will cause an immediate I2C write to the associated register unless immediate write setting is changed on Register Map page.																
				Power	Resources			Sequence									
;	B U C	Bucks Switching Mode Switching Mode Quasi-fixed fre Note: Default Switching Mode config	equency V	Buck1_EN	Disabled	d in Active state	~	Buck2 Buck2_EN BUCK2_STBY_EN	Disabled in Ac	tive state 🗸	Bucks Bucks	3 6_EN 3 STBY EN	Disabled in Act	ive state 🗸			
	K s	should not be changed. Spread Spectrum Disabled	~	Output Voltage	0.600V	a in Standby Stat	~	Output Voltage	0.600V		Outpu UV m	it Voltage onitor	0.600V	v v			
		Note: Spread Spectrum setting has r when Bucks configured for quasi-fixe	no effect ed frequency	Bandwidth	low band	dwidth	~	Bandwidth Phase Config	low bandwidth 0 degrees	*	Bandy Phase	width e Config	low bandwidth 0 degrees	~			
	L D	LDO1			LDO2					LDO3				LDO4			
	0	LDO1_EN Disabled in	Active state 🗸		LDO2_EN	Di	isable	d in Active state 🐱		LDO3_EN		Disabled in A	ctive state 🗸	LDO4_EN	Disabled in Activ	ve state 🗸	
	s	Output Voltage 0.600V	Standby stat ~		Output Volta	tage 0.6	isableo 600V	d in Standby stat ~		Output Volt	age	Disabled in S 1.200V	tandby stat ~	Output Voltage	Disabled in Star	dby stat ~	
		UV monitor -5% UV	~		UV monitor	-5'	i% UV	~		UV monitor		-5% UV	~	UV monitor	-5% UV	~	
		LDO1_LSW_CONFIG 0 - LDO1 N	IOT configured as	Load-Switch 🗸	LDO2_LSW	V_CONFIG 0.	- LDO	2 NOT configured as Lo	ad-Switch 🗸	Configuration	on	LDO Mode	~	Configuration	LDO Mode	~	
		LD01_BYP_CONFIG 0 - LD01 or	onfigured as LDO	~	LDO2_BYP	CONFIG 0.	- LDO	2 configured as LDO	~	Power-op i	Ramp	Fast ramp	~	Power-Up Ramp	Fast ramp	~	
		Reference for L	DO1 and LD	02 Configuration	on												
		LDOx_LSW_CONFIG	LDO	x_BYP_CONFIG	с	Configuration											
		0		0		LDO											
		0		1		Bypass											
		1		х	9	Load-Switch											



#### Table 4-1. NVM Registers for Enable Settings

	Pogistor Address		Bit	Sottings
	Register Address	Bit #	Field Name	Settings
Enable rails in Active state	0x02	6	LDO4_EN	0h = Disabled 1h = Enabled
		5	LDO3_EN	0h = Disabled 1h = Enabled
		4	LDO2_EN	0h = Disabled 1h = Enabled
		3	LDO1_EN	0h = Disabled 1h = Enabled
		2	BUCK3_EN	0h = Disabled 1h = Enabled
		1	BUCK2_EN	0h = Disabled 1h = Enabled
		0	BUCK1_EN	0h = Disabled 1h = Enabled

	Deviator Address	Bit		Sottingo
	Register Address	Bit #	Field Name	Settings
Enable rails in Standby state	0x21	6	LDO4_STBY_EN	0h = Disabled 1h = Enabled
		5	LDO3_STBY_EN	0h = Disabled 1h = Enabled
		4	LDO2_STBY_EN	0h = Disabled 1h = Enabled
		3	LDO1_STBY_EN	0h = Disabled 1h = Enabled
		2	BUCK3_STBY_EN	0h = Disabled 1h = Enabled
		1	BUCK2_STBY_EN	0h = Disabled 1h = Enabled
		0	BUCK1_STBY_EN	0h = Disabled 1h = Enabled

#### Table 4-1. NVM Registers for Enable Settings (continued)

## 4.2 Configuring the Bucks

There are several settings that can be programmed for the Buck converters. These include the output voltages, under voltage (UV) monitoring, and bandwidth among others.

- Figure 4-3 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-2, Table 4-3, Table 4-4 and Table 4-5 show the register fields to be written when NOT using the TPS65219-GUI.

*	Configuration - NVM fields
	- Configuration - Ny IN ficius

۵	READ /	ALL REGISTERS Note: C	Changing the valu	ue in a dropdo	wn menu will cause	an immedia	ate I2C write to t	the as	sociated register unless ir	nmediate write s	etting is chang	ed on Register Map pa	ge.				
/		PMIC Status			Power	Resource	s		Sequence			Di	gital Pins Configu	ration			Mask Setting
8	В	Bucks Switching Mod	le		Buck1				Buck2			Buck3					
ŗ	C K s	Switching Mode Note: Default Switching should not be changed. Spread Spectrum	Quasi-fixed freque g Mode configura Sisabled In setting has no e for quasi-fixed f	ency V tion	Buck1_EN BUCK1_STBY_E Output Voltage UV monitor Bandwidth	Disable N Disable 0.600V -5% U Iow ba	led in Active stat led in Standby sl V V andwidth	te v tat v v	Buck2_EN BUCK2_STBY_EN Output Voltage UV monitor Bandwidth Phase Config	Disabled in Ac Disabled in St 0.600V -5% UV Iow bandwidth 0 degrees	tive state v andby stat v v i v	Buck3_EN BUCK3_STBY_EN Output Voltage UV monitor Bandwidth Phase Config	Disabled in Ac Disabled in Sta 0.600V -5% UV Iow bandwidth 0 degrees	andby stat			
	L D S	LDO1_EN LDO1_STBY_EN Output Voltage UV monitor LDO1_LSW_CONFIG LDO1_BYP_CONFIG	Disabled in Ac Disabled in Sta 0.600V -5% UV 0 - LDO1 NOT 0 - LDO1 confi	tive state   andby stat	Load-Switch V	LDO2_EP LDO2_S <sup>2</sup> Output V0 UV monit LDO2_LS LDO2_B <sup>3</sup>	N [ TBY_EN [ foltage [ tor [ SW_CONFIG ] YP_CONFIG [	Disat Disat 0.600 -5% I 0 - LI	bled in Active state  bled in Standby stat  bled in Standby stat	pad-Switch ♥	LDO3_EN LDO3_EN LDO3_STI Output Vol UV monito Configurat Power-Up	Disabled in / Disabled in 1 1.200V r -5% UV on LDO Mode Ramp Fast ramp	Active state   Standby stat	LDO4_EN LDO4_EN LDO4_STBY_ Output Voltag UV monitor Configuration Power-Up Ra	_EN D ge 1 - amp F	isabled in Active s isabled in Standby 200V 5% UV DO Mode ast ramp	tate × v stat × v
		Refere	ence for LDO G	D1 and LD	O2 Configuratio	on	Configuration	'n									
		0			0 1 X		LDO Bypass	_									

#### Figure 4-3. Bucks Settings Using the TPS65219-GUI



#### Table 4-2. NVM Registers for Buck1 Configuration

	Pogistor Address		Bit	Sottings	
	Register Address	Bit # Field Name		Settings	
Bandwidth	0x0A	7	BUCK1_BW_SEL	0h = low bandwidth 1h = high bandwidth	
UV monitoring		6	BUCK1_UV_THR_SEL	0h = -5% UV detection level 1h = -10% UV detection level	
Output Voltage		5-0	BUCK1_VSET	see register map on data sheet	

#### Table 4-3. NVM Registers for Buck2 Configuration

	Desister Address		Bit	Sottingo	
	Register Address	Bit #	Field Name	Settings	
Bandwidth	0x09	7	BUCK2_BW_SEL	0h = low bandwidth 1h = high bandwidth	
UV monitoring		6	BUCK2_UV_THR_SEL	0h = -5% UV detection level 1h = -10% UV detection level	
Output Voltage		5-0	BUCK2_VSET	see register map on data sheet	

#### Table 4-4. NVM Registers for Buck3 Configuration

	Pogistor Address		Bit	Settings	
	Register Address	Bit #	Field Name		
Bandwidth	0x08	7	BUCK3_BW_SEL	0h = low bandwidth 1h = high bandwidth	
UV monitoring		6	BUCK3_UV_THR_SEL	0h = -5% UV detection level 1h = -10% UV detection level	
Output Voltage		5-0	BUCK3_VSET	see register map on data sheet	

#### Table 4-5. NVM Registers for Switching Mode (Only Applicable if BUCK\_FF\_ENABLE = 1h)

	Register Address		Bit	Settings	
		Bit #	Field Name		
Spread Spectrum	0x03	5	BUCK_SS_ENABLE	0h = Spread spectrum disabled 1h = Spread spectrum enabled	
Switching Mode		4	BUCK_FF_ENABLE	DO NOT CHANGE THIS BIT	
Buck2/Buck3 phase config		3-2	BUCK3_PHASE_CONFIG	0h = 0 degrees 1h = 90 degrees 2h = 180 degrees 3h = 270 degrees	
		1-0	BUCK2_PHASE_CONFIG	0h = 0 degrees 1h = 90 degrees 2h = 180 degrees 3h = 270 degrees	

### 4.3 Configuring LDOs

There are several settings that can be programmed for the LDO regulators. These include the output voltages, and under voltage (UV) monitoring among others.

- Figure 4-4 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-6, Table 4-7, Table 4-8 and Table 4-9 show the register fields to be written when NOT using the TPS65219-GUI.



ŧ.	22	Configuration -	- NVM fields												
٥	READ	ALL REGISTERS Note: 0	Changing the value in	n a dropdown menu will caus	e an immedi	iate I2C write to th	e ass	ociated register unless in	nmediate write s	etting is chang	ed on Register Map (	age.			
		PMIC Status		Powe	r Resource	25		Si	equence			Digital Pins Configu	iration		
<b>F</b>	B U C K s	Bucks Switching Mode Switching Mode Note: Default Switching should not be changed Spread Spectrum When Bucks configured	Le Duasi-fixed frequency Mode configuration Disabled In setting has no effect for quasi-fixed frequ	Buck1 Buck1_EN BUCK1_STBY_ Output Voitage UV monitor Bandwidth	Disab Disab 0.600 -5% L Iow b	oled in Active state oled in Standby sta IV JV andwidth	* it * *	Buck2 Buck2_EN BUCK2_STBY_EN Output Voltage UV monitor Bandwidth Phase Config	Disabled in Ac Disabled in St 0.600V -5% UV Iow bandwidth 0 degrees	tive state  andby stat	Buck3 Buck3_EN BUCK3_STBY_E Output Voltage UV monitor Bandwidth Phase Config	Disabled in Ac Disabled in St 0.600V -5% UV Iow bandwidth 0 degrees	tive state  andby stal		
	L D S	LDO1_EN LDO1_STBY_EN Output Voltage UV monitor LDO1_LSW_CONFIG LDO1_BYP_CONFIG	Disabled in Active Disabled in Standt 0.600V -5% UV 0 - LDO1 NOT con 0 - LDO1 configure	state v by stat v v hfgured as Load-Switch v ed as LDO v	LDO2_E LDO2_S Output V UV mon LDO2_L LDO2_E	STBY_EN C Voltage 0 Itor 4 SW_CONFIG 0 3YP_CONFIG 0	Disabl Disabl 1.600\ 5% U 1 - LDI 1 - LDI	ed in Active state v ed in Standby stat v / v V 22 NOT configured as L O2 configured as LDO	oad-Switch 🗸	LDO3_EN LDO3_EN LDO3_STE Output Volt UV monitoi Configurati Power-Up I	Disabled i SY_EN Disabled i age 1.200V 	n Active state	LDO4_EN LDO4_EN LDO4_STBY_EN Output Voltage UV monitor Configuration Power-Up Ramp	Disabled in Active state v Disabled in Standby stat v 1.200V v -5% UV v LDO Mode v Fast ramp v	
		Refer LDOx_LSW_CONFI 0 0 1	ence for LDO1 a	and LDO2 Configural LDOx_BYP_CONFIG 0 1 X	ion	Configuration LDO Bypass Load-Switch									

## Figure 4-4. LDOs Settings Using the TPS65219-GUI

## Table 4-6. NVM Registers for LDO1 Settings

	Pogistor Address		Bit	Sottings	
	Register Address		Field Name	oettings	
Output Voltage	0x07	5-0	LDO1_VSET	see register map on data sheet	
		7	LDO1_LSW_CONFIG	0h = LDO1 NOT configured as load-switch 1h = LDO1 configured as Load-switch	
Configuration		6	LDO1_BYP_CONFIG	0h = LDO1 configured as LDO 1h = LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG 0x0)	
UV monitoring	0x1E	3	LDO1_UV_THR	0h = -5% UV 1h = -10% UV	

#### Table 4-7. NVM Registers for LDO2 Settings

	Pogistor Address		Bit	Settings	
	Register Address	Bit #	Field Name		
Output Voltage	0x06	7	LDO2_VSET	see register map on data sheet	
		6	LDO2_LSW_CONFIG	0h = LDO1 NOT configured as load-switch 1h = LDO1 configured as Load-switch	
Configuration		5-0	LDO2_BYP_CONFIG	0h = LDO1 configured as LDO 1h = LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG 0x0)	
UV Monitoring	0x1E	4	LDO2_UV_THR	0h = -5% UV 1h = -10% UV	

## Table 4-8. NVM Registers for LDO3 Settings

	Pogistor Address		Bit	Sottings		
	Bit :		Field Name	oettings		
Output Voltage	0x05	5-0	LDO3_VSET	see register map on data sheet		
Configuration		6	LDO3_LSW_CONFIG	0h = LDO Mode 1h = LSW Mode		
Ramp		7	LDO3_SLOW_PU_RAMP	0h = Fast ramp for power-up 1h = Slow ramp for power-up		



#### Table 4-8. NVM Registers for LDO3 Settings (continued)

			•			
	Pagistar Address		Bit	Settings		
	Register Address	Bit #	Field Name	Settings		
UV Monitoring	0x1E	5	LDO3_UV_THR	0h = -5% UV 1h = -10% UV		

#### Table 4-9. NVM Registers for LDO4 Settings

	Pagistar Address		Bit	Sattingo		
	Register Address	Bit #	Field Name	Settings		
Output Voltage	0x04	5-0	LDO4_VSET	see register map on data sheet		
Configuration		6	LDO4_LSW_CONFIG	0h = LDO Mode 1h = LSW Mode		
Ramp		7	LDO4_SLOW_PU_RAMP	0h = Fast ramp for power-up 1h = Slow ramp for power-up		
UV Monitoring	0x1E	6	LDO4_UV_THR	0h = -5% UV 1h = -10% UV		

## 4.4 Configuring GPIOs

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E Configuration - NVM fields

GPIOs can be used to enable external discrete components. GPIO can also be used for multi-PMIC configuration to sync the power-up and power-down sequence between two TPS65219 devices.

- Figure 4-5 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-10, Table 4-11 show the register fields to be written when NOT using the TPS65219-GUI.

**	PMIC Status	Po	wer Resources		Sequence	Digital Pins Configuration
			Deglitch Reference			
	A	Pin Configuration	Short_deglitch(TYP)	Long_deglitch(TYP)		
	B Pin Configuration Enable ~	Enable	120us	50ms		
	L Deglitch Short Deglitch ✓	VSENSE	120us	50ms		
		Push-Button	200ms	600ms		
	V         VSEL_SD / VSEL_DDR (pin# 12)           Pin Configuration         DDR           Rail Selection         LDO1           VSEL_SD_POLARITY         0           Note: See Table "VSEL_SD/VSEL_DDR configure in the data sheet for more information about pin p           VSEL_SD Control via I2C         1.8V           Note: VSEL_SD Control has no effect if pin 12 co SD	MOD     Pin C     Rese     MOD     ation options"     Note     the d     nfigured as	E / RESET (pin#28) onfiguration M I Selection C E_RESET_POLARITY 0 : See Table "MODE, STBY an lata sheet for more information	ODE  v old Reset v d RESET configuration" in about pin polarity	MODE / STBY (pin# 31) Pin Configuration MODE_STBY_POLARITY Note: See Table "MODE, ST the data sheet for more infor BUCK MODE Control via 120	MODE    MODE
	GPIO (pin# 16) GPIO Config GPIO Config GPIO Active State GPIO_Standby State Disabled v	GPO1 (pin# 8) GPO1 Active State GPO1 Standby Sta	te Disabled V GF	202 (pin# 17)       202 Active State       Disab       202 Standby State	led v led v	

Figure 4-5. GPIOs Configuration



	Desister Address		Bit	Sottingo			
	Register Address	Bit #	Field Name	Settings			
Enable settings in Active state	0x1E	2	GPIO_EN	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.			
		1	GPO2_EN	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.			
		0	GPO1_EN	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.			
Enable settings in Standby state	0x22	2	GPIO_STBY_E N	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.			
		1	GPO2_STBY_E N	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.			
		0	GPO1_STBY_E N	0h = Disabled. The output state is low. 1h = Enabled. The output state is Hi-Z.			

#### Table 4-10. NVM Registers for GPIO Settings

#### Table 4-11. NVM Register for Multi-PMIC Configuration

	Pogistor Address		Bit	Sottings
	Register Address		Field Name	Settings
GPO2 configuration	0x1F	3	MULTI_DEVICE_ENABLE	0h = Single-device configuration 1h = Multi-device configuration

### 4.5 Configuring Sequence

The process to configure the PMIC sequence consist of the following two steps:

- 1. Power-up/Power-down slot assignment: The slot assignment defines the order in which rails turn ON or OFF. Each of the PMIC rails must have a slot assigned. There are 16 slots available (0-15). Multiple rails (including GPIOs) can be assigned to the same slot so they be enabled at the same time.
- 2. Power-up/Power-down slot duration: The slot duration is the timing between the start of one slot to the start of the next slot. For example, if Buck1 is assigned to slot0 with a 3ms duration and Buck2 is assigned to slot 1, then Buck2 turns ON 3ms after Buck1.

#### Note

The slot duration does not dictate how long it takes for the rails to ramp. The slot duration only specifies how long the PMIC waits before enabling (or disabling) the rails that were assigned to the next slot.

- Figure 4-6 shows the settings to be changed when using the TPS65219-GUI
- Table 4-12, Table 4-13, Table 4-14 and Table 4-15 show the register fields to be written when NOT using the TPS65219-GUI.



#### Programming Instructions

,	PMIC S	Status	Power Reso	urces		Digital Pins Configu	uration	Powe	er-Up Sequence		Power-Do	own Sequend
					Po	<u>ower-Up Sequen</u>	<u>ce</u>					
9	Slot	Assignment	Sie	ot Duration			Do	wor Up Sog	luonco			
F	Buck1	slot_4 🗸	Slot_0	10 ms	~		FU	wei-op seq	uence			
	Buck2	slot_2 🛩	Slot_1	0 ms	~	r i				i î		
~	Buck3	slot_3 🛩	Slot_2	3 ms	~	GPO2					GPO2 BUCK2	
	LDO1	slot_2 🛩	Slot_3	1.5 ms	~	BUCK2					LD01	
	LDO2	slot_5 🛩	Slot_4	1.5 ms	~	LDOI					LD04	
	LDO3	slot_2 🗸	Slot_5	1.5 ms	~	LDOI-					BUCK1	
	LDO4	slot_2 🗸	Slot_6	10 ms	~	LD03					GPIO	
	GPIO	slot_6 🛩	Slot_7	1.5 ms	~	LDO4					GP01	
	GPO1	slot_6 🛩	Slot_8	10 ms	~	BUCK3				L		
	GPO2	slot_0 🖌	Slot_9	0 ms	~	BUCK1						
	nRSTOUT	slot_8 🛩	Slot_10	0 ms	~	LDO2						
			Slot_11	0 ms	~	GPI0 GP01						
			Slot_12	0 ms	~	nRSTOUT						
			Slot_13	0 ms	~	Oms	10ms	20ms	30ms	40ms		
			Slot_14	0 ms	~			time (ms)				
			Slot_15	0 ms	~			1				
								GENERATE PLO	т			

## Figure 4-6. Sequence Configuration

## Table 4-12. Power-Up Sequence - Slot Assignments

	Pagiatar Address		Bit	Sattinga
	Register Address	Bit#	Field Name	Settings
	0x11	7-4	BUCK1_SEQUENCE_ON_SLOT	see register map on data sheet
	0x10	7-4	BUCK2_SEQUENCE_ON_SLOT	see register map on data sheet
	0xF	7-4	BUCK3_SEQUENCE_ON_SLOT	see register map on data sheet
	0xE	7-4	LDO1_SEQUENCE_ON_SLOT	see register map on data sheet
Power-up	0xD	7-4	LDO2_SEQUENCE_ON_SLOT	see register map on data sheet
Sequence	0xC	7-4	LDO3_SEQUENCE_ON_SLOT	see register map on data sheet
Slot Assignment	0xB	7-4	LDO4_SEQUENCE_ON_SLOT	see register map on data sheet
	0x15	7-4	GPO1_SEQUENCE_ON_SLOT	see register map on data sheet
	0x14	7-4	GPO2_SEQUENCE_ON_SLOT	see register map on data sheet
	0x13	7-4	GPIO_SEQUENCE_ON_SLOT	see register map on data sheet
	0x12	7-4	nRST_SEQUENCE_ON_SLOT	see register map on data sheet



	Pagistar Address		Bit	Sattinga
	Register Address	Bit#	Field Name	Settings
		7-6	POWER_UP_SLOT_0_DURATION	see register map on data sheet
	0×16	5-4	POWER_UP_SLOT_1_DURATION	see register map on data sheet
	0,10	3-2	POWER_UP_SLOT_2_DURATION	see register map on data sheet
		1-0	POWER_UP_SLOT_3_DURATION	see register map on data sheet
		7-6	POWER_UP_SLOT_4_DURATION	see register map on data sheet
	0x17	5-4	POWER_UP_SLOT_5_DURATION	see register map on data sheet
		3-2	POWER_UP_SLOT_6_DURATION	see register map on data sheet
Power-up Sequence		1-0	POWER_UP_SLOT_7_DURATION	see register map on data sheet
Slot Duration	0x18	7-6	POWER_UP_SLOT_8_DURATION	see register map on data sheet
		5-4	POWER_UP_SLOT_9_DURATION	see register map on data sheet
		3-2	POWER_UP_SLOT_10_DURATION	see register map on data sheet
		1-0	POWER_UP_SLOT_11_DURATION	see register map on data sheet
	0x19	7-6	POWER_UP_SLOT_12_DURATION	see register map on data sheet
		5-4	POWER_UP_SLOT_13_DURATION	see register map on data sheet
		3-2	POWER_UP_SLOT_14_DURATION	see register map on data sheet
		1-0	POWER_UP_SLOT_15_DURATION	see register map on data sheet

## Table 4-14. Power-Down Sequence - Slot Assignments

	Pagistar Address		Bit	Sottingo	
	Register Address	Bit# Field Name		Settings	
	0x11	7-4	BUCK1_SEQUENCE_OFF_SLOT	see register map on data sheet	
	0x10	7-4	BUCK2_SEQUENCE_OFF_SLOT	see register map on data sheet	
	0xF	7-4	BUCK3_SEQUENCE_OFF_SLOT	see register map on data sheet	
	0xE	7-4	LDO1_SEQUENCE_OFF_SLOT	see register map on data sheet	
Power-down	0xD	7-4	LDO2_SEQUENCE_OFF_SLOT	see register map on data sheet	
Slot	0xC	7-4	LDO3_SEQUENCE_OFF_SLOT	see register map on data sheet	
Assignment	0xB	7-4	LDO4_SEQUENCE_OFF_SLOT	see register map on data sheet	
	0x15	7-4	GPO1_SEQUENCE_OFF_SLOT	see register map on data sheet	
	0x14	7-4	GPO2_SEQUENCE_OFF_SLOT	see register map on data sheet	
	0x13	7-4	GPIO_SEQUENCE_OFF_SLOT	see register map on data sheet	
	0x12	7-4	nRST_SEQUENCE_OFF_SLOT	see register map on data sheet	



		-		
	Register Address		Bit	Settings
	Register Address	Bit#	Field Name	Octangs
		7-6	POWER_DOWN_SLOT_0_DURATION	see register map on data sheet
	0×14	5-4	POWER_DOWN_SLOT_1_DURATION	see register map on data sheet
	UXIA	3-2	POWER_DOWN_SLOT_2_DURATION	see register map on data sheet
		1-0	POWER_DOWN_SLOT_3_DURATION	see register map on data sheet
		7-6	POWER_DOWN_SLOT_4_DURATION	see register map on data sheet
	0x1B	5-4	POWER_DOWN_SLOT_5_DURATION	see register map on data sheet
		3-2	POWER_DOWN_SLOT_6_DURATION	see register map on data sheet
Power-down		1-0	POWER_DOWN_SLOT_7_DURATION	see register map on data sheet
Slot Duration	0x1C	7-6	POWER_DOWN_SLOT_8_DURATION	see register map on data sheet
		5-4	POWER_DOWN_SLOT_9_DURATION	see register map on data sheet
		3-2	POWER_DOWN_SLOT_10_DURATION	see register map on data sheet
		1-0	POWER_DOWN_SLOT_11_DURATION	see register map on data sheet
	0x1D	7-6	POWER_DOWN_SLOT_12_DURATION	see register map on data sheet
		5-4	POWER_DOWN_SLOT_13_DURATION	see register map on data sheet
		3-2	POWER_DOWN_SLOT_14_DURATION	see register map on data sheet
		1-0	POWER_DOWN_SLOT_15_DURATION	see register map on data sheet

#### Table 4-15. Power-Down Sequence - Slot Duration

## **4.6 Configuring Multi-Function Pins**

The TPS65219 PMIC has three configurable multi-function pins. MODE/STBY and MODE/RESET can be configured as MODE to select the switching, as STBY to trigger a transition to Standby state, or as RESET to trigger a cold or warm reset. The VSEL\_SD/VSEL\_DDR pin can be configured to set the output voltage on LDO1 or LDO2 (selectable) or to set the output voltage on Buck3. Refer to the data sheet for information on pin polarity.

#### Note

If VSEL\_SD/VSEL\_DDR is not used to set the output voltage on LDO1 (or LDO2), then it must be configured as DDR and pulled to GND with a pull-down resistor in the schematic. Additionally, VSEL\_SD\_I2C\_CTRL must be programmed to 1h.

- Figure 4-7 shows the settings to be changed when using the TPS65219-GUI
- Figure 4-7 show the register fields to be written when NOT using the TPS65219-GUI.



Programming Instructions

- 1	Di No Circlus		B			Divitel Dire Configuration	45
1		٢	ower Resources		sequence	Digital Pins Configurat	aon
			Deglitch Reference				
•	A	Pin Configuration	Short_deglitch(TYP)	Long_deglitch(TYP)			
ε	B Pin Configuration Enable V	Enable	120us	50ms			
7	L Deglitch Short Deglitch ~	VSENSE	120us	50ms			
	E PSD Disable V	Push-Button	200ms	600ms			
	VSEL_SD / VSEL_DDR (pin# 12) Pin Configuration Rail Selection USEL_SD_POLARITY Note: See Table "VSEL_SD/VSEL_DDR configure in the data sheet for more information about pin p VSEL_SD Control via I2C Note: VSEL_SD Control has no effect if pin 12 co SD	MOl Pin Res MOl ation options" Not figured as	DE / RESET (pin#28) Configuration M et Selection DE_RESET_POLARITY te: See Table "MODE, STBY ar e data sheet for more informatio	old Reset V value of the second secon	MODE / STBY (pin# 31) Pin Configuration MODE_STBY_POLARITY Note: See Table "MODE, STE the data sheet for more inform BUCK MODE Control via I2C	MODE	
	G     GPIO (pin# 16)       I     GPIO Config       GPIO Active State     Disabled       GPIO_Standby State     Disabled	GPO1 (pin# 8) GPO1 Active State Disabled ~ GPO1 Standby State Disabled ~		PO2 (pin# 17) PO2 Active State Disable PO2 Standby State Disable	led v led v		

## Figure 4-7. Multi-Function Configuration using the TPS65219-GUI

	Pagiotor Address	Bit		Sottingo			
	Register Address	Bit #	Field Name	Settings			
Pin Function	0x1F	0	VSEL_DDR_SD	0h = VSEL pin configured as DDR to set the voltage on Buck3 1h = VSEL pin configured as SD to set the voltage on the VSEL_RAIL			
VSEL rail selection		2	VSEL_RAIL	0h = LDO1 1h = LDO2			
Pin polarity		1	VSEL_SD_POLARITY	0h = • LOW: 1.8V • HIGH: LDOx_VOUT register 1h = • HIGH: 1.8V • LOW: LDOx_VOUT register			

## Table 4-16. NVM Registers for VSEL\_SD / VSEL\_DDR

### Table 4-17. NVM Registers for MODE / STBY

	Pogiotor Address	Bit		Sattingo	
	Register Address		Field Name	Gettings	
Pin Function	0x20	1-0	MODE_STBY_CONFIG	0h = MODE 1h = STBY	
				2h = MODE and STBY 3h = MODE	
Pin Polarity	0x1F	4	MODE_STBY_POLARITY	see register map on data sheet	



## Table 4-18. NVM Registers for MODE / RESET

	Pagistor Address	Bit		Sattings	
	Register Address	Bit # Field Name		Settings	
Pin Function	0x20	2	MODE_RESET_CONFIG	0h = MODE 1h = RESET	
RESET config		6	WARM_COLD_RESET_CONFIG	0h = COLD RESET 1h = WARM RESET	
Pin Polarity	0x1F	5	MODE_RESET_POLARITY	see register map on data sheet	



## 4.7 Configuring the EN/PB/VSENSE Pin

The enable pin of the PMIC can be configured as Enable, Push-Button, or VSENSE. In addition to the function, the deglitch can also be configured. Additionally, this pin has the option for first supply detection (FSD) to ignore the state of the EN/PB/VSENSE pin during the first power-up.

- Figure 4-8 shows the settings to be changed when using the TPS65219-GUI.
- Table 4-19 show the register fields to be written when NOT using the TPS65219-GUI.

	Configuration	n - NVM fields								
RE	AD ALL REGISTERS Note	: Changing the value in	a dropdown me	nu will ca	use an immediate I2C wri	te to the associated register u	Inless	s immediate write setting is cha	nged on Register Map page.	
	PMIC Stat	us		Po	wer Resources		S	equence	Digital Pins Confi	guration
E		(nin# 05)			Deglitch Referen	ce				
A	ENTERVIENSE	<u>(pin# 25)</u>	Pin Configu	uration	Short_deglitch(TYP	P) Long_deglitch(TYP)				
В	Pin Configuration	Enable 🗸	Enabl	e	120us	50ms				
L	Deglitch	Short Deglitch 🗸	VSENS	SE	120us	50ms				
E	FSD	Disable v	Push-Bu	tton	200ms	600ms				
	VSEL_SD / VSEL_DDR (pin# 12)       M         Pin Configuration       DDR       •         Rail Selection       LDO1       •         VSEL_SD_POLARITY       0       •         Note: See Table "VSEL_SD/VSEL_DDR configuration options" in the data sheet for more information about pin polarity       M         VSEL_SD Control via I2C       1.8V       •         Note: VSEL_SD Control via I2C       1.8V       •         Note: VSEL_SD Control via I2C       1.8V       •		MOD Pin C Rese MOD Note the c	E / RESET (pin#28) onfiguration t Selection E_RESET_POLARITY : See Table "MODE, STB" iata sheet for more inform	MODE  Cold Reset Y and RESET configuration" ation about pin polarity	n	MODE / STBY (pin# 31) Pin Configuration MODE_STBY_POLARITY Note: See Table "MODE, ST the data sheet for more infor BUCK MODE Control via 120	MODE 0 V and RESET configuration" in mation about pin polarity Auto PFM		
G P I O S	GPIO (pin# 16) GPIO Config GPIO Active State GPIO_Standby State	Single-device config ~ Disabled ~ Disabled ~	GPO1 (pin# 8) GPO1 Active State Disabled V GPO1 Standby State Disabled V			GPO2 (pin# 17) GPO2 Active State Di GPO2 Standby State Di	sableo	d v d v		

### Figure 4-8. EN/PB/VSENSE Configuration Using the TPS65219-GUI

	Register		Bit	Cottin no	
	Address	Bit #	Field Name	Sectings	
First Supply Detection	0x20	7	PU_ON_FSD	0h = FSD Disabled 1h = FSD Enabled	
Pin Configuration		5-4	EN_PB_VSENSE_CONFIG	0h = Enable 1h = Push Button 2h = VSENSE 3h = Enable	
Deglitch		3	EN_PB_VSENSE_DEGL	see register map on data sheet	

## 4.8 Changing I2C Address

The TPS6521905 has the default I2C address configured as 0x30. This configuration can be changed if needed by searching for register *I2C\_ADDRESS\_REG* in the register map of the TPS65219\_GUI and changing the default 0x30 address as shown in Figure 4-9. Once the register is changed, the new value must be saved into the NVM by writing 0x0A to register 0x34.



Note

When using multiple TPS65219 devices in multi-PMIC configuration, each device must have a unique I2C address. The I2C address for the 2nd, 3rd and other PMICs must be changed from the default 0x30 to a new value.

ħ	Register Map     Q lzc_address					Auto Rea	d Off			READ REGISTE Search Bitfie	R READ	ALL REGISTERS	WRITE REGISTER WRITE ALL REGISTERS
E	Register Name		Address	Value	7	6	5	Bi 4	ts 3	2	1	0	FIELD VIEW I2C_ADDRESS_REG
0	I2C_ADDRESS_REG	Ø	0x26	0x30	0	0	1	1	0	0	0	0	Device Registers / I2C_ADDRESS_REG 0x 30

### Figure 4-9. I2C\_ADDRESS\_REG

#### Table 4-20. I2C\_ADDRESS\_REG

Register Address	Bit			
	Bit#	Field Name		
0x26	6-0	I2C_ADDRESS_REG		

## 4.9 Configuring Mask Settings

There are several interrupt settings that can be masked to bypass specific PMIC monitoring features or modify how PMIC reacts when interrupts are detected. The interrupts that can be masked include undervoltage monitoring, temperature monitoring, among others. Figure 4-10 shows the mask settings in the configuration tab of the GUI.

**Note** If any of the Mask registers is not shown in the configuration tab of the TPS65219-GUI, they can be found in the Register Map which includes the full list of registers.

<b>f</b>	幸 Configuration - NVM fields								
٥	READ ALL REGISTERS Note: Changing the value in a dropdown menu will cause an immediate I2C write to the associated register unless immediate write setting is changed on Register Map page.								
	PMIC	Status Power F	esources	Digital Pins Configuration	ı Power			nce	Mask Settings
	MASK_EFFECT Ino state change / no nINT reaction / no bit set for Faults v								
	Underv	voltage (UV) Mask settings	Die T	emperature Mask Settings		Other Mask Settings			
ų.	Buck1 UV	un-masked (Faults reported)	Sensor 0	un-masked (Faults reported)	MASK_INT_FOR_PB	un-masked (nINT pulled low	v for any PB events) 🗸		
~	Buck2 UV	un-masked (Faults reported)	Sensor 1	un-masked (Faults reported)	MASK_INT_FOR_RV	un-masked (nINT pulled low	v for any RV events) 🗸		
	Buck3 UV	un-masked (Faults reported)	Sensor 2	un-masked (Faults reported)	MASK_RETRY_COUNT	Device will retry up to 2 time	es 🗸		
	LDO1 UV	un-masked (Faults reported) 🗸	Sensor 3	un-masked (Faults reported) 👻					
	LDO2 UV	un-masked (Faults reported) V							
	LDO3 UV	un-masked (Faults reported) V							
	L004 UV	un-masked (Hauits reported)							

Figure 4-10. Mask Settings in TPS65219-GUI

#### Table 4-21. MASK Settings on Register 0x1E

Register Address	Bit	
	Bit#	Field Name
0x1E	7	BYPASS_RAILS_DISCHA RGED_CHECK

Register Address	Bit	
	Bit#	Field Name
0x24	7	MASK_RETRY_COUNT
	6	BUCK3_UV_MASK
	5	BUCK2_UV_MASK
	4	BUCK1_UV_MASK
	3	LDO4_UV_MASK
	2	LDO3_UV_MASK
	1	LDO2_UV_MASK
	0	LDO1_UV_MASK

Table 4-22 MASK Settings on Register 0x1E

#### Table 4-23. MASK Settings on Register 0x1E

Register Address	Bit	
	Bit#	Field Name
0x25	7	MASK_INT_FOR_PB
	6-5	MASK_EFFECT
	4	MASK_INT_FOR_RV
	3	SENSOR_0_WARM_MASK
	2	SENSOR_1_WARM_MASK
	1	SENSOR_2_WARM_MASK
	0	SENSOR_3_WARM_MASK

## 4.10 NVM Re-Programming

Once the register settings are updated, the new values can be saved into the NVM by writing 0x0A to register address 0x34.

- Figure 4-11 shows the button that saves the register settings into the NVM when using the TPS65219-GUI.
- Table 4-24 shows the register field to be written when NOT using the TPS65219-GUI.



### Figure 4-11. NVM Re-programming Using TPS65219-GUI



#### Table 4-24. I2C Write to Save Register Settings into NVM

Register Address		Data	
	Bit#	Field Name	
0x34	3-0	USER_NVM_CMD	0x0A

#### Note

It is recommended to export the selected register settings into a CSV and JSON file using the TPS65219-GUI. Figure 4-12 shows how to export the NVM settings. The file format must be selected on "Register File Format" before using the "Save Registers As".



Figure 4-12. Export NVM Settings Using TPS65219-GUI

## A Non-NVM Registers

The PMIC register map contains NVM and non-NVM bits. Register addresses 0x00 to 0x27 contains the NVM bits which are backed up by EEPROM. This register settings can be changed by I2C and default values can be re-programmed as described in the programming guide. The reset value for each of the NVM bits is marked as "X" in the data sheet register map as those can be re-programmed and are unique for each orderable part number.

Non-NVM bits are located in register addresses 0x28 to 0x41. These registers settings can be changed by I2C but the default values cannot be re-program. Register settings for non-NVM bits go back to their default values after a power cycle and every time the PMIC enters Initialize state. The default value for non-NVM bits can be found in the data sheet register map, under "Reset" column.



## **B** Loading a NVM Configuration File to PMIC

The diagram shown in Figure B-1 describes the process to load a pre-configured NVM file (.CSV or .JSON extension) into the PMIC NVM. The soldered down EVM (TPS65219EVM) is used as a reference but the socketed EVM can be used as well. The TPS6521905 product page has multiple NVM files that are pre-configured to meet the requirements of specific processors or SoCs. TI's customers can reuse these files to re-program the PMICs on their production line or by working with a distributor.

**Note** If the pre-configured NVM files do not meet all the application requirements, they can still be loaded to the PMIC NVM, make the necessary changes, and generate a new NVM file using the TPS65219-GUI.



Figure B-1. Loading NVM Configuration File



## **C PMIC Configurable Fields**

This section shows the list of programmable NVM fields for each of the PMIC power and digital resources. Some of the register fields have "x" to simplify the list. Replace "x" with the corresponding rail number to identify the correct register field in the data sheet or programming guide. Similarly, for the sequence slot duration, "y" was used to simplify the list but those can be replaced with the specific slot#.



PMIC rail	Configurable Setting	Register Field		
	Enable settings	Active State: Buck <b>x_</b> EN Standby State: BUCK <b>x_</b> STBY_EN		
	Output voltage	BUCK <b>x_</b> VSET		
Bucks	Under-voltage monitoring	BUCKx_UV_THR_SEL		
	Bandwidth	BUCK <b>x_</b> BW_SEL		
	Power-up sequence	Slot#: BUCKx_SEQUENCE_ON_SLOT Duration: POWER UP SLOT y DURATION		
	Power-down sequence	Slot#: BUCKx_SEQUENCE_OFF_SLOT Duration: POWER_DOWN_SLOT_y_DURATION		
	Enable settings	Active State: LDOx_EN Standby State: LDOx_STBY_EN		
	Output voltage	LDOx_VSET		
	Under-voltage monitoring	LDOx_UV_THR_SEL		
LDOs	Rail config (LDO, load-switch, bypass)	LDOx_LSW_CONFIG LDOx_BYP_CONFIG (LDO1, LDO2 only)		
	Ramp	LDOx_SLOW_PU_RAMP (LDO3, LDO4 only)		
	Power-up sequence	Slot#: LDOx_SEQUENCE_ON_SLOT Duration: POWER_UP_SLOT_y_DURATION		
	Power-down sequence	Slot#: LDOx_SEQUENCE_OFF_SLOT Duration: POWER_DOWN_SLOT_y_DURATION		
	Enable settings GPIO	Active State: GPI/Ox_EN Standby State: GPI/Ox_STBY_EN		
	Pin Function	MULTI_DEVICE_ENABLE (GPIO only)		
GPIOs	Power-up sequence	Slot#: GPI/Ox_SEQUENCE_ON_SLOT Duration: POWER_UP_SLOT_y_DURATION		
	Power-down sequence	Slot#: GPI/Ox_SEQUENCE_OFF_SLOT Duration: POWER_DOWN_SLOT_y_DURATION		
	Pin Function	EN_PB_VSENSE_DEGL		
Enable pin	Deglitch	EN_PB_VSENSE_CONFIG		
	First Supply Detection (FSD)	PU_ON_FSD		
	Pin Function	VSEL_DDR_SD		
VSEL_SD	Rail Selection	VSEL_RAIL		
VSEL_DDK	Pin Polarity	VSEL_SD_POLARITY		
	Pin Function	MODE_STBY_CONFIG		
MODE/STBY	Pin Polarity	MODE_STBY_POLARITY		
MODE/RESET	Pin Function	MODE_RESET_CONFIG		
	RESET selection	WARM_COLD_RESET_CONFIG		
	Pin Polarity	MODE_RESET_POLARITY		
nRSTOLIT	Power-up sequence	Slot#: nRST_SEQUENCE_ON_SLOT Duration: POWER_UP_SLOT_y_DURATION		
in stoot	Power-down sequence	Slot#: nRST_SEQUENCE_OFF_SLOT Duration: POWER_DOWN SLOT y DURATION		

Figure C-1	. NVM	programmable	Fields
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# D References

- 1. Texas Instruments, TPS6521905 data sheet
- 2. Texas Instruments, TPS65219EVM-SKT user's guide

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