Texas Instruments

GC5316 Daughtercard GC Studio Reference User Guide

User's Guide

February 2006

SLWU032

The GC5316 is a high density digital upconverter and downconverter. It is optimized for UMTS, TD-SCDMA and CDMA2000-1X standards. It provides 12 UMTS upconversion and 12 UMTS downconversion channels. Alternately, the chip can handle 24 CDMA upconversion and downconversion channels. The GC5316 daughtercard for the GC101 Motherboard provides a means for testing and evaluating this part, using the GC Studio program for device control.

1 GC5316 Daughtercard and GC101 EVM Setup

To operate the system, simply plug the GC5316 daughtercard into the DIMM socket on the GC101 motherboard, connect the parallel port interface cable to the GC101 and Host Computer (PC), and connect the power supply to the GC101.

Figure 1. GC101 EVM and GC5316 Daughtercard

2 GC Studio and the GC5316/GC101 Evaluation Hardware

GC Studio includes a software “plug-in” to control the GC101 motherboard, GC5316 daughtercard and the GC5316 device. Input data from a text file on the host computer (PC) is loaded into the GC101 input memory and used to stimulate the GC5316 input ports. Output data from the GC5316 is captured in the GC101 capture memory and transferred to the host computer. GC Studio configures the GC5316 internal registers using the interactive GUI.

Several GC Studio projects for the GC5316 are included in the installation. These projects can be used as the starting point for creating new experiments as desired.

2.1 GC Studio Installation

2.1.1 Required Elements

- GC101 evaluation motherboard, the external 5V power supply for the GC101 and a ECP parallel port enhanced speed cable.
- GC Studio software, downloaded or provided on a CD
- GC5316 Rev A daughtercard
- Host Computer (PC) with BIOS supporting ECP mode for LPT1, running Win98 Rel 2, WinME, Win2000 SP1, WinXP Home or WinXP Professional.
- Administrator Group Privileges

2.1.2 GC Studio Installation Instructions

Locate the “GC Studio_Setup.exe” file on the CD or in the downloaded location on the host computer and double click on it to install.

2.2 GC Studio Projects

Several projects (sometimes referred to as experiments) are provided for the GC5316 in the GC Studio release. Users can execute these existing projects and create and save new projects using the GC Studio GUI interface.

2.2.1 Creating a New GC Studio Project for a CDMA Configuration

This project demonstrates the ability of the GC5316 to downconvert channels from a real, parallel input stream. The input spectrum shows the input image (which is a real signal, which explains the negative image in the spectrum).

The resampler is turned on, which downshifts the data by $F_S/4$ (122.88/4 = 30.72). Therefore, Channel 0 A&B, which have their NCO's tuned to ±.625 are filtering and isolating the signals centered at 30.72 ±.625MHz.

- A real CDMA carrier is applied to the GC5316 rxin_a inputs with a simulated sample rate of 61.44 Msps and an IF frequency of 30.72MHz.
- Simulated rxclk to the gc5316 is 122.88MHz
- Receive FIFOs are enabled
- Receive Channel 0 is configured to process the signal
- The resampler is turned on, which downshifts the data by $F_S/4$ (122.88/4 = 30.72).
- Channel 0 A&B, which have their NCO's tuned to ±.625 are filtering and isolating the signals centered at 30.72 ±.625MHz
- The CIC filter is programmed to decimate by 25 using a m=2 comb section configuration. The output sample rate at the CIC output is 4.9152 MSPS
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 48 tap filter.
- The 64 tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the half rxclk rate.

1. Start GC Studio
2. Click on File > New Project to bring up the following window.
3. Choose a name for this new project, and click create.
4. Select GC5316 for the Plugin and click OK.
5. Using the wizard style interface, setup the GC101 evaluation board, then click next.

   "Evaluation Board Setup" Menu allows the user to set up the data source (input and output), pattern length, capture length, and clock rates and sources. At this point, click the "NEXT" tab to proceed to the next screen:

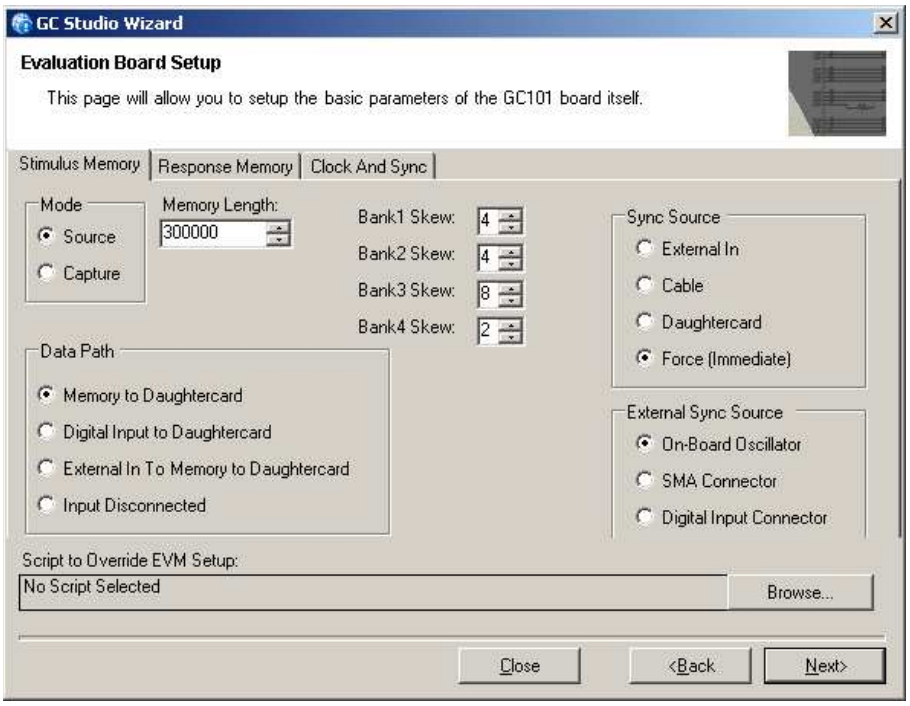

Figure 2. CDMA - Evaluation Board Setup

6. Setup the GC5316 I/O mode selection as shown and click next. In this example, be sure the ADC clock rate is set to 3/4. Because we are using a receive channel for this experiment, set the Input Mode and Output Mode boxes to Receive Ports as shown below. We will ignore the Output Clock Source and leave it also set to TX Clk Out. Ensure that the Output Syncs and Strobes are set to “Rx Sync Out and PB Data”. Otherwise, the frame strobe for the receive output serial stream will not be output, and GC Studio will be incapable of deciphering the serial output data from the chip. Click “Next” to see the Simulated Clock Rates screen.

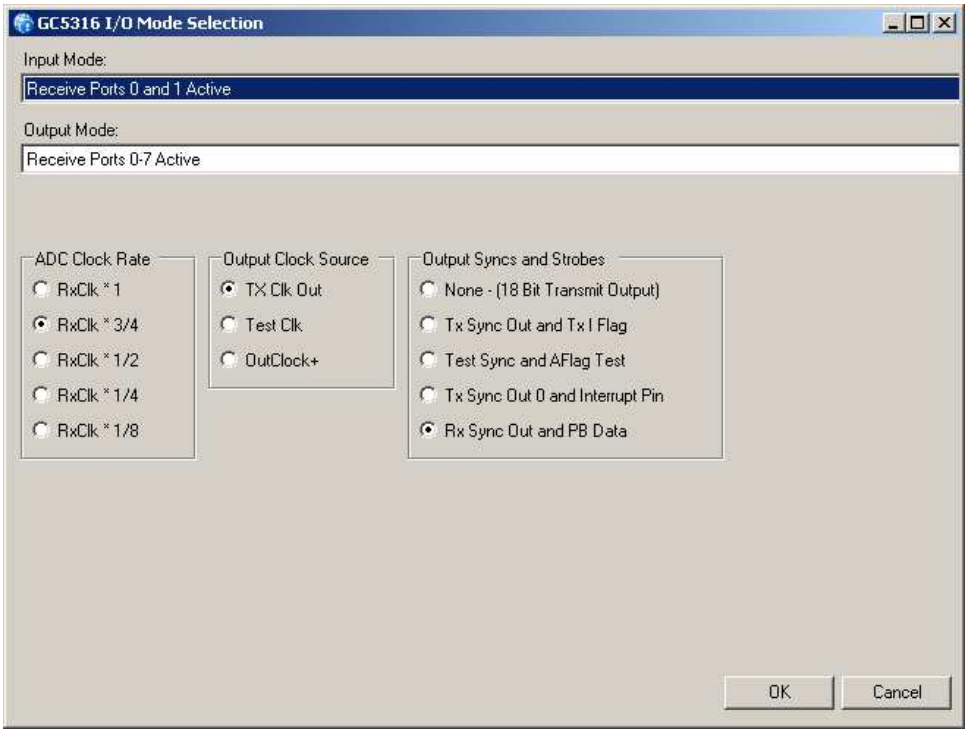

Figure 3. CDMA – I/O Mode Selection

7. Set the simulated clock rate to 122.88 MHz and click next.

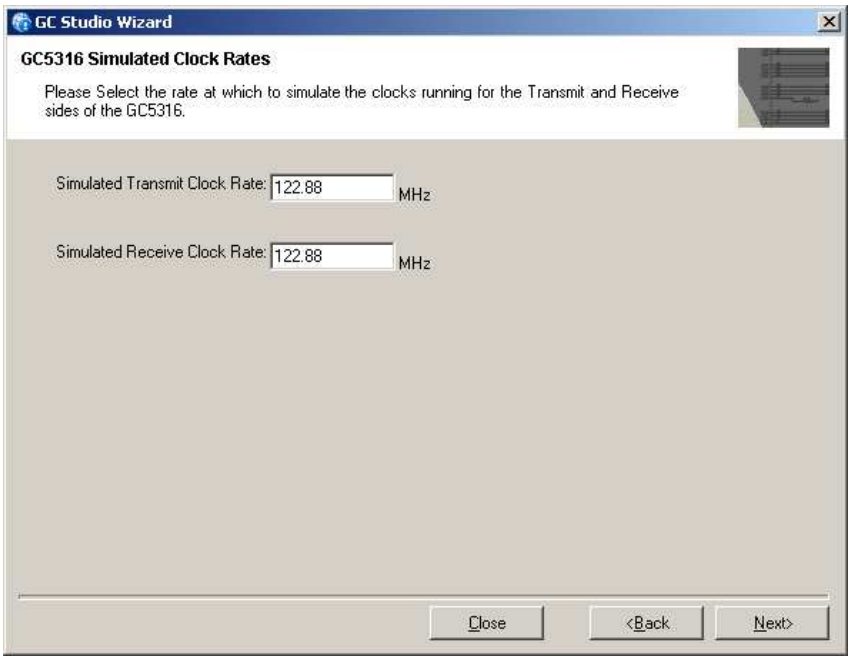

Figure 4. CDMA – Simulated Clock Rates

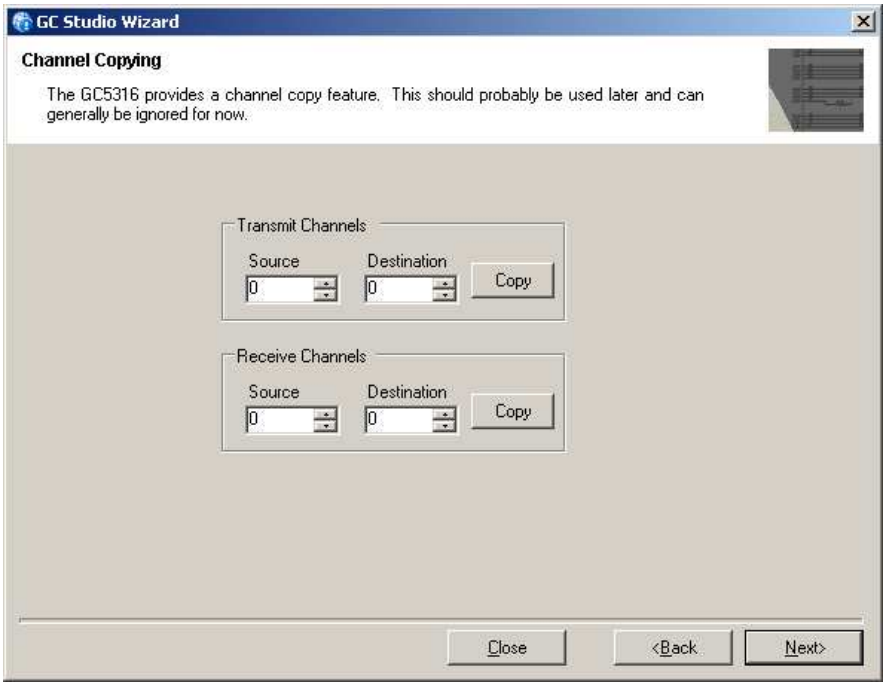

Figure 5. CDMA – Channel Copying

8. Channel Copying will be skipped for now, click Next.
9. Project description can be added to explain the details. Finish the set-up Wizard by clicking the “Finish” tab on the next screen.
10. Click on the large gc5316 box to display the global control registers.

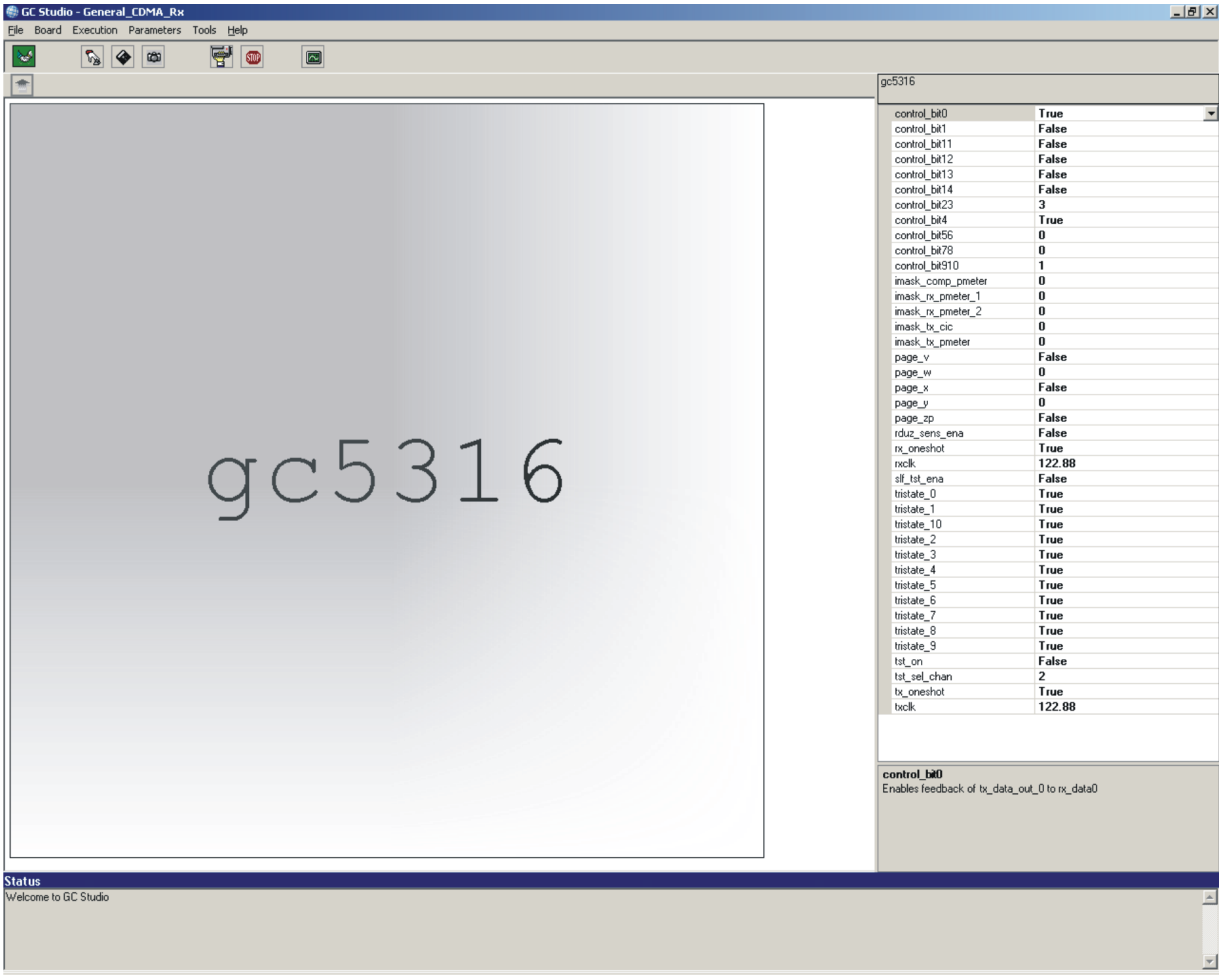

Figure 6. CDMA – Displaying Global Control Registers

11. Next, double click on the gc5316 block to “push down” one level into the gc5316.
12. Click on the Receive Input Interface block to display and edit the receive input interface registers.
13. Make sure that the "adc_fifo_bypass" is set to FALSE to enable the rxin_a/b/c/d input FIFO circuits.

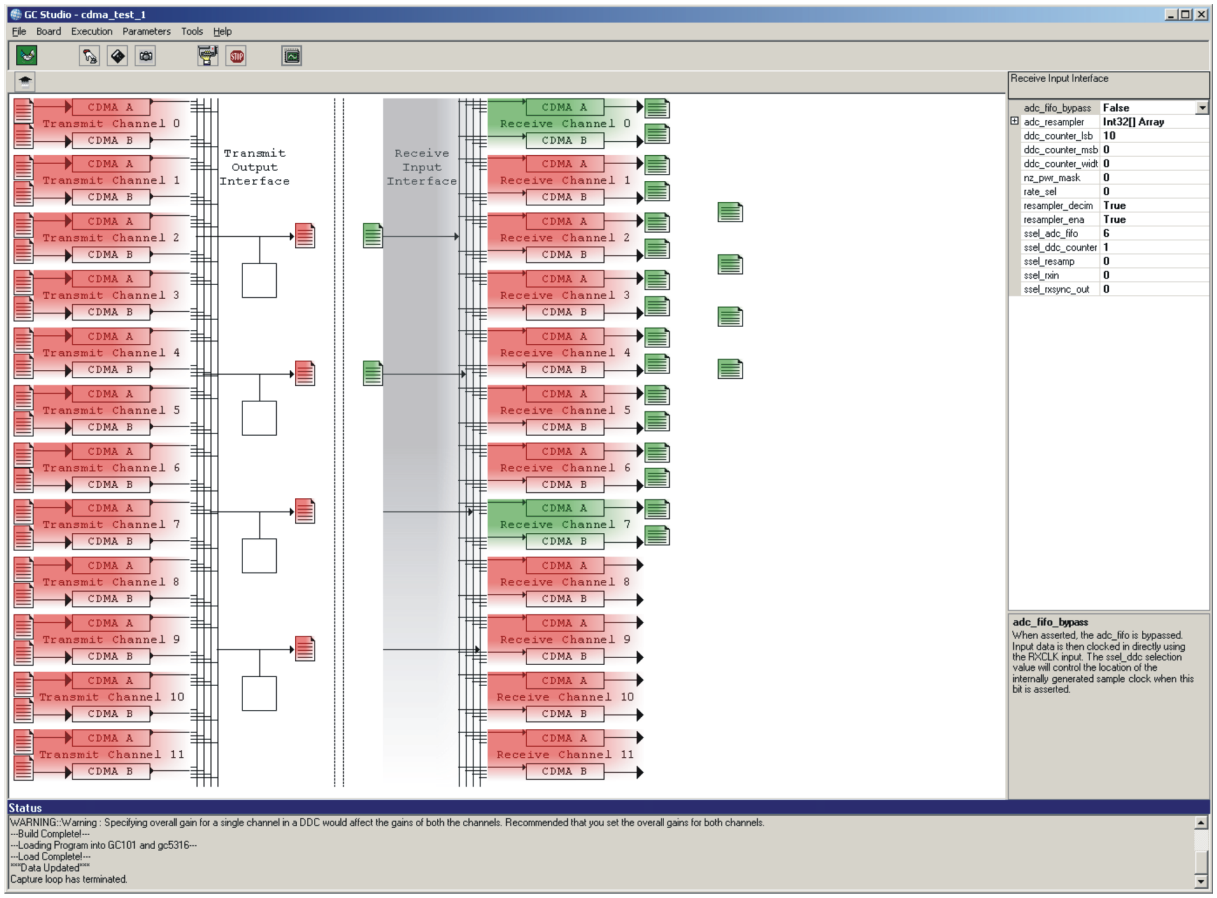

Figure 7. CDMA – Receive Input Interface Registers

14. Next, since the ADC runs at 3/4 the GC5316 clock rate (92.16 MSPS), the resampler needs to be enabled and coefficients loaded. Enable the resampler and set its parameters by following the picture below:

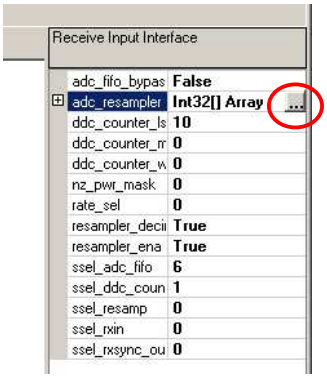

Figure 8. CDMA - Receive Input Interface, adc-resampler

15. Click on the "adc_resampler" Array (circled above) and load the following coefficients:

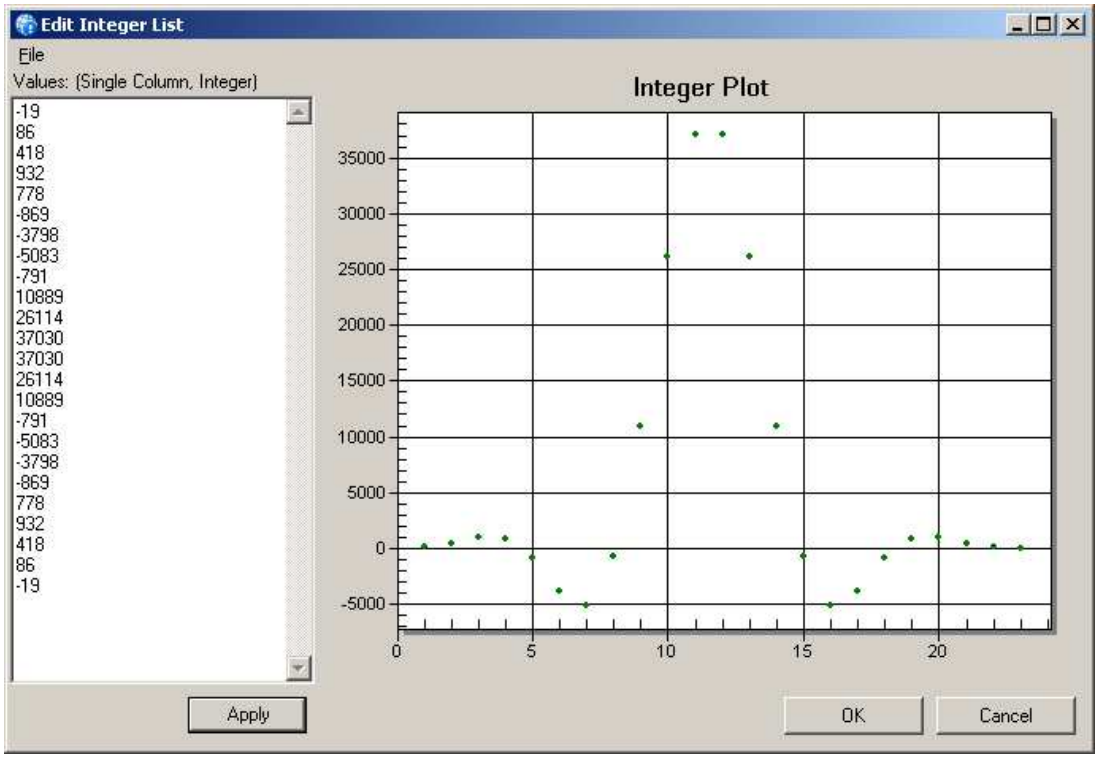

Figure 9. CDMA - Integer Plot

16. Click on "File", then "Load", then navigate on the provided CD for the Filter file named "cdma_RS_92p16to122p88.taps". This file contains the coefficients to be used by the resampler. Select this file. After the file is loaded, the Integer plot should look as shown above. Click on "OK".
17. Click on the upper Receive Channel 1 0 block. Set ddc_duc_ena to True. Make sure that the cdma_mode is set to True. The "ch_rate_sel" bit needs to be set to 1 to match the ADC rate.
18. Set the freqa to 0.625 (MHz) and freqb to -0.625 in order to tune to the positive and negative side of the real signal.

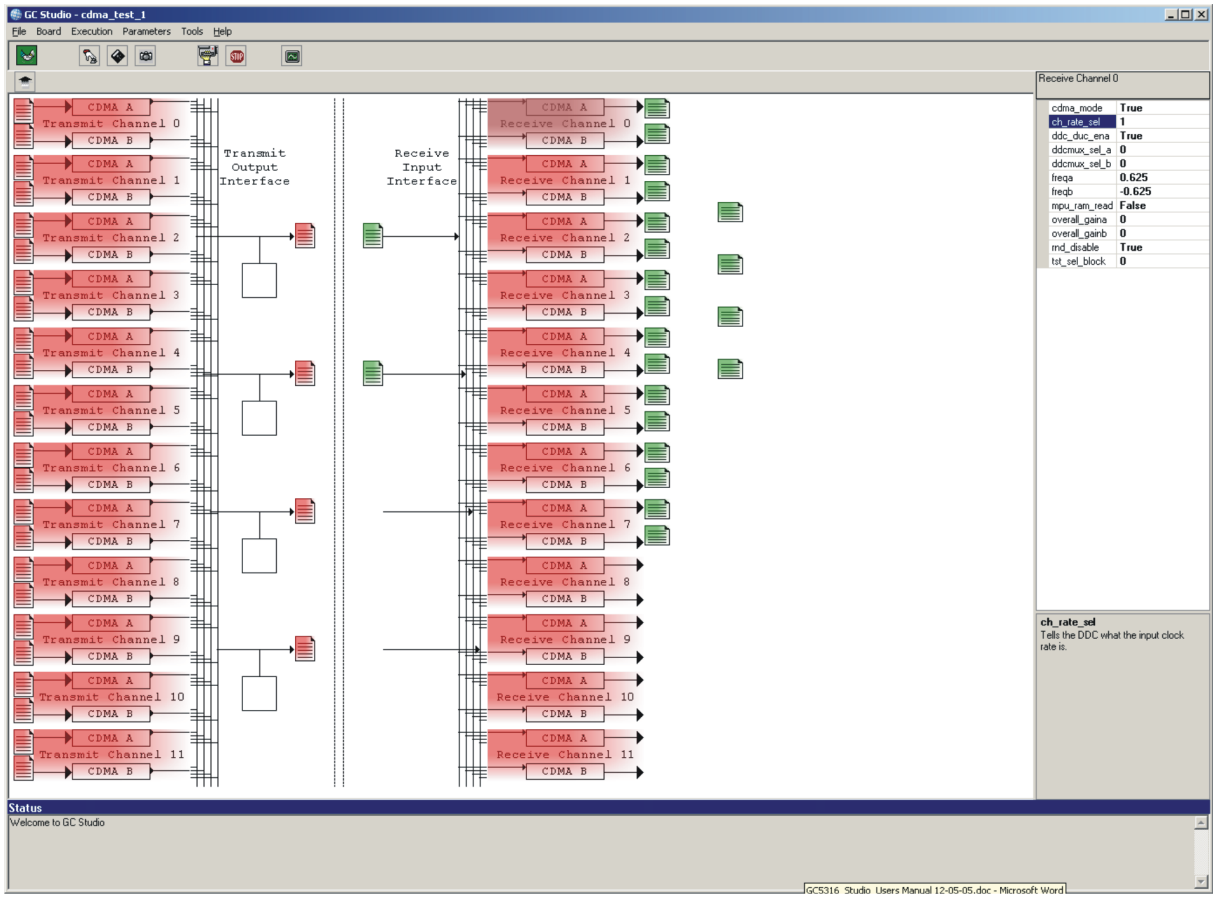

Figure 10. CDMA – Setting Frequency in Receive Channel Block

19. Double-click on the Receive Channel 0. Select the Delay Adjust and Zero Stuff block. Because the input sample rate is set to the rxclk rate, set the interpolation rate to 1. The tadj_offset_coarse and tadj_offset_fine settings allow the user to adjust the delay between various receive channels if desired. Set both tadj_offset_coarse_a and tadj_offset_coarse_b to 1.

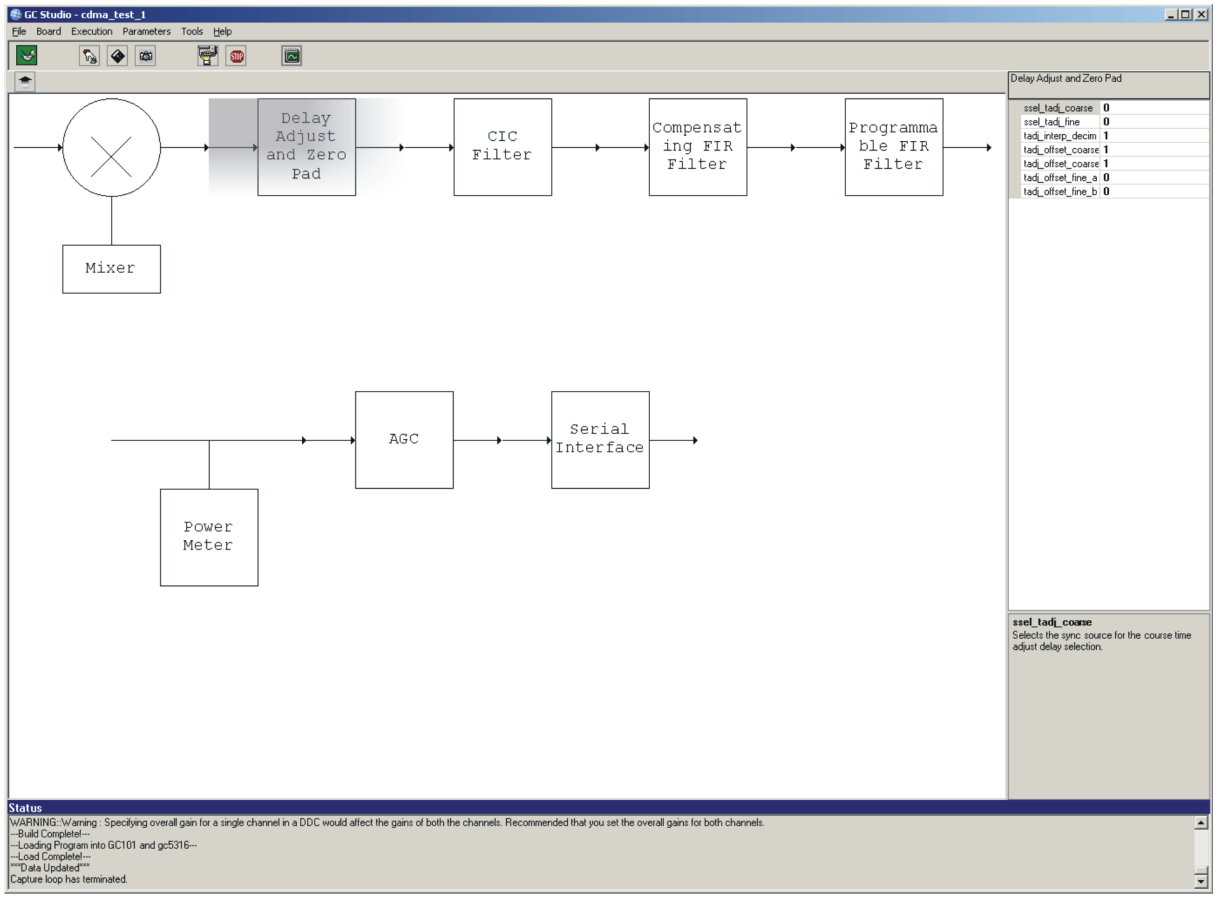

Figure 11. CDMA – Delay Adjust and Zero Stuff Block

20. Click on the CIC filter block and set the registers as shown in the following panel. The decimation in the CIC is set to 25x, resulting in a 4.9152Msps CIC output rate (4x chip rate). For this example, all 6 CIC comb stages are set to m=2 (63 decimal = 111111 in binary).

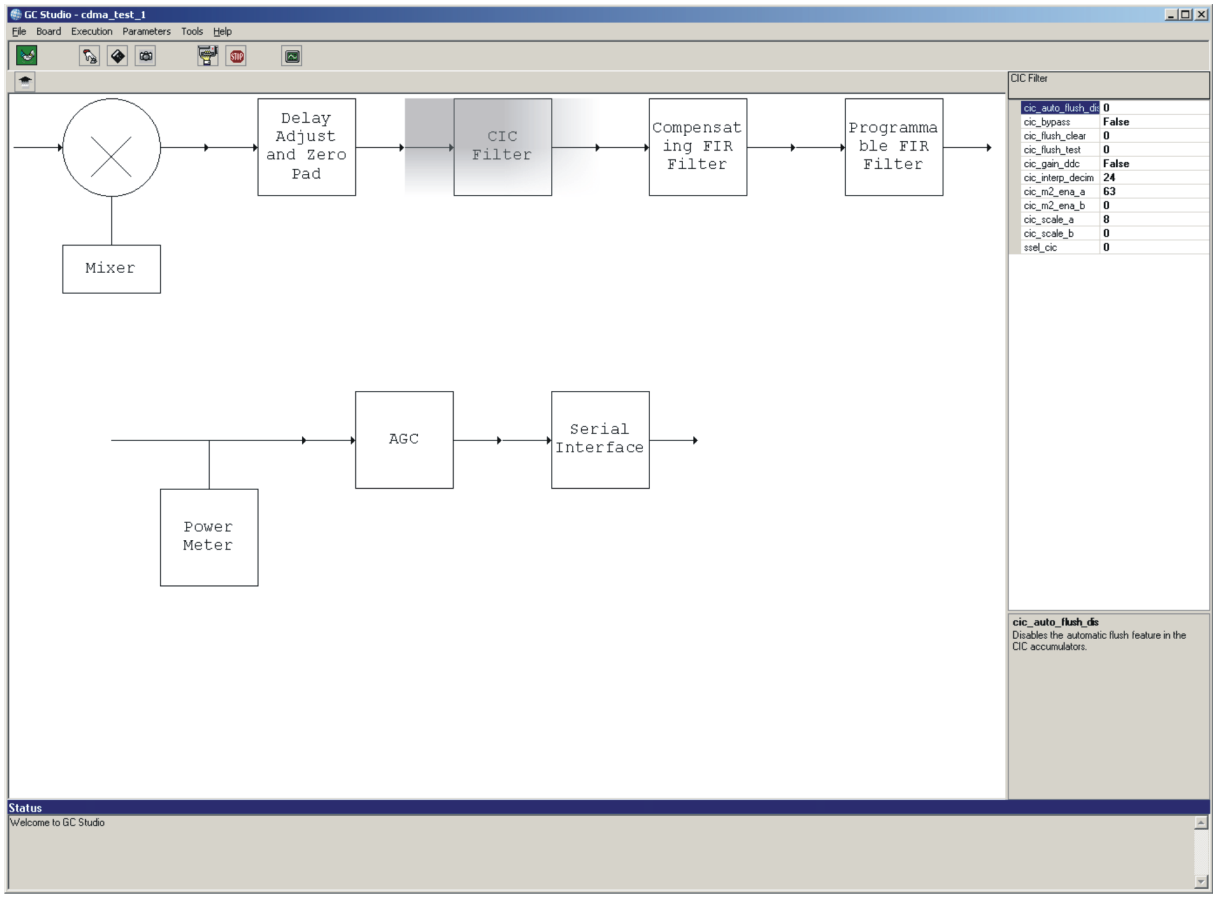

Figure 12. CDMA – CIC Filter Block

21. Select the CFIR block and set the cfir_gain to 0 (2.00E-18).
22. Next, select the cfir_coeff register setting by clicking on it, and then click on the browse button, to open the Edit Filter window and fill in the CFIR filter tap weights.

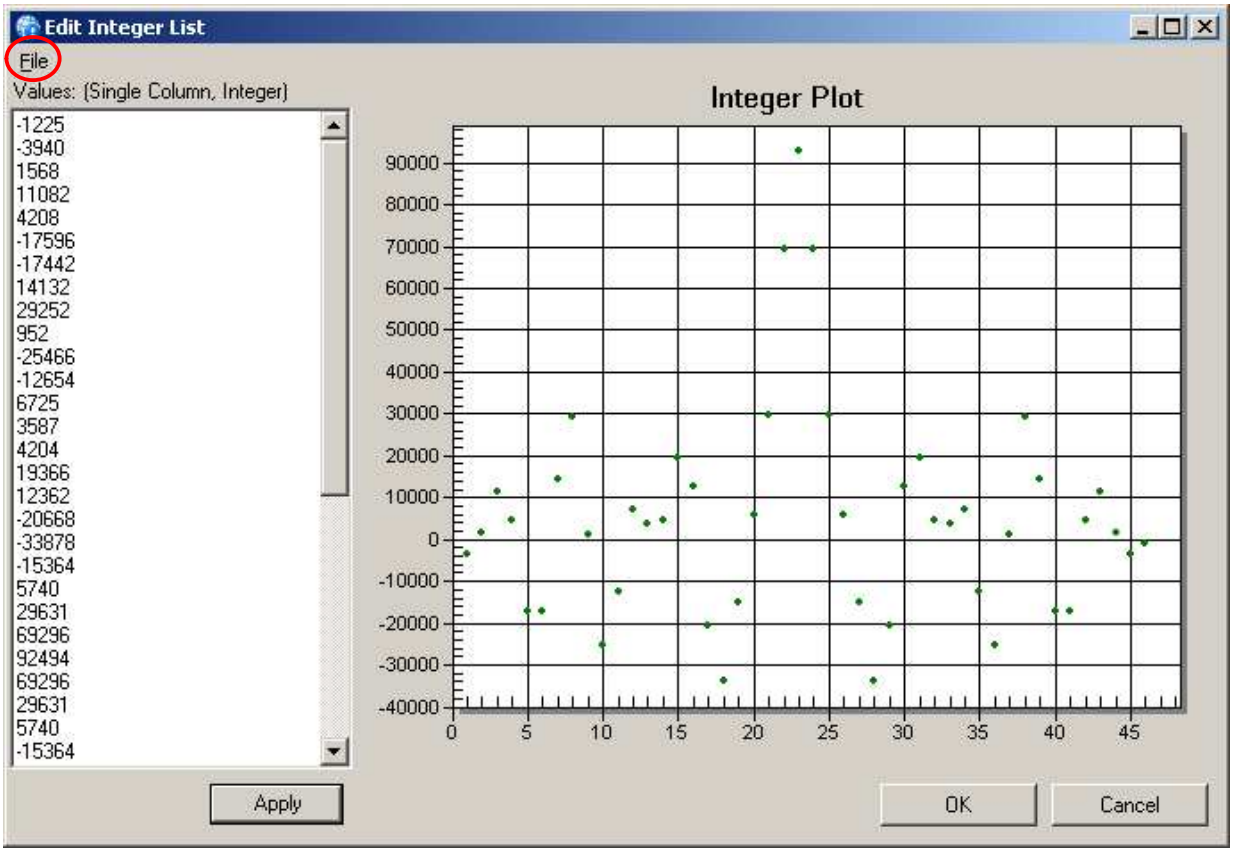

Figure 13. CDMA – Edit Filter Window

23. To load the provided Filter coefficient file, click on the File tab (circled above) then click "Load", then navigate on the provided CD for the Filter file named "CDMA_CFIR_4x2x.taps". This file contains the coefficients to be used by the CIC filter. Select this file. After the file is loaded, the Integer plot should look as shown above. Click on "OK".
24. Select the PFIR block, set the pfir_gain to 1 (2.00E-18).
25. Load the Filter coefficient file by clocking on the File tab (circled above) and by selecting the “CDMA_PFIR_2x2x.taps” file that can be found on the provided CD.

    The following 64 taps are used for the PFIR coefficients (only half are shown in Figure 14).

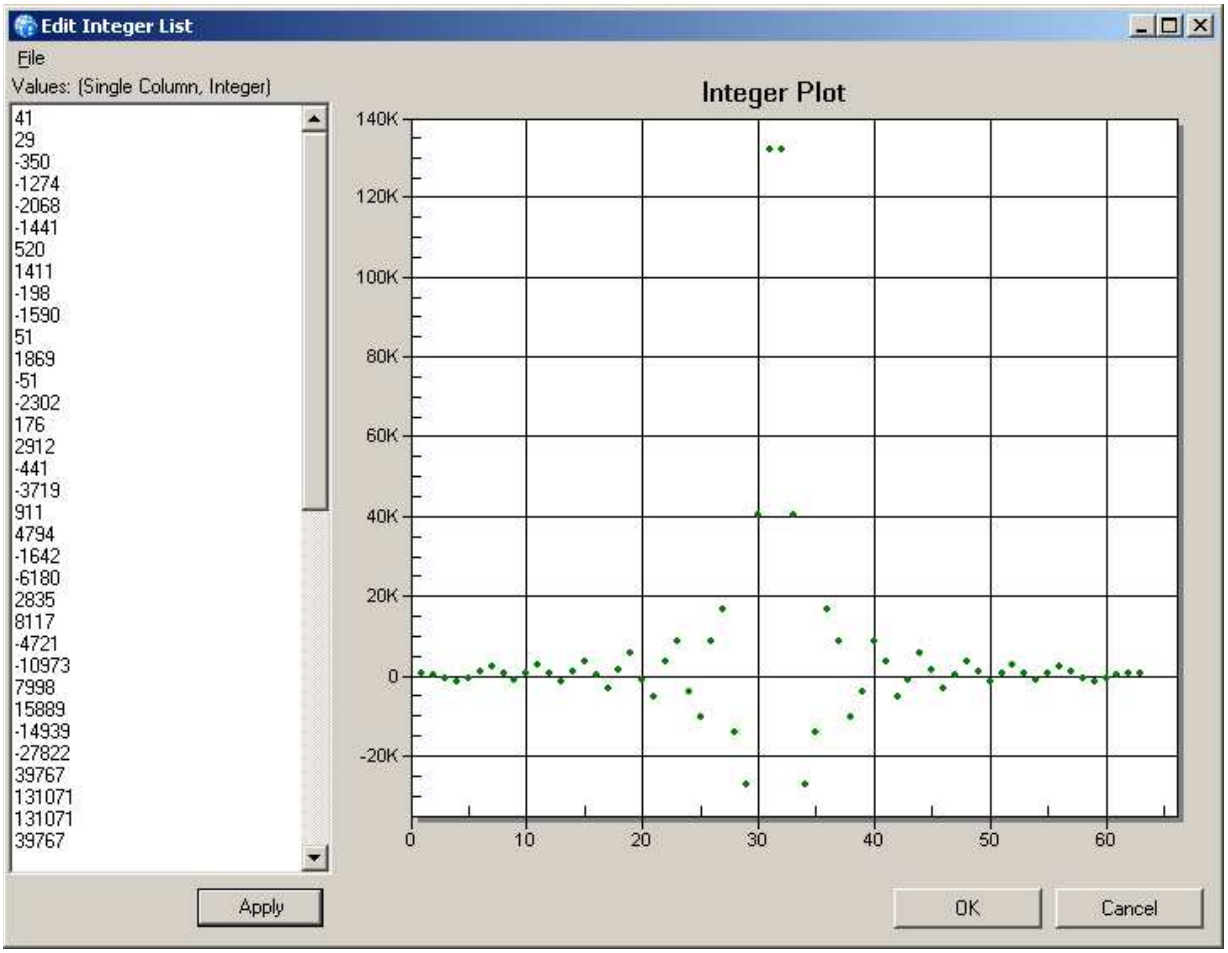

Figure 14. CDMA – PFIR Coefficients

Note: Note that these coefficients are only for learning and test purposes and would not necessarily meet CDMA Receive Specifications.

26. Click on "OK". Select the AGC block and set the registers as shown in Figure 15.

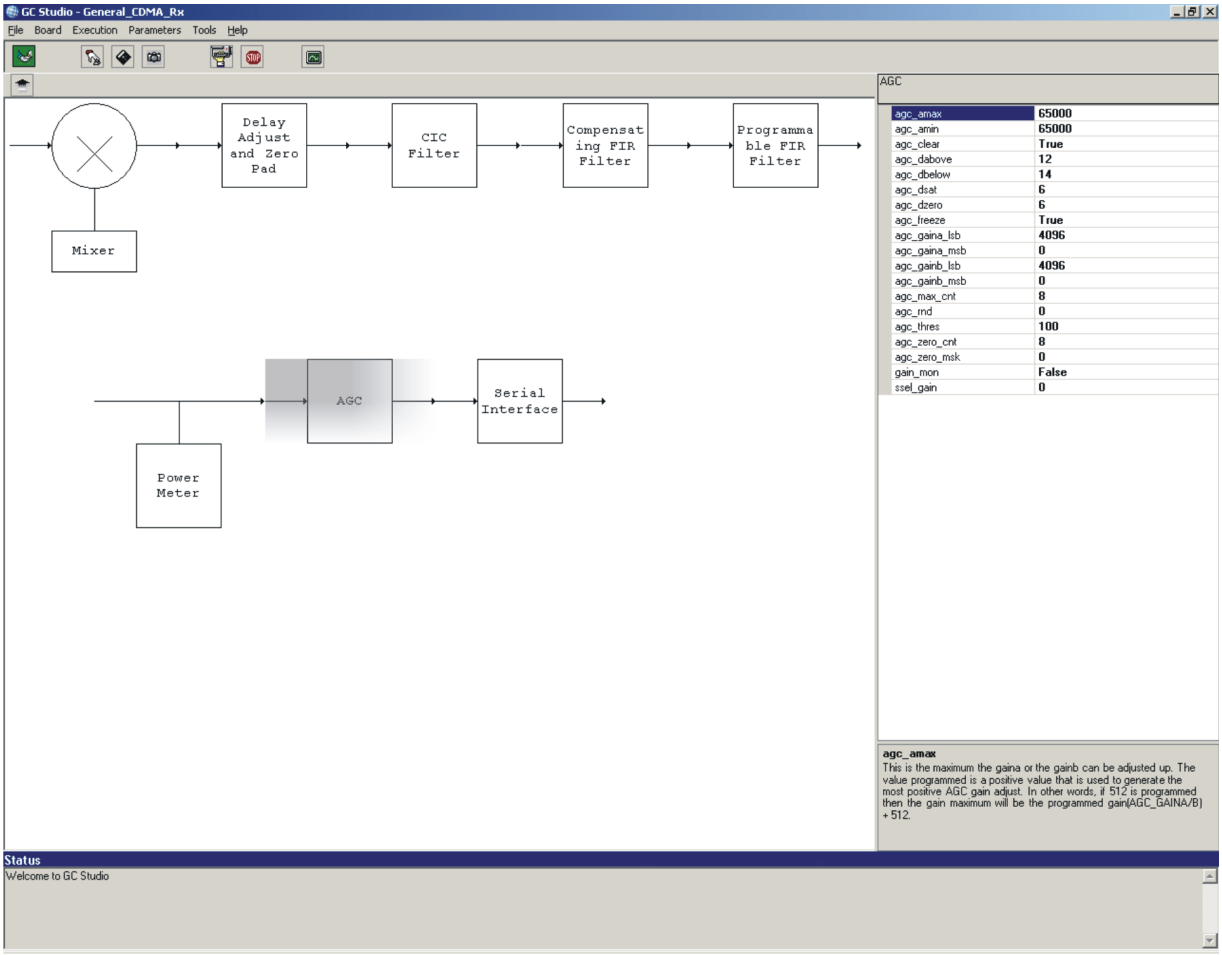

Figure 15. CDMA – AGC Block

The maximum and minimum gains are set to the same value, the agc_freeze and agc_clear are both set to True for this example. This puts the AGC in unity fixed gain mode. *GC Studio will calculate the required values for the agc_gaina_msb and the agc_gaina_lsb registers after the experiment is executed*.

27. Select the Serial Interface block and set the parameters as indicated. Since the overall decimation is 50, and the maximum number of bits on the serial output is 18 (set value to 17), the output clock rate is set to the input clock divided by 2 (program a value of 1 in the register).

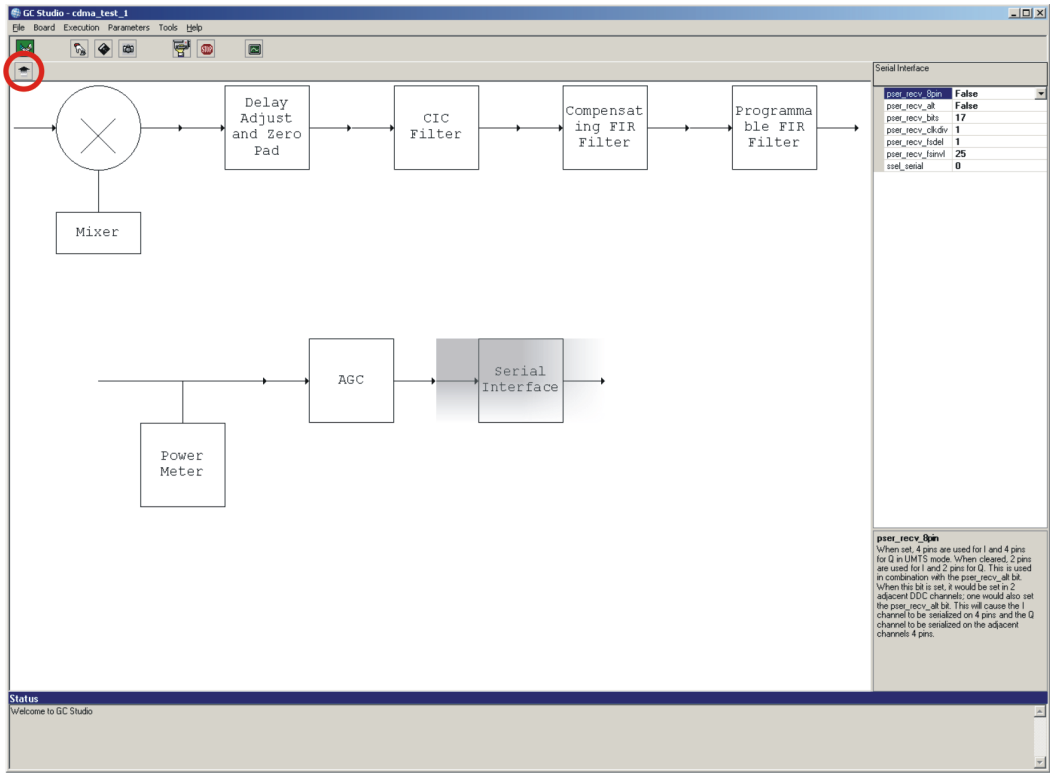

Figure 16. CDMA – Serial Interface Block

28. After verifying the values for the serial interface, click the arrow circled shown above to pop up one level in the GC5316 hierarchy.
29. Receive Channel 0 has now been configured to process:
    - a CDMA signal at 122.88Msps with a 30.72MHz IF mixer/nco block shifts the signal to DC
    - CIC block decimates by 25x to 4.9152Msps
    - 48 tap CFIR compensates for the CIC droop, filters and decimates the signal to 2.4576 MSPS
    - 64 tap PFIR filters the signal
    - Channel AGC is set to a fixed gain of unit
    - Serial interface is used to output the baseband signal at serial output clock of 61.44 MHz

30. Input data presented to the GC5316 device comes from text format data files. Two input file icons can be seen in the block diagram to the left of the Input Interface block. Click on the top icon, shown in Figure 17.

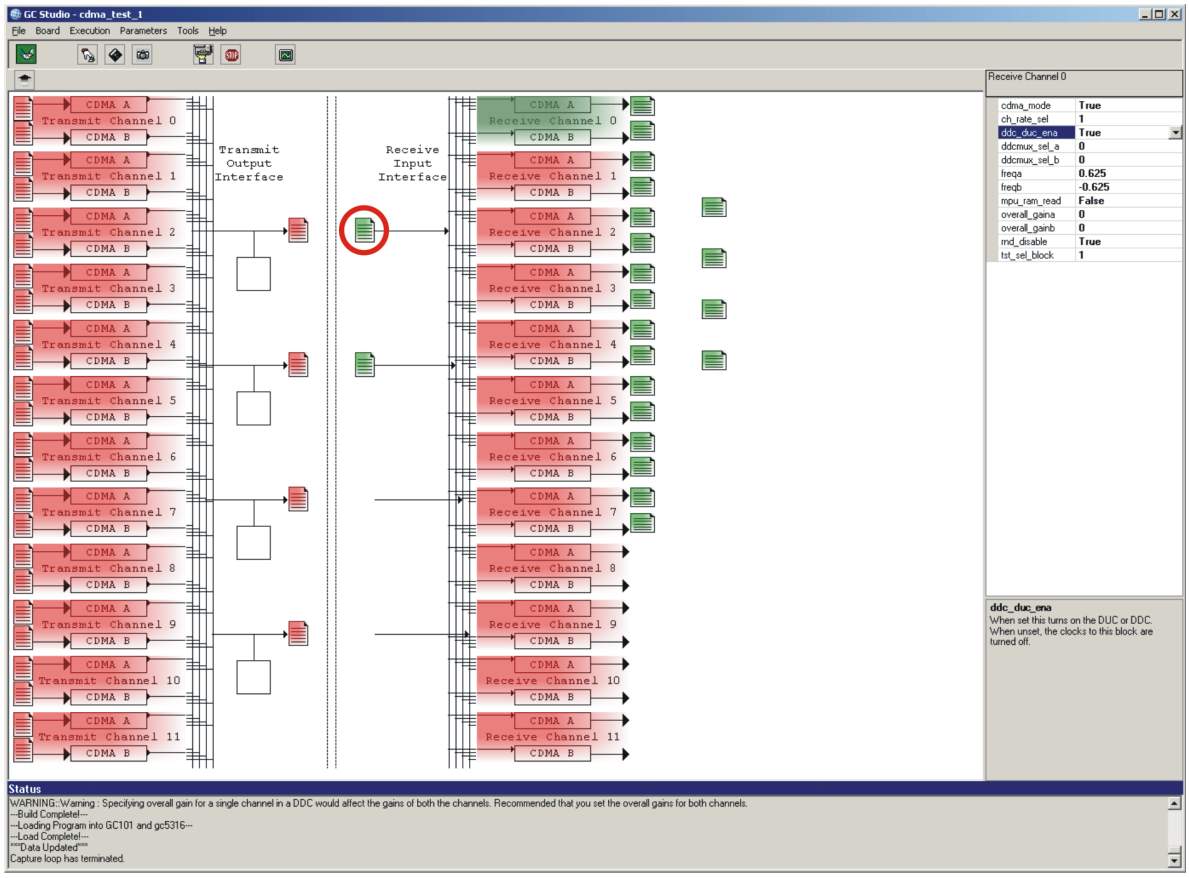

Figure 17. CDMA – Input Interface Block

31. The upper file icon is connected to the rxin_a input port, and the lower is connected to the rxin_b input port. For this demonstration, load the file pattern from file "parallel_in.gcin", located on the provided CD. Click "OK".

32. Next, click on the icon circled in Figure 18 for the graphical display settings.

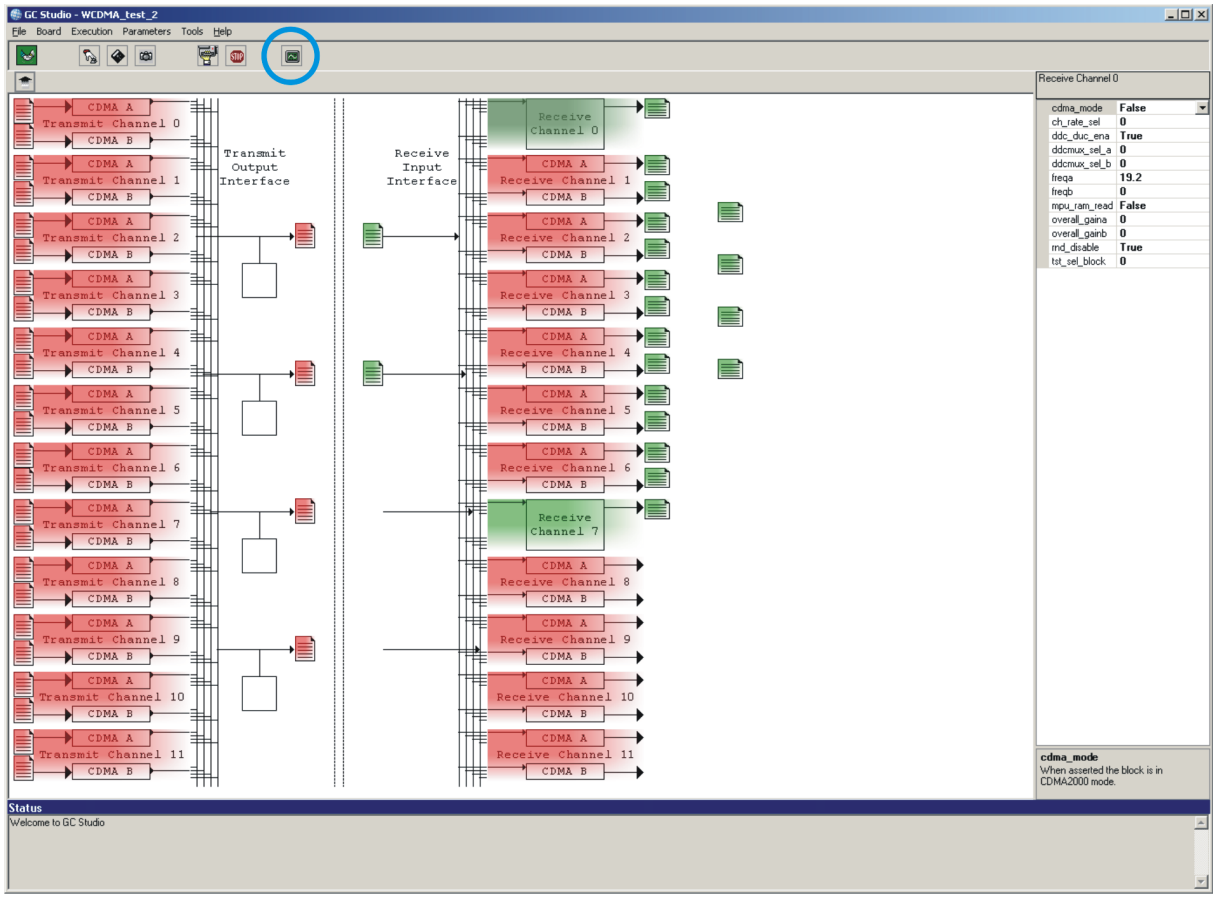

Figure 18. Graphical Display Settings

33. Click the Add New Data Source button circled in Figure 19.

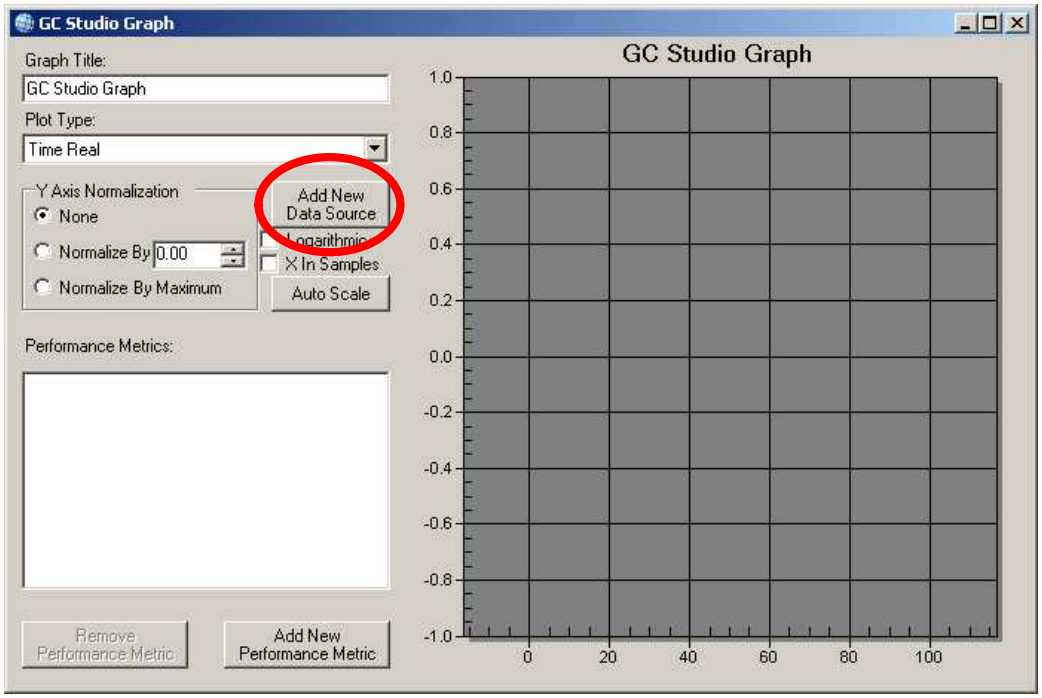

Figure 19. CDMA – Add New Data Source

34. In the Choose Source panel, select Receive Output Port A, and click "OK".

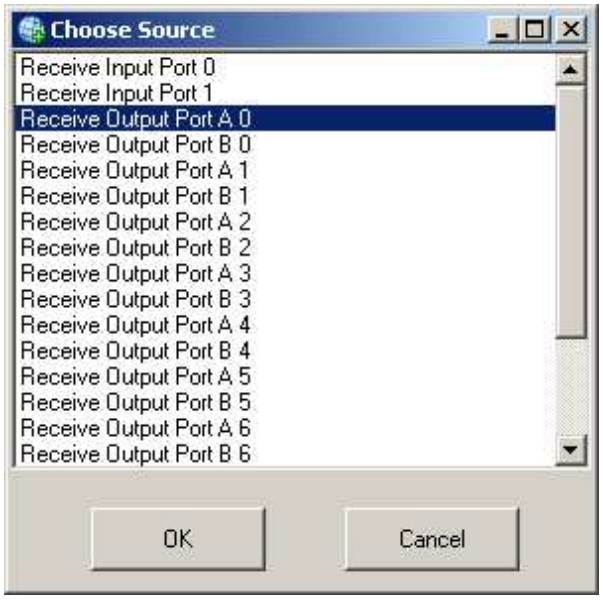

Figure 20. CDMA – Choose Source Panel

35. In the graph panel, set the Plot Type to Spectral Magnitude, and check Logarithmic.
36. Next, copy the settings from Receive Channel 0 to Receive Channel 7, to match the delays for the capture, by going to Parameters, and selecting the channel copying option. Channel 7 should turn green as shown in Figure 21.
37. On the GC Studio panel, click the Build and Load buttons shown in Figure 21. This will execute the experiment.

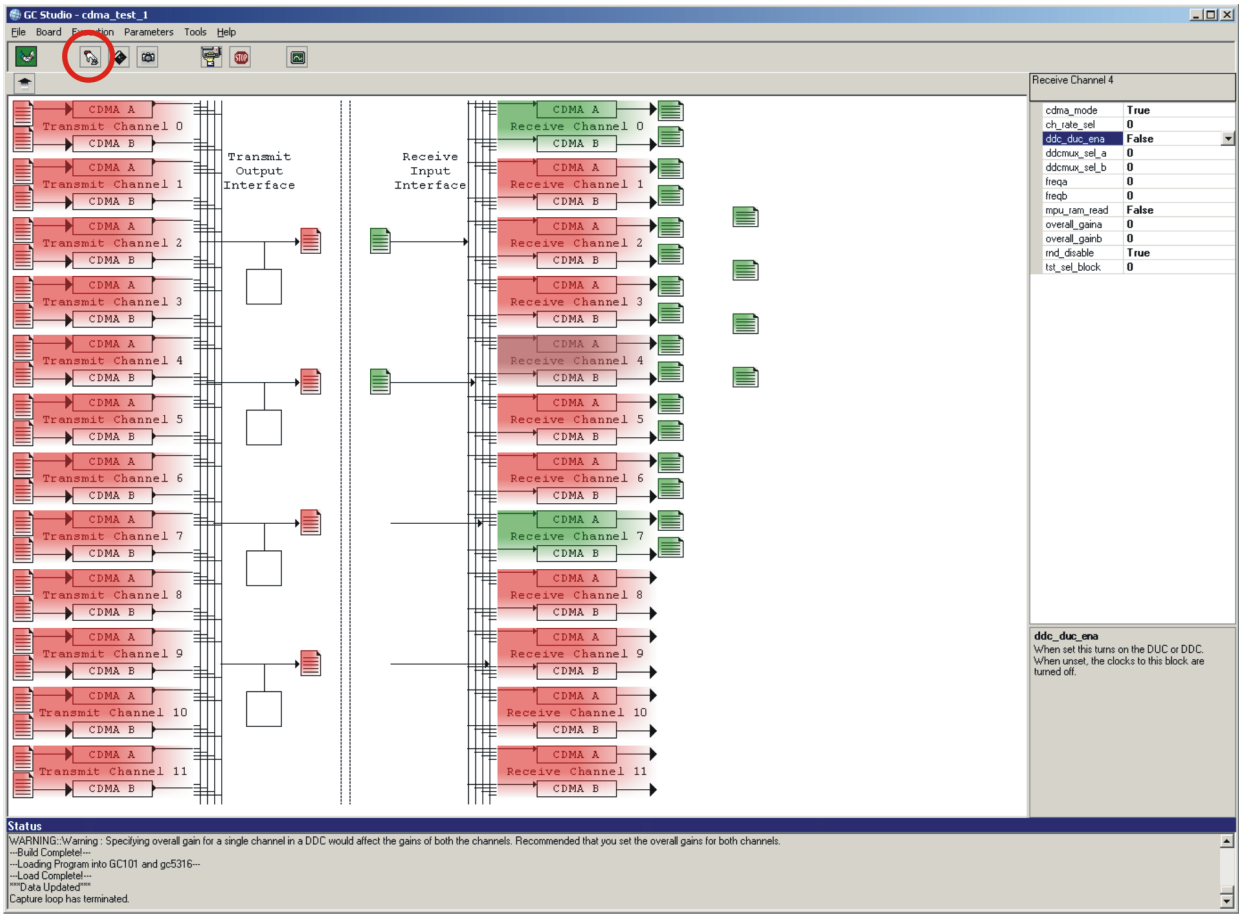

Figure 21. CDMA – Build and Load Buttons

38. The graph window will be automatically updated with the results shown in Figure 22.

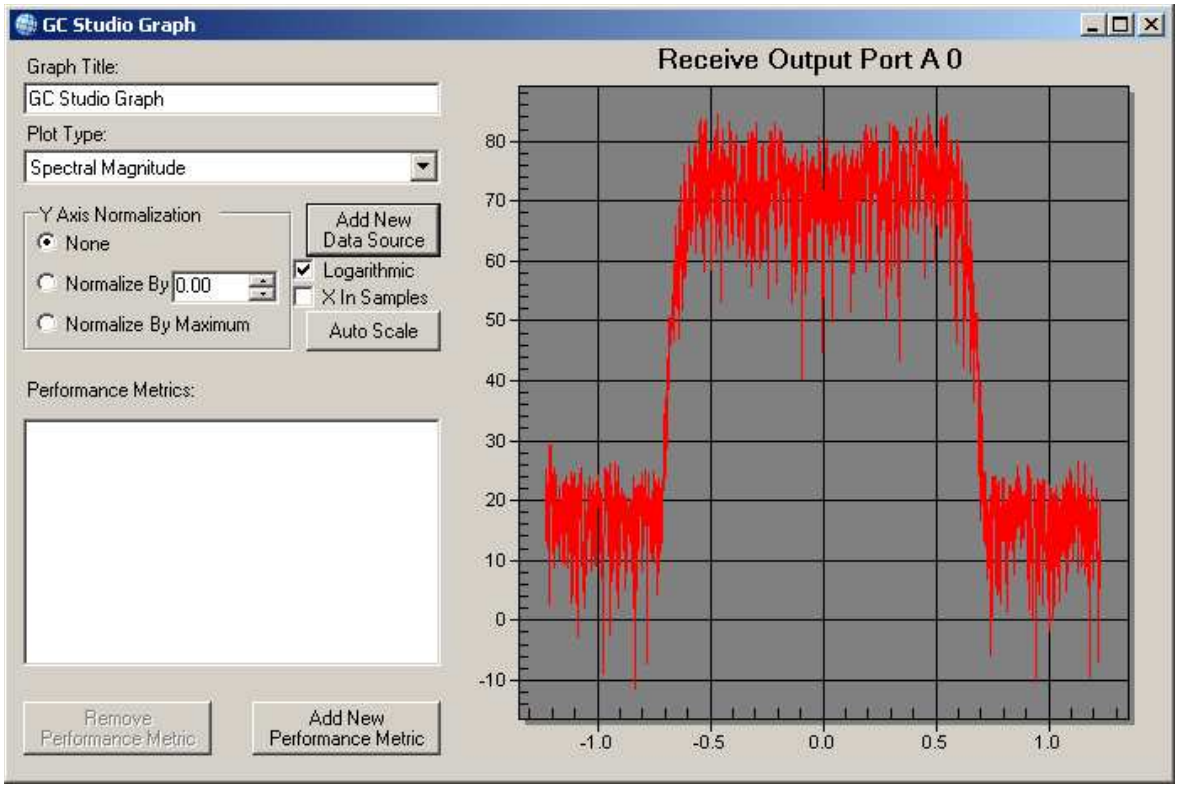

Figure 22. CDMA – Graph Window

39. On the GC Studio panel, click on the stop button, shown circled in Figure 23, to stop the experiment, then select File -> Save Project to save this project.

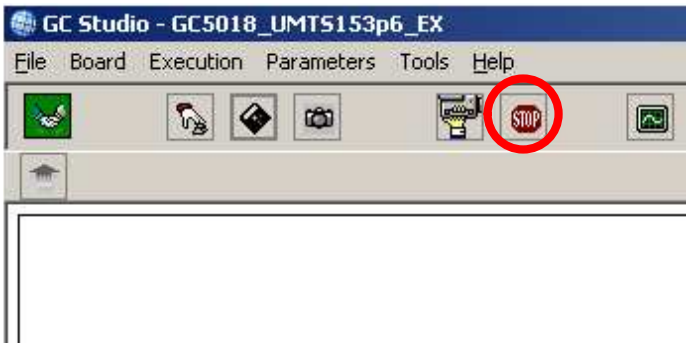

Figure 23. CDMA – Stop Experiment and Save Project

40. Close the GC Studio Graph Window.
41. The raw response memory can be captured in a text format by selecting "Options…" in the Tools > window. Select the Debug tab, then select the "Dump Contents of Response Memory" option. Enter a file name for the data to be written to.

Figure 24. CDMA – Tools -> Options Window

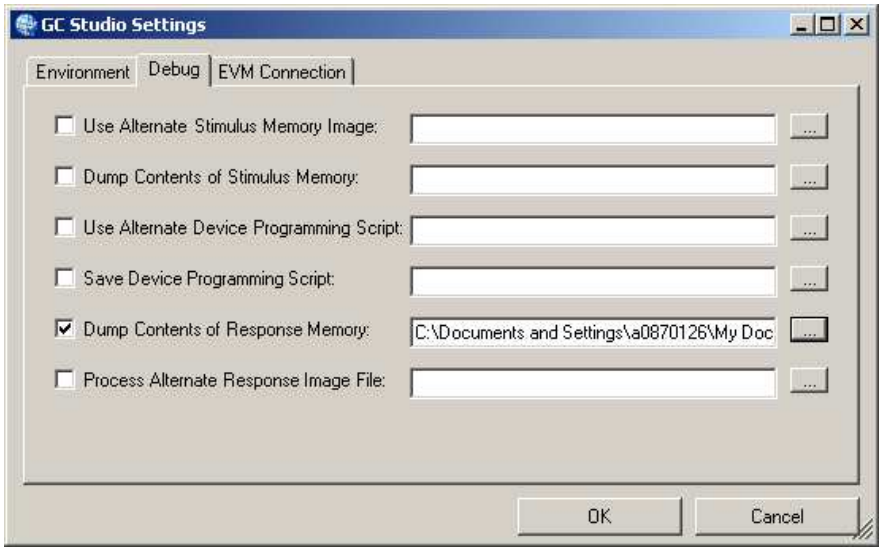

Figure 25. CDMA – Capturing Raw Response Memory in Text Format

For this file to be generated, you must run the experiment after making this change.

The format of the file is hexadecimal, with the 32 bit response memory as the first 8 characters, a space, and then a single character for the other 4 special bits {sp7, sp6, sp5, syncout+} as shown below.

```
00000000 0
00000000 0
00000000 0
00000000 0
00000000 2
00000000 2
00045000 0
00045000 0
00045000 0
00045000 0
```

2.2.2 Creating a New GC Studio Project for a TD-SCDMA Transmit Configuration

- Eight Real baseband TD-SCDMA signals are applied to the GC5316 inputs with an input rate of 1x (1.28 MSPS)
- Simulated txclk to the GC5316 is 81.92MHz (64x)
- The PFIR interpolates by two, and is configured for 63 taps
- The CFIR interpolates by two, and is configured for 31 taps
- The CIC filter is programmed to interpolate by 16, and uses 6. The output sample rate at the CIC output is 81.92 MSPS.
- The NCOs and Mixers are set to eight different IFs
- Eight outputs from four channels are MUXed on the output bus

1. Start GC Studio
2. Click on File > New Project to bring up the following window.
3. Choose a name for this new project, and click create.
4. Select GC5316 for the Plugin and click OK.
5. Using the wizard style interface, setup the GC101 evaluation board, then click next.
6. Setup the GC5316 I/O mode selection as shown and click next.

   In this example, be sure the ADC clock rate is set to 1. Because we are using the transmit channels for this experiment, set the Input Mode and Output Mode boxes to Receive Ports as shown below. We will ignore the Output Clock Source and leave it also set to TX Clk Out. Click “Next” to see the Simulated Clock Rates screen.

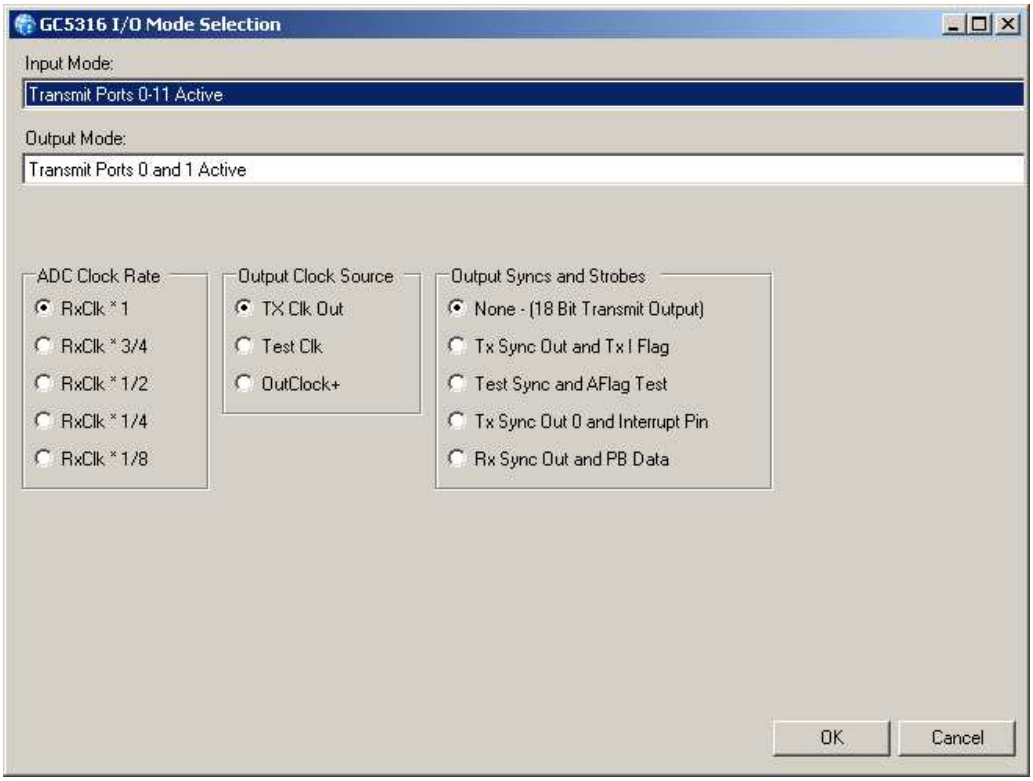

Figure 26. TD-SCDMA – I/O Mode Selection

7. Set the simulated clock rate to 81.92 MHz and click next.

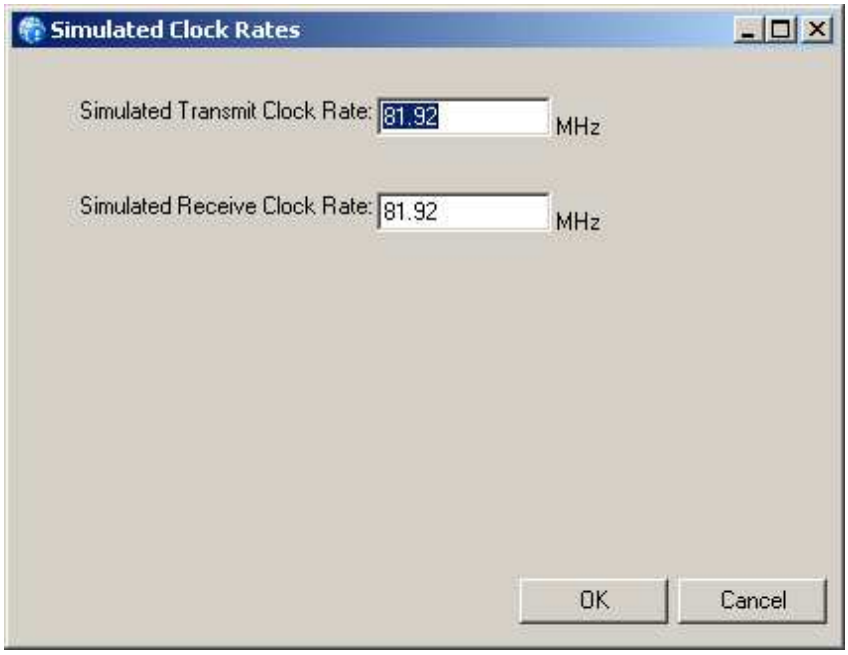

Figure 27. TD-SCDMA – Simulated Clock Rates

8. Channel Copying will be skipped for now, click Next.

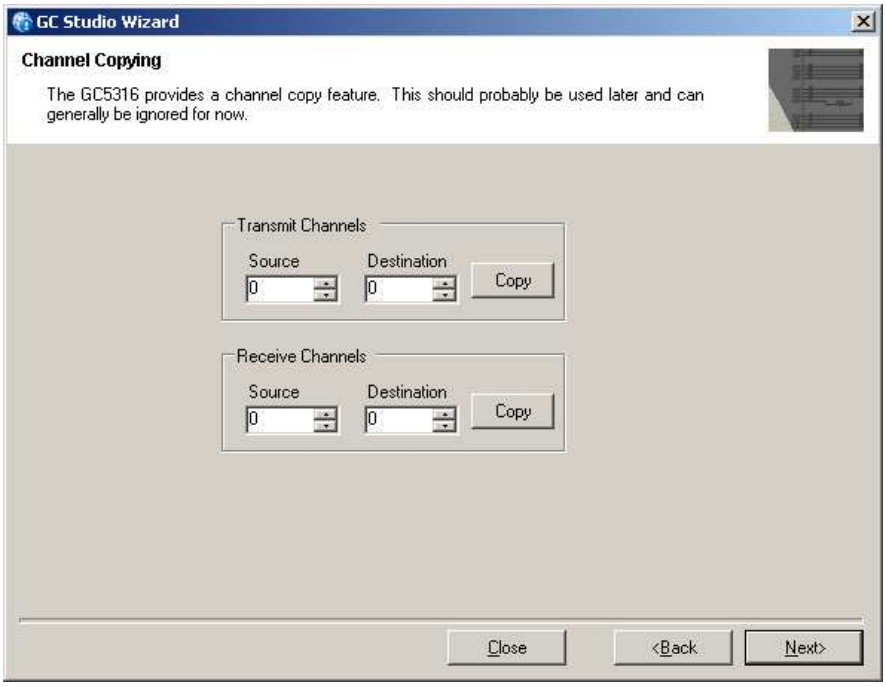

Figure 28. TD-SCDMA – Channel Copying

9. Finish the set-up Wizard as explained in the previous example.
10. Click on the large gc5316 box to display the global control registers.

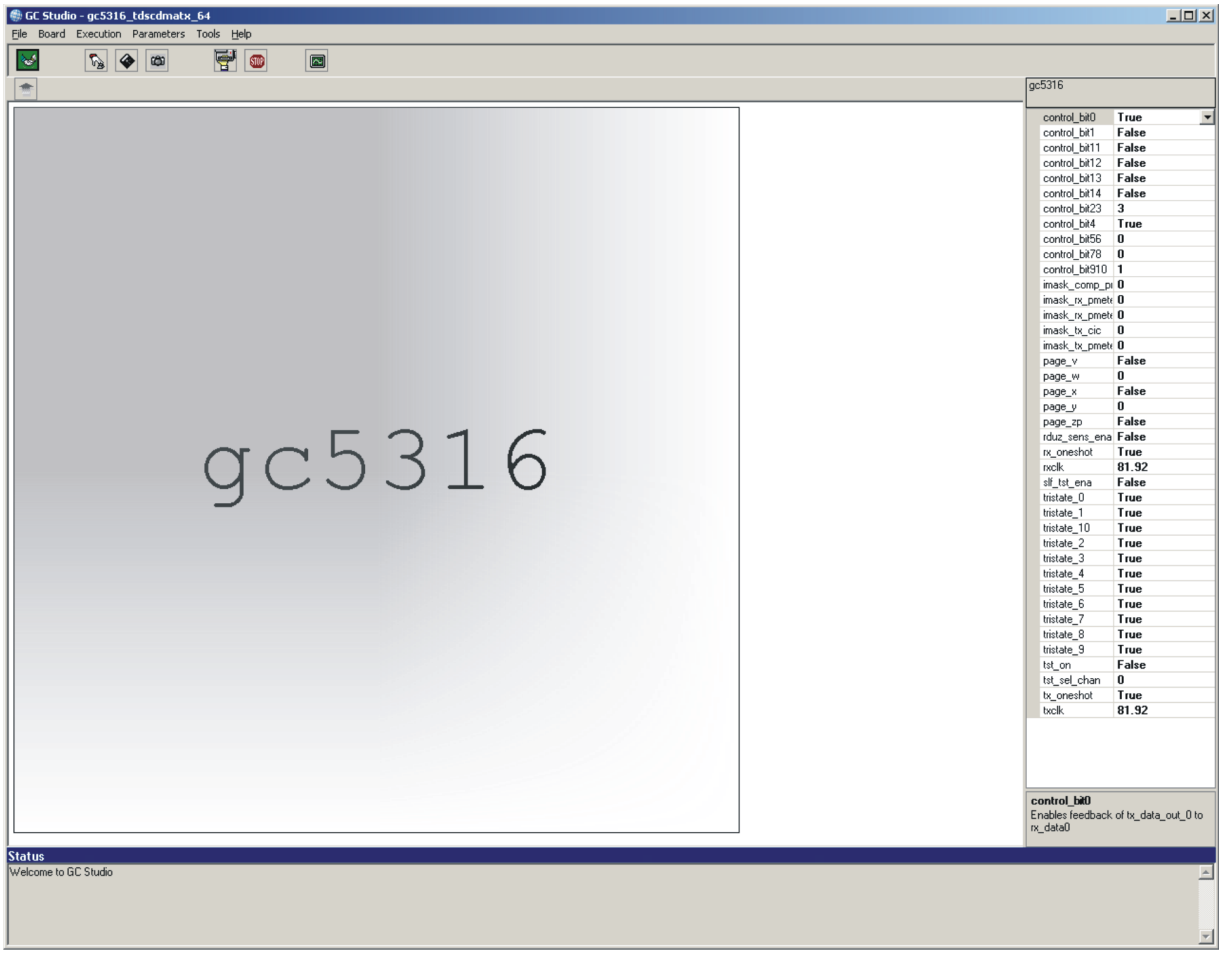

Figure 29. TD-SCDMA – Displaying Global Control Registers

11. Next, double click on the gc5316 block to “push down” one level into the gc5316.
12. Click on the Input File block (in blue), then load the file parameters by clicking to the field on the right (in red). Load the input files at zero IF.

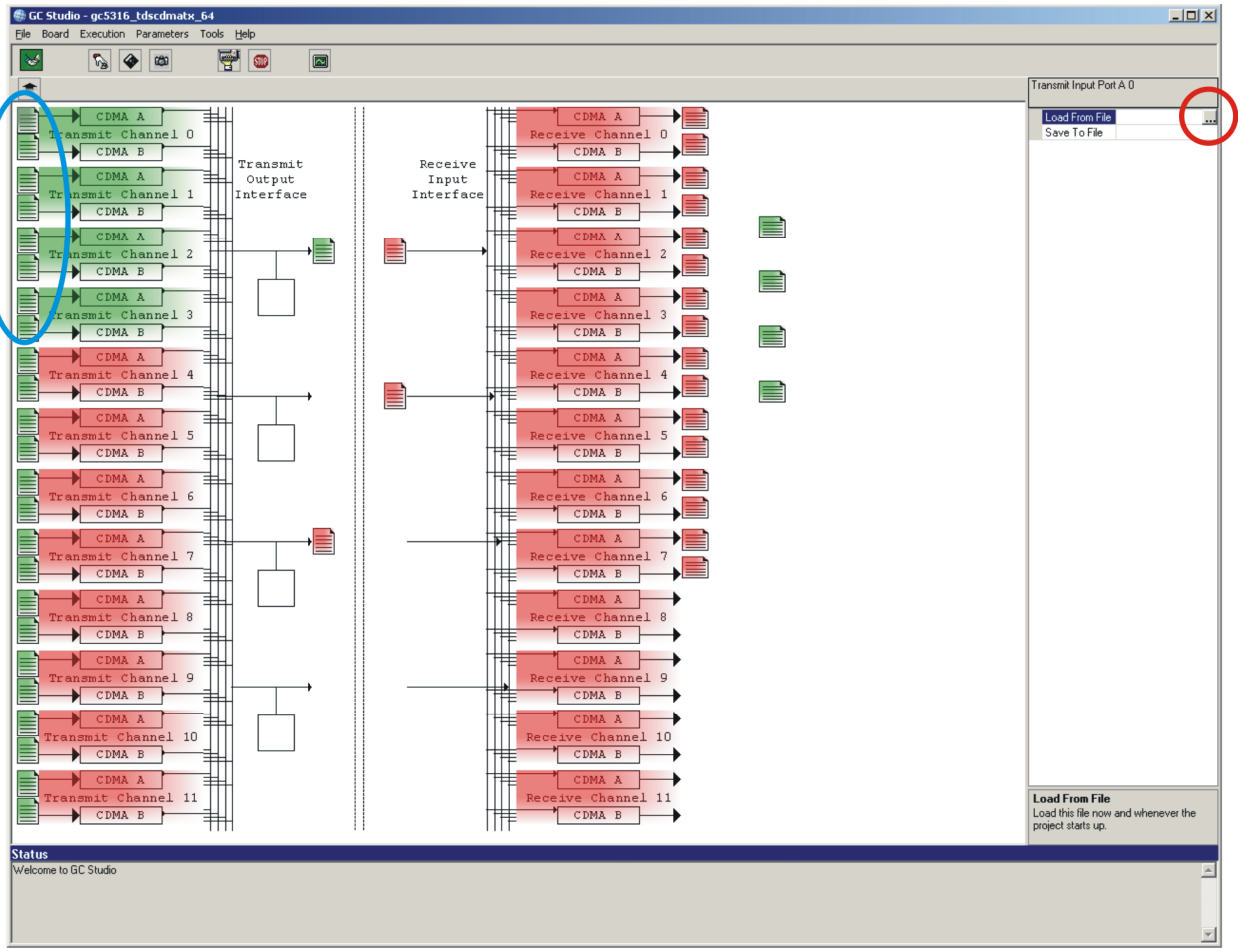

Figure 30. TD-SCDMA – Input File Block

13. Click on the upper Transmit Channel 0 block. Set ddc_duc_ena to True. Make sure that the cdma_mode is set to True.
14. Set the freqa to 9 (MHz) and freqb to -1. Since this example explains 8-channel output, NCO frequencies need to be set in channels 0-3. Also, since all eight channels will be summed on the same output, make sure that “sumchn_sel_a” and “sumchn_sel_b” of all four channels (0-3) is set to same output port, in this case to 1.

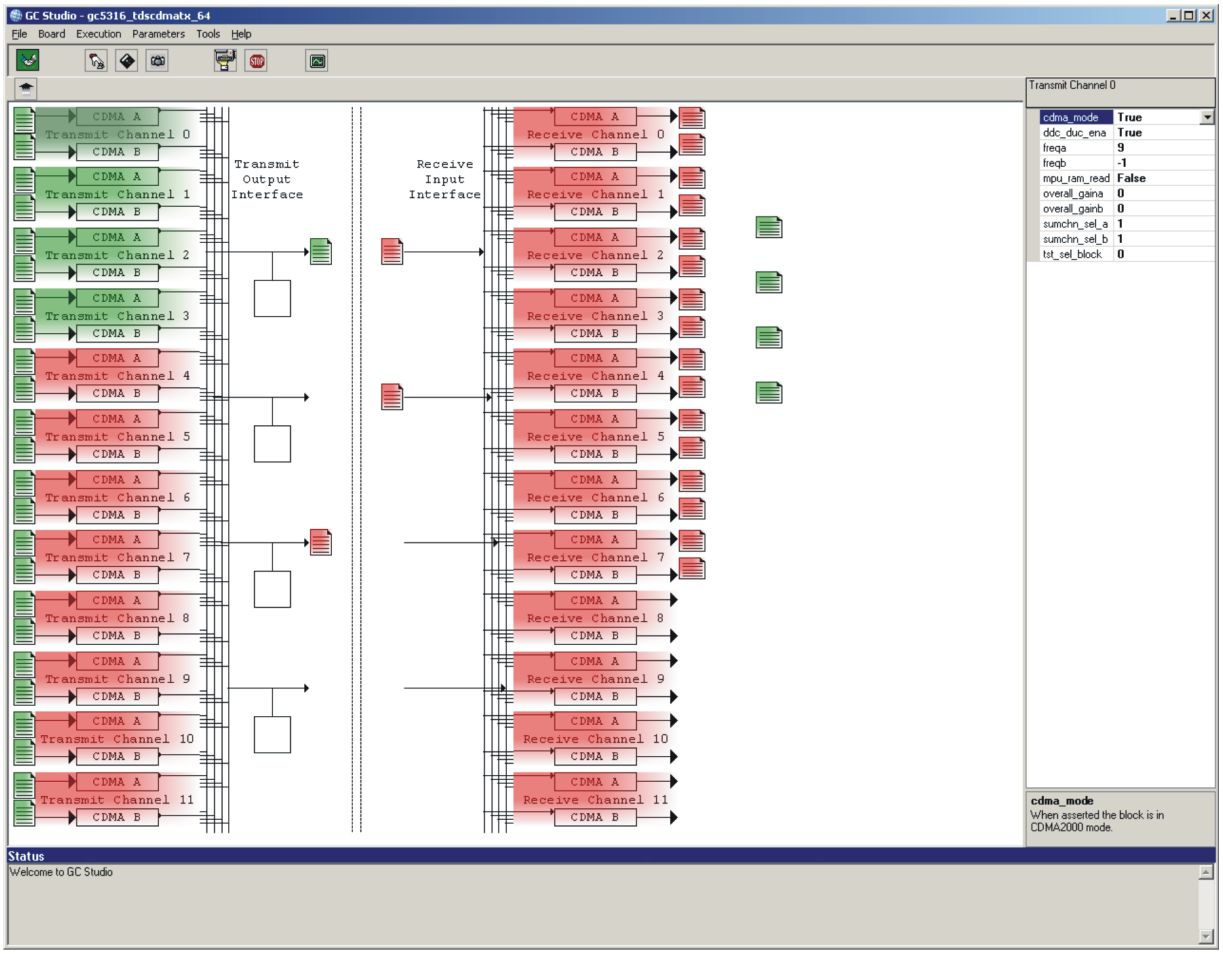

Figure 31. TD-SCDMA – Transmit Channel Block

15. Double-click on the Transmit Channel 0. The serial interface number of input bits should be set to 16 (“serp_tran_bits” = 15).

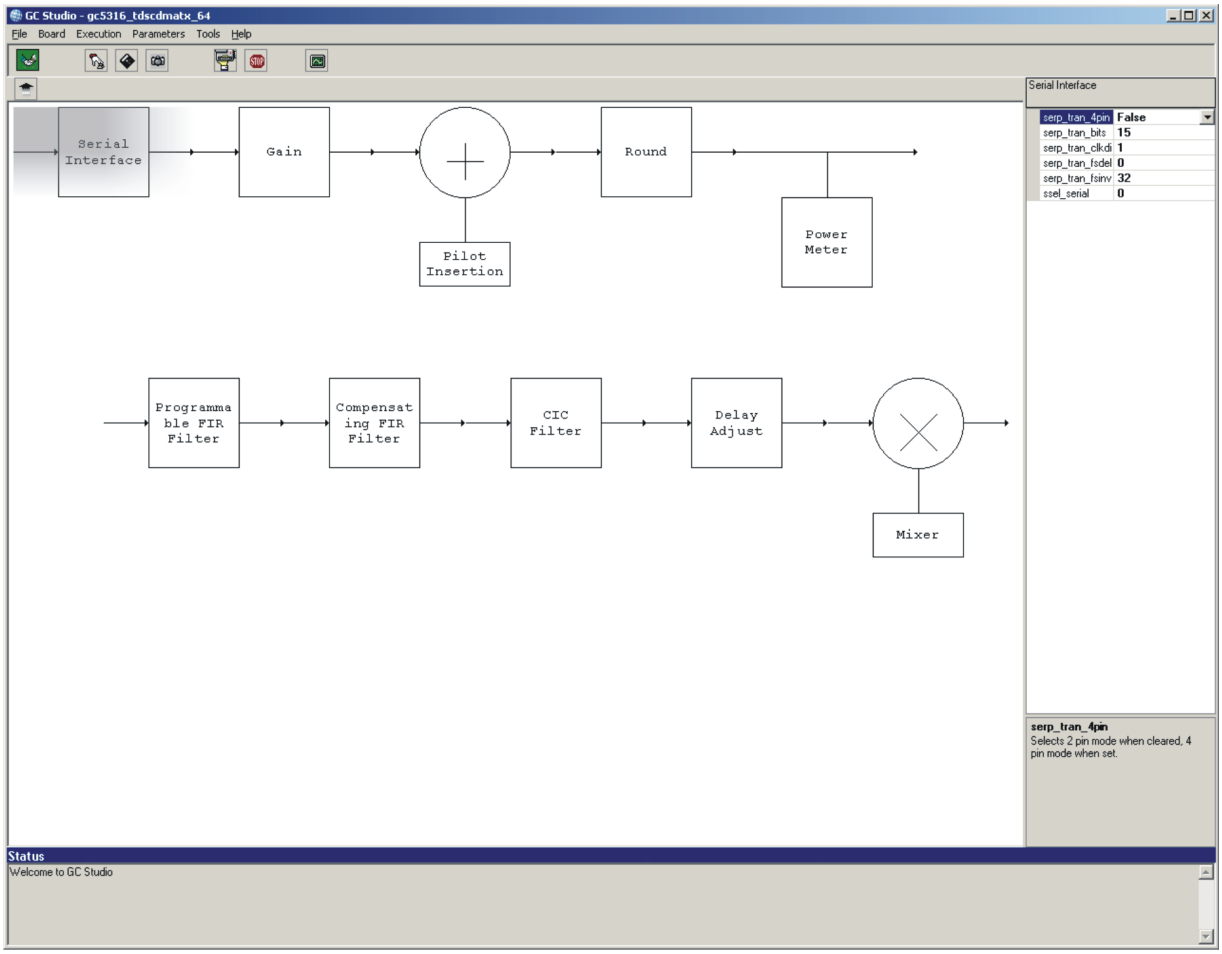

Figure 32. TD-SCDMA – Transmit Channel 0

16. Next, set the value for the input gain.

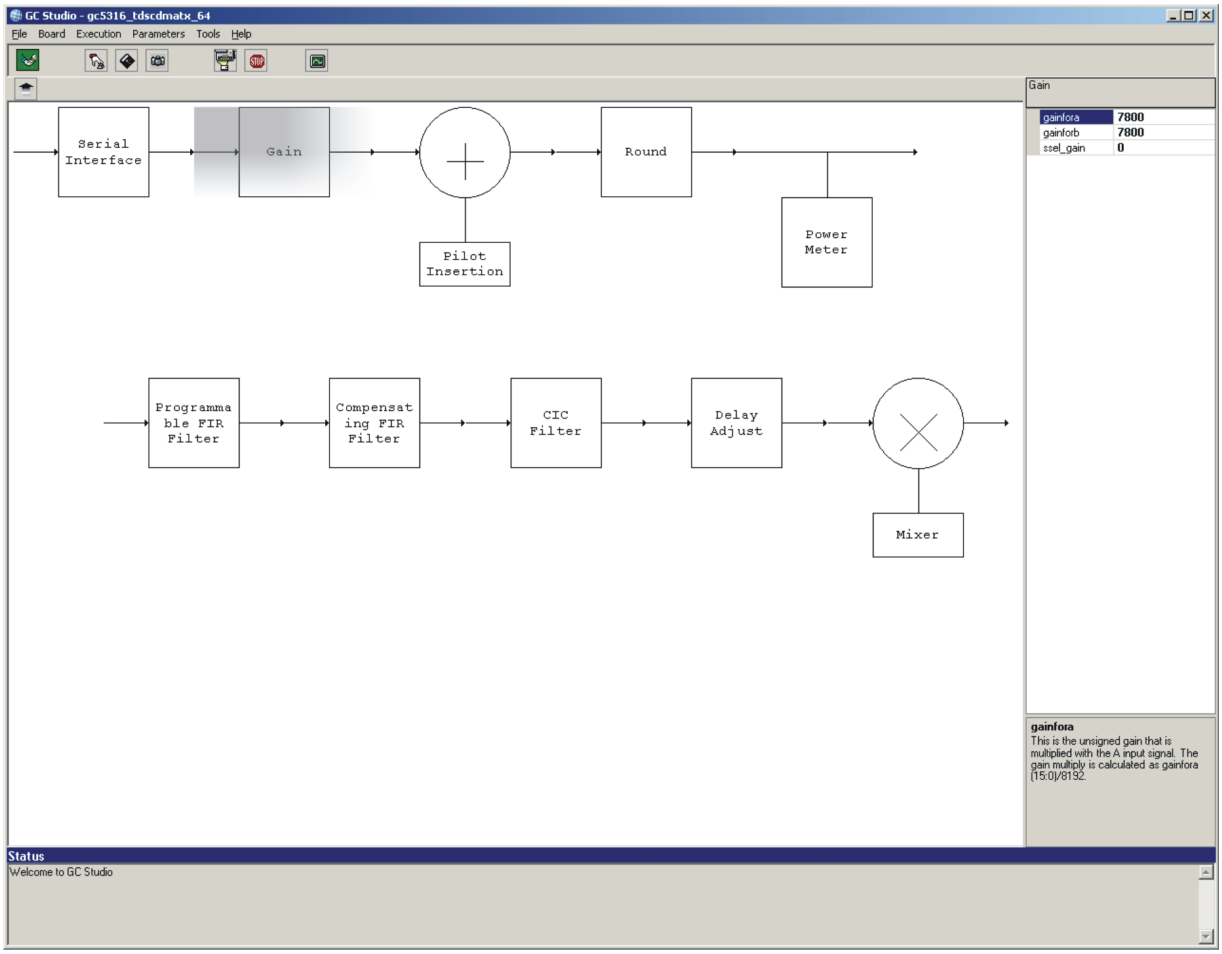

Figure 33. TD-SCDMA – Input Gain Setting

Notice the Pilot insertion is available for CDMA application. The Power Meter is provided but will not be used in this example.

17. Select the PFIR block and set the cfir_gain to 0 (2.00E-19).

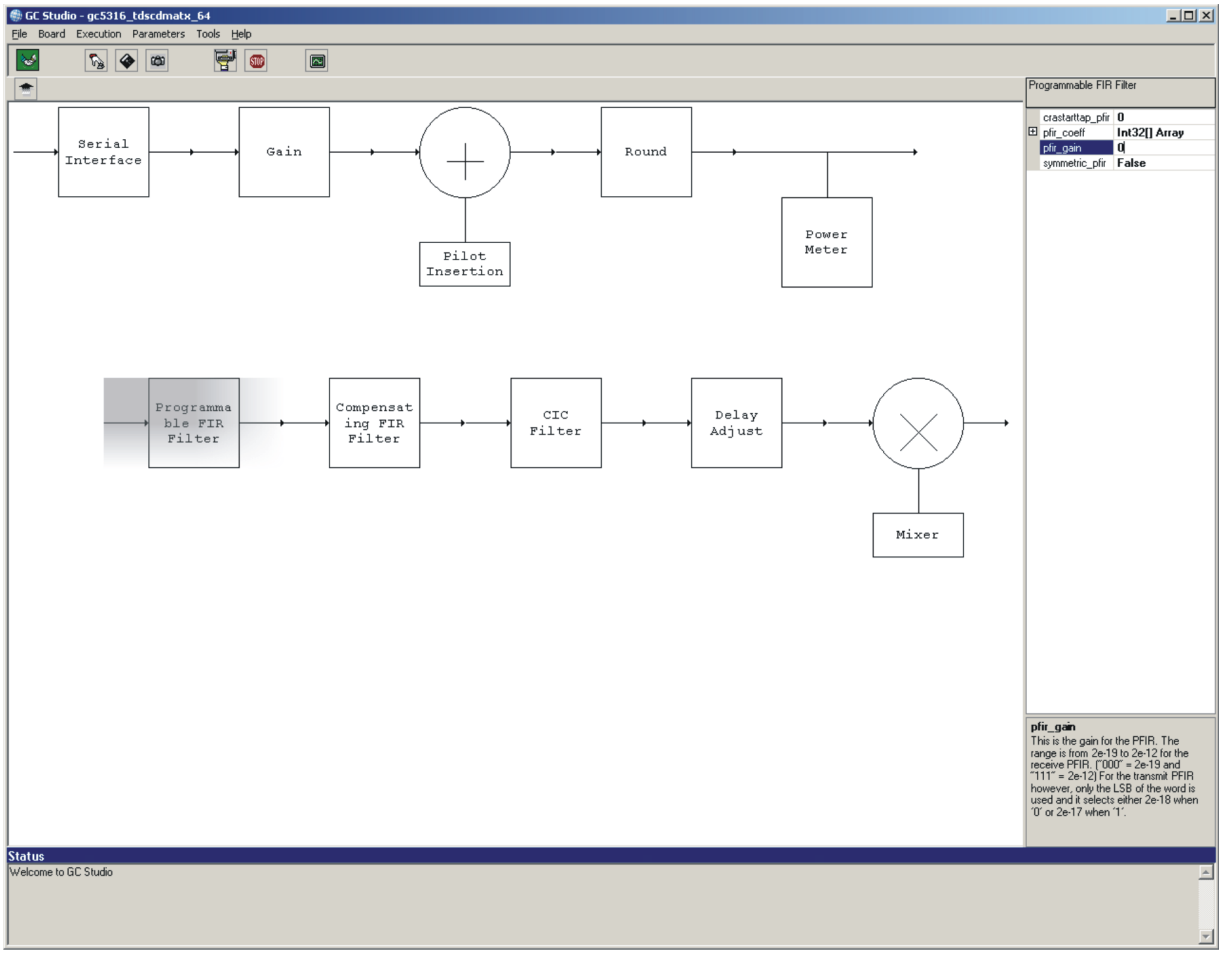

Figure 34. TD-SCDMA – PFIR Block

18. Next, select the pfir_coeff register setting by clicking on it, and then click on the browse button, to open the Edit Filter window and fill in the PFIR filter tap weights.

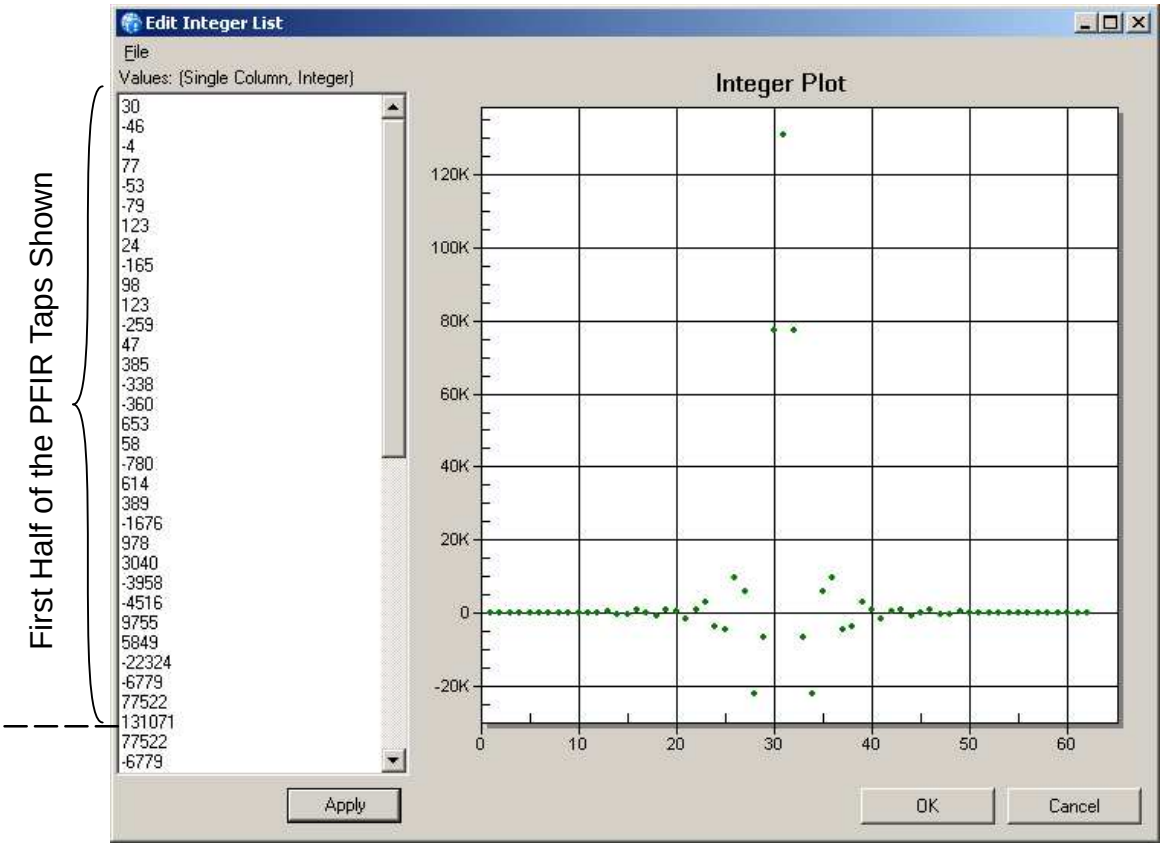

Figure 35. TD-SCDMA – pfir_coeff Register Setting

19. Select the CFIR block next, set the cfir_gain to 0 (2.00E-18).

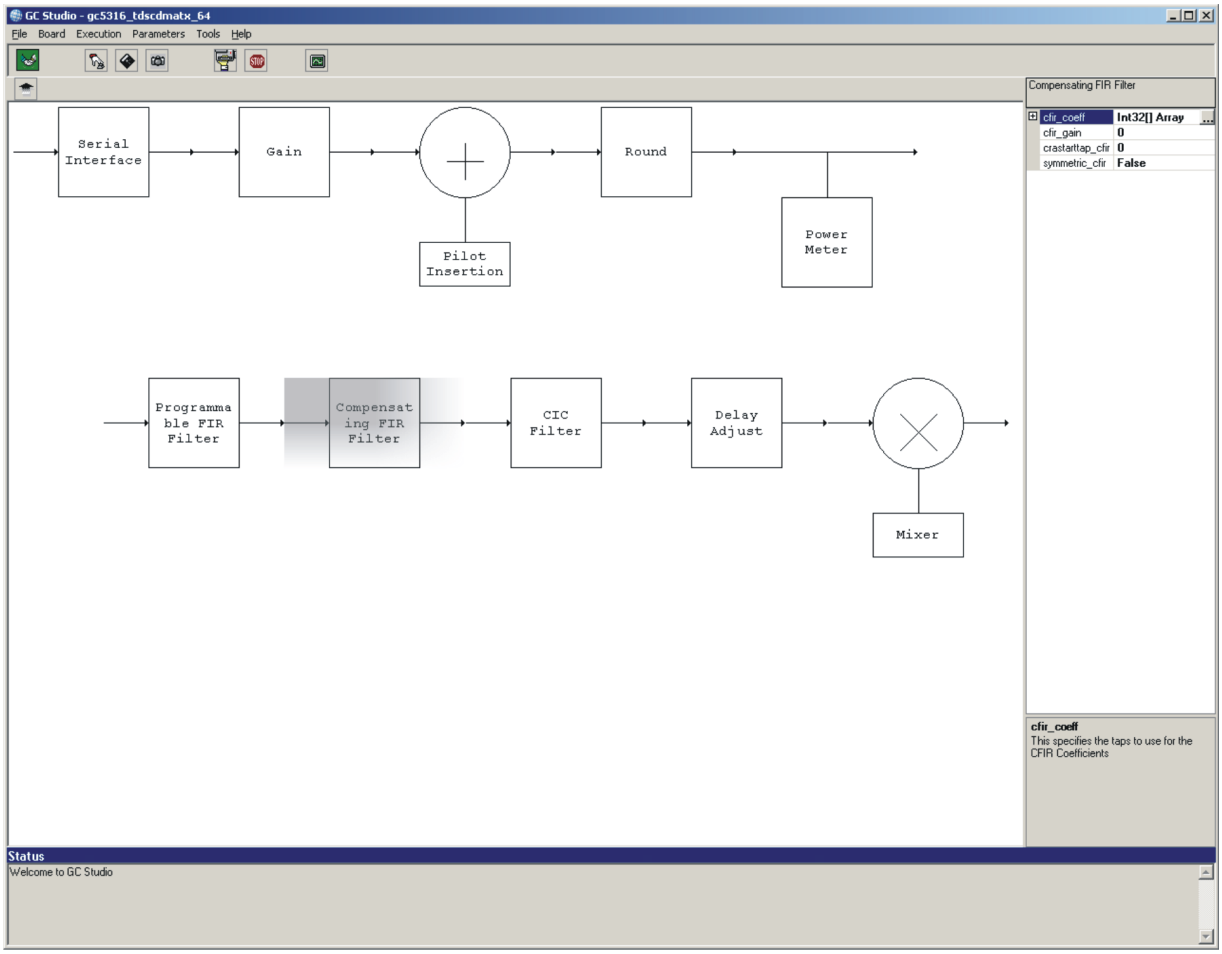

Figure 36. TD-SCDMA – CFIR Block Setting

20. Select the pfir_coeff register, and again select the browse button.

21. Enter the following 31 taps for the CFIR coefficients.

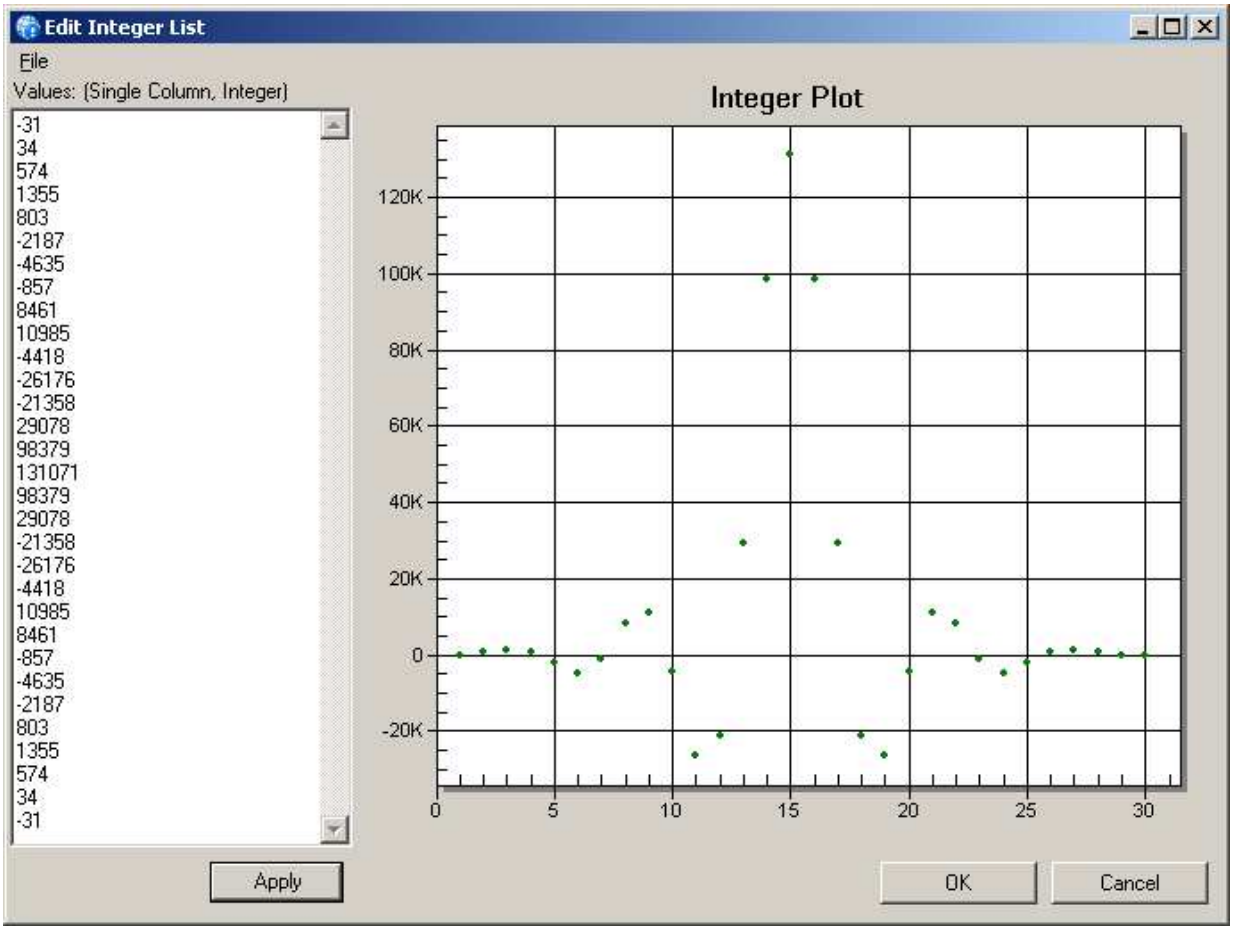

Figure 37. TD-SCDMA – CFIR Coefficients

22. Next, select the CIC Filter block. Set the interpolation to 16 (“cic_interp_decim” = 15), and the CIC scale factor to (pre-calculated) value of 12. Please see the datasheet about the formulas to calculate the CIC Filter scale values (“cic_scale_x”).

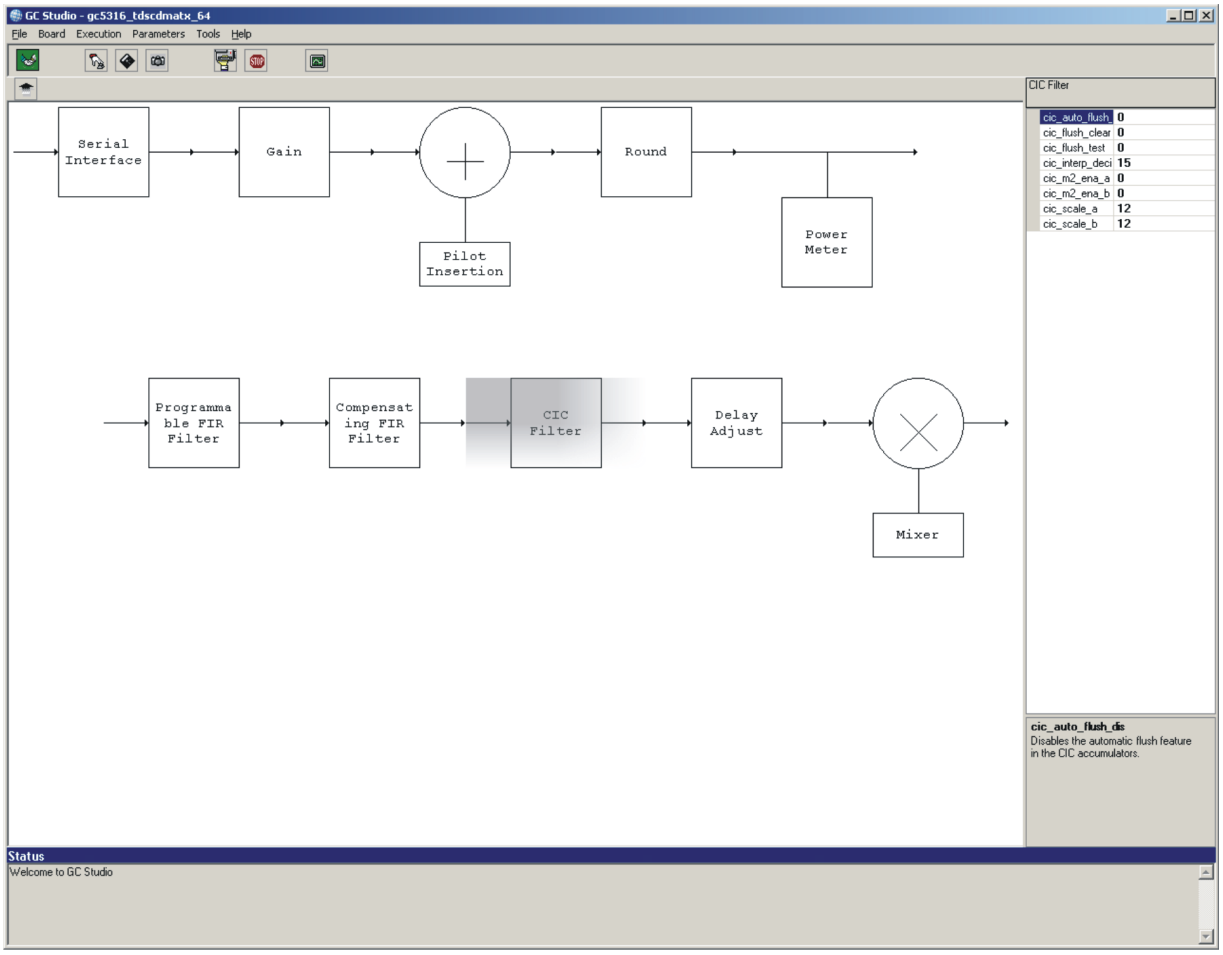

Figure 38. TD-SCDMA – CIC Block Filter

The other parameters can be set as default when GC Studio opened.

23. Transmit Channel 0 has now been configured to process:
    - A TD-SCDMA signal from the input rate of 1.28Msps with a 0 MHz IF
    - The PFIR shapes the signal, and interpolates by two; the output of the PFIR is at 2.56 MSPS
    - The CFIR further filters the unwanted interpolation images and filters images outside the band of interest. The CFIR interpolates by 2; the output of the CFIR is at 5.12 MSPS
    - The six-stage CIC filter interpolates by 16, to the final output rate of 81.92 MSPS.
    - The NCO is set for the mixing frequency in mixer.

    After all four channels are appropriately set, the block diagram should show first four channels as active (green).

    Input data presented to the gc5316 pins comes from text format data files. Two input file icons can be seen in the block diagram to the far left since the mode is set to CDMA

24. Click on the top icon, circled as shown in Figure 39, and make sure that the input files are selected.

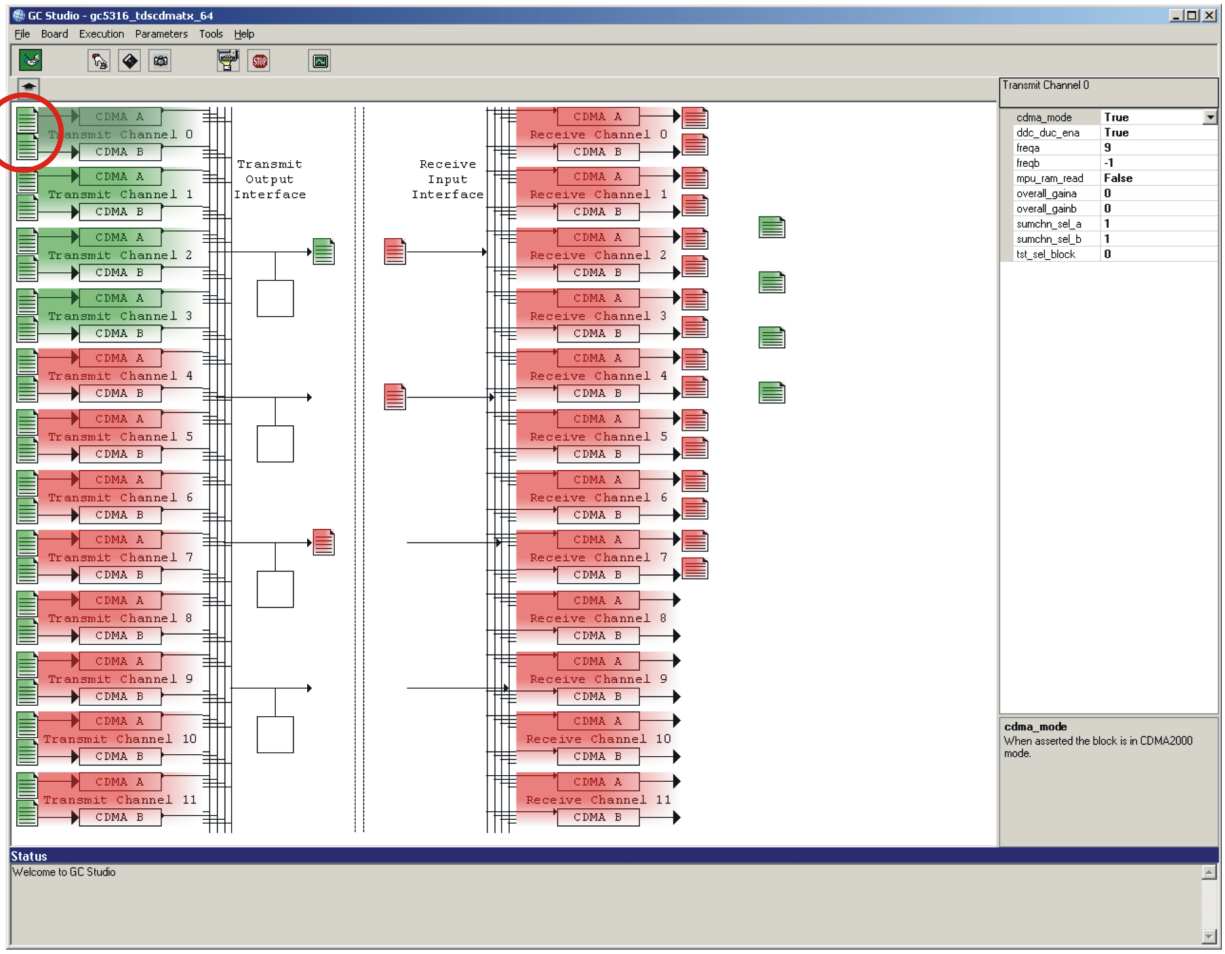

Figure 39. TD-SCDMA – Input Files

25. Now, select the data to be shown on the output.

26. Click the Add New Data Source button circled as shown in Figure 40.

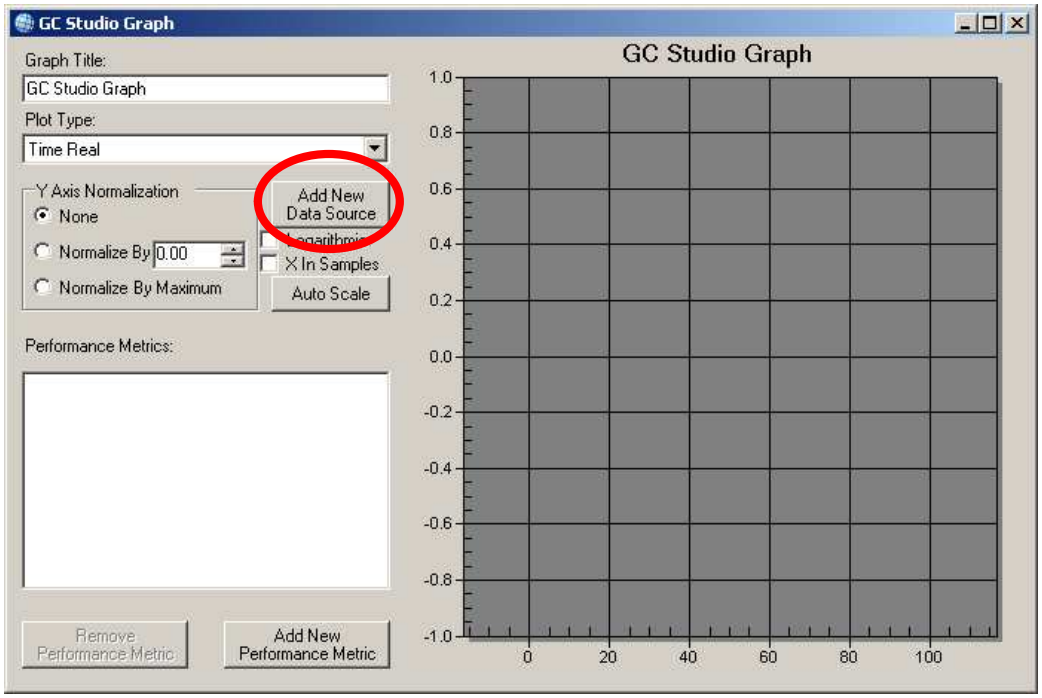

Figure 40. TD-SCDMA – Add New Data Source

27. In the Choose Source panel, select both Transmit Output Port 0, and click OK. Since all eight outputs are muxed on a single transmit port, this will allow us to see them all displayed.

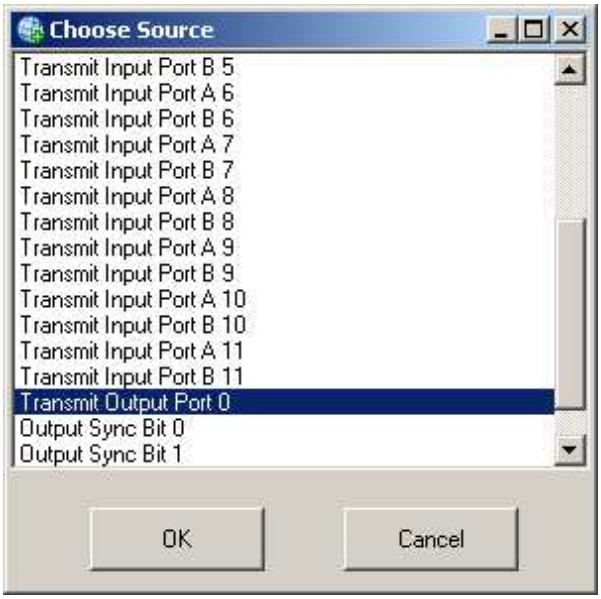

Figure 41. TD-SCDMA – Choose Source

28. In the graph panel, set the Plot Type to Spectral Magnitude, and check Logarithmic.

29. On the GC Studio panel, click the Build and Load buttons, circled as shown in Figure 42. The buttons will turn grey while the project is running.

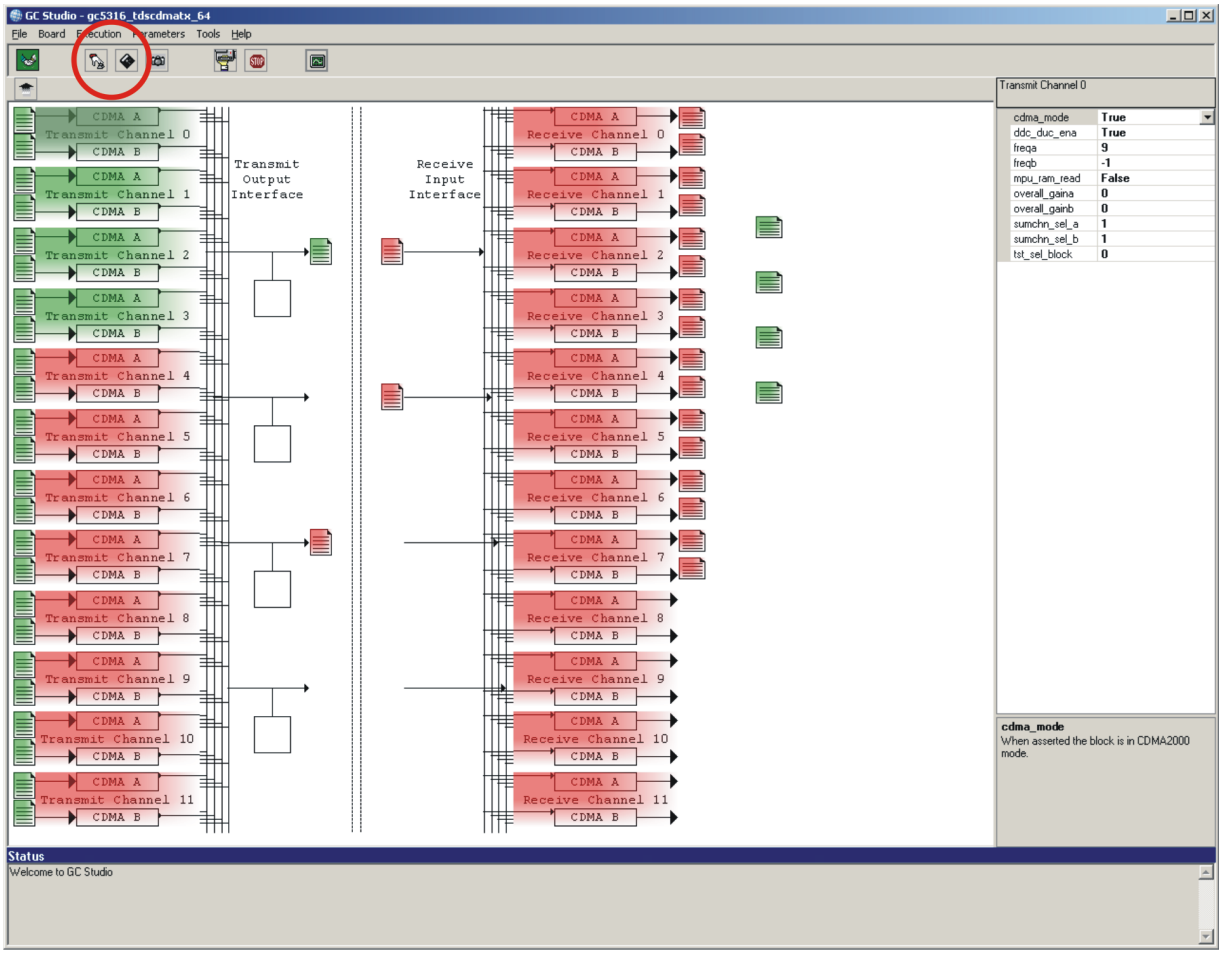

Figure 42. TD-SCDMA – Build and Load Buttons

30. The graph window will be automatically updated with the results as shown in Figure 43.

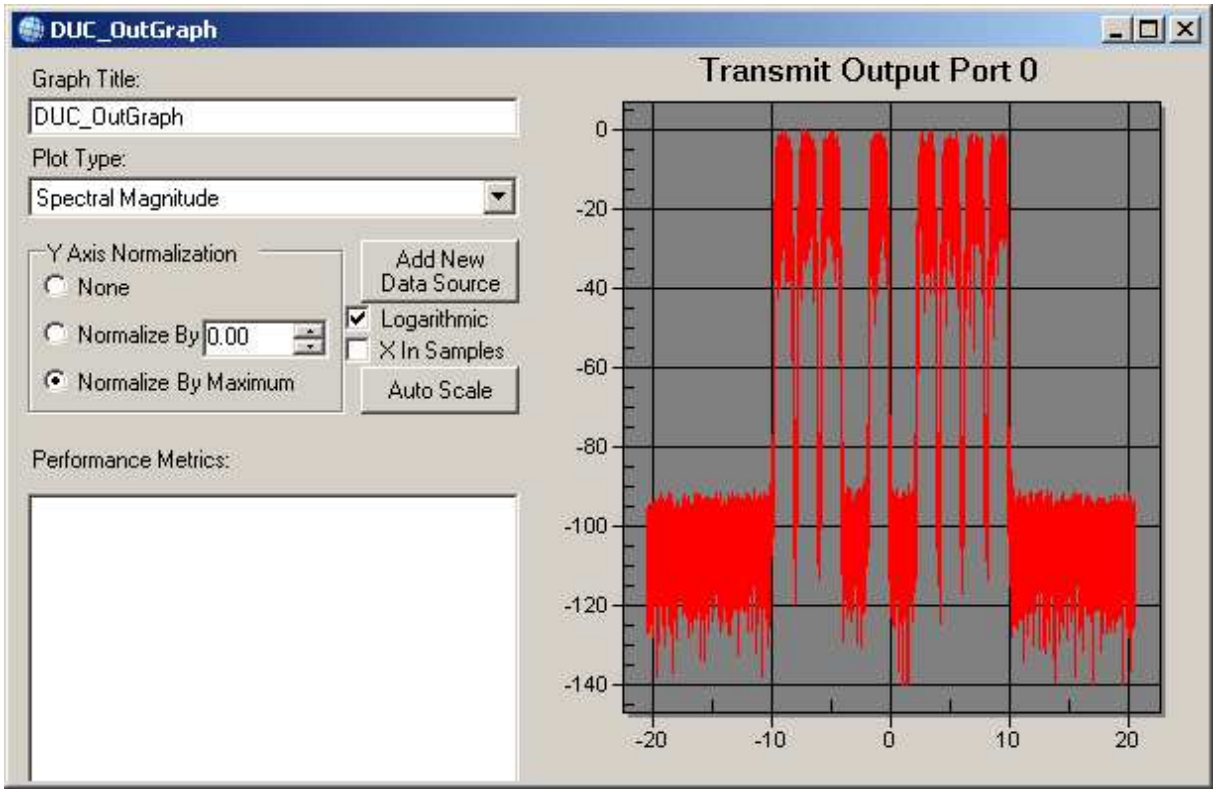

Figure 43. TD-SCDMA – Graph Window Results

31. On the GC Studio panel, click on the stop button, shown circled below, to stop the experiment, then select File > Save Project to save this project.

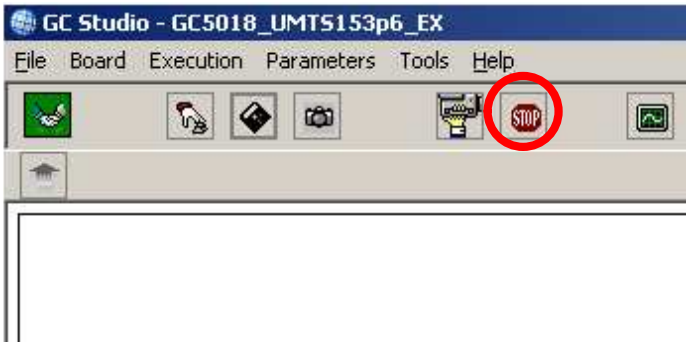

Figure 44. TD-SCDMA – Stop and Saving Project

32. Close the GC Studio Graph Window.

2.2.3 Creating a New GC Studio Project for a WCDMA Receive Configuration

This project demonstrates the ability of the GC5316 to downconvert channels from a real, parallel input stream. The input spectrum shows the input image (which is a real signal, which explains the negative image in the spectrum).

- One real WCDMA carriers is applied to the GC5316 rxin_a
- Simulated rxclk to the GC5316 is 122.88MHz
- Receive FIFOs are enabled
- Receive Channel 0 is configured to process the signal

- Channel NCOs tune to an IF of 19.2 MHz
- The CIC filter is programmed to decimate by 8. The output sample rate at the CIC output is 15.36Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 32-tap filter. It decimates by 2.
- The 64 tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the full rxclk rate.

1. Start GC Studio
2. Click on File > New Project to bring up the following window.
3. Choose a name for this new project, and click create.
4. Select GC5316 for the Plugin and click OK.
5. Using the wizard style interface, setup the GC101 evaluation board, then click next.
6. Setup the GC5316 I/O mode selection as shown and click next. In this example, be sure the ADC clock rate is set to 1. Because we are using a Receive channel for this experiment, set the Input Mode and Output Mode boxes to Transmit Ports as shown below. We will set the Output Clock Source to TX Clk Out. Ensure that the Output Syncs and Strobes are set to “Rx Sync Out and PB Data”. Click “Next” to see the Simulated Clock Rates screen.

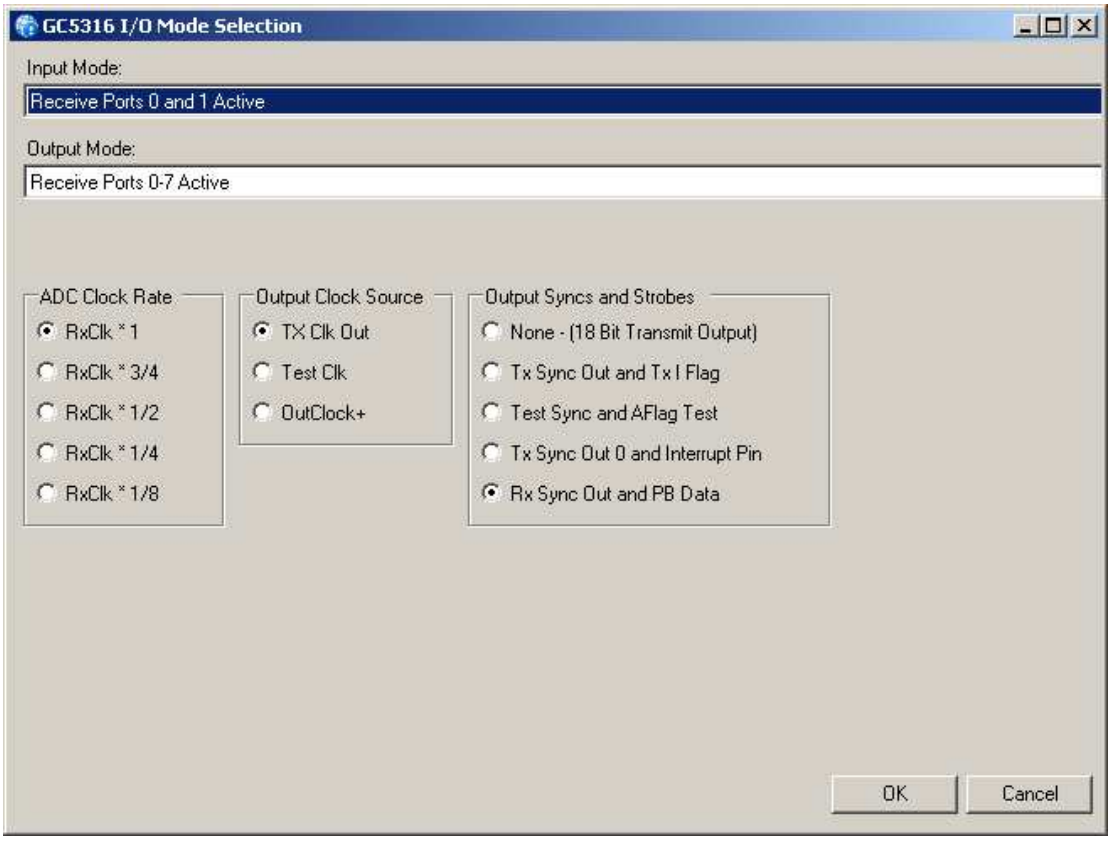

Figure 45. WCDMA – I/O Mode Selection

7. Set the simulated clock rate to 122.88 MHz and click next.

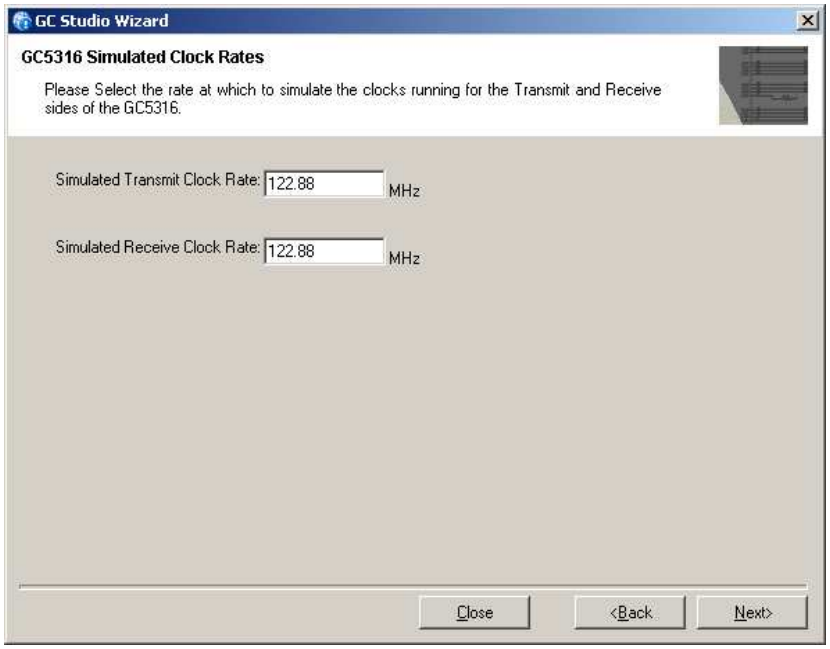

Figure 46. WCDMA – Simulated Clock Rates

8. Channel Copying will be skipped for now, click Next

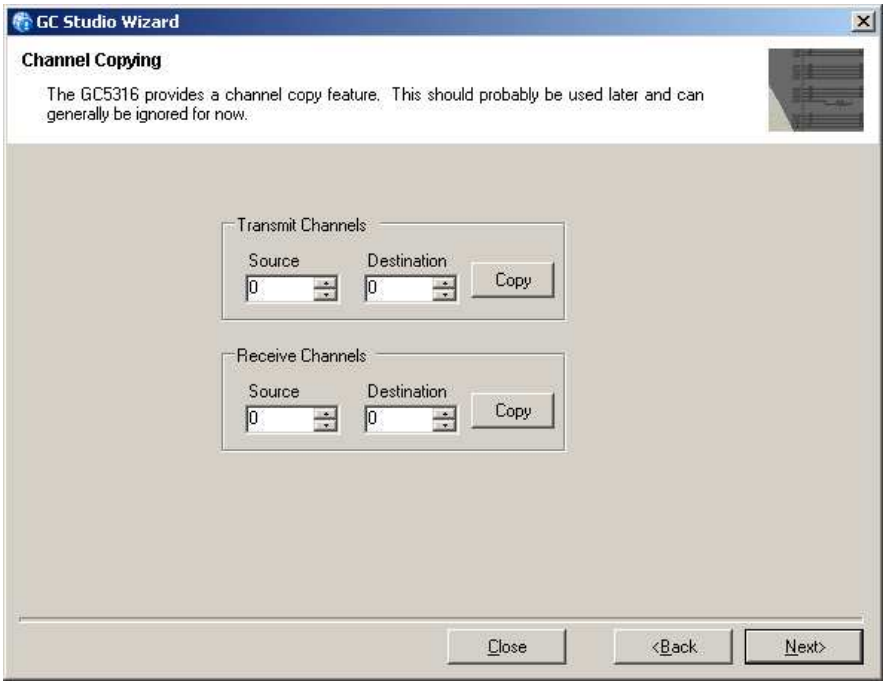

Figure 47. WCDMA – Channel Copying

9. Finish the set-up Wizard as explained in the previous example.
10. Click on the large gc5316 box to display the global control registers.

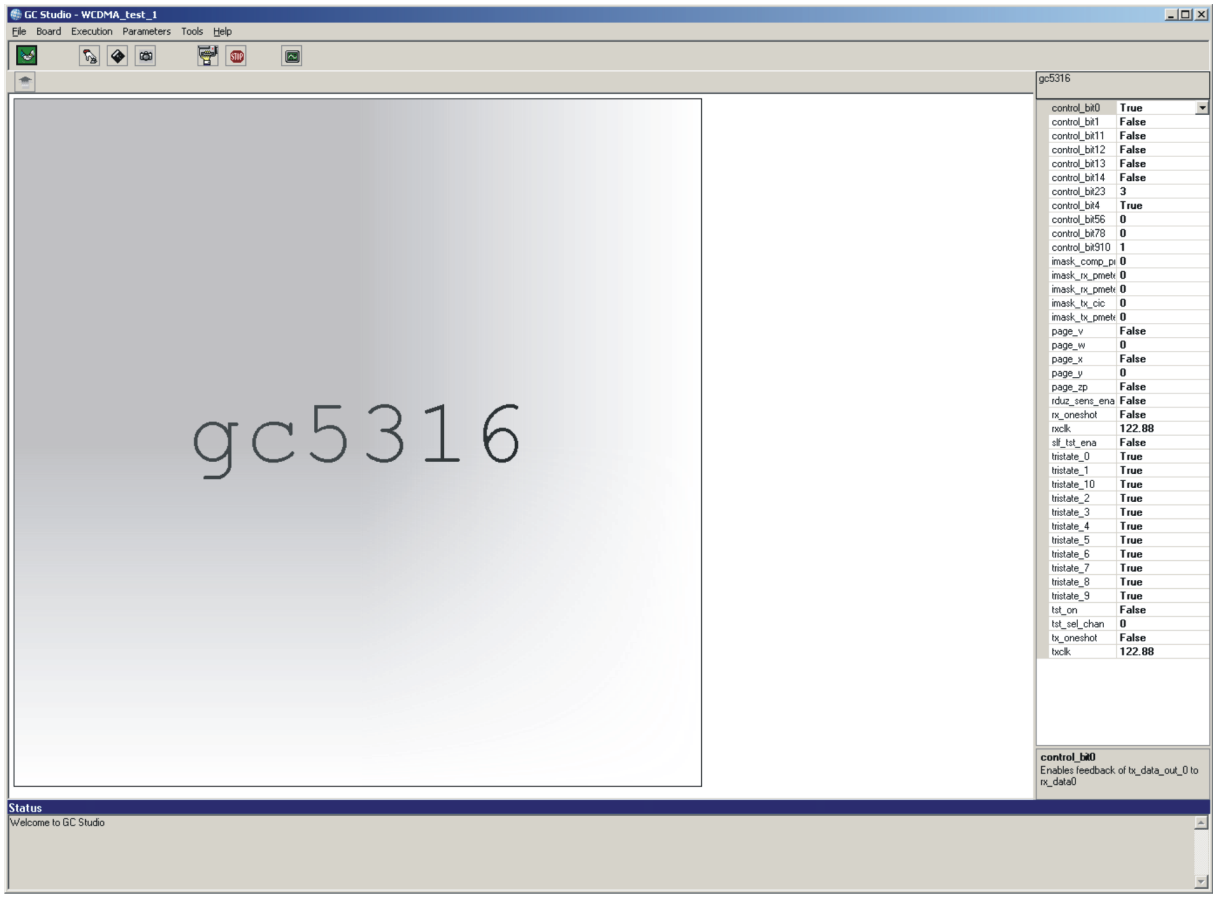

Figure 48. WCDMA – Global Control Registers

11. Next, double click on the gc5316 block to “push down” one level into the gc5316.
12. Click on the Input Interface block to display and edit the receive input interface registers. Set adc_fifo_bypass to FALSE to enable the rxin_a/b/c/d input FIFO circuits.

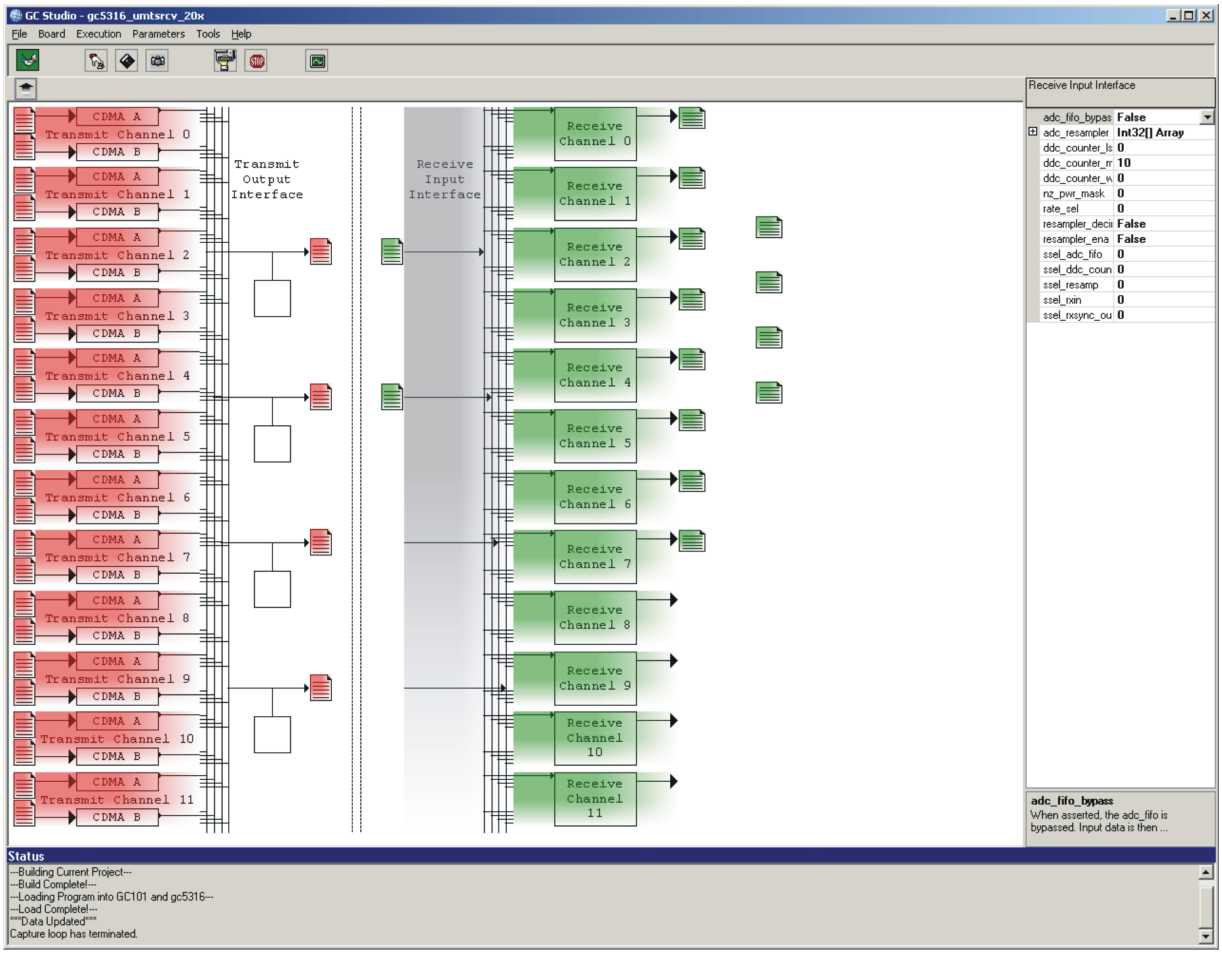

Figure 49. WCDMA – Input Interface Block

13. Click on the upper Receive Channel 0 block. Set ddc_duc_ena to True. Make sure that the cdma_mode is set to False, since this example is processing the WCDMA signal.

14. Click on the area circled by "Load From File", as shown in Figure 50. Load the stimulus file “TM1_300k_IF19.2_Fup122.88_1000.GCIN” found on the provided CD. This file will simulate a real TM1 WCDMA signal at an IF of 19.2 MHz.

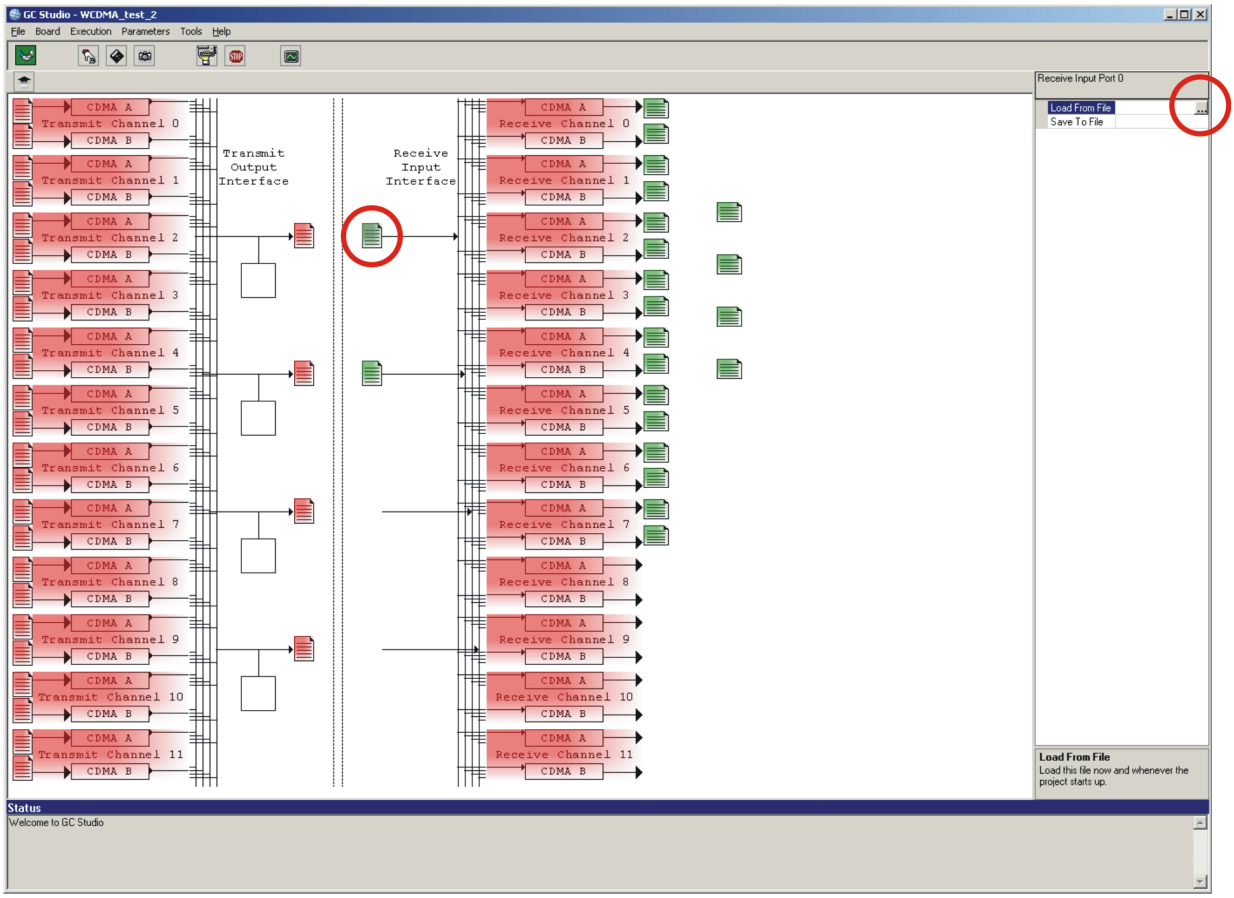

Figure 50. WCDMA - Loading the Stimulus File

15. Click on the Receive Input Interface section, then make sure that the "resampler_decimate" is set to "FALSE".

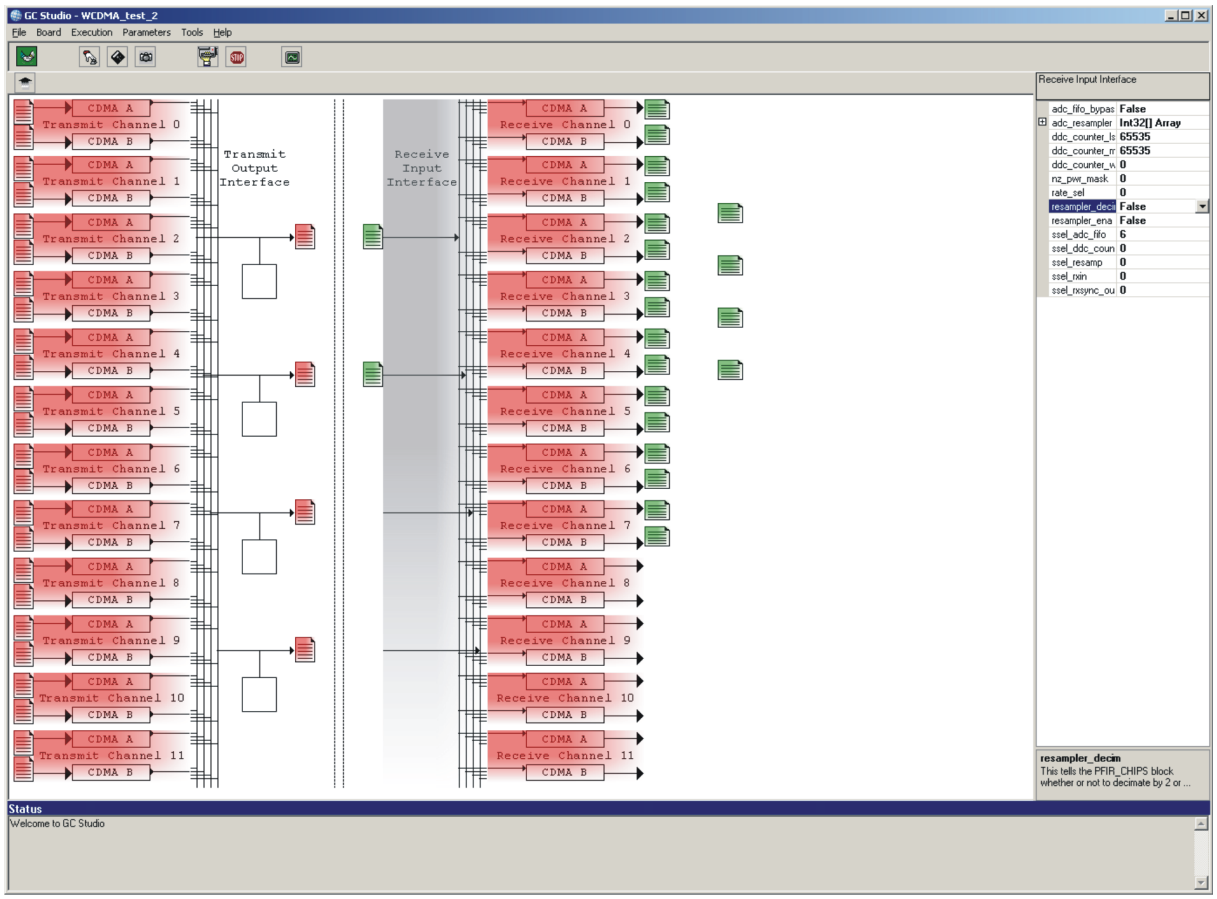

Figure 51. WCDMA – Receive Channel Block

16. Next, click on Receive Channel 0, and make sure cdma_mode is set to "False". Set the NCO Frequency (freqa) to 19.2 (MHz). Re-set the "ch_rate_sel" to 0 to guarantee this register gets set properly. This is shown in Figure 52.

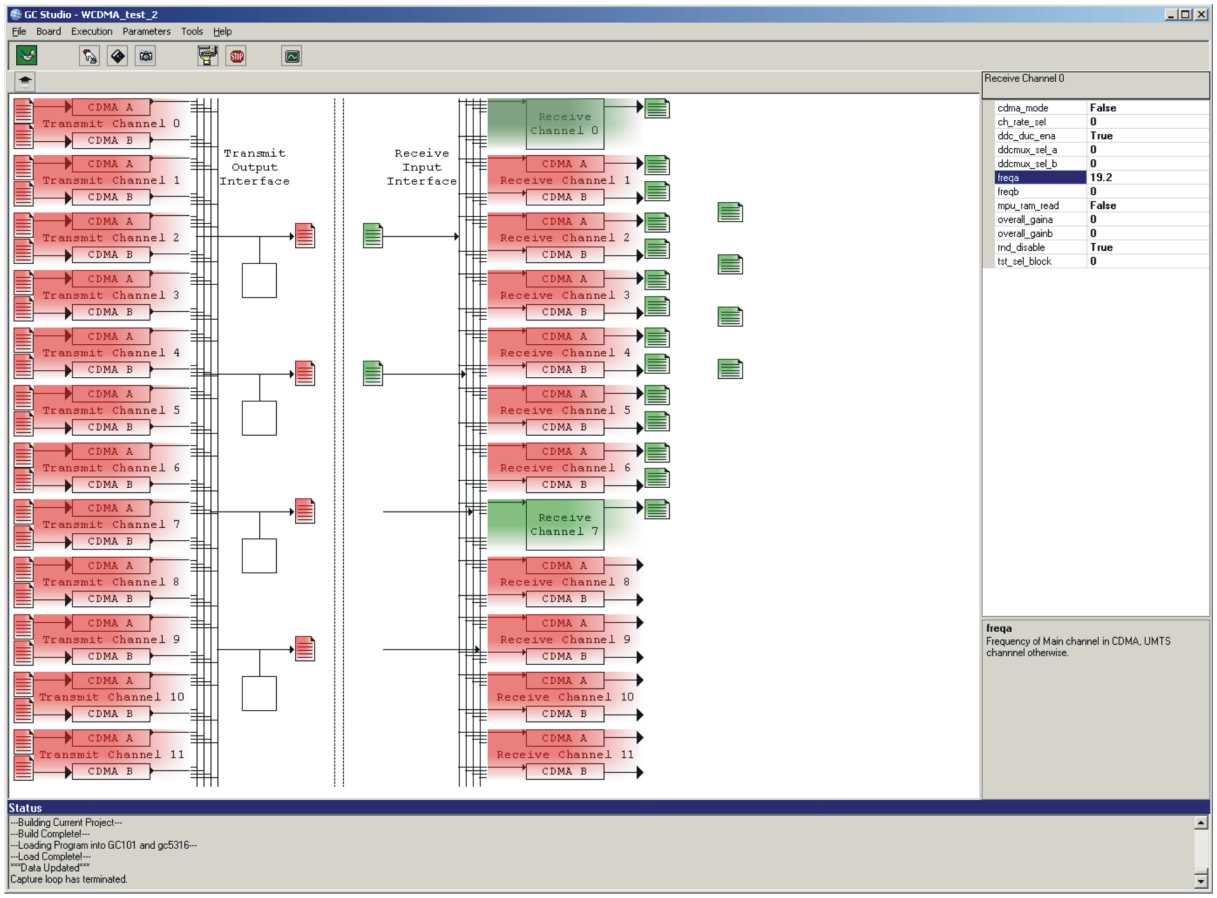

Figure 52. WCDMA - Enable Channel 0

17. Double-click on Receive Channel 0 to define the parameters inside the channel. Click on the "Delay Adjust and Zero Pad" box.

Since the ADC will run at the DDC rate, “tadj_interp_dec” bit needs to be set to 0, to interpolate by 1 as shown in Figure 53.

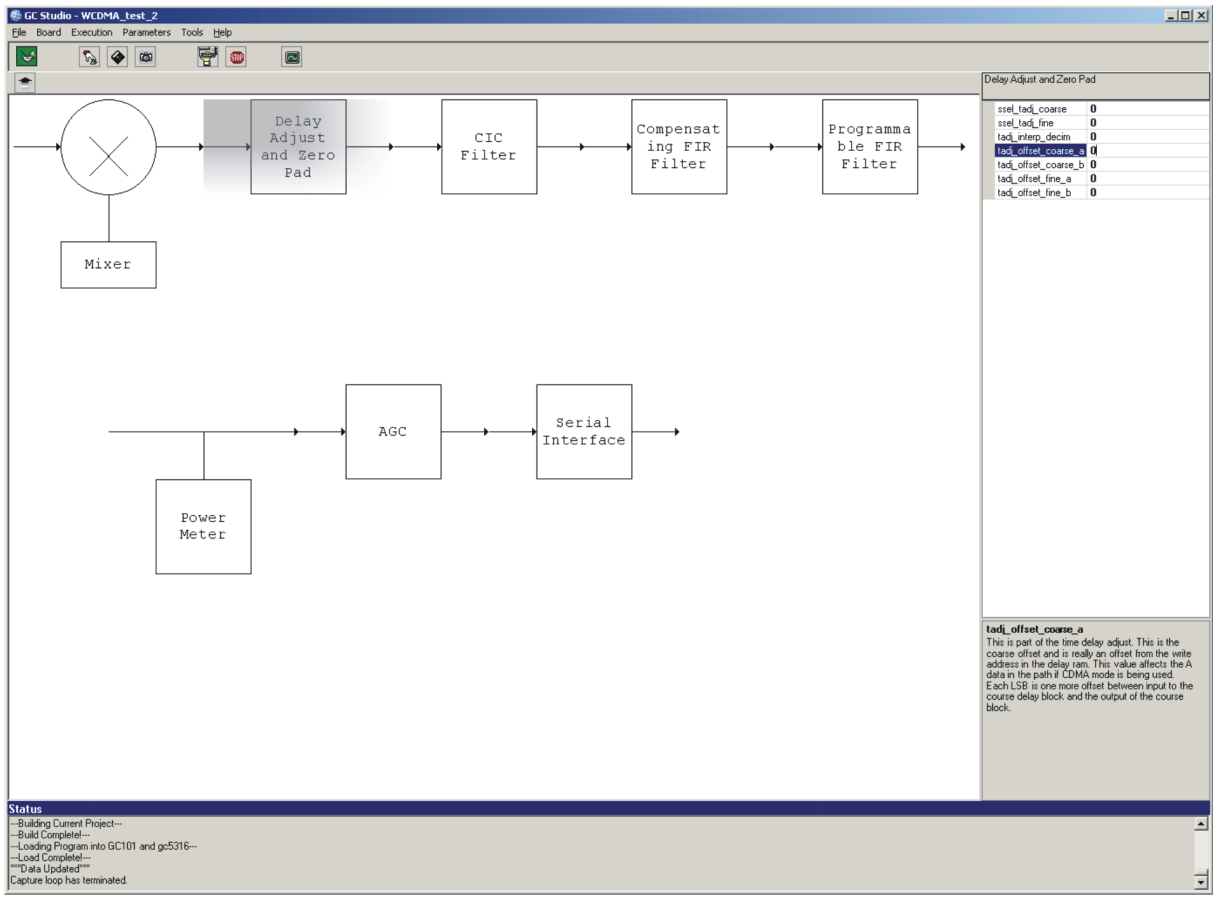

Figure 53. WCDMA – Delay Adjust and Zero Stuff Block

18. The CIC filter decimates by 8, and the CIC shifter gain needs to be scaled as shown (see the formula in the datasheet):

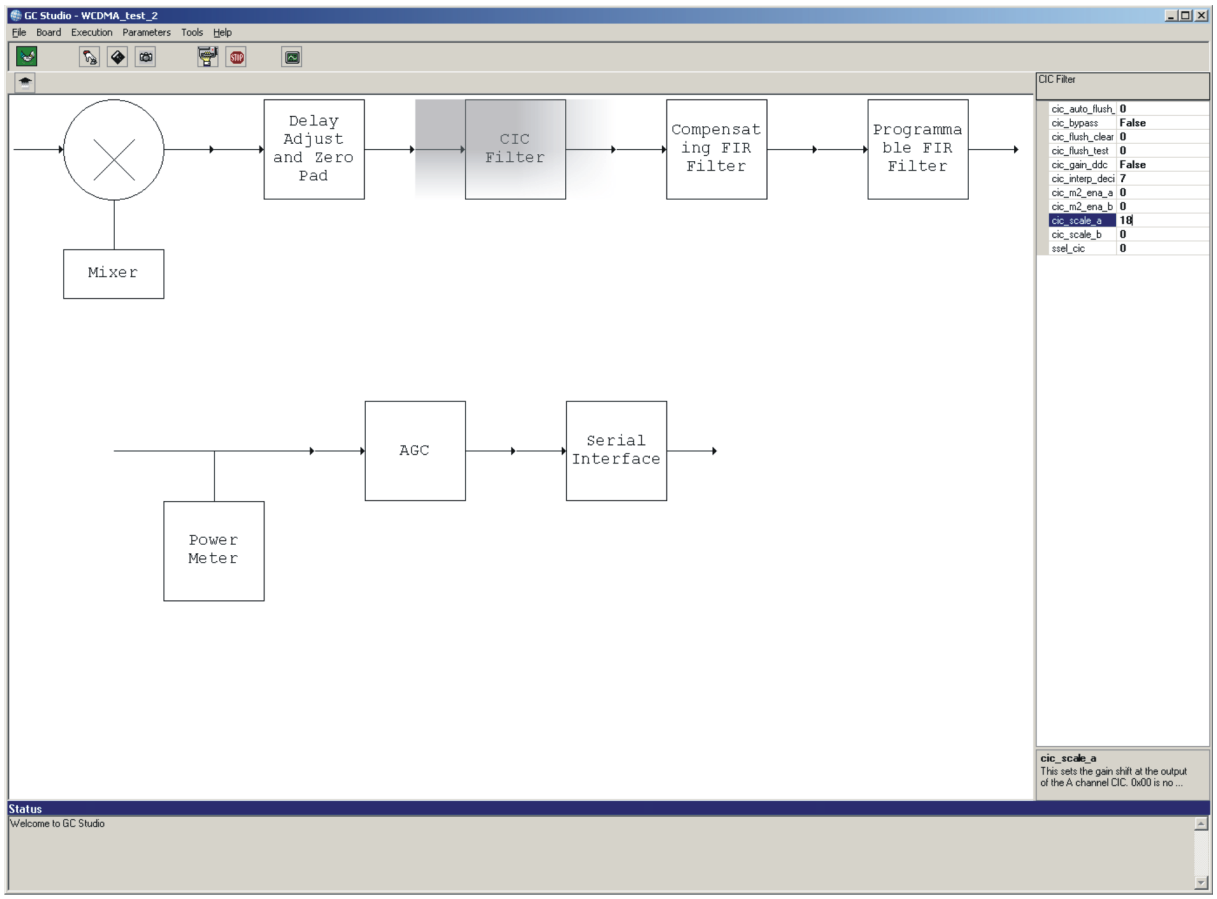

Figure 54. WCDMA – CIC Filter Block

19. The CFIR is 32 taps long with the coefficients loaded from the file"UMTS_CFIR_32.taps", which is located on the provided CD.

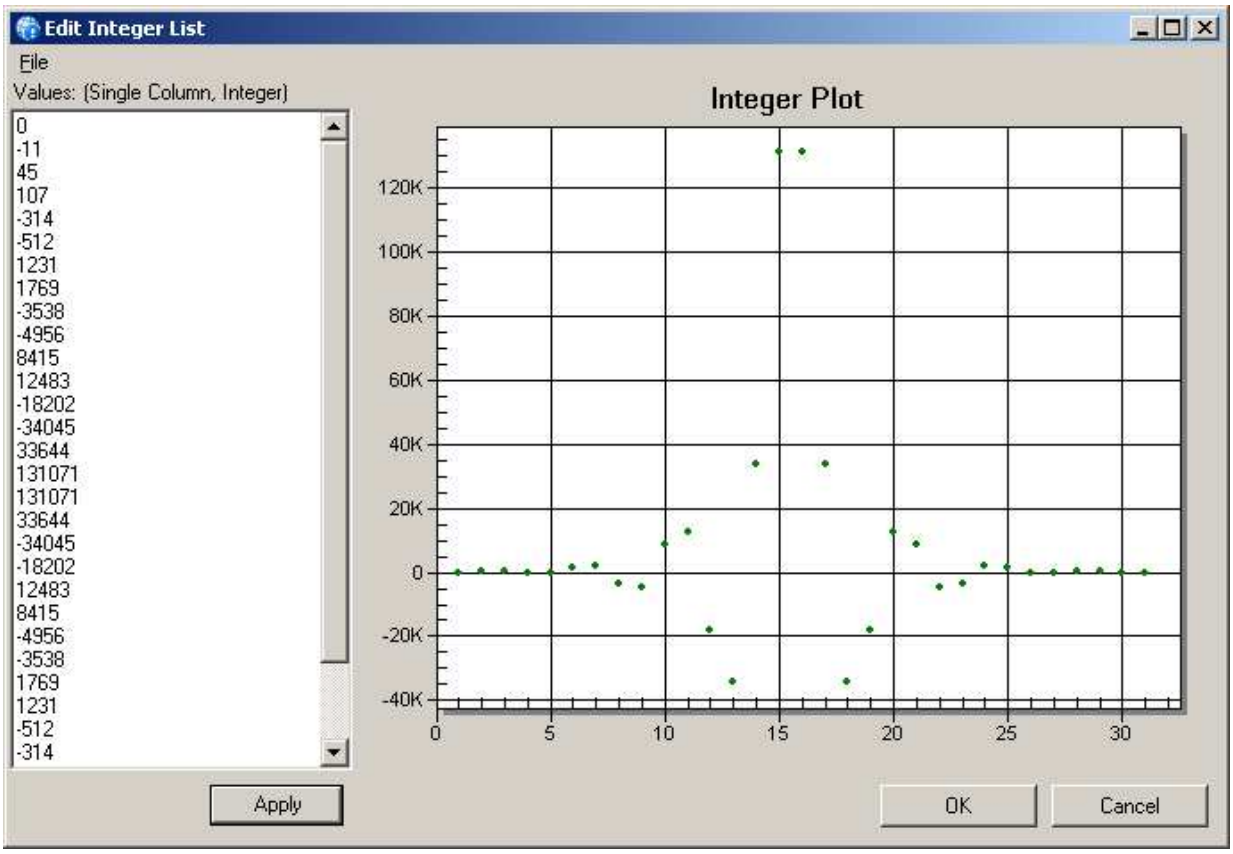

Figure 55. WCDMA – CFIR Block

20. The PFIR is 64 taps long, decimating by 1. Load coefficients from the file “UMTS_PFIR_64.taps”, which is located on the provided CD.

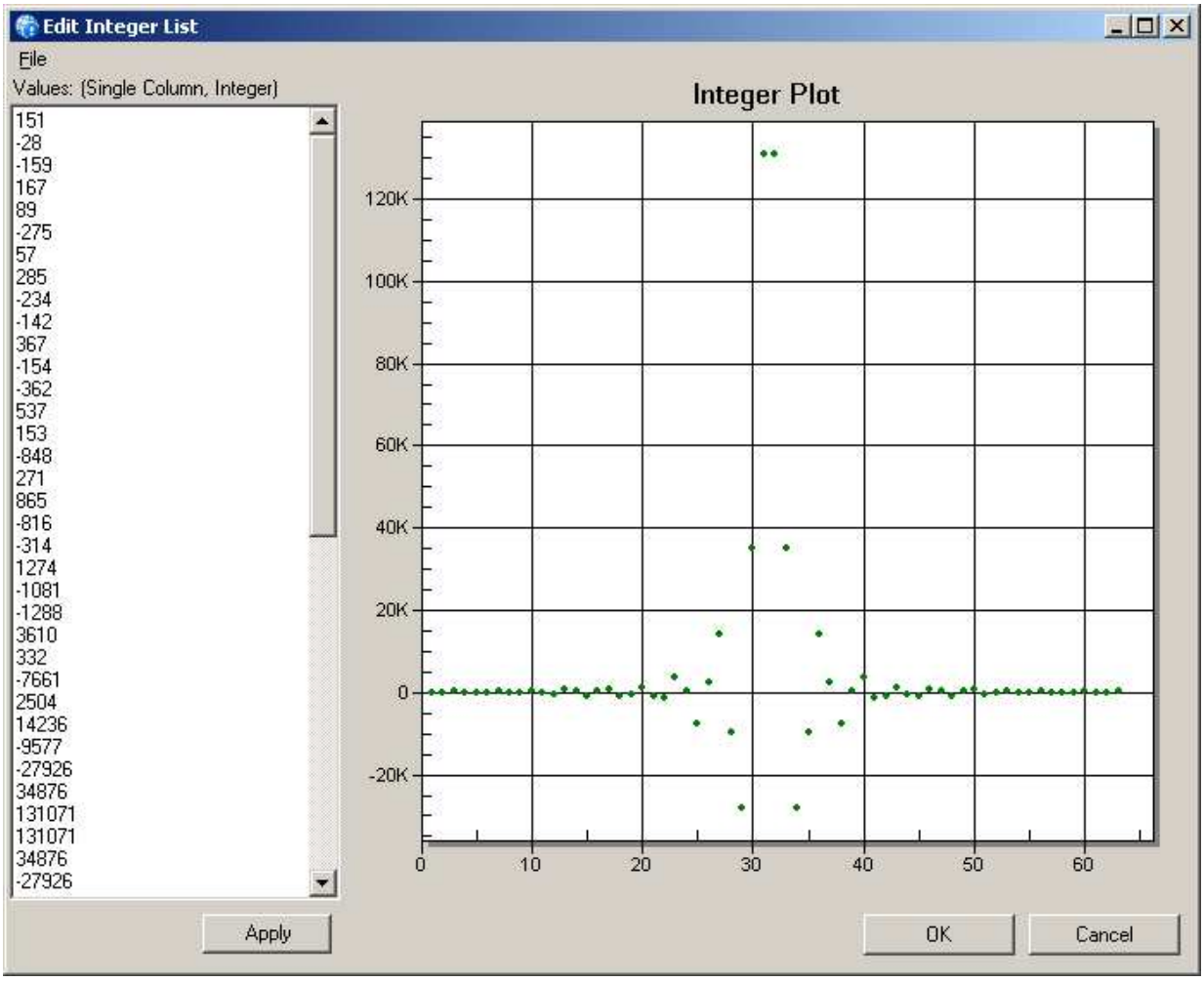

Figure 56. WCDMA – PFIR Block

21. Set the gain of PFIR to "1".

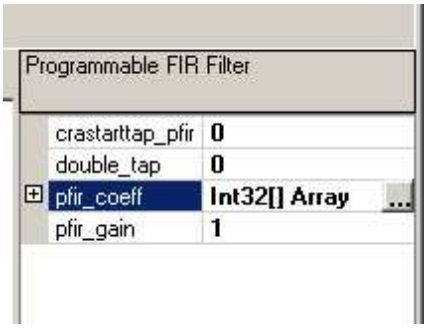

Figure 57. WCDMA - Setting PFIR Gain

22. Click on the "AGC" block and set the registers as shown in Figure 58.

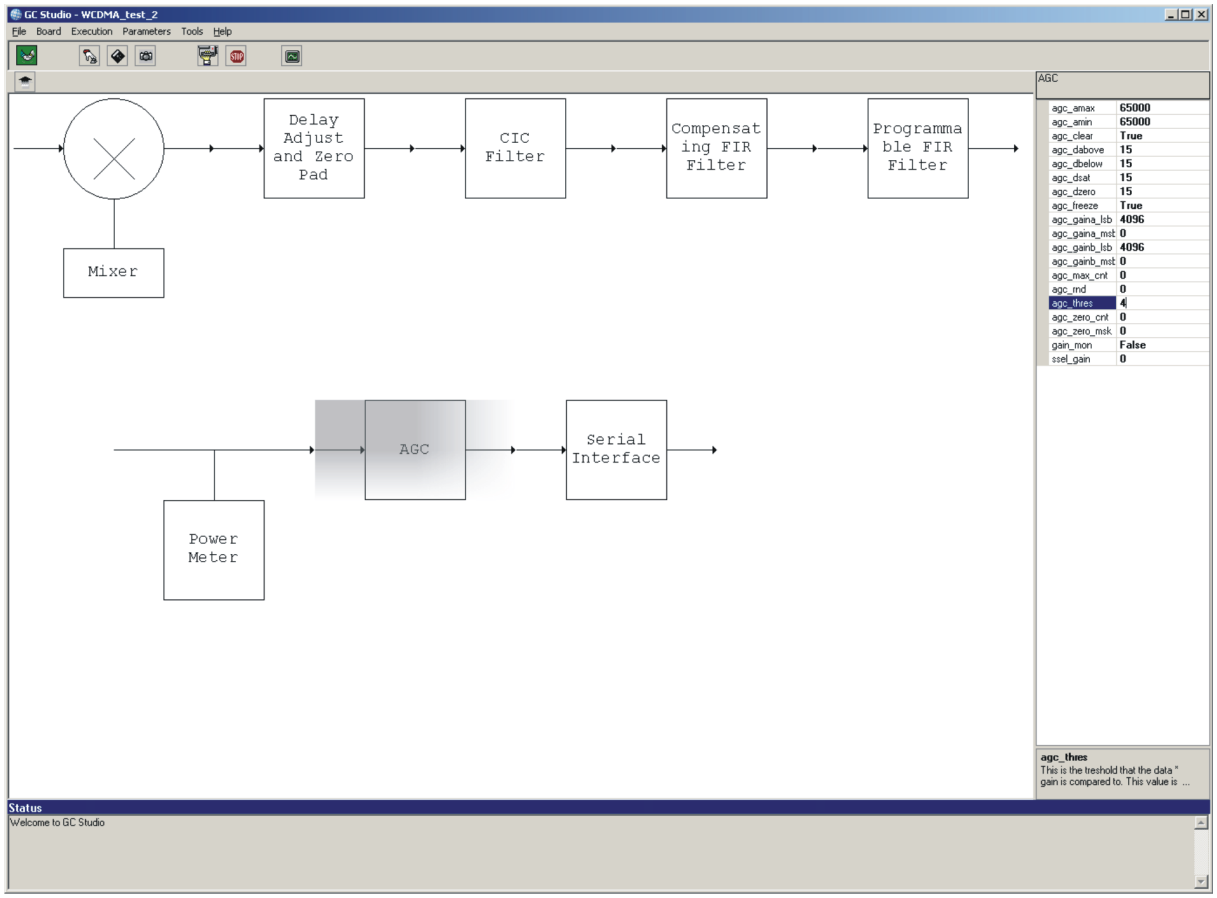

Figure 58. WCDMA – ACG Block

23. Select the Serial Interface block and set the parameters as indicated. Set the number of output bits to 16 (“pser_recv_bits” = 15) as shown in Figure 59. No clock division will be used. After verifying the values of the serial interface, click the arrow as shown in Figure 60 to pop up one level in the GC5316 hierarchy.

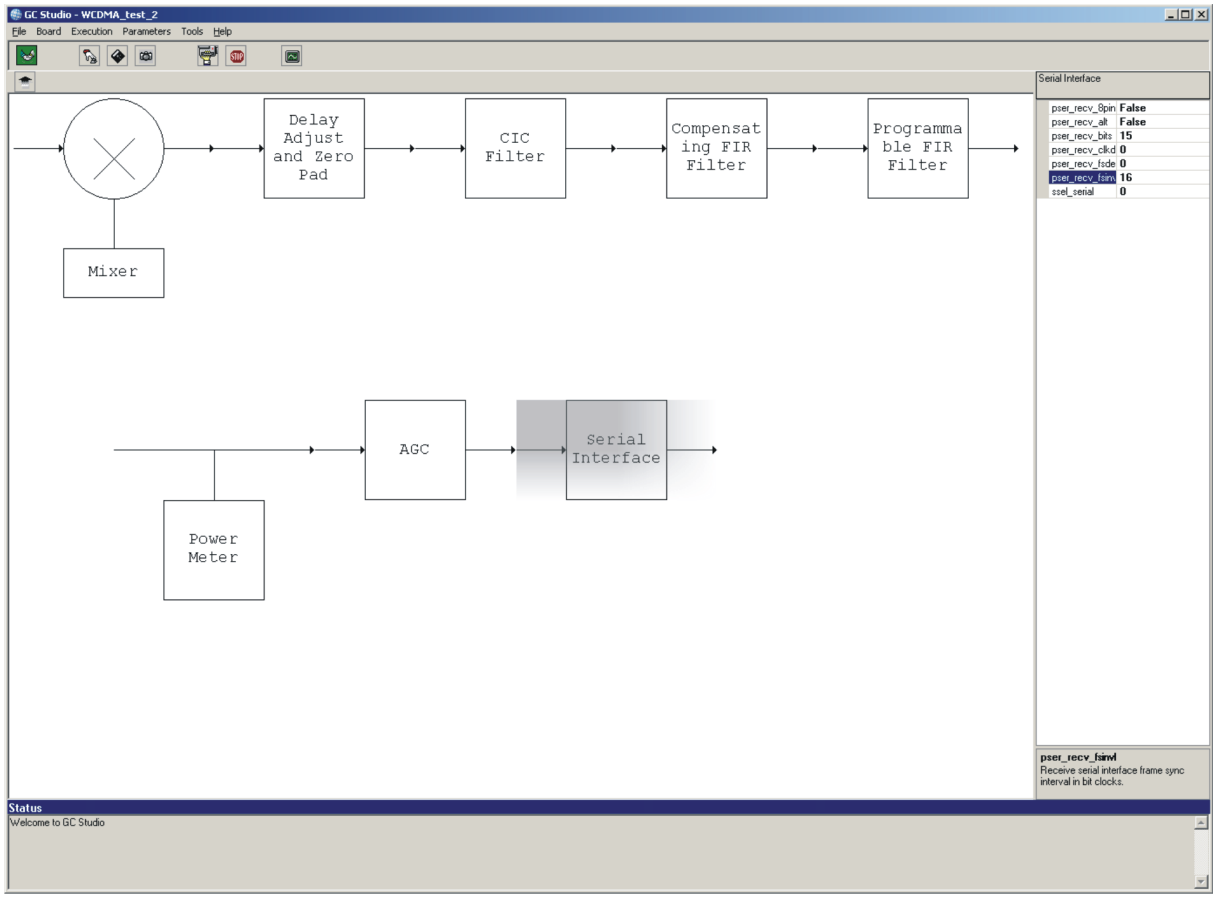

Figure 59. WCDMA - Serial Interface Block

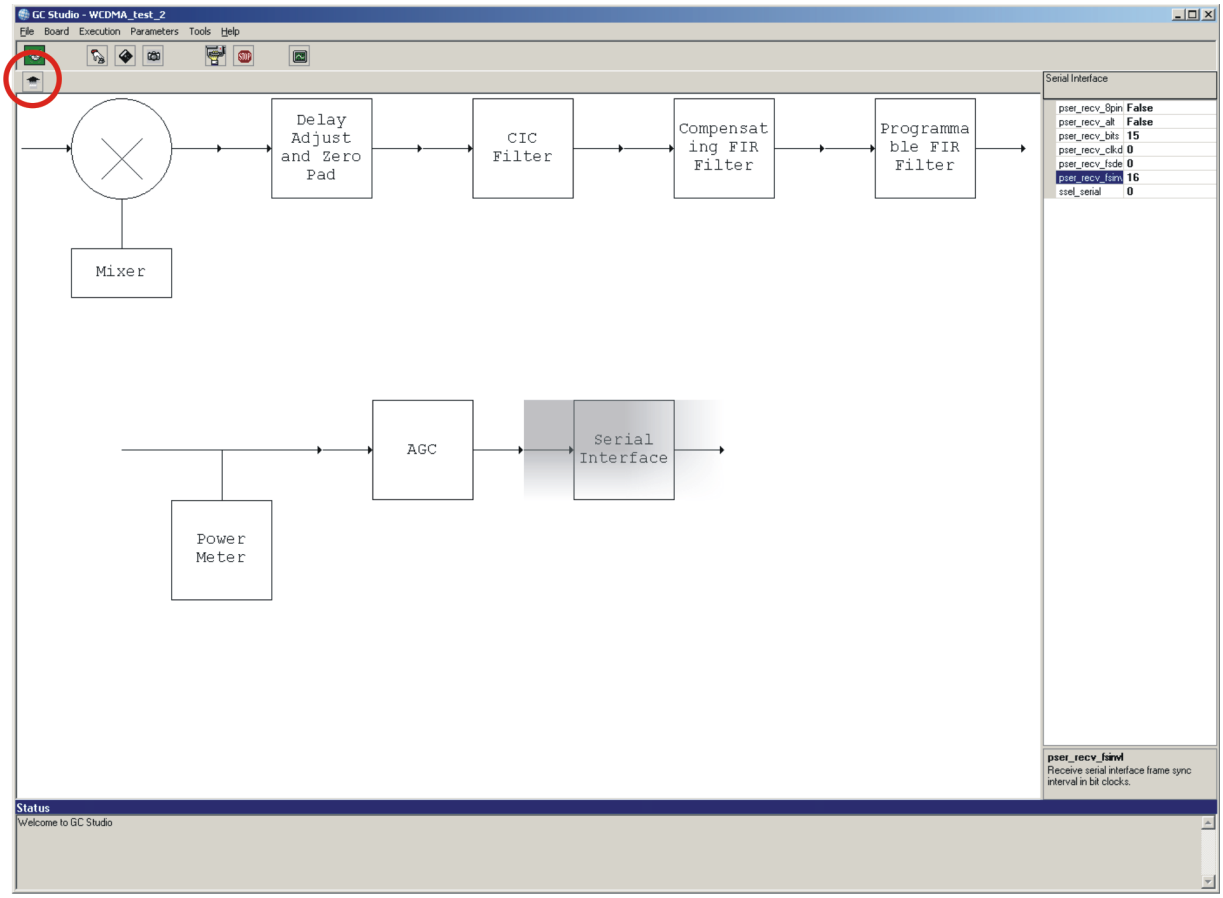

Figure 60. WCDMA – Serial Interface Block

24. Receive Channel 0 has now been configured to process:
    - Four WCDMA signals at 122.88 MSPS
    - Mixer/nco block shifts the signal to DC
    - The CIC block decimates by 8x to 15.36 MSPS
    - 32-tap CFIR compensates for the CIC droop, filters and decimates the signal to 7.68 MSPS
    - 64-tap PFIR filters the signal
    - Channel AGC is set
    - Serial interface is used to output the baseband signal at serial output clock of 122.88 MHz
25. Copy the Receive Channel 0 settings to Receive Channel 7 by going to Parameter → GC5316 Channel Copy.
26. Next, click on the icon circled as shown in Figure 61 for the graphical display settings:

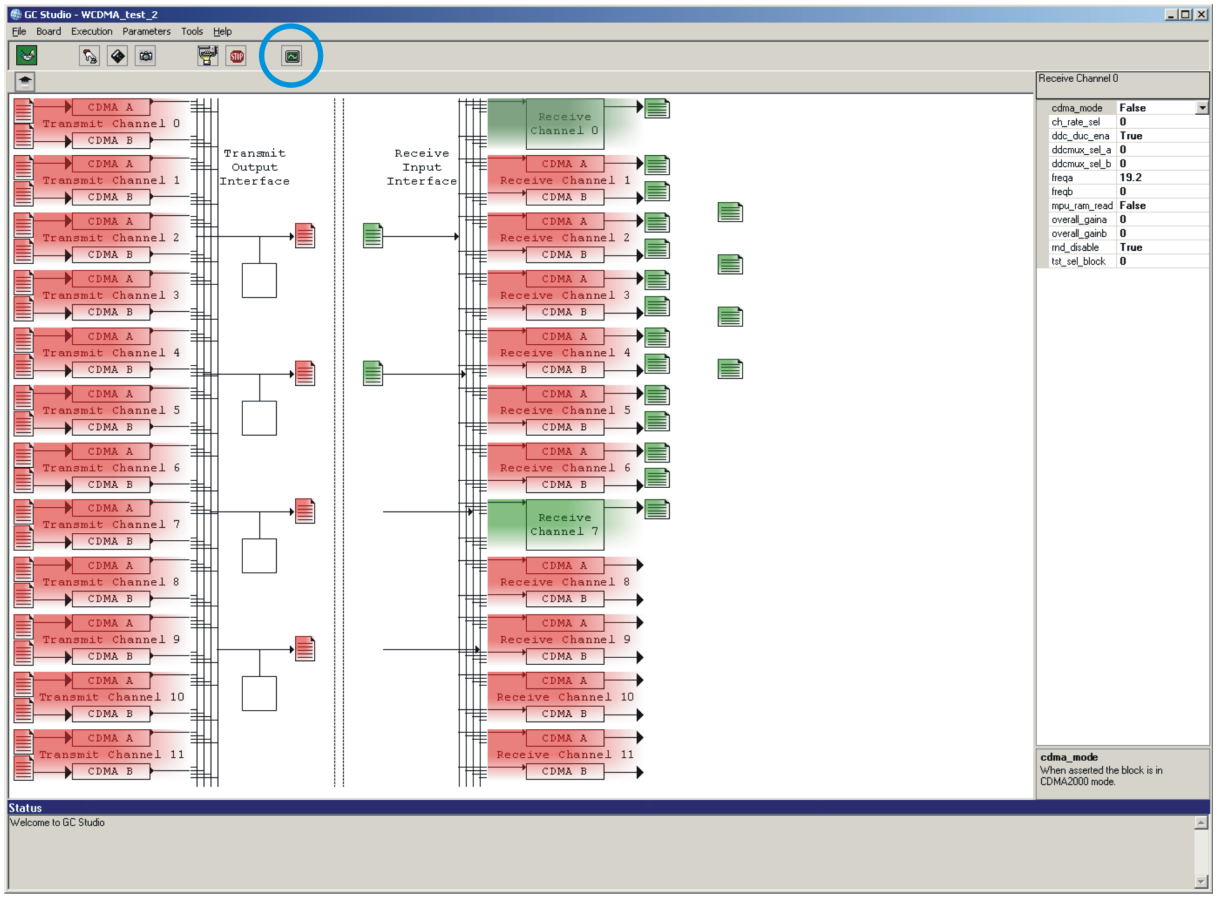

Figure 61. WCDMA – Input Interface Block

27. Click the Add New Data Source button circled shown in Figure 62.

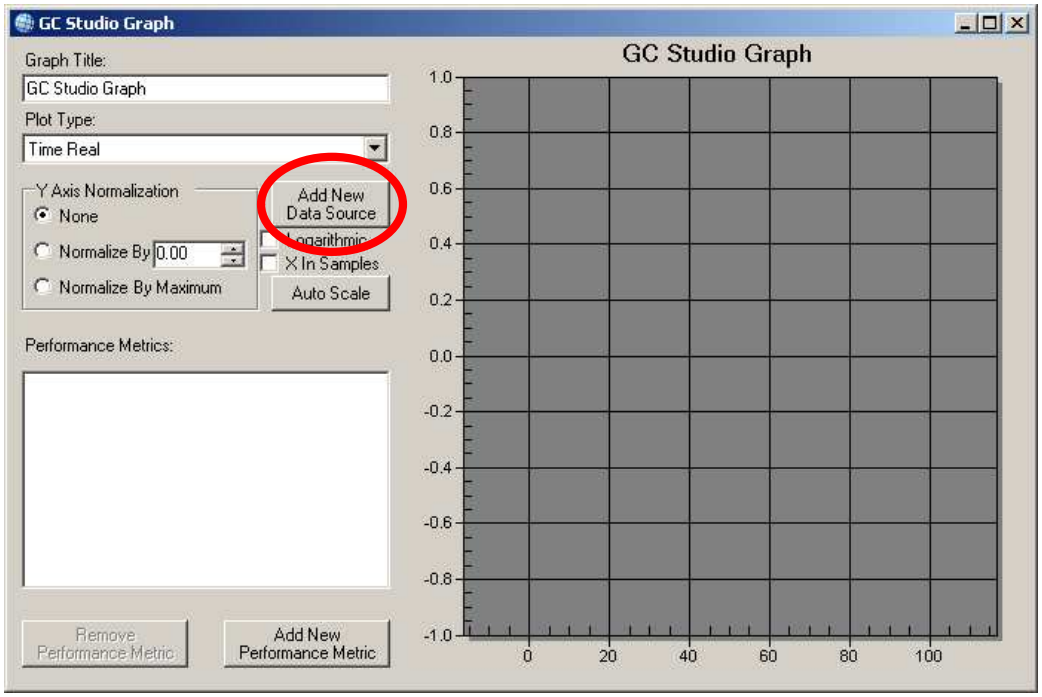

Figure 62. WCDMA – Add New Data Source (1)

28. In the Choose Source panel, select Receive Output Port A 0, and click OK.

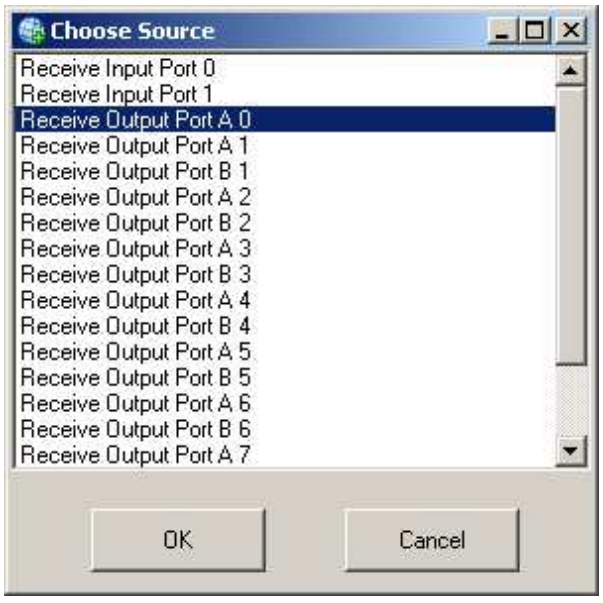

Figure 63. WCDMA – Choose Source (1)

29. In the graph panel, set the Plot Type to Spectral Magnitude, and check Logarithmic.
30. Again, click on the plot button to open another plot to view the input data.
31. Click the Add New Data Source button circled as shown in Figure 64.

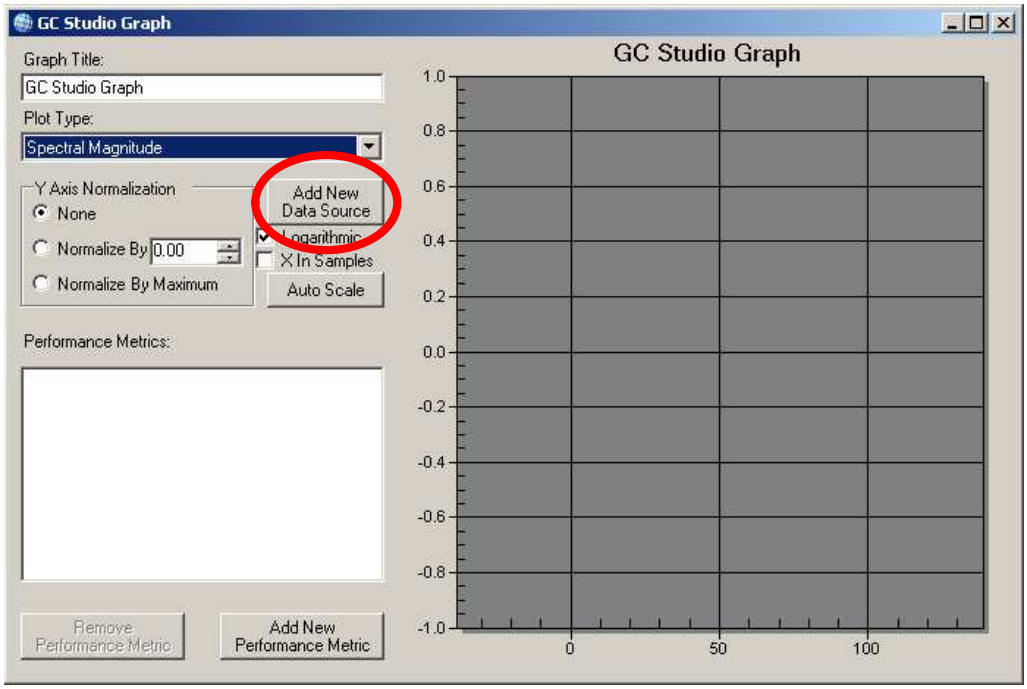

Figure 64. WCDMA – Add New Source Data (2)

32. In the Choose Source panel, select Receive Input Port 0, and click OK.

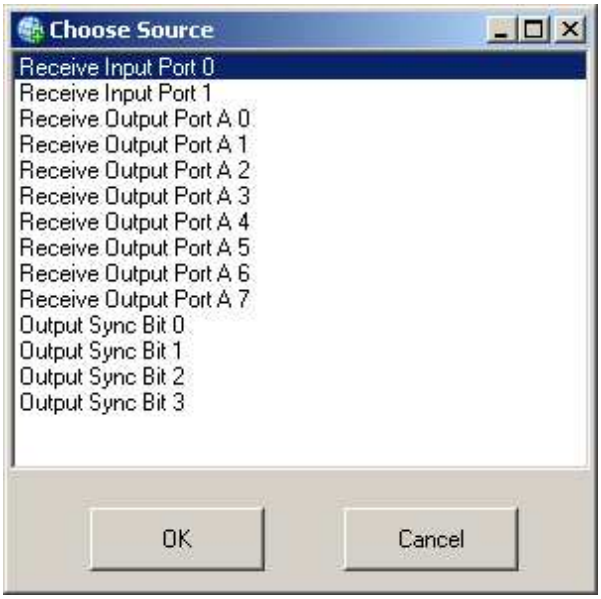

Figure 65. WCDMA – Choose Source (2)

33. On the GC Studio panel, click the Build and Load buttons, circled in Figure 66. This will execute the experiment.

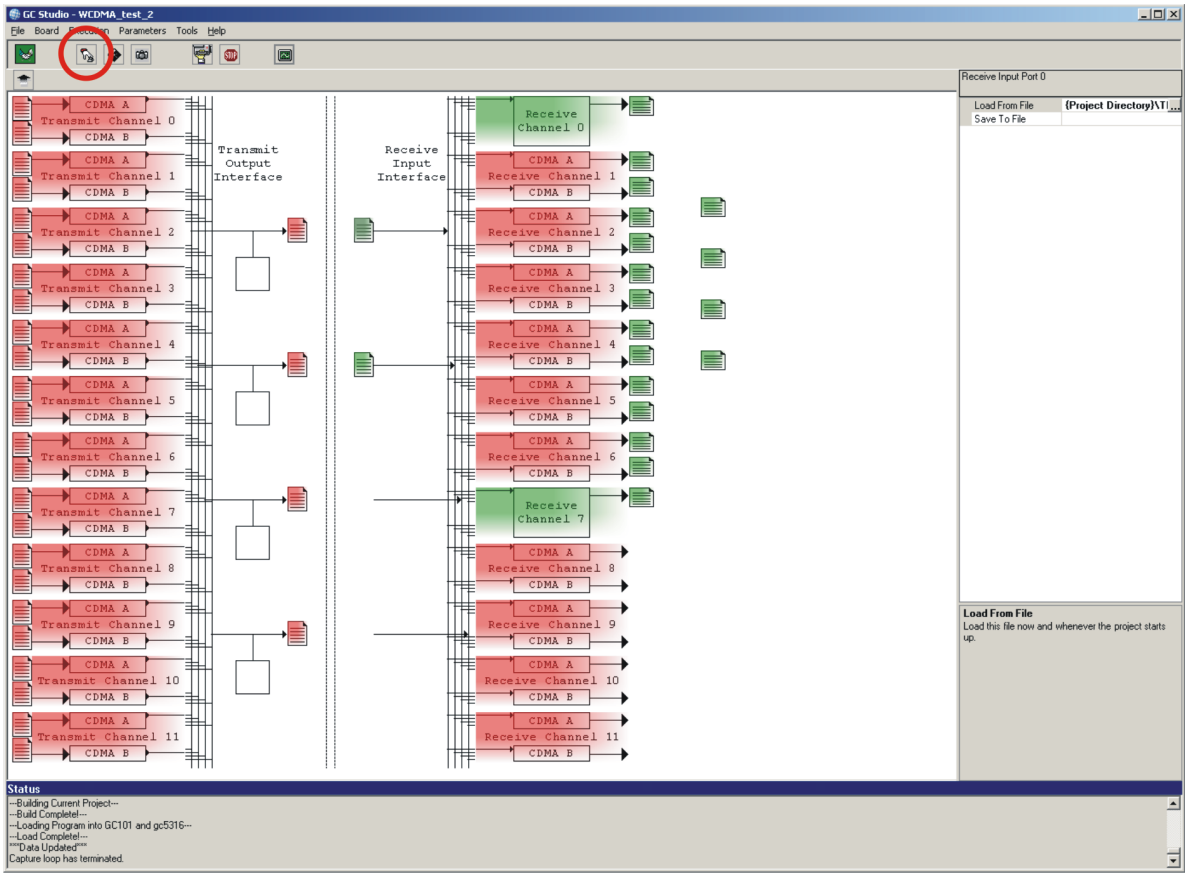

Figure 66. WCDMA – Build and Load Buttons

34. The graph window will be automatically updated with the results as shown in Figures 67 and 68.

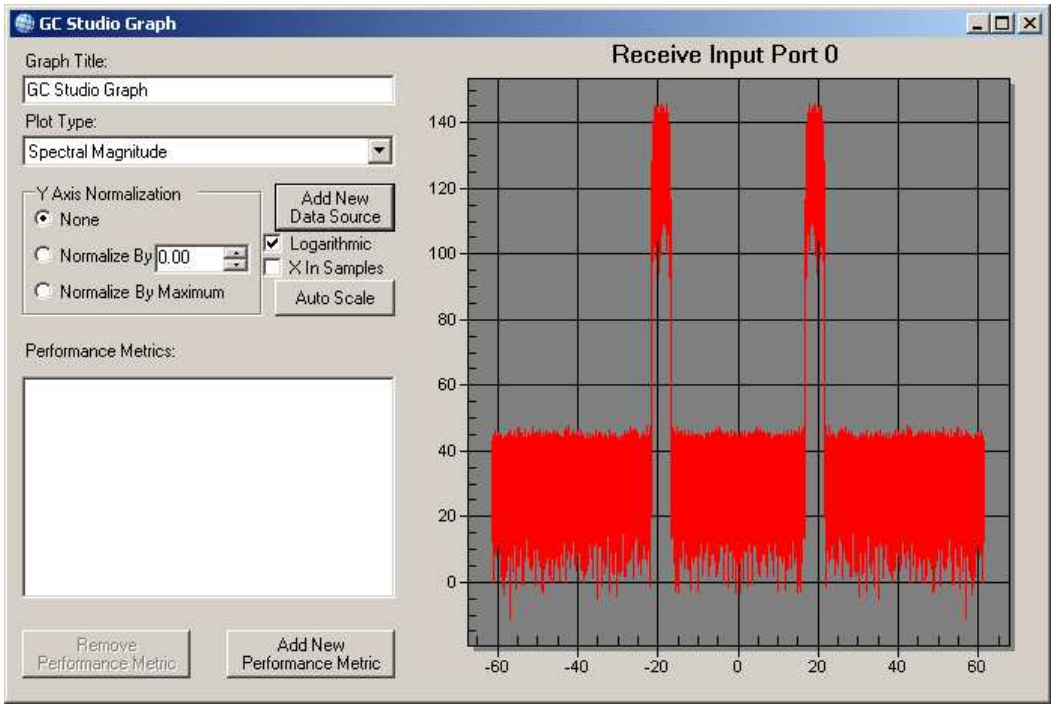

Figure 67. WCDMA – Receive Input Port 0 Results

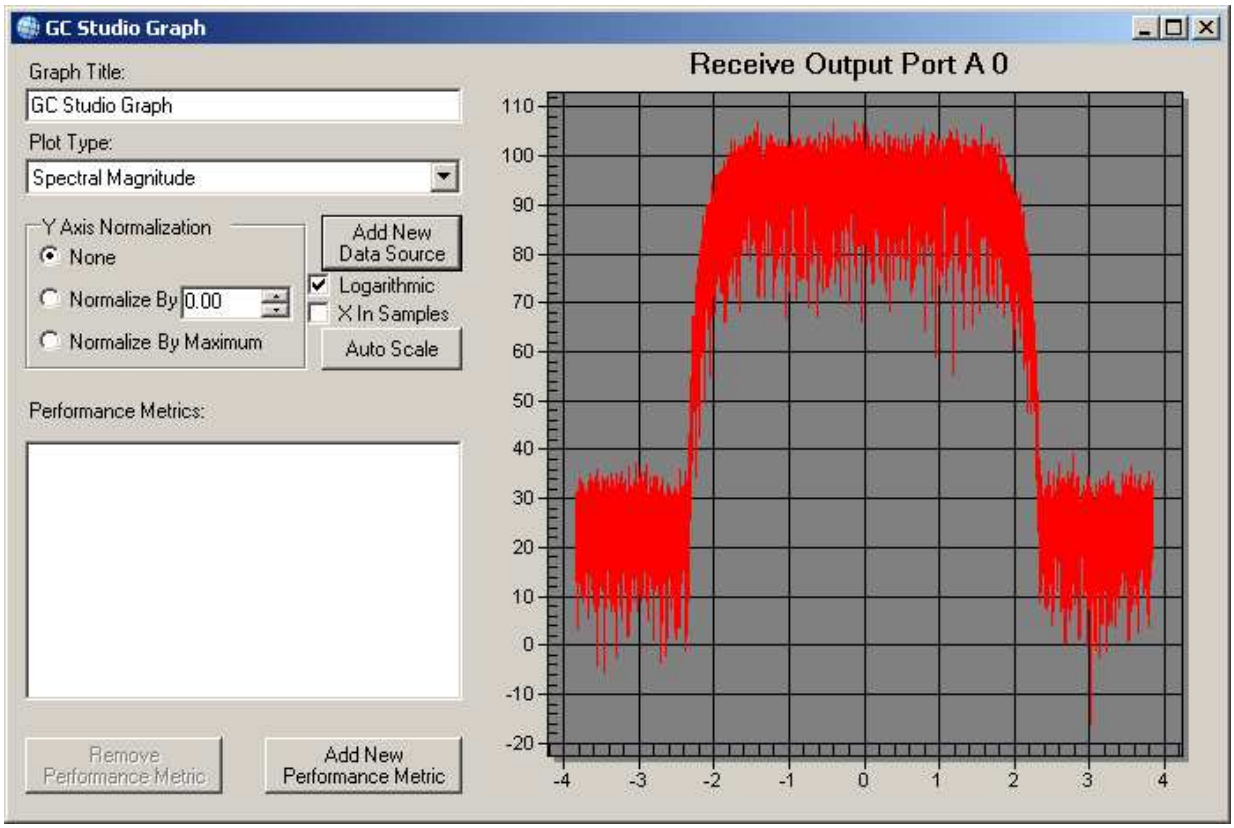

Figure 68. WCDMA – Receive Output Port A0 - A3 Results

35. On the GC Studio panel, click on the stop button, shown circled below, to stop the experiment, then select File → Save Project to save this project.

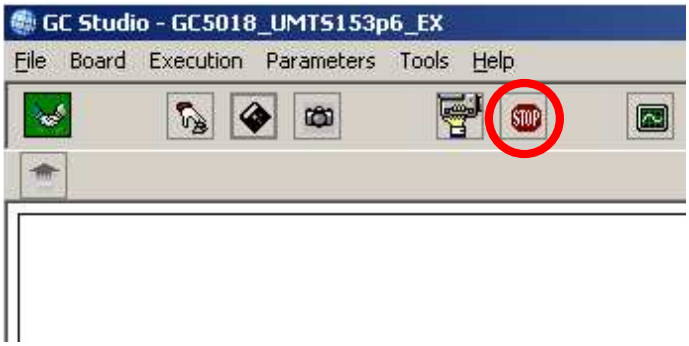

Figure 69. WCDMA – Stop and File -> Save

36. Close the GC Studio Graph Window.

2.2.4 GC5316 Projects included in the GC Studio Release

The following example projects are included in the GC Studio Release

CDMA2000 Rx

- A real CDMA carrier is applied to the GC5316 rxin_a inputs with a simulated sample rate of 61.44 Msps and an IF frequency of 30.72MHz.
- Simulated rxclk to the GC5316 is 122.88MHz
- Receive FIFOs are enabled
- Receive AGC is set to a constant gain

- Receive Channel 0 is configured to process the signal
- The resampler is turned on, which downshifts the data by $F_S/4$ (122.88/4 = 30.72).
- Channel 0 A&B, which have their NCO's tuned to ± .625 are filtering and isolating the signals centered at 30.72 ±.625MHz.
- The CIC filter is programmed to decimate by 25 using a m=2 comb section configuration. The output sample rate at the CIC output is 4.9152Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 48 tap filter.
- The 64 tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the half rxclk rate

CDMA2000 Tx

- Each of the transmit channels is fed a typical CDMA baseband signal at approximately 1.2288 MHz bandwidth.
- Simulated rxclk to the GC5316 is 122.88MHz
- This project shows a general CDMA transmit case, using 50x total interpolation.
- Front Gain is set to 78 dB
- First 8 Channels are configured to process 8 CDMA signals
- The output of this experiment shows the channels stacked against each other. The frequency spacing in the stack is 1.25MHz.
- The channel that would be just to the left of 0MHz has been turned off in order to show the noise rejection between two channels of the chip.

TD-SCDMA

- A 3 carrier TD-SCDMA signal is applied to the GC5316 inputs with a simulated sample rate of 76.8Msps and an IF frequency of 9.6MHz.
- Simulated rxclk to the gc5316 is 76.8MHz
- Receive FIFOs are enabled
- Receive AGC is bypassed
- Receive Channel 0 is configured in CDMA mode and therefore processes two TD-SCDMA channels, referred to as A and B.
- A channel mixer/nco shifts the 11.2MHz carrier to DC, the B channel shifts the 8MHz carrier to DC.
- The CIC filter is programmed to decimate by 15 using a m=2 comb section configuration. The output sample rate at the CIC output is 5.12Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 28 tap filter, which is the maximum length that can be computed with rxclk at 76.8MHz and the CFIR output rate of 5.12Msps.
- The 60 tap PFIR provides final symbol shaping and filtering. 60 taps is the maximum length that can be computed with a 76.8MHz rxclk and 5.12Msps output rate
- Channel AGC is configured as fixed unity gain
- Baseband data is decimated by 2 in the output interface, and then transmitted and captured using the serial interface at the full rxclk rate.

GSM

- A 24-carrier GSM signal is applied to the GC5316 inputs with a simulated sample rate of 34.6665Msps.
- Simulated rxclk to the GC5316 is 69.333MHz
- Receive FIFOs are enabled
- Receive AGC is bypassed
- The DDC channel has a 64-tap PFIR at 4x, 48-tap CFIR at 8x, 32 Decimation ratio for CIC filter. (The DUC would be similar and would have 63-tap PFIR at 4x, and a 47-tap CFIR at 8x. The CIC ratio is 32, the CFIR ratio is 2, and the PFIR ratio is 1).
- Baseband data is transmitted and captured using the serial interface at the full rxclk rate.

WCDMA

- Four real WCDMA carriers is applied to the GC5316 rxin_a
- Simulated rxclk to the GC5316 is 122.88MHz
- Receive FIFOs are enabled
- Receive Channels 0-3 are configured to process the signal
- Channel NCOs tune to four different IF frequencies
- The CIC filter is programmed to decimate by 5. The output sample rate at the CIC output is 15.36Msps
- The CFIR filter compensates for the droop in the CIC filter, and provides some low pass filtering. It is configured as a 20 tap filter.
- The 40 tap PFIR provides final symbol shaping and filtering
- Channel AGC is configured as fixed unity gain
- Baseband data is transmitted and captured using the serial interface at the full rxclk rate.

2.2.5 GC Studio References

For more information on GC Studio, see the GC Studio User's Manual included with the software distribution. GC Studio also contains a powerful scripting language for expert users, see the SCR GC101 Language Reference also included in the software distribution. Selecting Help > User's Manuals in the GC Studio menu to these documents.

3 GC5316 Daughtercard Description

3.1 GC5316 Power and Ground Signal Description

- VDUT1 – 3.3V power from GC101 EVM to the daughtercard
- GND

See the GC101 EVM Manual for the 168 pin connector table. Detailed schematics for the GC5316 daughtercard can be found in Section 3.

3.2 GC5316 Daughtercard Jumpers

3.3V power for the GC5316 daughtercard can be supplied by the GC101 motherboard or an external power supply. A regulator on the daughtercard can be used to generate the 1.5V core supply voltage or an external supply can be used.

Jumper W1 – Selects source for GC5316 core 1.5V power

position 1:2 selects an external supply connected to J2 for the 1.5V core supply

position 2:3 selects the regulator on the daughtercard as the 1.5V core supply

Jumper W2 Selects source for GC5316 I/O 3.3V power

position 1:2 selects an external supply connected to J3 for the 3.3V I/O supply

position 2:3 selects the GC101 motherboard as the source for the 3.3V I/O supply

3.3 GC5316 Daughtercard Power Supplies

The GC5316 core power supply is 1.5V. The daughtercard includes a regulator that can be used to supply this 1.5V to the GC5316 or an external power supply can be connected at J2.

The GC5316 I/O power supply is 3.3V, and can be supplied by the GC101 motherboard or an external power supply connected to J3.

4 Physical Description

This chapter describes the physical characteristics and PCB layout of the GC5316 Daughtercard and lists the components used on the module.

4.1 PCB Layout

The board is constructed on a 8-layer, 5.25-inch x 2.7-inch, 0.056-inch thick PCB using FR-4 material. Figures 70 through 77 show the PCB layout for the daughtercard

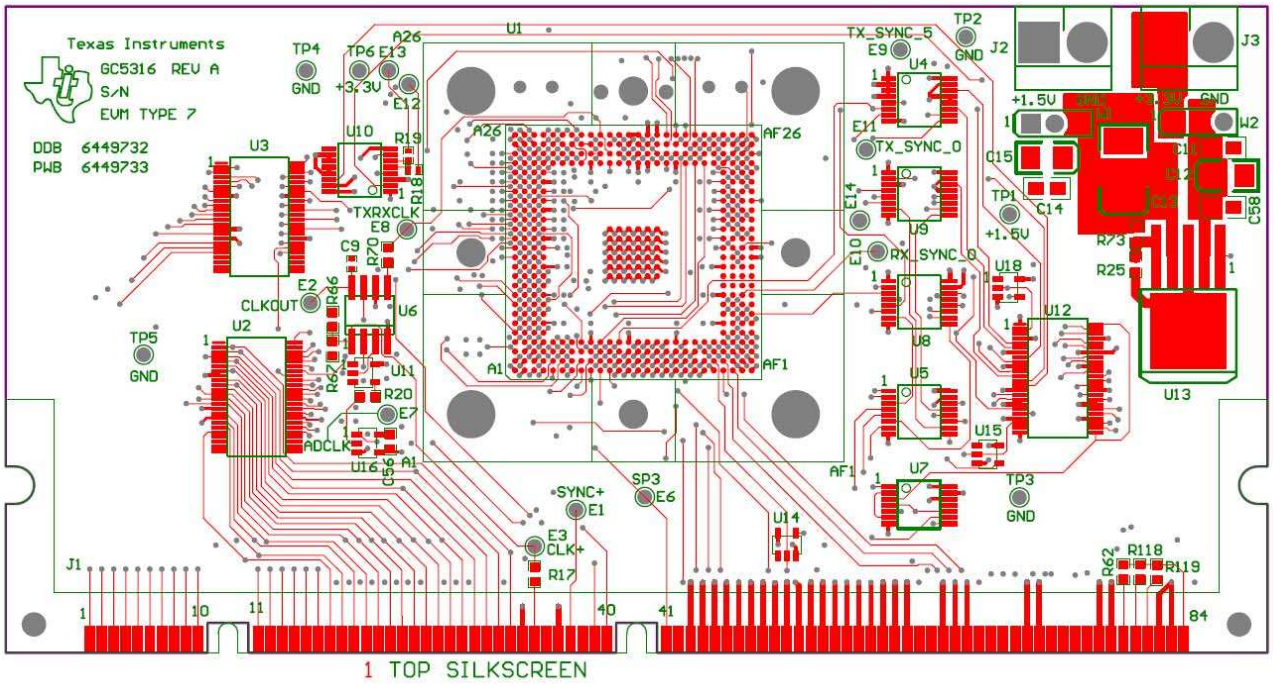

Figure 70. Top Layer 1

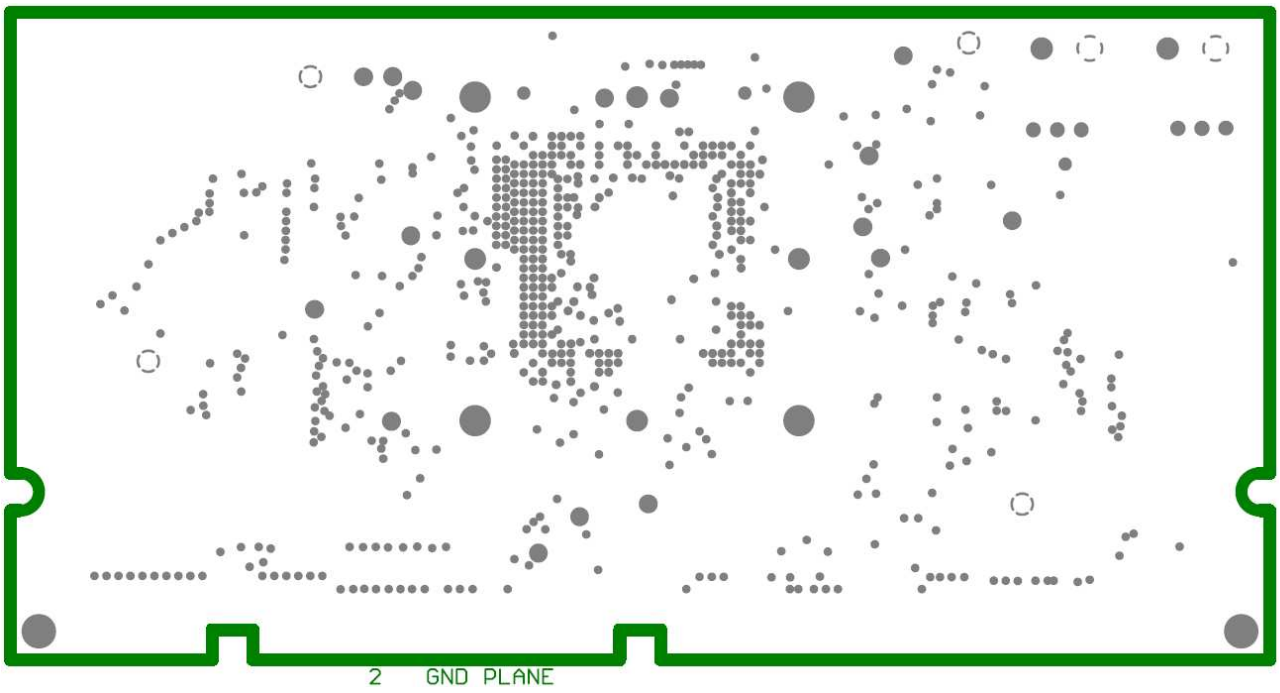

Figure 71. Ground Plane Layer 2

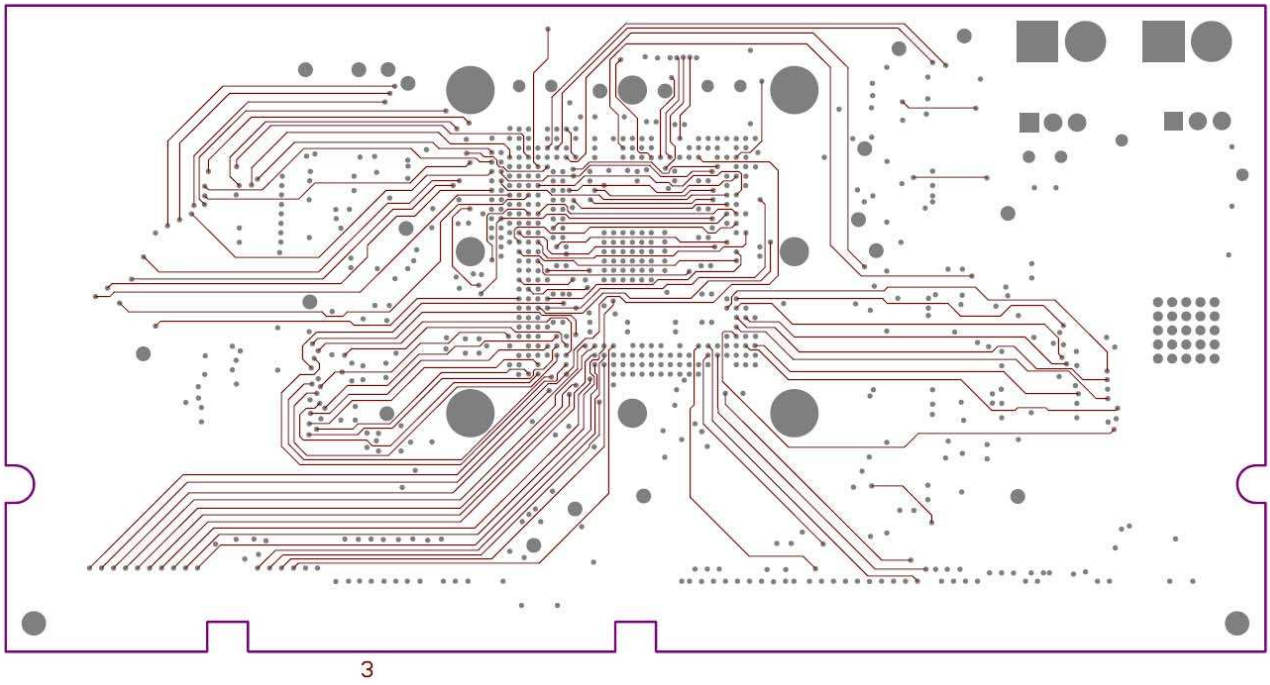

Figure 72. Signal Layer 3

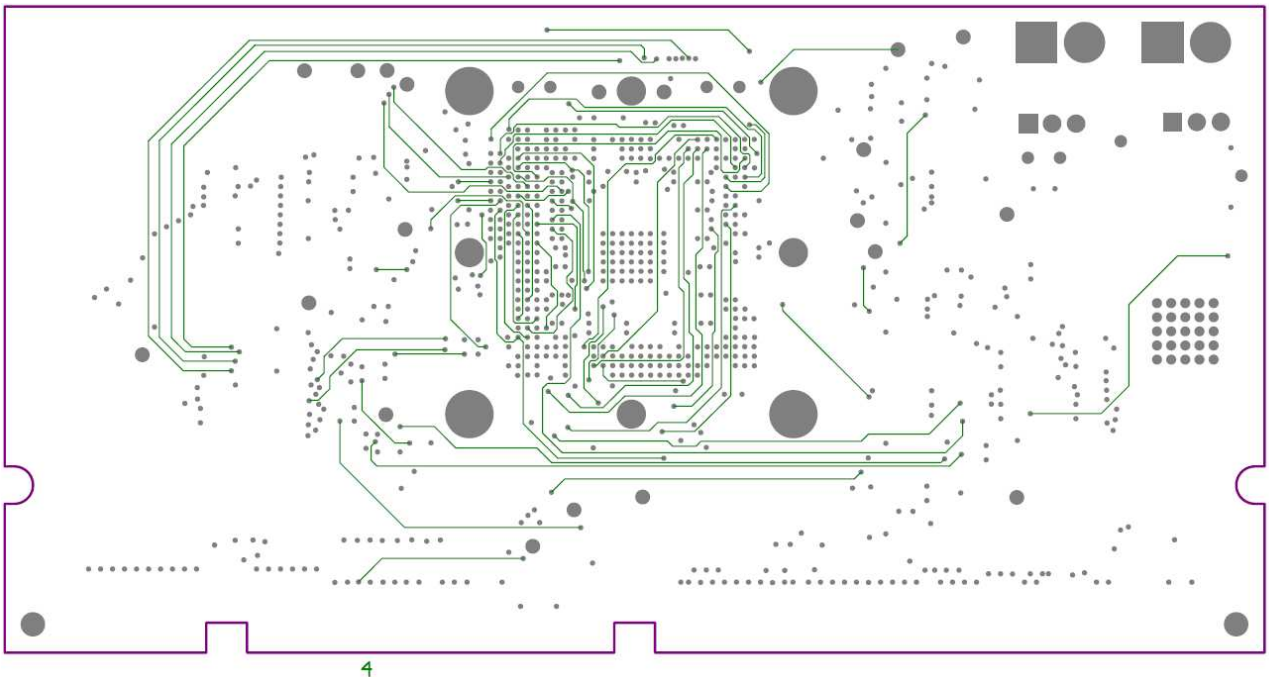

Figure 73. Signal Layer 4

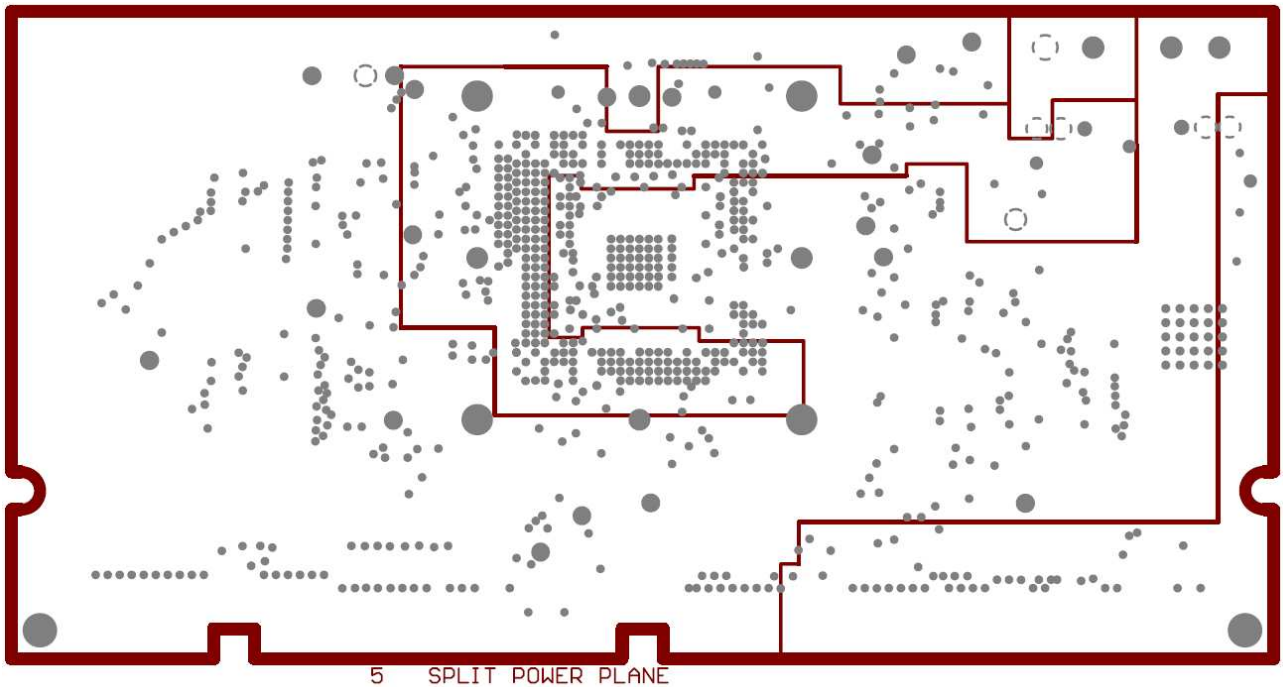

Figure 74. Power Plan Layer 5

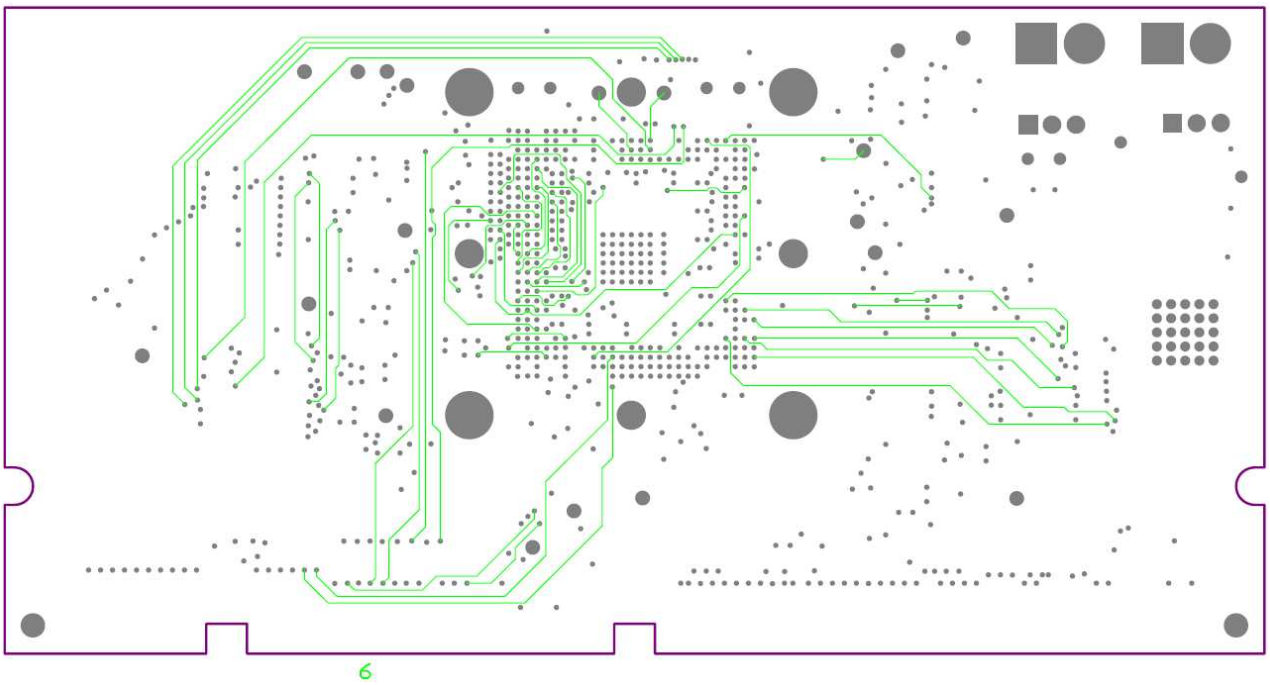

Figure 75. Signal Layer 6

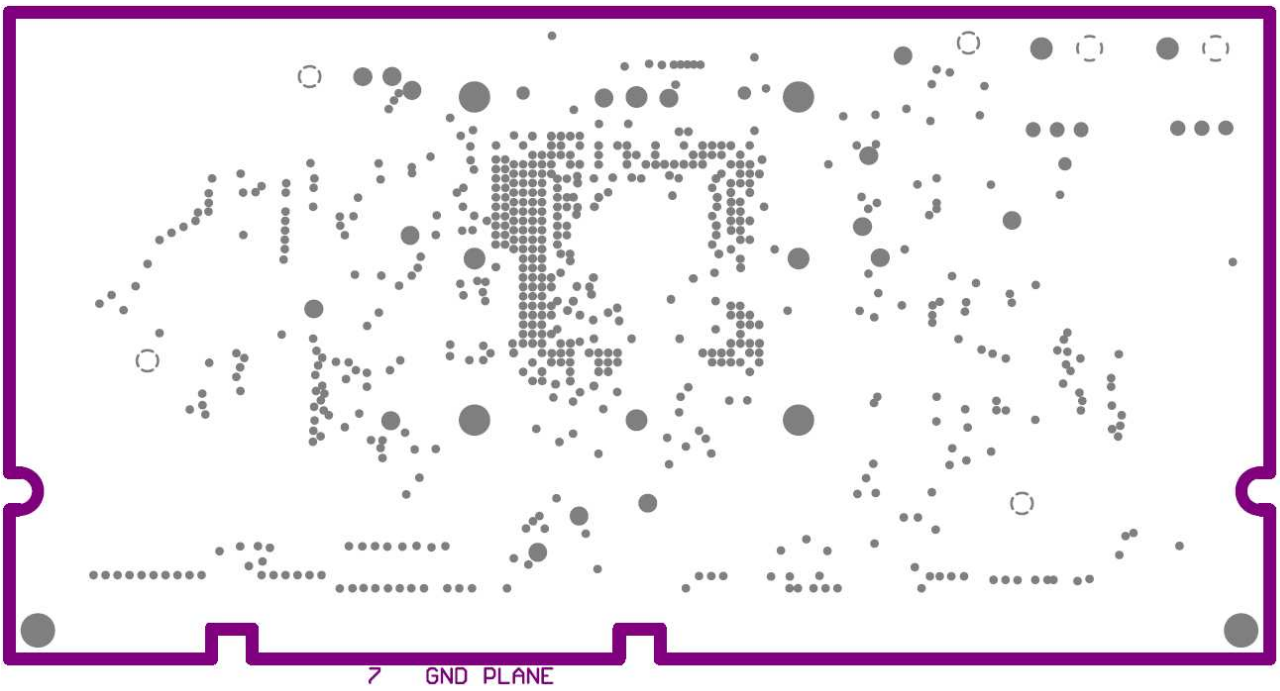

Figure 76. Ground Plane Layer 7

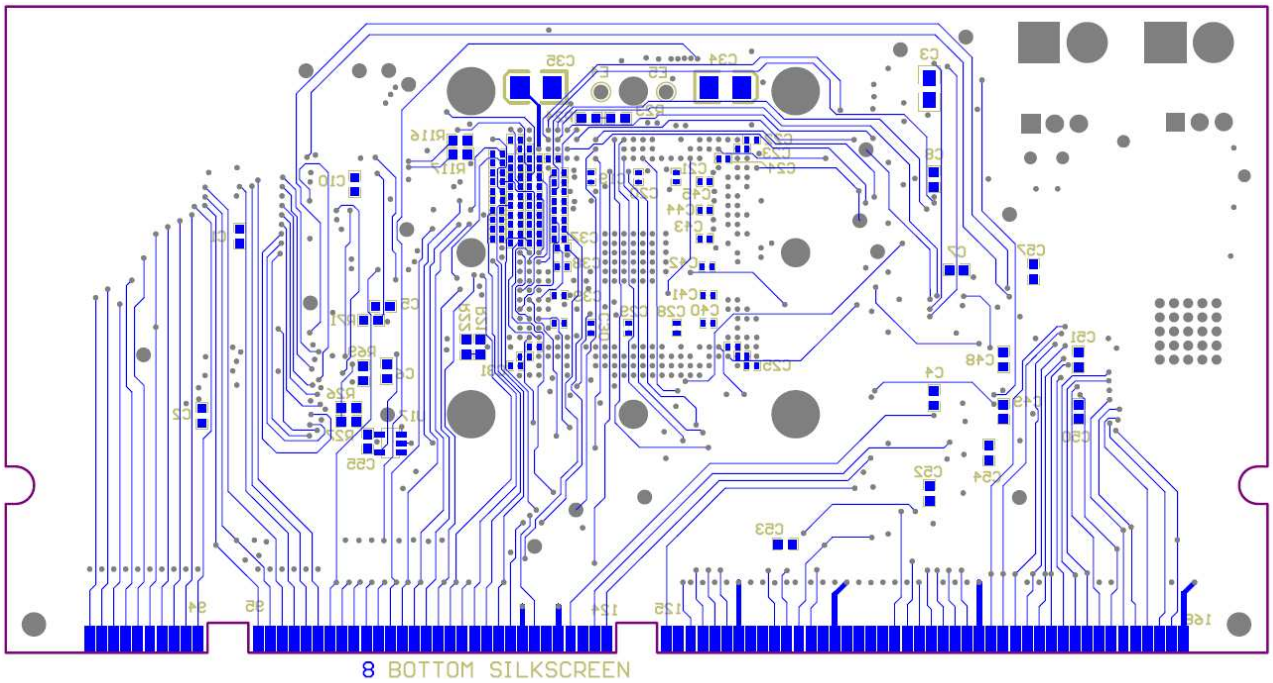

Figure 77. Bottom Layer 8

4.2 Parts List

Table 5-1 lists the parts used in constructing the GC5316 Daughtercard.

Table 1. Bill of Materials

VALUE	QTY	PART NUMBER	VENDOR	REF DES	NOT INSTALLED
CAPACITORS					
47uF, 10V, 10%, Capacitor	1	ECS-T1AD476R	PANASONIC	C13	
2.2uF, 20V, 10%, Capacitor	1	ECS-T1DX225R	PANASONIC	C34	
10uF, 20V, 10%, Capacitor	3	ECS-T1DX106R	PANASONIC	C12 C15 C35	
1uF, 10V, 10%, Capacitor	1	ECJ-2YB1A105K	PANASONIC	C58	
0.1uF, 16V, 10%, Capacitor	3	ECJ-2VB1C104K	PANASONIC	C3 C11 C14	
0.1uF, 16V, 10%, Capacitor	18	ECJ-1VB1C104K	PANASONIC	C1 C2 C4-C8 C10 C48-C57	
0.01uF,16V, 10%, Capacitor	13	ECJ-0EF1C103Z	PANASONIC	C19 C21 C23 C25 C27 C29 C31 C33 C36 C37 C38 C39 C40	
0.1uF,16V, 10%, Capacitor	17	ECJ-0EF1C104Z	PANASONIC	C16 C17 C18 C20 C22 C24 C26 C28 C30 C32 C41-C47	
22pF,50V, 5%, Capacitor	1	ECJ-1VC1H220J	PANASONIC	C22	
10pF,50V, 5%, Capacitor	1	ECJ-0EC1H100D	PANASONIC	C9	
RESISTORS					
100 ohm resistor, 1/16 W, 1%	3	ERJ-3EKF1000V	PANASONIC	R62 R118 R119	
130 ohm resistor, 1/16 W, 1%	4	ERJ-3EKF1300V	PANASONIC	R26 R27 R66 R67	R21 R23 R24
10 Ohm Resistor, 1/16 W, 1%	2	ERJ-3EKF100V	PANASONIC	R69 R70 R71	
0 Ohm Resistor, 1/16 W, 1%	2	ERJ-3GEY0R00V	PANASONIC	R17 R20	
6.81K Ohm Resistor, 1/16 W, 1%	1	ERJ-3EKF6811V	PANASONIC	R73	
30.1K Ohm Resistor, 1/16 W, 1%	1	ERJ-3EKF3011V	PANASONIC	R25	
22.1ohm resistor, 1/16 W, 1%	2	ERJ-3EKF22R1V	PANASONIC	R116 R117	
0 Ohm Resistor, 1/16 W, 5%	2	9C040210R00JLHF3	YAGEO	R18 R19	
22.1ohm resistor, 1/16 W, 1%	36	ERJ-2RKF22R1V	PANASONIC	R1-R16 R32-R36 R38-R48 R76 R77 R80 R81	
CONNECTORS, HEADERS, SWITCHES, LED'S & TEST POINTS					
Red test point	2	5000k	KEYSTONE	TP1 TP6	
Black test point	4	5001k	KEYSTONE	TP2 TP3 TP4 TP5	
CON_2TERM_SCREW	2	KRMZ3	LUMBERG	J2 J3	
3POS-HEADER	2	TWS-150-07-L-S	SAMTEC	W1 W2	
ICs					
GC5316IZED	1	GC5316IZED	TEXAS INSTRUMENTS	U1	
CDCVF2505D	1	CDCVF2505D	TEXAS INSTRUMENTS	U6	
SN74CBTLV16210GR	2	SN74CBTLV16210GR	TEXAS INSTRUMENTS	U2 U3	
SN74CBTLV3253PWR	4	SN74CBTLV3253PWR	TEXAS INSTRUMENTS	U4 U8 U9 U10	
SN74CBTLV3257PWR	1	SN74CBTLV3257PWR	TEXAS INSTRUMENTS	U5	

Table 1. Bill of Materials (continued)

VALUE	QTY	PART NUMBER	VENDOR	REF DES	NOT INSTALLED
SN74LVC08APWR	1	SN74LVC08APWR	TEXAS INSTRUMENTS	U7	
SN74ALVTH16374(DGG)	1	SN74ALVTH16374(DGG)	TEXAS INSTRUMENTS	U12	
SN74CBTLV1G125DBVR	2	SN74CBTLV1G125DBVR	TEXAS INSTRUMENTS	U16 U17	
SN74LVC1G02DBVR	1	SN74LVC1G02DBVR	TEXAS INSTRUMENTS	U11	
SN74LVC1G04DBVR	3	SN74LVC1G04DBVR	TEXAS INSTRUMENTS	U14 U15 U18	
TPS75701KTTT	1	TPS75701KTTT	TEXAS INSTRUMENTS	U13	

4.3 Schematics

TEST IN BUS

J1A
168-CONN-AMP-RA-TH

SIGIN[31]	1	RX_DATA1_15	
SIGIN[30]	2	RX_DATA1_14	
SIGIN[29]	3	RX_DATA1_13	
SIGIN[28]	4	RX_DATA1_12	
SIGIN[27]	5	RX_DATA1_11	
SIGIN[26]	6	RX_DATA1_10	
SIGIN[25]	7	RX_DATA1_9	
SIGIN[24]	8	RX_DATA1_8	
SIGIN[23]	9	RX_DATA1_7	
SIGIN[22]	10	RX_DATA1_6	
SIGIN[21]	11	RX_DATA1_5	
SIGIN[20]	12	RX_DATA1_4	
SIGIN[19]	13	RX_DATA1_3	
SIGIN[18]	14	RX_DATA1_2	
SIGIN[17]	15	RX_DATA1_1	
SIGIN[16]	16	RX_DATA1_0	
SIGIN[15]	17	SIGIN15	
SIGIN[14]	18	SIGIN14	
SIGIN[13]	19	SIGIN13	
SIGIN[12]	20	SIGIN12	
SIGIN[11]	21	SIGIN11	
SIGIN[10]	22	SIGIN10	
SIGIN[9]	23	SIGIN9	
SIGIN[8]	24	SIGIN8	
SIGIN[7]	25	SIGIN7	
SIGIN[6]	26	SIGIN6	
SIGIN[5]	27	SIGIN5	
SIGIN[4]	28	SIGIN4	
SIGIN[3]	29	SIGIN3	
SIGIN[2]	30	SIGIN2	
SIGIN[1]	31	SIGIN1	
SIGIN[0]	32	SIGIN0	
GND	33		
CLK+	34	R17 0 E3	CLK+ (SH 4)
CLK-	36	E1	
GND	37	SYNC+	SYNC+ (SH 2)
SYNCIN+	38		
SYNCIN-	39	test5	test5 (SH 2)
SP1	40	SP2	SP2 (SH 4)
SP2	41	SP3	E6 SP3 (SH 2)
SP3	42		
SP4			

RX_DATA1_[0..15] (SH 2)

SIGIN[0..15] SIGIN[0..15] (SH 2)

+3.3V

U2
SN74CBTLV16210

	1	NC	1OE	48	C0 (SH 3)
SIGIN0	2	1A1	2OE	47	
SIGIN1	3	1A2	1B1	46	RX_DATA0_0
SIGIN2	4	1A3	1B2	45	RX_DATA0_1
SIGIN3	5	1A4	1B3	44	RX_DATA0_2
SIGIN4	6	1A5	1B4	43	RX_DATA0_3
SIGIN5	7	1A6	1B5	42	RX_DATA0_4
	8	GND	GND	41	
SIGIN6	9	1A7	1B6	40	RX_DATA0_5
SIGIN7	10	1A8	1B7	39	RX_DATA0_6
SIGIN8	11	1A9	1B8	38	RX_DATA0_7
SIGIN9	12	1A10	1B9	37	RX_DATA0_8
SIGIN10	13	1A3	1B10	36	RX_DATA0_9
SIGIN11	14	2A2	2B1	35	RX_DATA0_10
	15	VCC	2B2	34	RX_DATA0_11
SIGIN12	16	2A3	2B3	33	RX_DATA0_12
	17	GND	GND	32	
SIGIN13	18	2A4	2B4	31	RX_DATA0_13
SIGIN14	19	2A5	2B5	30	RX_DATA0_14
SIGIN15	20	2A6	2B6	29	RX_DATA0_15
	21	2A7	2B7	28	
	22	2A8	2B8	27	
	23	2A9	2B9	26	
	24	2A10	2B10	25	

C1 .1uF C2 .1uF

U3
SN74CBTLV16210

	1	NC	1OE	48	C1 (SH 3)
TX_DATA_OUT_0_0	2	1A1	2OE	47	
TX_DATA_OUT_0_1	3	1A2	1B1	46	RX_DATA0_0
TX_DATA_OUT_0_2	4	1A3	1B2	45	RX_DATA0_1
TX_DATA_OUT_0_3	5	1A4	1B3	44	RX_DATA0_2
TX_DATA_OUT_0_4	6	1A5	1B4	43	RX_DATA0_3
TX_DATA_OUT_0_5	7	1A6	1B5	42	RX_DATA0_4
	8	GND	GND	41	
TX_DATA_OUT_0_6	9	1A7	1B6	40	RX_DATA0_5
TX_DATA_OUT_0_7	10	1A8	1B7	39	RX_DATA0_6
TX_DATA_OUT_0_8	11	1A9	1B8	38	RX_DATA0_7
TX_DATA_OUT_0_9	12	1A10	1B9	37	RX_DATA0_8
TX_DATA_OUT_0_10	13	1A3	1B10	36	RX_DATA0_9
TX_DATA_OUT_0_11	14	2A2	2B1	35	RX_DATA0_10
	15	VCC	2B2	34	RX_DATA0_11
TX_DATA_OUT_0_12	16	2A3	2B3	33	RX_DATA0_12
	17	GND	GND	32	
TX_DATA_OUT_0_13	18	2A4	2B4	31	RX_DATA0_13
TX_DATA_OUT_0_14	19	2A5	2B5	30	RX_DATA0_14
TX_DATA_OUT_0_15	20	2A6	2B6	29	RX_DATA0_15
	21	2A7	2B7	28	
	22	2A8	2B8	27	
	23	2A9	2B9	26	
	24	2A10	2B10	25	

TX_DATA_OUT_0_[0..15]

J1B
168-CONN-AMP-RA-TH

GND	43		
GND	44		
GND	45		
GND	46		
GND	47		
GND	48		
GND	49		
GND	50	VDUT1	
GND	51		
VDUT1	52		
VDUT1	53		
VDUT1	54		
VDUT1	55		
VDUT1	56		
GND	57		
GND	58		
GND	59		
GND	60		
GND	61		
GND	62		
VDUT3	63		
VDUT3	64		
GND	65		
GND	66		
GND	67		
VDUT2	68		
VDUT2	69		
VDUT2	70		
VDUT2	71		
GND	72		
GND	73		
VDUT4	74		
VDUT4	75		
AGND	76		
AGND	77		
EVM-Type4	78		
EVM-Type3	79	R62 100	
EVM-Type2	80		
EVM-Type1	81	R118 100	
EVM-Type0	82		
GND	83	R119 100	
GND	84		
3P3V			

U1A
GC5316_BGA

RX_DATA0_15	E4	rx_data0_15	tx_data_out_0_17	B19	RAO17	R1 22.1 TX_DATA_OUT_0_17
RX_DATA0_14	C1	rx_data0_14	tx_data_out_0_16	A20	RAO16	R2 22.1 TX_DATA_OUT_0_16
RX_DATA0_13	D2	rx_data0_13	tx_data_out_0_15	C19	RAO15	R3 22.1 TX_DATA_OUT_0_15
RX_DATA0_12	E3	rx_data0_12	tx_data_out_0_14	B20	RAO14	R4 22.1 TX_DATA_OUT_0_14
RX_DATA0_11	F4	rx_data0_11	tx_data_out_0_13	A21	RAO13	R5 22.1 TX_DATA_OUT_0_13
RX_DATA0_10	D1	rx_data0_10	tx_data_out_0_12	D19	RAO12	R6 22.1 TX_DATA_OUT_0_12
RX_DATA0_9	E2	rx_data0_9	tx_data_out_0_11	C20	RAO11	R7 22.1 TX_DATA_OUT_0_11
RX_DATA0_8	F3	rx_data0_8	tx_data_out_0_10	B21	RAO10	R8 22.1 TX_DATA_OUT_0_10
RX_DATA0_7	G4	rx_data0_7	tx_data_out_0_9	A22	RAO9	R9 22.1 TX_DATA_OUT_0_9
RX_DATA0_6	E1	rx_data0_6	tx_data_out_0_8	D20	RAO8	R10 22.1 TX_DATA_OUT_0_8
RX_DATA0_5	F2	rx_data0_5	tx_data_out_0_7	C21	RAO7	R11 22.1 TX_DATA_OUT_0_7
RX_DATA0_4	G3	rx_data0_4	tx_data_out_0_6	B22	RAO6	R12 22.1 TX_DATA_OUT_0_6
RX_DATA0_3	H4	rx_data0_3	tx_data_out_0_5	A23	RAO5	R13 22.1 TX_DATA_OUT_0_5
RX_DATA0_2	F1	rx_data0_2	tx_data_out_0_4	C22	RAO4	R14 22.1 TX_DATA_OUT_0_4
RX_DATA0_1	G2	rx_data0_1	tx_data_out_0_3	B23	RAO3	R15 22.1 TX_DATA_OUT_0_3
RX_DATA0_0	H3	rx_data0_0	tx_data_out_0_2	A24	RAO2	R16 22.1 TX_DATA_OUT_0_2
			tx_data_out_0_1	D22	RAO1	R76 22.1 TX_DATA_OUT_0_1
			tx_data_out_0_0	C23	RAO0	R77 22.1 TX_DATA_OUT_0_0
RX_DATA1_15	G1	rx_data1_15	tx_data_out_2_17	C9	RAO17	
RX_DATA1_14	H2	rx_data1_14	tx_data_out_2_16	D10	RAO16	
RX_DATA1_13	J3	rx_data1_13	tx_data_out_2_15	A8	RAO2	
RX_DATA1_12	K4	rx_data1_12	tx_data_out_2_14	B9	RAO3	
RX_DATA1_11	H1	rx_data1_11	tx_data_out_2_13	C10	RAO4	
RX_DATA1_10	J2	rx_data1_10	tx_data_out_2_12	A9	RAO5	
RX_DATA1_9	K3	rx_data1_9	tx_data_out_2_11	D11	RAO6	
RX_DATA1_8	J1	rx_data1_8	tx_data_out_2_10	B10	RAO7	
RX_DATA1_7	L4	rx_data1_7	tx_data_out_2_9	C11	RAO8	
RX_DATA1_6	K2	rx_data1_6	tx_data_out_2_8	A10	RAO9	
RX_DATA1_5	L3	rx_data1_5	tx_data_out_2_7	B11	RAO10	
RX_DATA1_4	K1	rx_data1_4	tx_data_out_2_6	A11	RAO11	
RX_DATA1_3	L2	rx_data1_3	tx_data_out_2_5	C12	RAO12	
RX_DATA1_2	M4	rx_data1_2	tx_data_out_2_4	B12	RAO13	
RX_DATA1_1	L1	rx_data1_1	tx_data_out_2_3	A12	RAO14	
RX_DATA1_0	M3	rx_data1_0	tx_data_out_2_2	D13	RAO15	
			tx_data_out_2_1	C13	RAO1	
			tx_data_out_2_0	B13	RAO0	
	M2		tx_data_out_1_17	B14	RCO17	R32 22.1 TX_DATA_OUT_1_17
	M1	rx_data2_15	tx_data_out_1_16	C14	RCO16	R33 22.1 TX_DATA_OUT_1_16
	N3	rx_data2_14	tx_data_out_1_15	D14	RCO15	R34 22.1 TX_DATA_OUT_1_15
	N2	rx_data2_13	tx_data_out_1_14	A15	RCO14	R35 22.1 TX_DATA_OUT_1_14
	P2	rx_data2_12	tx_data_out_1_13	B15	RCO13	R36 22.1 TX_DATA_OUT_1_13
	P3	rx_data2_11	tx_data_out_1_12	C15	RCO12	R38 22.1 TX_DATA_OUT_1_12
	P4	rx_data2_10	tx_data_out_1_11	A16	RCO11	R39 22.1 TX_DATA_OUT_1_11
	R1	rx_data2_9	tx_data_out_1_10	B16	RCO10	R40 22.1 TX_DATA_OUT_1_10
	R2	rx_data2_8	tx_data_out_1_9	A17	RCO9	R41 22.1 TX_DATA_OUT_1_9
	R3	rx_data2_7	tx_data_out_1_8	C16	RCO8	R42 22.1 TX_DATA_OUT_1_8
	T1	rx_data2_6	tx_data_out_1_7	B17	RCO7	R43 22.1 TX_DATA_OUT_1_7
	R4	rx_data2_5	tx_data_out_1_6	D16	RCO6	R44 22.1 TX_DATA_OUT_1_6
	T2	rx_data2_4	tx_data_out_1_5	A18	RCO5	R45 22.1 TX_DATA_OUT_1_5
	U1	rx_data2_3	tx_data_out_1_4	C17	RCO4	R46 22.1 TX_DATA_OUT_1_4
	T3	rx_data2_2	tx_data_out_1_3	B18	RCO3	R47 22.1 TX_DATA_OUT_1_3
	U2	rx_data2_1	tx_data_out_1_2	A19	RCO2	R48 22.1 TX_DATA_OUT_1_2
		rx_data2_0	tx_data_out_1_1	D17	RCO1	R80 22.1 TX_DATA_OUT_1_1
			tx_data_out_1_0	C18	RCO0	R81 22.1 TX_DATA_OUT_1_0
	T4		tx_data_out_3_17	C4	RCO17	
	V1	rx_data3_15	tx_data_out_3_16	D5	RCO16	
	U3	rx_data3_14	tx_data_out_3_15	A3	RCO2	
	V2	rx_data3_13	tx_data_out_3_14	B4	RCO3	
	W1	rx_data3_12	tx_data_out_3_13	C5	RCO4	
	U4	rx_data3_11	tx_data_out_3_12	A4	RCO5	
	V3	rx_data3_10	tx_data_out_3_11	B5	RCO6	
	W2	rx_data3_9	tx_data_out_3_10	C6	RCO7	
	Y1	rx_data3_8	tx_data_out_3_9	D7	RCO8	
	W3	rx_data3_7	tx_data_out_3_8	A5	RCO9	
	Y2	rx_data3_6	tx_data_out_3_7	B6	RCO10	
	AA1	rx_data3_5	tx_data_out_3_6	C7	RCO11	
	W4	rx_data3_4	tx_data_out_3_5	D8	RCO12	
	Y3	rx_data3_3	tx_data_out_3_4	A6	RCO13	
	AA2	rx_data3_2	tx_data_out_3_3	B7	RCO14	
	AB1	rx_data3_1	tx_data_out_3_2	C8	RCO15	
		rx_data3_0	tx_data_out_3_1	A7	RCO1	
			tx_data_out_3_0	B8	RCO0	

(SH 3) TX_DATA_OUT_0_[0..17] TX_DATA_OUT_0_[0..17]

RAO[0..17] RAO[0..17] (SH 2)

RCO[0..17] RCO[0..17] (SH 2)

(SH 3) TX_DATA_OUT_1_[0..17] TX_DATA_OUT_1_[0..17]

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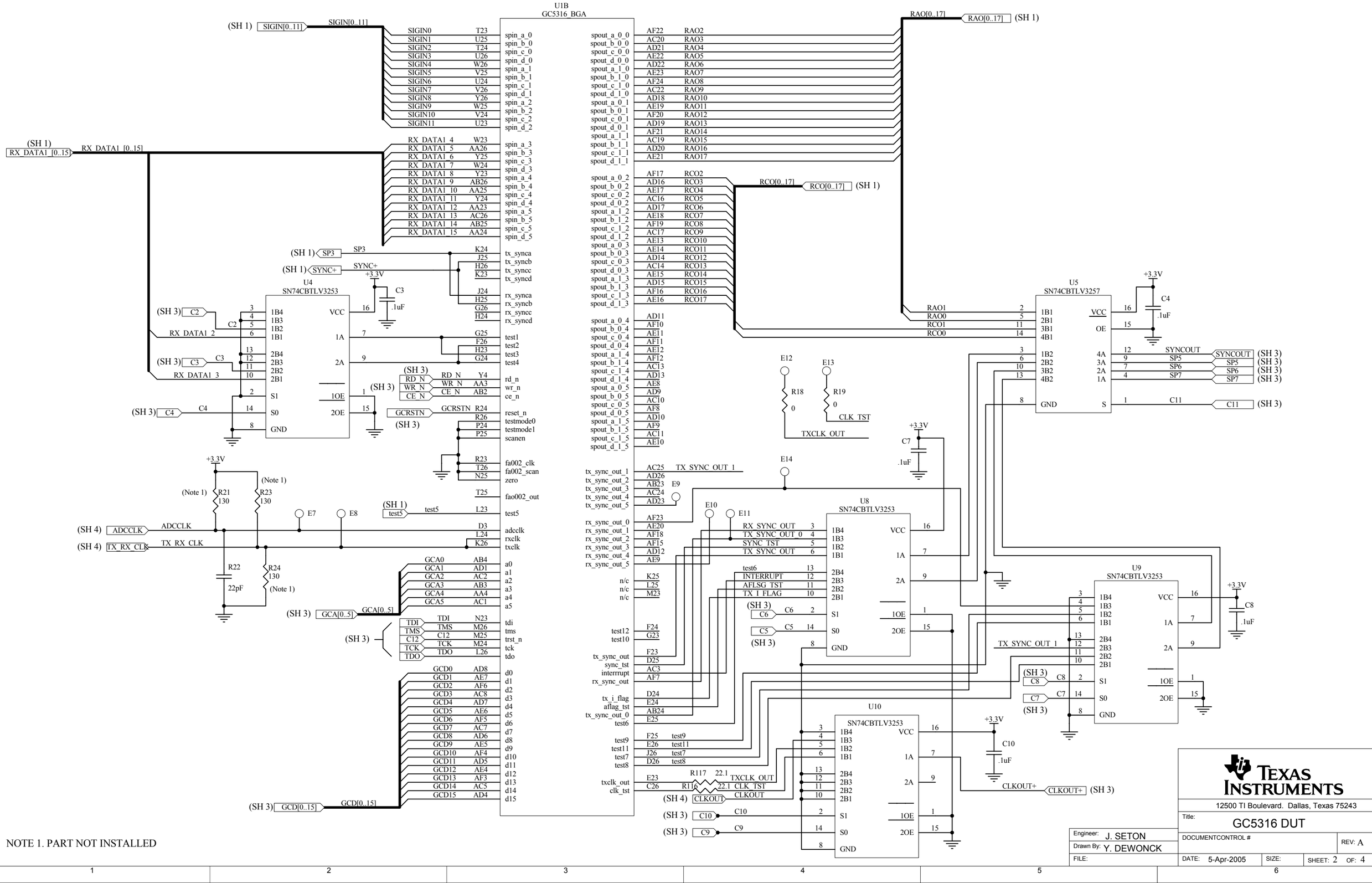
Title: GC5316 DUT			
Engineer: J. SETON	DOCUMENTCONTROL #		REV: A
Drawn By: Y. DEWONCK	DATE: 5-Apr-2005	SIZE:	SHEET: 1 OF: 4
FILE:			



NOTE 1. PART NOT INSTALLED

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Engineer: J. SETON	DOCUMENTCONTROL #		REV: A
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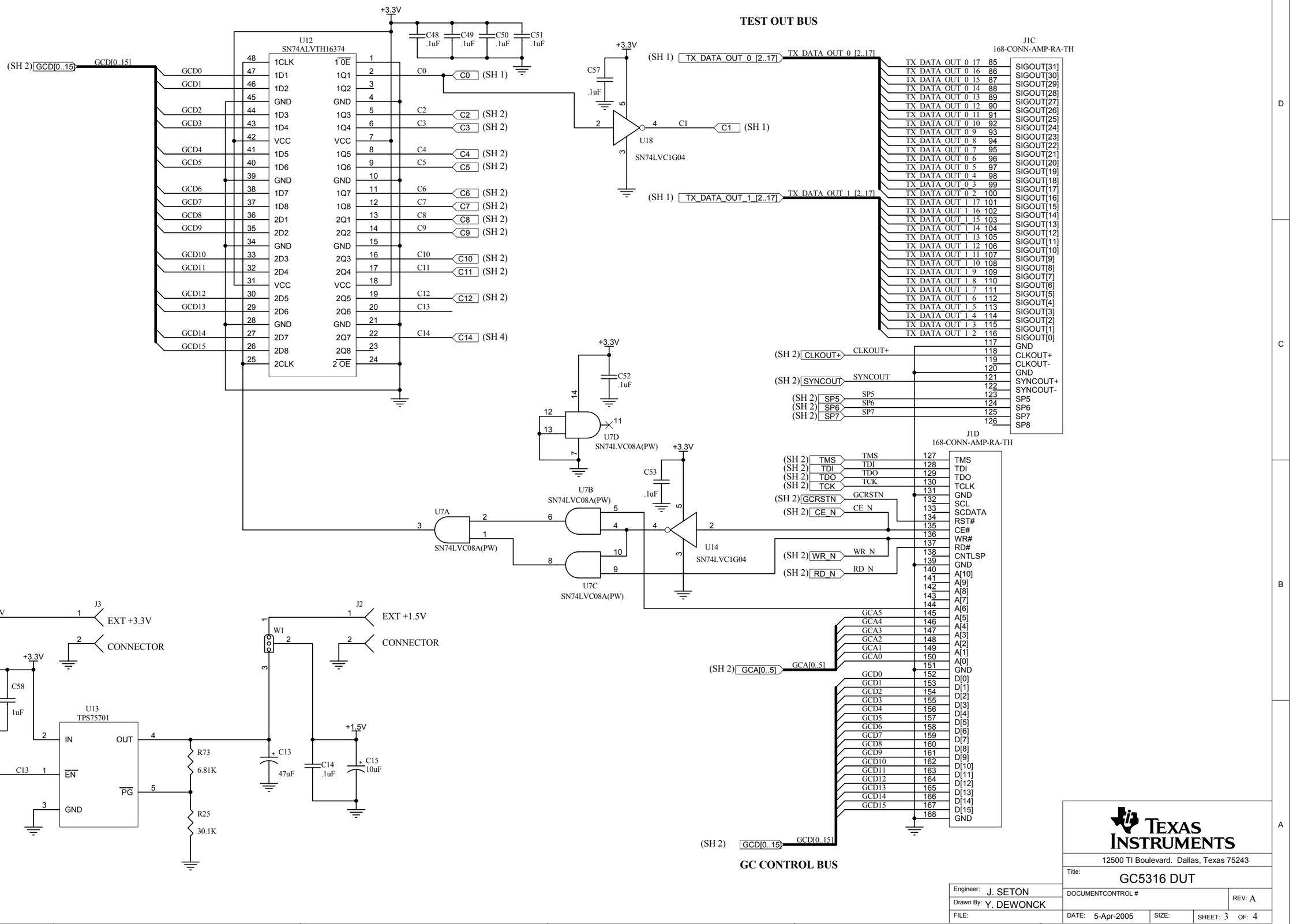
FILE:	DATE: 5-Apr-2005	SIZE:	SHEET: 2 OF: 4



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FILE:	Title: GC5316 DUT
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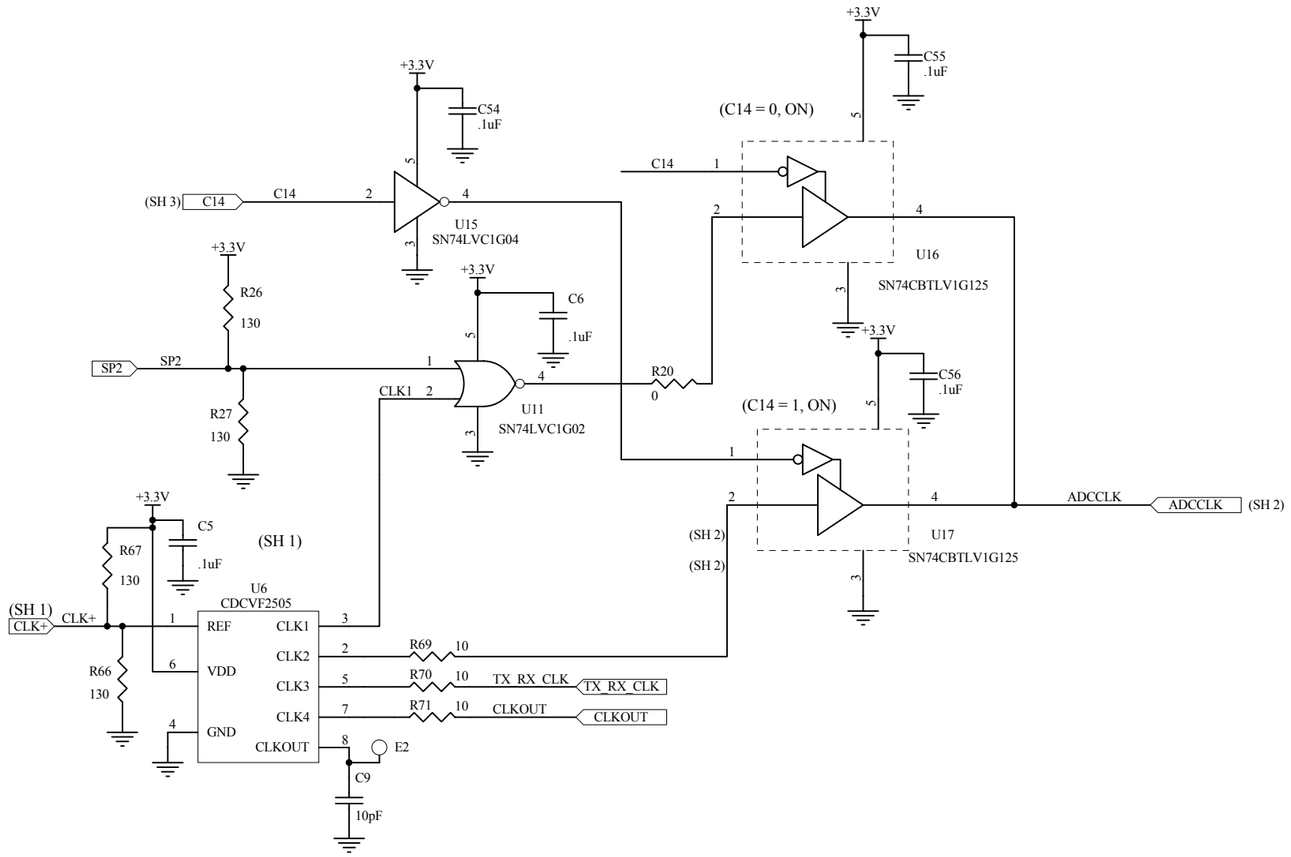
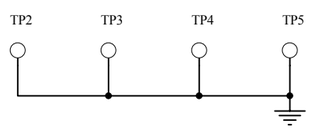
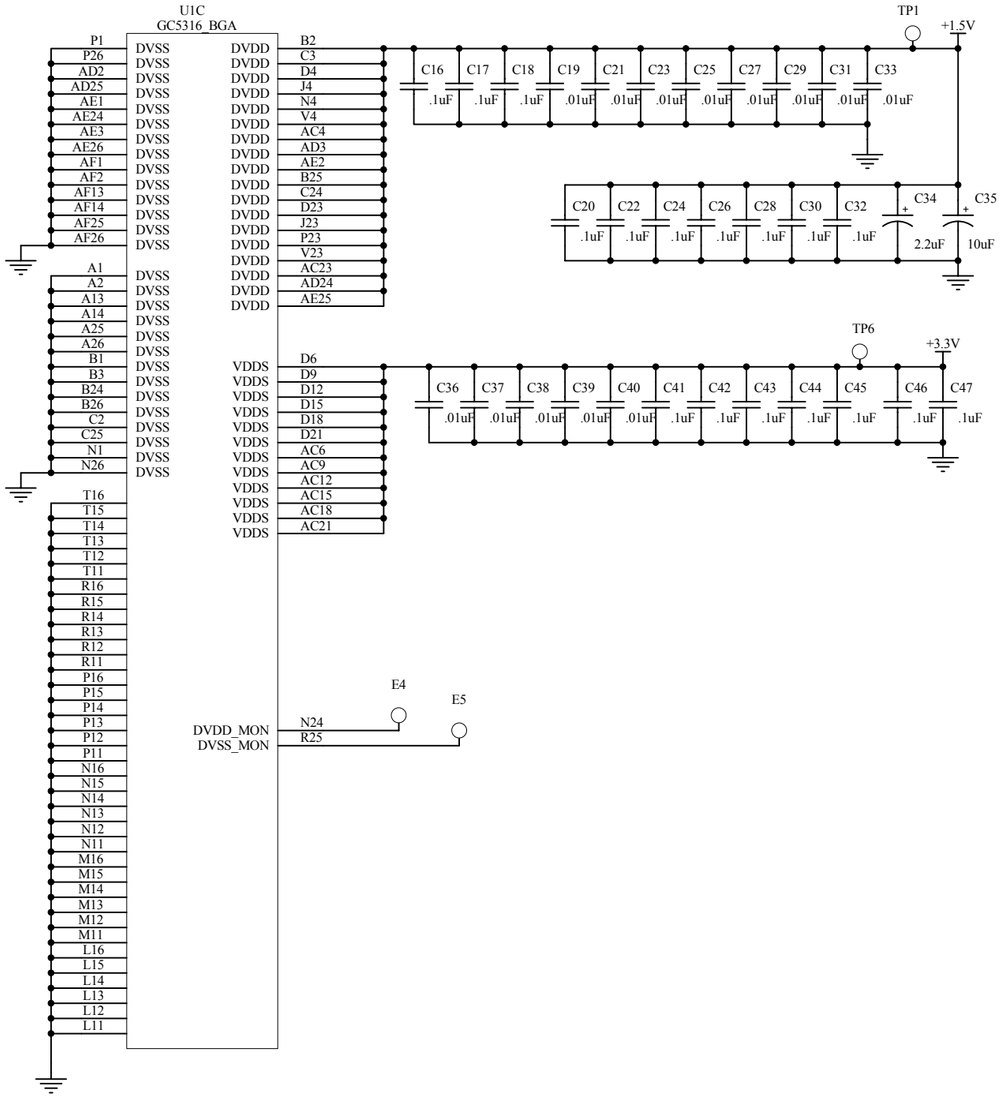
	DATE: 5-Apr-2005 — SIZE: — SHEET: 3 OF: 4

Revision History		
REV	ECN Number	Approved







Engineer:	J. SETON
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FILE:	Sheet4.Sch

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It is important to operate this EVM within the input voltage range of 4.75 V to 5.25 V and the output voltage range of 4.75 V to 5.25 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 70ï½ C. The EVM is designed to operate properly with certain components above 70ï½ C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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