TRF2443 EEPROM

EEPROM Overview

The TRF2443 contains an integrated EEPROM that can easily be read from an external read-back pin (pin RDBKSPI, pin 64). The embedded EEPROM contains information measured and stored at RF final test that allows the user to optimize performance of the TRF2443. In order to ensure the integrity of the EEPROM contents, it is important that the user adhere to the correct power supply sequence. The pin VCCREF (pin 15) must be powered to 3.3 V at the same time or before pin VCCSPI (pin 75). If VCCSPI is powered before VCCREF, the contents of the EEPROM registers will be erased. For this reason, it is recommended that the user read the EEPROM contents once and store this data in memory outside of the TRF2443 for future use. The EEPROM SPI block (address <00>) has three 32-bit registers (Reg0, 1, 2). Register 1 and Register 2 contain the actual bit information stored in the EEPROM registers. These registers are READ ONLY. Register 0 is used to invoke a read-back operation of the information stored in the EEPROM registers 1 and 2 by specifying which register to read back. This register is a WRITE ONLY register.

Register Description

Register 0

Register 0 is written to the SPI to initiate a read back of the EEPROM registers. The first 5 bits, B<4,0>, of Register 0, make up the address and never change. The first 3 bits, B<2,0>, contain the register address <000> whereas the next 2 bits, B<4,3>, contain the EEPROM SPI address <00>. B<26,5> must all be set to zeroes. B<27> and B<31> must be set to 1. B<30,28> must contain the EEPROM register address that the user wishes to read. If the information stored in Register 1 of the EEPROM is desired, Register 0 must be written with B<30,28>=<001>. If the information stored in Register 2 of the EEPROM is desired, Register 0 must be written with B<30,28>=<010>. The read-back timing is the same as other registers and it is LSB first (i.e., the address information comes out first followed by the data).

Reg0																														
	REG SEL																								Address					
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	x	x	x	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Register 1

The first 5 bits, B<4,0>, of Register 1, make up the address and never change. The first 3 bits, B<2,0>, contain the register address <001> whereas the next 2 bits, B<4,3>, contain the EEPROM SPI address <00>. The remaining bits of Register 1, B<31,5>, contain the information stored in the EEPROM register. An explanation of what information is stored and how this information can be used to optimize device performance is provided in a following section entitled EEPROM Contents.

Reg01																														
Spare Bits																					Q-Trim Value						Address				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	1

Register 2:

The first 5 bits, B<4,0>, of Register 2 make up the address and never change. The first 3 bits, B<2,0>, contain the register address <010>, whereas the next 2 bits, B<4,3>, contain the EEPROM SPI address <00>. The remaining bits of Register 2, B<31,5>, contain the information stored in the EEPROM register. An explanation of what information is stored and how this information can be used to optimize device performance is provided in the section EEPROM Contents.

Reg02																													
Parity/Check Sum						X-Coordinate					Y-Coordinate					Wafer Number					I-Trim Value						Address				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	1	0

Reading Information From EEPROM

In order to read back a register from the EEPROM, the user must issue a read-back command by writing Register 0 of the EEPROM to the SPI. Register 0 must be set up as described in the preceding Register Description of Register 0 with B<30,28> set to the address of the desired register to be read. Register 0 is clocked into the SPI with 32 clock cycles. Register 0 is then latched into the SPI when the LATCH ENABLE signal goes high. During this time when LATCH ENABLE is HIGH, an extra clock cycle is required. The register contents of the desired EEPROM register are clocked out of the RDBKSPI pin on the next 32 clock cycles. In summary, a minimum of 65 clocks are required to read a single register from the EEPROM: 32 clocks to write Register 0, 1 clock during latch of Register 0, and 32 clocks to bring out the register contents. The timing of this procedure is shown in Figure 1.

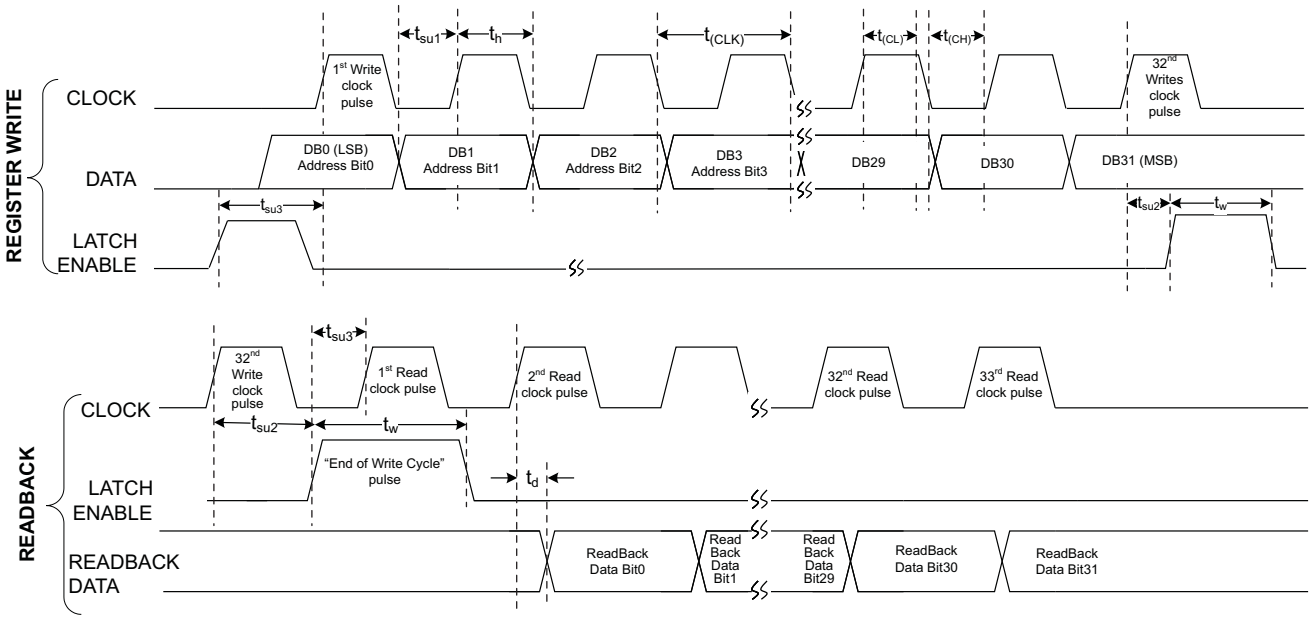

Figure 1. SPI Read-Back Timing

Table 1. SPI Read-Back Timing

Symbol	Parameter	Minimum	Units	Comments
t_h	Hold time, data to clock	20	ns	
t_{SU1}	Setup time, data to clock	20	ns	
$T_{(CL)}$	Clock Low duration	20	ns	
$T_{(CH)}$	Clock High duration	20	ns	
t_{SU2}	Setup time, clock to enable	20	ns	
t_{SU3}	Setup time, latch to clock	70	ns	
t_d	Delay time, clock to read-back data output	10	ns	
t_W	Enable time	50	ns	Equals Clock period
$t_{(CLK)}$	Clock period	50	ns	

Note: The first-time read back of an EEPROM register is used after a power-on-reset of the IC (VCC applied); one DUMMY read-back command needs to be issued. This command is used to internally identify and record the data. An example of a read-back programming following a power-on-reset follows:

Example of Reading EEPROM Data After Power-on-Reset (MSB – LSB):

Command 1 – **<1001,1000,0000,0000,0000,0000,0000,0000> (Dummy read-back command)**
Command 2 – **<1001,1000,0000,0000,0000,0000,0000,0000> (Read-back EEPROM Reg1)**
Command 3 – **<1010,1000,0000,0000,0000,0000,0000,0000> (Read-back EEPROM Reg2)**

EEPROM Error Detection

After reading the information from the EEPROM registers, it is important to check if the data read is correct. This can be done by using the Hamming Code that was generated at the time the EEPROM was programmed at final test. The Hamming Code is located in EEPROM SPI-0, Register 2, B<31,26>. Because of the limitation on the number of bits that a 6-bit Hamming Code can check, the address bits of the EEPROM registers are not checked by the Hamming Code. However, because the address bits never change, the user can check that these bits are correct when reading the EEPROM registers. Register 1 of the EEPROM must always return B<4,0> = <00001>. Register 2 of the EEPROM must always return B<4,0> = <00010>. The remaining data to be checked by the Hamming Code is shown in the following examples and numbered sequentially. B<31,5> of Register 1 becomes B<26,0> of the new data string and B<25,5> of Register 2 becomes B<47,27> of the new data string to be checked by the Hamming Code.

Reg01																														
Spare Bits																					**Q-Trim Value**									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					

The shaded row indicates data checked with Hamming Code.

Reg02																														
Parity/Check Sum						**X-Coordinate**					**Y-Coordinate**					**Wafer Number**					**I-Trim Value**						**Address**				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27					

The new data string is parity checked as follows:

Hamming Code	Register 1																										
New Data String to Be Checked with Hamming code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
REG2<26>: Parity Check 1 (if sum is even parity bit=0, else 1)	x	x		x	x		x		x		x	x		x		x		x		x		x		x		x	x
REG2<27>: Parity Check 2 (if sum is even parity bit=0, else 1)	x		x	x		x	x			x	x		x	x			x	x			x	x			x	x	
REG2<28>: Parity Check 3 (if sum is even parity bit=0, else 1)		x	x	x				x	x	x	x				x	x	x	x					x	x	x	x	
REG2<29>: Parity Check 4 (if sum is even parity bit=0, else 1)					x	x	x	x	x	x	x								x	x	x	x	x	x	x	x	
REG2<30>: Parity Check 5 (if sum is even parity bit=0, else 1)												x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
REG2<31>: Parity Check 6 (if sum is even parity bit=0, else 1)																											x

Hamming Code	Register 2																			
New Data String to Be Checked with Hamming code	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
REG2<26>: Parity Check 1 (if sum is even parity bit=0, else 1)		x		x		x		x		x		x		x		x		x		x	
REG2<27>: Parity Check 2 (if sum is even parity bit=0, else 1)	x	x			x	x			x	x			x	x			x	x			x
REG2<28>: Parity Check 3 (if sum is even parity bit=0, else 1)			x	x	x	x					x	x	x	x					x	x	x
REG2<29>: Parity Check 4 (if sum is even parity bit=0, else 1)							x	x	x	x	x	x	x	x							
REG2<30>: Parity Check 5 (if sum is even parity bit=0, else 1)															x	x	x	x	x	x	x
REG2<31>: Parity Check 6 (if sum is even parity bit=0, else 1)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The user must compare the results of this check with that stored in Register 2, B<31,26>. If the results do not match, an error has occurred and the read-back operation must be repeated until the parity check matches.

EEPROM Contents

The EEPROM inside the TRF2443 contains information measured and stored at RF final test that allows the user to optimize performance of the TRF2443. By using this information, the carrier leakage at the output of the transmitter can be minimized. This section describes how the data that is read from EEPROM is used to achieve this target.

TX Carrier Leakage Optimization

The EEPROM registers contain settings that represent the optimum common-mode bias voltage for the IQ mixer of the transmitter chain. With this optimum bias voltage, the carrier leakage seen on the output of the transmitter chain can be minimized. The optimum setting for the Q-mixer is located in Register 1, B<10,5> whereas the same for the I-mixer is located in Register 2, B<10,5>.

Reg01																														
Spare Bits																				Q-Trim Value						Address				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	1

Reg02																														
Parity/Check Sum						X-Coordinate					Y-Coordinate					Wafer Number					I-Trim Value						Address				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	1	0

Once read from the EEPROM registers, this data must be written to the SPI as follows:

- EEPROM SPI-0, Register 1, B<10,5> write to TX/RX SPI-3, Register 3, B<24,19>
- EEPROM SPI-0, Register 2, B<10,5> write to TX/RX SPI-3, Register 3, B<30,25>

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