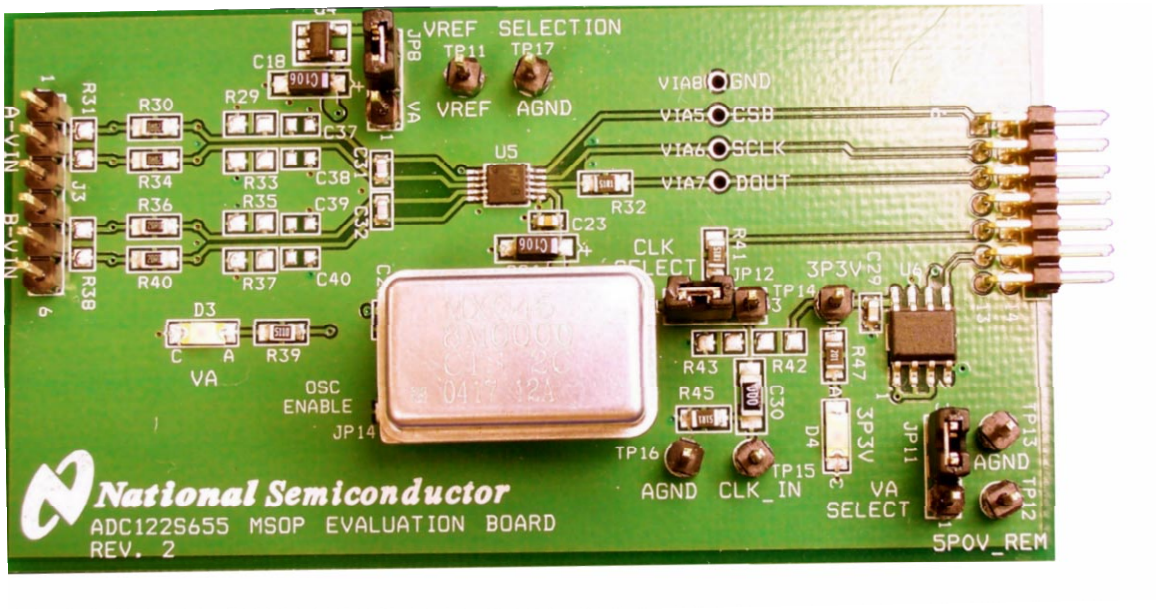
National Semiconductor

January 18, 2008
Rev – 1.0/CS
RoHS Compliant

Evaluation Board User's Guide

ADC122S655 Dual 12-Bit, 200 kSPS to 500 kSPS, Simultaneous Sampling A/D Converter



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1.0 Introduction

The ADC122S655EB/RoHS Design Kit (consisting of the ADC122S655 Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of the National Semiconductor ADC122S655 12-bit Analog-to-Digital Converter. This ADC has two analog input channels that are sampled simultaneously and can operate at speeds up to 500 kSPS. The converter's digital outputs are available on single or dual data ouput pins.

The evaluation board can be used in either of two modes. In Stand Alone, suitable test equipment such as a logic analyzer can be used with the board to evaluate the ADC122S655's performance.

In the Computer mode, data capture and evaluation is simplified by connecting the evaluation board to National Semiconductor's Data Capture Board (order number WAVEVSN BRD 4.1 or higher) which connects to a personal computer through a USB port and runs WaveVision 4 software revision 4.4 or higher.

The latest version of the WaveVision 4 software should be downloaded from the web at http://www.national.com/adc.

Note: WaveVision software version 4.4 or higher is required to evaluate this part with the WV4 Evaluation System.

The WaveVision 4 software operates under Microsoft Windows. The signal at the analog input is digitized, captured, and displayed on a PC monitor in the time and frequency domains.

The software will perform an FFT on the captured data upon command. This FFT plot shows the dynamic performance in the form of SNR, SINAD, THD, SFDR, and ENOB. A software histogram of the captured data is also available.

The signals at analog input J3 are digitized by U5, the ADC122S655. The ADC122S655 either uses a crystal oscillator (Y2) which is provided on this board or an externally supplied clock at TP15.

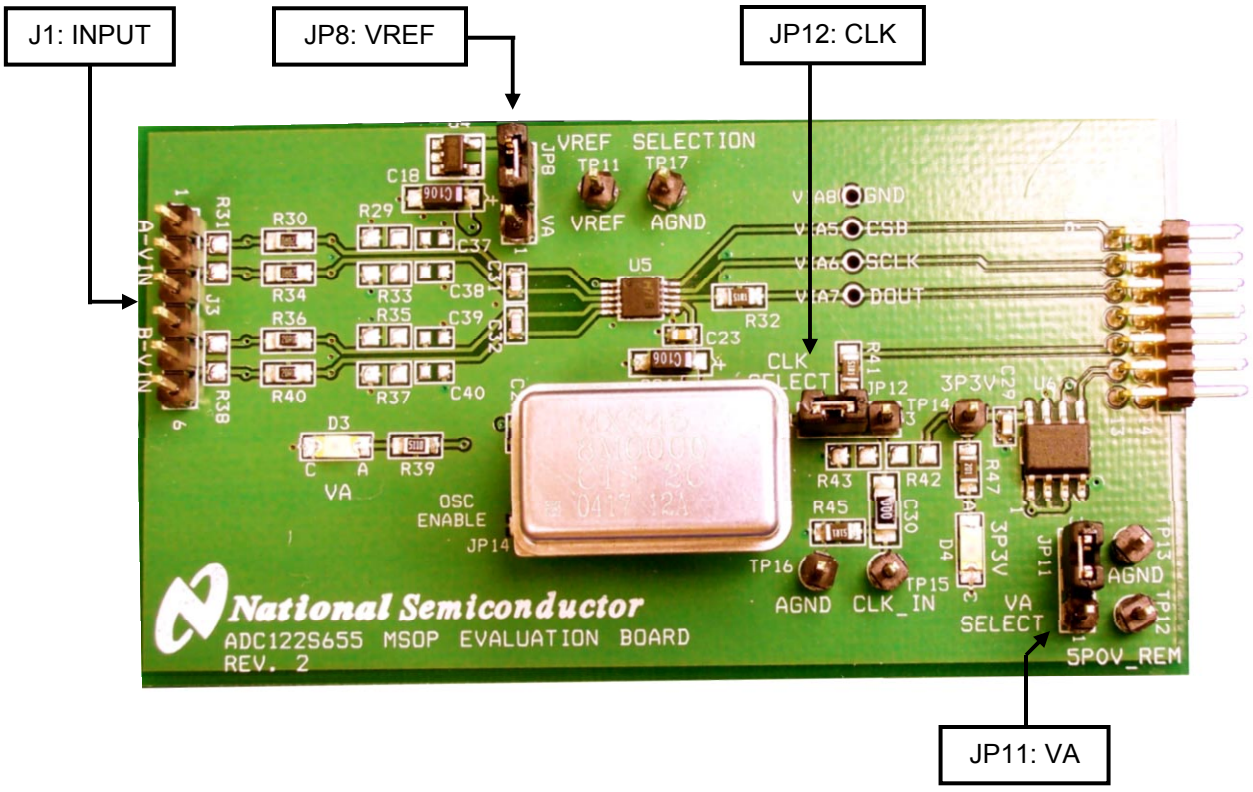

Figure 1 Component and Test Point Locations

2.0 Board Assembly

The ADC122S655EB evaluation board comes fully assembled and ready for use. The provided shorting jumpers are in their recommended locations and suit the needs of most users. The evaluation board also includes a crystal oscillator (Y2). Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement, and to *Figure 10* for the evaluation board schematic.

While the board has been populated in a manner that is most advantageous for typical usage, the board can be customized by adding components to meet the user's specific needs. The board comes ready to use with a DC coupled input signal (*Figure 2*). However, by adding capacitors C21, C22, C25, C26 (value 1µF), adding DC bias resistors R25, R26, R27, R28, R29, R33, R35, R37 (value 4.99kΩ), and removing R30, R34, R36, R40 (value 20Ω), the board can be used with an AC coupled input signal (*Figure 3*).

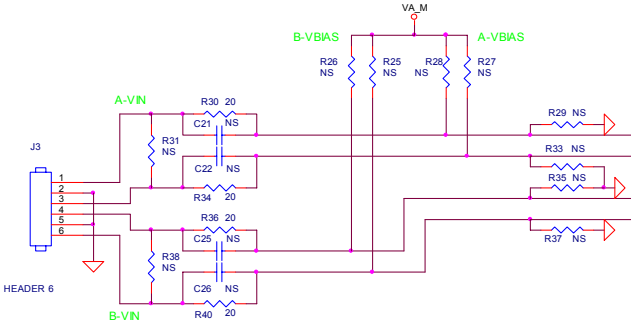

Figure 2: DC Coupled Input Configuration

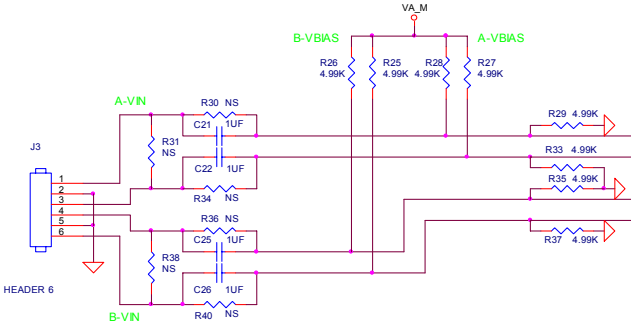

Figure 3: AC Coupled Input Configuration

The board was tested with several different capacitor configurations, and the best performance was found to occur when capacitors C37, C38, C39, C40 were not populated and only differential capacitors C31 and C32 were left in place. If your analog input signal has a great deal of common-mode noise, the user can populate C37, C38, C39, C40 with 470pF capacitors.

3.0 Quick Start

The ADC122S655EB evaluation board may be used in the Stand-Alone mode to capture data with a logic analyzer or third party equipment, or it may be used in the Computer Mode with a WaveVision 4 Data Capture Board, referenced throughout the remainder of this document as WV4. In both cases, the data may be analyzed with the WaveVision 4 software.

3.1 Stand Alone Mode

Refer to *Figure 1* for locations of test points and major components.

1. Remove the jumper from **JP12** and the oscillator **Y2** from its socket. The SPI interface signals (CSB and SCLK) may be driven directly at **J6** or with wires soldered to VIA5 and VIA6 (step 7). DOUT may also be monitored at J6 or with a wire at VIA7. Frequently, a Logic Analyzer with a built-in pattern generator is used to drive CSB and SCLK while monitoring the data output. It is necessary to remove Y2 because the presence of a second clock source could add noise to the conversion process.
2. Connect a clean analog (not switching) +5.0V power source with a 300mA current limit to the external power connector **TP12**. Ground **TP13**.
3. Place a shorting jumper across **pins 1 & 2 of JP11** and turn on the power supply.
4. To analyze the performance of channel A, connect a differential signal across **pins 1 & 3 of J3** (pin 2 is ground). Please note the evaluation board is assembled for a DC-coupled input source. To analyze channel B, connect your signal across **pins 4 & 6 of J3** (pin 5 is ground). If the source has a 50 ohm output impedance, install a 51 ohm resistor at R31 or R38, depending on which channel you are using (match the source impedance with resistors R31 or R38). To accurately evaluate the performance of the ADC122S655, the source must be better than 90dB THD.
5. Select the 2.5V voltage reference as V_{REF} by placing a shorting jumper across **pins 2 & 3 of JP8**.
6. If it is desirable to provide an external reference voltage, the jumper must be removed from JP8 and TP11 (VREF) may be driven directly. Refer to the datasheet for acceptable common mode voltage ranges for specific reference voltages.

7. Apply the signals to control the SPI interface at J6 or VIA5 to VIA7. See the evaluation board schematic (*Figure 10*) or the J6 header pin out (*Figure 5*) for more details.

3.2 Computer Mode

Refer to *Figure 1* for locations of test points and major components.

1. Run the WV 4 program, version 4.4 or higher is required to interface to the WV4 board. While the program is loading, continue below.
2. Connect a USB cable between the WV4 board and the PC running the WaveVision 4 software.
3. Connect the **J6** header on the ADC122S655 evaluation board to the **J7** WV4 serial connector on the WV4 board. Refer to *Figure 4* for the serial connection and *Figure 5* for the J6 header pin out.

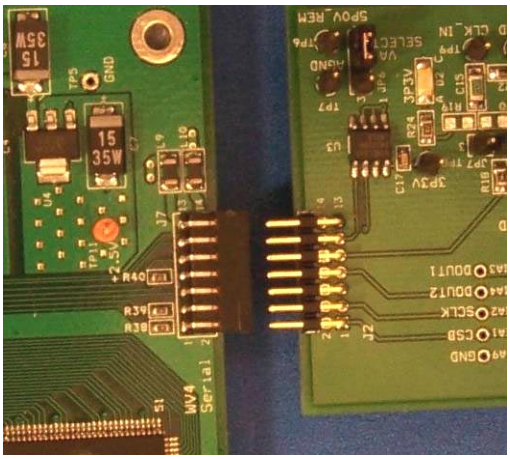

Figure 4: WV4 to ADC122S655 Connection

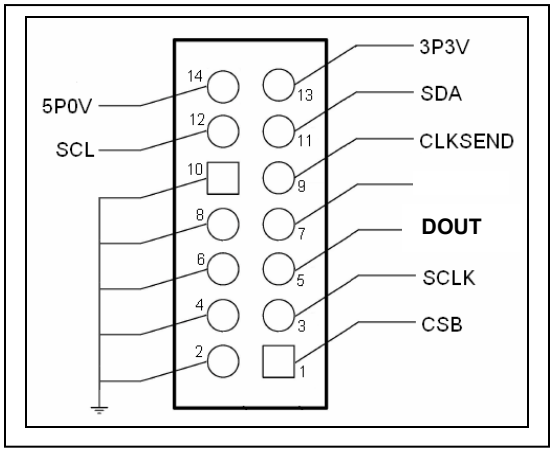

Figure 5: J6 (WV4S) Header Pin Out

4. Connect a clean analog (not switching) +5.0V power source with a 300mA current limit to power connector **J3** on the WV4 board. Ground the GND connector and turn on the power.
5. Connect a clean analog (not switching) +5.0V power source with a 300mA current limit to power connector **TP12** on the ADC board. Ground pin **TP13** and turn on the power. Place a shorting jumper between **pins 1 & 2 of JP11** to power the board. LED D3 should be ON.

   Note: The evaluation board can also be powered directly from the WV4 board by placing a shorting jumper between pins 2 & 3 and removing the external supply.
6. Place an 8 MHz crystal oscillator into the socket at Y2 and place a shorting jumper between **pins 1 & 2 of JP12**. Alternatively, connect a signal generator to TP15 (CLK_IN) and place a shorting jumper between **pins 2 & 3 of JP12** to use an external clock.
7. Place a shorting jumper across **pins 2 & 3 of JP8**, see *table 1* for more details.
8. Perform step 4 of section 3.1 to drive the analog inputs. For information on changing the configuration of the analog input section, read section 2.0 Board Assembly for details. The board comes ready for a DC coupled differential input signal.
9. Perform step 5 or 6 of section 3.1 to select the reference voltage.
10. Refer to section 5.0 on Software Operation and Settings to setup WaveVision 4.

4.0 Functional Description

Table 1 describes the function of the various jumpers on the ADC122S655 evaluation board. The evaluation board schematic is shown in *Figure 10*.

Jumper	Pins 1 & 2	Pins 2 & 3
JP8	Select V_A as V_{REF}	Select +2.5V reg. as V_{REF}
JP11	Select +5.0V external supply	Select +5.0V from J6 (WV4S)
JP12	Select on-board clock OSC Y2	Select external clock from TP15
JP14	Enable OSC (not required)	

Table 1: Jumper Configurations

4.1 Analog Input Signal

The input signal to be digitized can be a differential voltage or a single-ended signal. A differential signal can have a maximum value of +/-VREF and is applied across pins 1 & 3 of J3 for channel A and pins 4 & 6 of J3 for channel B. Pins 2 and 5 are grounds. A single-ended signal can have a maximum value of $2V_{REF}$ and a minimum value of 0V. The signal may be applied to either the non-inverting or inverting input. The opposing input pin must be driven by a maximum voltage of V_{REF} where $V_{REF} \leq V_A / 2$.

R31 and R38 are terminating resistors for the input source. Since all sources do not have the same output impedance, those resistors are not populated. However, those resistors should be added by the user with the appropriate value that matches the source.

When using an AC coupled input signal, DC biasing is required. DC biasing is available for inputs applied to J3 but is currently not populated on the board. Add 4.99 kΩ resistors to R27, R28, R29, R33 to achieve a $V_A/2$ DC bias on channel A and add 4.99kΩ resistors to R25, R26, R35, R37 to achieve a $V_A/2$ DC bias on channel B. Proper DC biasing will allow each input to swing the full range ($-V_{REF}/2$ to $+V_{REF}/2$) where $V_{REF} \leq V_A$.

Dynamic input signals should be applied through a bandpass filter to eliminate the noise and harmonics commonly associated with signal sources. To accurately evaluate the performance of the ADC122S655, the source must be better than -90dBc THD.

4.2 ADC Reference Circuitry

This evaluation board includes the option of selecting a fixed 2.5V reference voltage, V_A, or an external voltage as the reference voltage. Select the 2.5V reference as V_{REF} by shorting pins 2 & 3 of JP8 or select V_A as V_{REF} by shorting pins 1 & 2 of JP8. If it is desirable to provide an external reference voltage, the jumper must be removed from JP8 and TP11 may be driven directly. The recommended range for V_{REF} is 1.0V to V_A.

4.3 SPI Interface

4.3.1 ADC Clock (SCLK)

The clock frequency can range from 6.4MHz to 16MHz. The 16MHz crystal-based oscillator provided on the evaluation board is selected by shorting pins 1 & 2 of JP12. It is best to remove any external signal generator when using this oscillator to reduce any unnecessary noise.

This board will also accept a clock signal from an external source by connecting that source to TP15 (CLK_IN) and shorting pins 2 & 3 of JP12. The input at TP15 is terminated by R45 (value 51Ω). To reduce any unnecessary noise, it is best to remove the oscillator at Y2 when using an external clock source.

Regardless of the clock source selected by JP12, the clock signal is designed to be routed off the ADC122S655 evaluation board to the WV4 board. This assumes computer mode operation of the evaluation board. For applications utilizing the evaluation board in manual mode, the clock is applied directly at J6 or VIA6.

4.3.2 Digital Data Output (DOUT)

The ADC122S655 takes two input signals (channel A and channel B) and outputs to a single data output line (DOUT). The output format is 2's complement with channel A's conversion result followed by channel B's conversion result. The DOUT can be monitored at VIA7 or pin 5 of J6. In computer mode, the DOUT is by the use of the WV4 board and WaveVision 4 software. See the Evaluation Board schematic (*Figure 10)* and ADC122S655 datasheet for further details.

4.3.3 Chip Select Bar (CSB)

The CSB pin may be monitored at VIA5 or pin 1 of J6. In computer mode, the CSB is provided by the WV4 board. In manual mode, the CSB should be driven directly at J6. The signal level for CSB needs to be CMOS compatible. See the ADC122S655 datasheet for logic threshold limits.

4.4 Power Supply Connections

In both the computer and manual modes, the analog supply voltage (V_A) can range between +4.5V and +5.5V. Typical supply currents when applying an external supply to TP12, 5P0V_REM are as follows:

- **for +4.5V** - I = 9mA
- **for +5.5V** - I = 11mA

Note: A majority of this current is for powering devices external to the ADC122S655. When operating in the computer mode, the supply voltage for V_A can be applied externally or supplied directly by the WV4 board through J6. The external supply voltage is selected by placing a shorting jumper across pins 1 & 2 of JP11 and applying a +5.0V power source with a 300mA current limit to TP12 and grounding TP13. To use the supply directly from the WV4 board, place a shorting jumper across pins 2 & 3 of JP11. For the best performance, use an external supply. The +3.3V required to power the EEPROM is obtained through J6 from the WV4 board. LED D4 on the evaluation board will be lit red indicating the EEPROM is powered.

When operating in manual mode, always use an external supply. Apply a +5.0V power source with a current limit of 300mA to TP12 and ground TP13. Place a shorting jumper across pins 1 & 2 of JP11.

5.0 Software Operation and Settings

The WaveVision 4 software is included with the WV4 board and the latest version can be downloaded for free from National's web site at http://www.national.com/adc. WaveVision software version 4.4 or later is required to evaluate this device with the WaveVision system.

To install this software, follow the procedure in the WV4 Board User's Guide. Once the software is installed, run and set it up as follows:

1. Connect the WV4 board to the host computer with a USB cable.
2. From the WaveVision main menu, go to Settings and then Board Settings to open the System Settings window (*Figure 6*) and select the following:
   - WaveVision 4.0 (USB)
   - Number of Samples: 2K to 32K, as desired
   - Data Format: Two's Complement

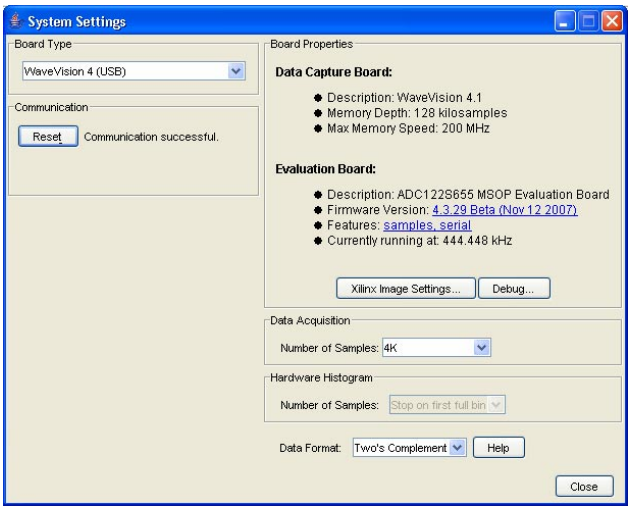

Figure 6: System Settings window

3. Apply power as specified in Section 4.4, click on the **"Test"** button and await the firmware to download.
4. Click on the **"Accept"** button to close the System Settings window.
5. Select the channel to collect data from, either channel A, B, or A & B (*Figure 7*).
6. After the steps outlined in Section 3.2 are completed, click on 'Acquire' then 'Samples' from the Main Menu (you can also press the *F1* shortcut key). If a dialog box opens, select 'Discard' or press the *Escape (Esc)* key to start collecting new samples.

WaveVision main menu will display an output plot. Make sure there is no clipping of data samples. Click on the software histogram tab and ensure data does not exceed the limit of the device. The samples may be further analyzed by clicking on the magnifying glass icon, then clicking and dragging across a specific area of the plot for better data inspection (*Figure 8*). See the WaveVision 4 Board User's Guide for more details.

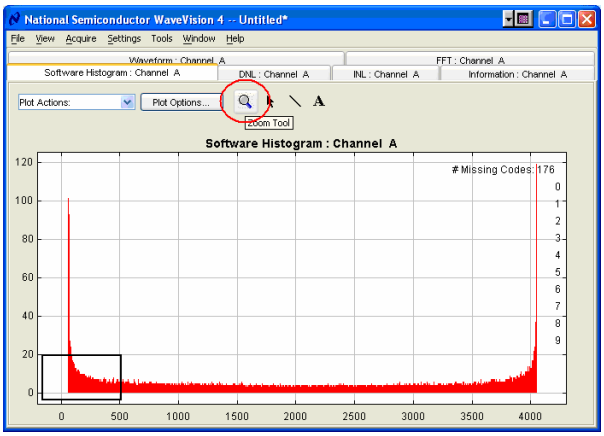

Figure 8: Software Histogram

To view an FFT of the data captured, click on the 'FFT' tab. This plot may be zoomed in on the data plot. A display of dynamic performance parameters in the form of SINAD, SNR, THD, SFDR and ENOB will be displayed at the top right hand corner of the FFT plot (*Figure 9*). Typical values using a V_{REF} = 2.5V and a V_{in} = 4.9 V_{pp} are:

- **SINAD**: 71.594
- **SNR**: 71.939
- **THD**: -82.767
- **SFDR**: 83.164
- **ENOB**: 11.6

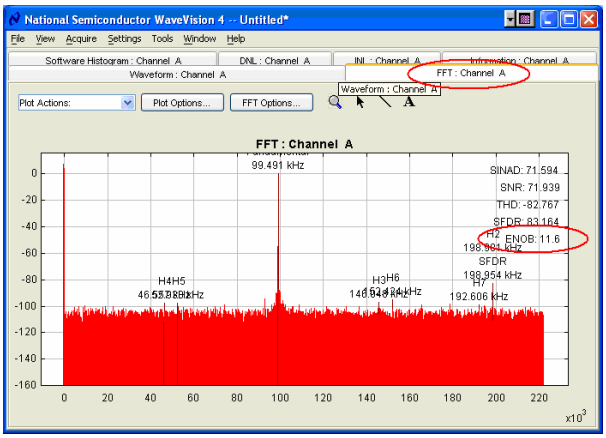

Figure 9: FFT

Acquired data may be saved to a file. Plots may also be exported as graphics. See the Data Capture Board User's Guide for details.

6.0 Evaluation Board Specifications

Board Size:	3.1" x 1.95" (7.9 cm x 5 cm)	
Power Requirements:	Min: +4.5V, 10mA	Max: +5.5V, 13mA
Clock Frequency Range:	6.4 MHz to 16 MHz	
Differential Analog Input:	+/- VREF	

7.0 Test Points, Connectors, and Jumpers

Test Points on the ADC122S655 Evaluation Board

TP11: VREF	V_{REF} test point. Located at the top middle of the board.
TP12: 5P0_REM	5.0V remote test point. Located at the lower left corner of the board.
TP13: AGND	Ground. Located at the lower left corner of the board.
TP14: 3P3V	3.3V test point. Located at the middle right area of the board.
TP15: CLK_IN	Input Clock Signal. Located at the bottom right of the board.
TP16: AGND	Ground. Located at the bottom right of the board.
TP17: AGND	Ground. Located at the top middle of the board.

Connectors on the ADC122S655 Evaluation Board

J3: A-VIN and B-VIN	6 pin male header: Differential input for A and B.
J6: WV4S	14 pin dual row right angle male header: Connects to WV4 board.

Selection Jumpers on the ADC122S655 Evaluation Board (Refer to *table 1* in Section 4.0 for configuration details)

JP8: VREF SELECT	Selects reference source for V_{REF}.
JP11: VA SELECT	Selects V_A (externally or from the WV4 board).
JP12: CLK SELECT	Selects clock source (on-board oscillator or external source).

8.0 Hardware Schematic

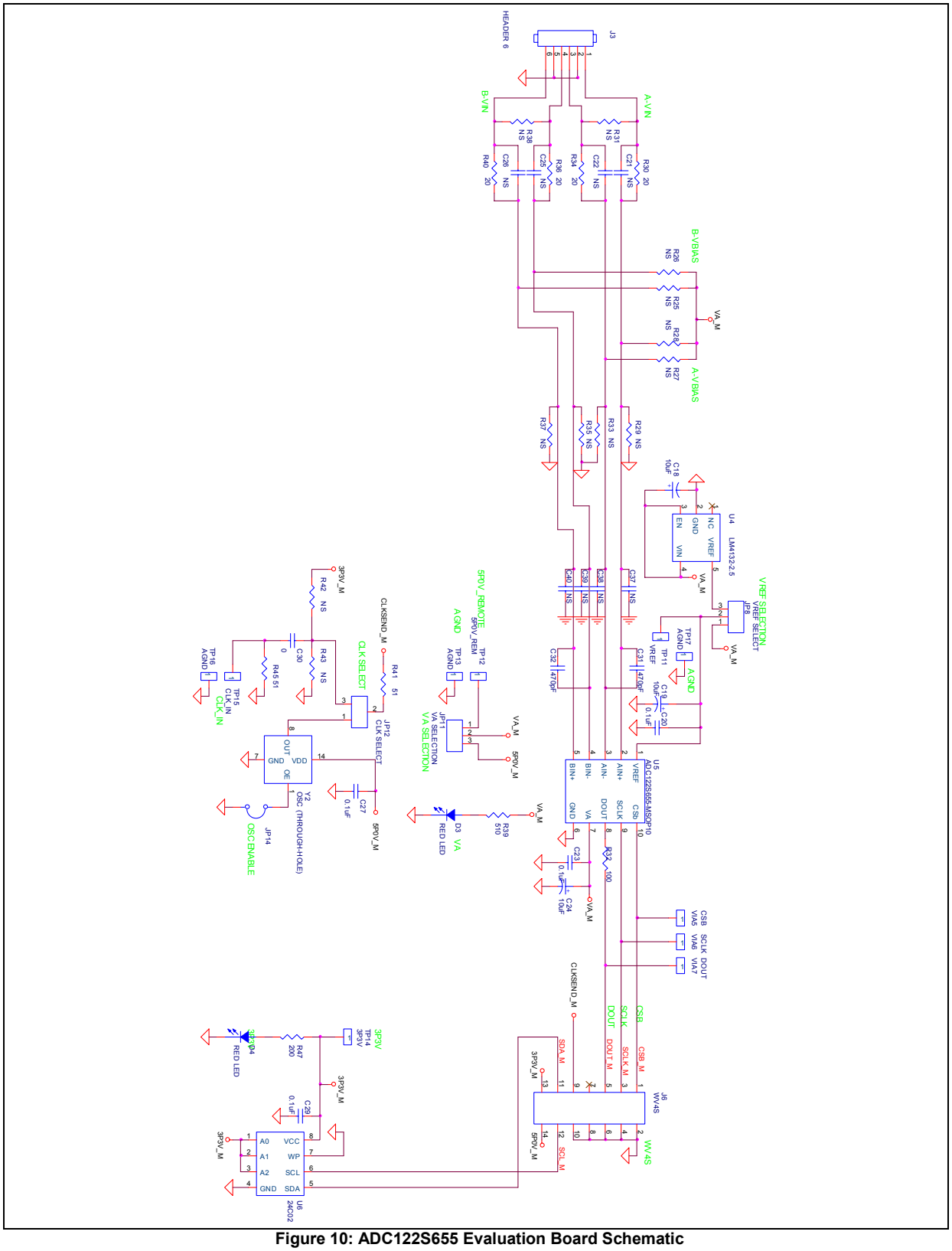

Figure 10: ADC122S655 Evaluation Board Schematic

9.0 Evaluation Board Layers

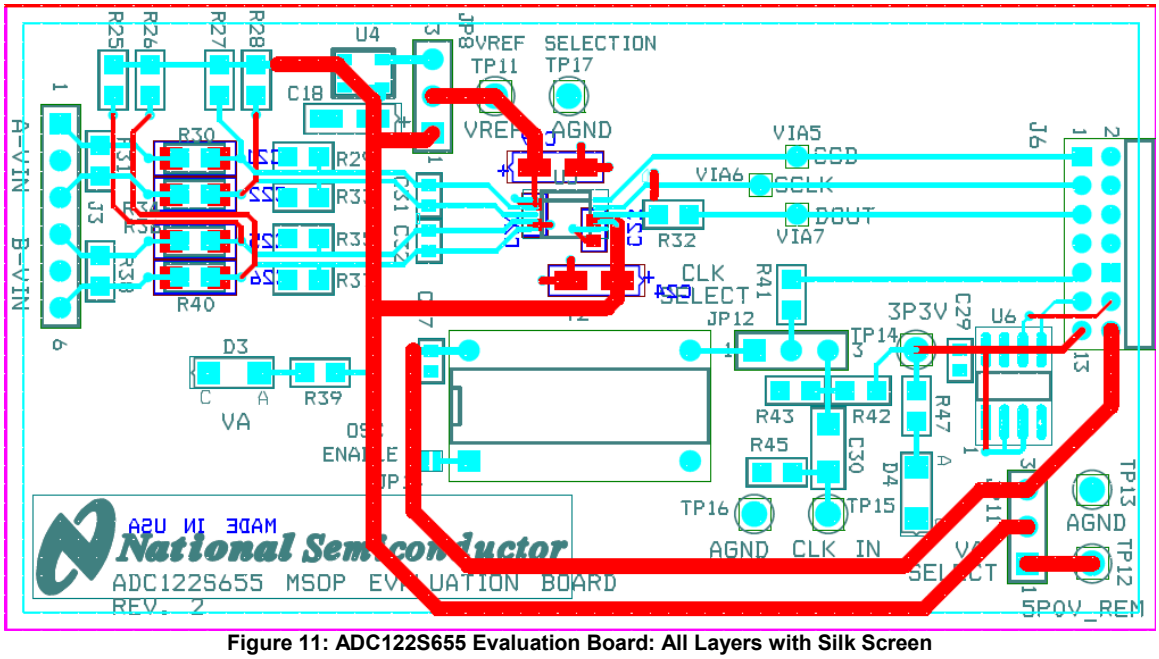

Figure 11: ADC122S655 Evaluation Board: All Layers with Silk Screen

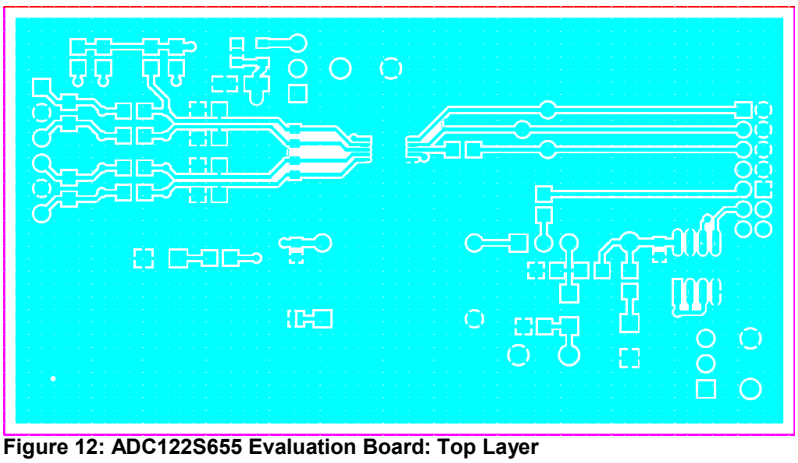

Figure 12: ADC122S655 Evaluation Board: Top Layer

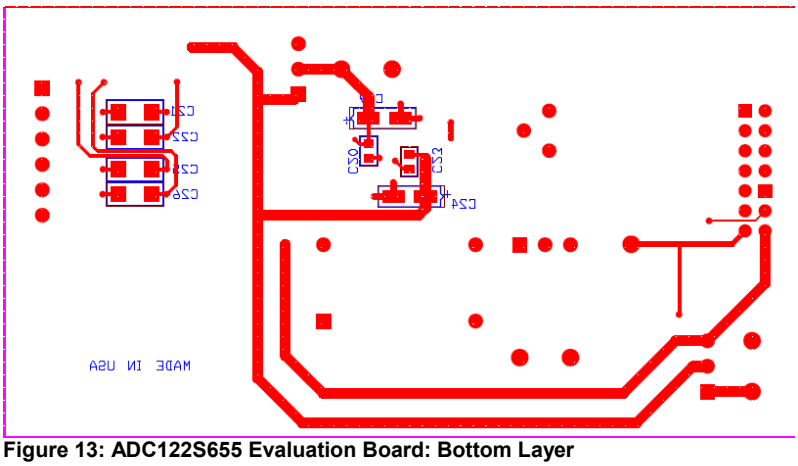

Figure 13: ADC122S655 Evaluation Board: Bottom Layer

10.0 Evaluation Board Bill of Materials

Qty.	Reference	PCB Footprint	Source	Source Part #	Rating	Value
3	C18,C19,C24	sm/ct_3216_12				10uF
4	C20,C23,C27,C29	sm/c_0603			50V	0.1uF
21	JP14,C21,C22,R25,C25, R26,C26,R27,R28,R29, R31,R33,R35,R37,R38, R42,R43,C37,C38,C39, C40					NS
1	C30	sm/c_1206			50V	0
2	C31,C32	sm/c_0603			50V	470pF
2	D3,D4	sm/led_21	Digikey	516-1440-1-ND		RED LED
1	JP8	blkcon.100/vh/tm1sq/w.100/3	Digikey	S1011E-36-ND		VREF SELECT
1	JP11	blkcon.100/vh/tm1sq/w.100/3	Digikey	S1011E-36-ND		VA SELECTION
1	JP12	blkcon.100/vh/tm1sq/w.100/3	Digikey	S1011E-36-ND		CLK SELECT
1	J3	blkcon.100/vh/tm1sq/w.100/6	Digikey	S1011E-36-ND		HEADER 6
1	J6	blkcon/2mm/ra/tm2oe/w2mm/14	Digikey	S5803-21-ND		WV4S
4	R30,R34,R36,R40	sm/r_0805				20
1	R32	sm/r_0805				100
1	R39	sm/r_0805				510
2	R41,R45	sm/r_0805				51
1	R47	sm/r_0805				200
1	TP11	TP_500X/40/W_CASE	Digikey	5003K-ND		VREF
1	TP12	TP_500X/40/W_CASE	Digikey	5003K-ND		5P0V_REM
3	TP13,TP16,TP17	TP_500X/40/W_CASE	Digikey	5011K-ND		AGND
1	TP14	TP_500X/40/W_CASE	Digikey	5003K-ND		3P3V
1	TP15	TP_500X/40/W_CASE	Digikey	5003K-ND		CLK_IN
1	U4	sm/sot23-5				LM4132-2.5
1	U5	SOG.50M/10/WG4.80/L3.00				ADC122S655-MSOP10
1	U6	sog.050/8/wg.244/l.200				24C02
1	VIA5	tp_37/60	Digikey	NS		CSB
1	VIA6	tp_37/60	Digikey	NS		SCLK
1	VIA7	tp_37/60	Digikey	NS		DOUT
1	Y2	crystal_socket	Digikey	A400-ND		OSC (THROUGH-HOLE)

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