CDCE6214-Q1 Register Map

User's Guide

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CDCE6214-Q1 Register Map

1 CDCE6214-Q1 Registers

Table 1 lists the CDCE6214-Q1 registers. All register offset addresses not listed in Table 1 should be considered as reserved locations and the register contents should not be modified.

Table 1. CDCE6214-Q1 Registers

Address	Acronym	Register Name	Section
0x0	R0		Go
0x1	R1		Go
0x2	R2		Go
0x3	R3		Go
0x4	R4		Go
0x5	R5		Go
0x6	R6		Go
0x7	R7		Go
0x8	R8		Go
0x9	R9		Go
0xA	R10		Go
0xB	R11		Go
0xC	R12		Go
0xD	R13		Go
0xE	R14		Go
0xF	R15		Go
0x10	R16		Go
0x11	R17		Go
0x12	R18		Go
0x13	R19		Go
0x14	R20		Go
0x15	R21		Go
0x16	R22		Go
0x17	R23		Go
0x18	R24		Go
0x19	R25		Go
0x1A	R26		Go
0x1B	R27		Go
0x1C	R28		Go
0x1D	R29		Go
0x1E	R30		Go
0x1F	R31		Go
0x20	R32		Go
0x21	R33		Go
0x22	R34		Go

Table 1. CDCE6214-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0x23	R35		Go
0x24	R36		Go
0x25	R37		Go
0x26	R38		Go
0x27	R39		Go
0x28	R40		Go
0x29	R41		Go
0x2A	R42		Go
0x2B	R43		Go
0x2C	R44		Go
0x2D	R45		Go
0x2E	R46		Go
0x2F	R47		Go
0x30	R48		Go
0x31	R49		Go
0x32	R50		Go
0x33	R51		Go
0x34	R52		Go
0x35	R53		Go
0x36	R54		Go
0x37	R55		Go
0x38	R56		Go
0x39	R57		Go
0x3A	R58		Go
0x3B	R59		Go
0x3C	R60		Go
0x3D	R61		Go
0x3E	R62		Go
0x3F	R63		Go
0x40	R64		Go
0x41	R65		Go
0x42	R66		Go
0x43	R67		Go
0x44	R68		Go
0x45	R69		Go
0x46	R70		Go
0x47	R71		Go
0x48	R72		Go
0x49	R73		Go
0x4A	R74		Go
0x4B	R75		Go
0x4C	R76		Go
0x4D	R77		Go
0x4E	R78		Go
0x4F	R79		Go
0x50	R80		Go
0x51	R81		Go

Table 1. CDCE6214-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0x52	R82		Go
0x53	R83		Go
0x54	R84		Go
0x55	R85		Go

Complex bit access types are encoded to fit into small table cells. Table 2 shows the codes that are used for access types in this section.

Table 2. CDCE6214-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

1.1 R0 Register (Address = 0x0) [reset = 0x1000]

R0 is shown in Table 3.

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Table 3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_A0	R/W	0x0	I2C Slave Address bit 0 when either EEPROM page is being used. When HW_SW_CTRL = 'Z', this bit is ignored.
14	PDN_INPUT_SEL	R/W	0x0	PDN pin input type select. Configures the PDN pin as a RESETN pin or SYNCN pin. 0h: RESETN. 1h: SYNCN.
13	GPIO4_DIR_SEL	R/W	0x0	GPIO4 direction select. Configures GPIO4 as Input or Output. 0h: Input. 1h: Output
12	GPIO1_DIR_SEL	R/W	0x1	GPIO1 direction select. Configures GPIO1 as Input or Output. 0h: Input. 1h: Output.
11	RESERVED	R	0x0	Reserved
10	ZDM_CLOCKSEL	R/W	0x0	Selects Internal ZDM Mode or External ZDM Mode. 0h: Internal ZDM Mode. 1h: External ZDM Mode.
9	RESERVED	R	0x0	Reserved
8	ZDM_EN	R/W	0x0	Enables Zero Delay Mode. There are two Zero Delay Modes: Internal Zero Delay Mode (Int. ZDM) and External Zero Delay Mode (Ext.ZDM). 0h: ZDM mode is disabled. 1h: ZDM mode is enabled.
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved

Table 3. R0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SYNC	W1C	0x0	Generates sync pulse (for output divider). This is a self clearing register bit and writing 1h will create the SYNC event.
4	RECAL	W1C	0x0	Self clearing bit. Writing 1h will re-calibrate the PLL
3	RESETN_SOFT	R/W	0x0	Configures the pin PDN as a soft reset pin. 0h: Hard Reset (Resets Registers and State Machine). 1h: Soft Reset (Resets only State Machine).
2	SWRST	W1C	0x0	Soft reset bit. This is a self clearing bit.Writing '1' creates a reset pulse which resets the digital logic except the programmable registers. Soft reset will restart the configuraton and calibration.
1	POWERDOWN	R/W	0x0	Analog Power Down. Powers down Analog sub-blocks. Register settings retained. 0h: Normal Mode. 1h: Power Down Mode.
0	MODE	R/W	0x0	Device mode. This bit should be written directly into EEPROM using direct access method and takes effect at next power-up from EEPROM. 0h: interface mode, I2C available. 1h: pin mode, I2C unavailable, SCL and SDA pins are configured as input GPIO pins.

1.2 R1 Register (Address = 0x1) [reset = 0x2310]

R1 is shown in Table 4.

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Table 4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	GPIO4_INPUT_SEL	R/W	0x2	Input select funciton, this selects the input that can be controlled through GPIO4 that can be programmed as input/output. 0h: FREQ_INC. 1h: FREQ_DEC. 2h: Global OE. 3h: SSC_EN. 4h: OE1. 5h: OE2. 6h: OE3. 7h: OE4. 8h-15h: Do not use
11:8	GPIO3_INPUT_SEL	R/W	0x3	Input select funciton, this selects the input that can be controlled through GPIO3 that can be programmed as input/output. 0h: FREQ_INC. 1h: FREQ_DEC. 2h: Global OE. 3h: SSC_EN. 4h: OE1. 5h: OE2. 6h: OE3. 7h: OE4. 8h-15h: Do not use
7:4	GPIO2_INPUT_SEL	R/W	0x1	Input select funciton, this selects the input that can be controlled through GPIO2 that can be programmed as input/output. 0h: FREQ_INC. 1h: FREQ_DEC. 2h: Global OE. 3h: SSC_EN. 4h: OE1. 5h: OE2. 6h: OE3. 7h: OE4. 8h-15h: Do not use

Table 4. R1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	GPIO1_INPUT_SEL	R/W	0x0	Input select funciton, this selects the input that can be controlled through GPIO1 that can be programmed as input/output. 0h: FREQ_INC. 1h: FREQ_DEC. 2h: Global OE. 3h: SSC_EN. 4h: OE1. 5h: OE2. 6h: OE3. 7h: OE4. 8h-15h: Do not use

1.3 R2 Register (Address = 0x2) [reset = 0x0]

R2 is shown in Table 5.

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Table 5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13:10	RESERVED	R	0x0	Reserved
9:6	GPIO4_OUTPUT_SEL	R/W	0x0	Output Status selection configuration for GPIO4, when it's configured as an output pin. 0h: PLL_LOCK. Others: Do not Use
5:2	GPIO1_OUTPUT_SEL	R/W	0x0	Output Status selection configuration for GPIO1, when it's configured as an output pin. 0h: PLL_LOCK. Others: Do not Use
1:0	REFSEL_SW	R/W	0x0	Reference Clock Selection in software. 0h or 1h: Select clock based on the pin value. 2h: SECREF. 3h: PRIREF.

1.4 R3 Register (Address = 0x3) [reset = 0x0]

R3 is shown in Table 6.

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Table 6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13	DISABLE_CRC	R/W	0x0	Disable the CRC compuation. 0h: CRC is enabled. 1h: CRC is disabled.
12	UPDATE_CRC	W1C	0x0	Writing a '1' will cause the re-computation of CRC. The computed CRC can be read from the live CRC (nvmlcrc) register. This is a self clearing register bit.
11	NVMCOMMIT	W1C	0x0	Commits contents of the EEPROM page selected by REGCOMMIT_PAGE to internal register. This register will self-clear.
10	REGCOMMIT	W1C	0x0	Commits contents of the registers to EEPROM selected by REGCOMMIT_PAGE register. This register will self-clear.

Table 6. R3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	REGCOMMIT_PAGE	R/W	0x0	Decide which page of EEPROM to use for the Register/NVM commit operations. 0h: Page 0. 1h: Page 1.
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	FREQ_DEC_REG	R/W	0x0	Decrements PLL frequency in DCO mode during 1 -> 0 transition. Must be cleared before next event.
5	FREQ_INC_REG	R/W	0x0	Increments PLL frequency in DCO mode during 1 -> 0 transition. Must be cleared before next event.
4	FREQ_INC_DEC_REG_MODE	R/W	0x0	Enables DCO mode through I2C write into the registers. (Pin mode is always enabled when GPIO pins are configured as FREQ_INC / FREQ_DEC). 0h: Disables DCO mode through I2C. 1h: Enables DCO mode through I2C
3	FREQ_INC_DEC_EN	R/W	0x0	Enables DCO mode. 0h: Disables DCO mode. 1h: Enables DCO mode.
2	RESERVED	R	0x0	Reserved
1:0	RESERVED	R	0x0	Reserved

1.5 R4 Register (Address = 0x4) [reset = 0x0]

R4 is shown in Table 7.

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Table 7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x0	Reserved
7	CH4_PD	R/W	0x0	Powers Down CH4 LDO. 0h: Power Up. 1h: Power Down.
6	CH3_PD	R/W	0x0	Powers Down CH3 LDO. 0h: Power Up. 1h: Power Down.
5	CH2_PD	R/W	0x0	Powers Down CH2 LDO. 0h: Power Up. 1h: Power Down.
4	CH1_PD	R/W	0x0	Powers Down CH1 LDO. 0h: Power Up. 1h: Power Down.
3:0	POST_EE_DLY	R/W	0x0	Adds additional powerup to clock output active delay time. Delay = 1ms * post_ee_delay

1.6 R5 Register (Address = 0x5) [reset = 0x8]

R5 is shown in Table 8.

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Table 8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0x0	Reserved
8	PLL_VCOBUFF_LDO_PD	R/W	0x0	VCO buffer LDO power down. 0h: Power Up. 1h: Power Down PFD.

Table 8. R5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	PLL_VCO_LDO_PD	R/W	0x0	VCO LDO power down. 0h: Power Up. 1h: Power Down PFD.
6	PLL_VCO_BUFF_PD	R/W	0x0	VCO buffer power down. 0h: Power Up. 1h: Power Down PFD.
5	PLL_CP_LDO_PD	R/W	0x0	Charge pump LDO power down. 0h: Power Up. 1h: Power Down PFD.
4	PLL_LOCKDET_PD	R/W	0x0	Analog clock detect power down. 0h: Enables Analog Lock Detect. 1h: Disables Analog Lock Detect.
3	PLL_PSB_PD	R/W	0x1	Prescalar B power down. 0h: Power Up. 1h: Power Down.
2	PLL_PSA_PD	R/W	0x0	Prescalar A power down. 0h: Power Up. 1h: Power Down.
1	PLL_PFD_PD	R/W	0x0	Phase frequency detector power down. 0h: Power Up. 1h: Power Down PFD.
0	RESERVED	R	0x0	Reserved

1.7 R6 Register (Address = 0x6) [reset = 0x0]

R6 is shown in Table 9.

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Table 9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.8 R7 Register (Address = 0x7) [reset = 0x0]

R7 is shown in Table 10.

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Table 10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	NVMCRCERR	R	0x0	This bit is set when a CRC error is detected while reading back on-chip EEPROM during device configuration. It is automatically cleared (while NVM is NOT busy) when 1) The NVMCOMMIT is submitted or 2) Update CRC is issued
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

Table 10. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0x0	Reserved
1	LOCK_DET_S	R/W	0x0	Lock Detect (Sticky Bit). This indicates any temporary loss of lock of the PLL and this is cleared only by re-calibration or a hard reset through PDN pin. 0h: No Temporary PLL Unlock. 1h: PLL temporary unlock.
0	LOCK_DET	R	0x0	Reads the PLL Lock status. 0h: PLL is Unlocked. 1h: PLL is locked.

1.9 R8 Register (Address = 0x8) [reset = 0x0]

R8 is shown in Table 11.

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Table 11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.10 R9 Register (Address = 0x9) [reset = 0x0]

R9 is shown in Table 12.

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Table 12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NVMLCRC	R	0x0	Contains the Live CRC byte that has been calculated while loading register values from EEPROM.

1.11 R10 Register (Address = 0xA) [reset = 0x0]

R10 is shown in Table 13.

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Table 13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NVMSCRC	R	0x0	Contains stored CRC value. This value is used to compare with the computed CRC and to update the CRC status bit

1.12 R11 Register (Address = 0xB) [reset = 0x0]

R11 is shown in Table 14.

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Table 14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R	0x0	Reserved
5:0	NVM_RD_ADDR	R/W	0x0	NVM Read Address. The register set (nvm_rd_addr, nvm_rd_data) is used for EEPROM read operation, nvm_rd_addr is the pointer to EEPROM and nvm_rd_data is the register where the read data is stored. To read a EEPROM word, first write the address to nvm_rd_addr, then read the data from nvm_rd_data.

1.13 R12 Register (Address = 0xC) [reset = 0x0]

R12 is shown in Table 15.

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Table 15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NVM_RD_DATA	R	0x0	NVM Read Data. The register set (nvm_rd_addr, nvm_rd_data) is used for EEPROM read operation, nvm_rd_addr is the pointer to EEPROM and nvm_rd_data is the register where the read data is stored. To read a EEPROM word, first write the address to nvm_rd_addr, then read the data from nvm_rd_data.

1.14 R13 Register (Address = 0xD) [reset = 0x0]

R13 is shown in Table 16.

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Table 16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R	0x0	Reserved
5:0	NVM_WR_ADDR	R/W	0x0	NVM Write Address. The register set (nvm_wr_addr, nvm_wr_data) is used for EEPROM write operation, nvm_wr_addr is the pointer to EEPROM and nvm_wr_data is the register which the data should be written to. To write a EEPROM word, first write the address to nvm_wr_addr, then write the data to nvm_wr_data.

1.15 R14 Register (Address = 0xE) [reset = 0x0]

R14 is shown in Table 17.

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Table 17. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NVM_WR_DATA	R/W	0x0	NVM Write Data. The register set (nvm_wr_addr, nvm_wr_data) is used for EEPROM write operation, nvm_wr_addr is the pointer to EEPROM and nvm_wr_data is the register which the data should be written to. To write a EEPROM word, first write the address to nvm_wr_addr, then write the data to nvm_wr_data.

1.16 R15 Register (Address = 0xF) [reset = 0xA020]

R15 is shown in Table 18.

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Table 18. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	EE_LOCK	R/W	0xA	Locks EEPROM for regcommit and EEPROM write operations. To unlock, write 5h.
11:9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	CAL_MUTE	R/W	0x1	Mute the output during the calibration. 0h: Output is unmute. 1h: Output is mute.

Table 18. R15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

1.17 R16 Register (Address = 0x10) [reset = 0x0]

R16 is shown in Table 19.

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Table 19. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x0	Reserved
10:5	RESERVED	R	0x0	Reserved
4:0	RESERVED	R	0x0	Reserved

1.18 R17 Register (Address = 0x11) [reset = 0x0]

R17 is shown in Table 20.

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Table 20. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:11	RESERVED	R	0x0	Reserved
10:8	RESERVED	R	0x0	Reserved
7:6	RESERVED	R	0x0	Reserved
5:0	RESERVED	R	0x0	Reserved

1.19 R18 Register (Address = 0x12) [reset = 0x0]

R18 is shown in Table 21.

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Table 21. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:0	RESERVED	R	0x0	Reserved

1.20 R19 Register (Address = 0x13) [reset = 0x0]

R19 is shown in Table 22.

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Table 22. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13:0	RESERVED	R	0x0	Reserved

1.21 R20 Register (Address = 0x14) [reset = 0x0]

R20 is shown in Table 23.

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Table 23. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.22 R21 Register (Address = 0x15) [reset = 0x0]

R21 is shown in Table 24.

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Table 24. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.23 R22 Register (Address = 0x16) [reset = 0x0]

R22 is shown in Table 25.

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Table 25. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.24 R23 Register (Address = 0x17) [reset = 0x0]

R23 is shown in Table 26.

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Table 26. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.25 R24 Register (Address = 0x18) [reset = 0x718]

R24 is shown in Table 27.

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Table 27. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	IP_PRIREF_BUF_SEL	R/W	0x0	PRIREF input buffer selection. 0h: Enables LVCMOS input. 1h: Enables Differential input.

Table 27. R24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12:8	IP_XO_CLOAD	R/W	0x7	Selects load cap for XO (up to 9pF) in 5 bit binary selection. Each step size ~ 200fF. This capacitance value is the series equivalent of two single-ended load capacitors in parallel with package parasitic capacitance. When this register is set to 0, internal load capacitors are disabled but equivalent pin / package capacitance is 3pF. 0h = 3.0 pF. 1h = 3.2 pF. 2h = 3.4 pF. 3h = 3.6 pF. 4h = 3.8 pF. 5h = 4.0 pF. 6h = 4.2 pF. 7h = 4.4 pF. 8h = 4.6 pF. 9h = 4.8 pF. Ah = 5.0 pF. Bh = 5.2 pF. Ch = 5.4 pF. Dh = 5.6 pF. Eh = 5.8 pF. Fh = 6.0 pF. 10h = 6.2 pF. 11h = 6.4 pF. 12h = 6.5 pF. 13h = 6.7 pF. 14h = 6.9 pF. 15h = 7.1 pF. 16h = 7.3 pF. 17h = 7.5 pF. 18h = 7.7 pF. 19h = 7.9 pF. 1Ah = 8.1 pF. 1Bh = 8.3 pF. 1Ch = 8.5 pF. 1Dh = 8.7 pF. 1Eh = 8.9 pF. 1Fh = 9.0 pF.
7:6	RESERVED	R	0x0	Reserved
5:2	IP_BIAS_SEL_XO	R/W	0x6	Bias Current settings of the XO. Sets the nominal Gm of the XO. 0h = Disabled. 1h = 14 µA. 2h = 29 µA. 3h = 44 µA. 4h = 59 µA. 5h = 148 µA. 6h = 295 µA. 7h = 443 µA. 8h = 591 µA. 9h = 884 µA. Ah = 1177 µA. Bh = 1468 µA. Ch = 1758 µA.
1:0	IP_SECREF_BUF_SEL	R/W	0x0	SECREF input buffer selection. 0h: Enables XTAL input. 1h: Enables LVCMOS input. 2h or 3h: Enables differential input.

1.26 R25 Register (Address = 0x19) [reset = 0x400]

R25 is shown in Table 28.

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Table 28. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	IP_REF_TO_OUT4_EN	R/W	0x0	Reference clock to output channel 4 enable. 0h: Disabled. 1h: Enabled.
13	IP_REF_TO_OUT3_EN	R/W	0x0	Reference clock to output channel 3 enable. 0h: Disabled. 1h: Enabled.
12	IP_REF_TO_OUT2_EN	R/W	0x0	Reference clock to output channel 2 enable. 0h: Disabled. 1h: Enabled.
11	IP_REF_TO_OUT1_EN	R/W	0x0	Reference clock to output channel 1 enable. 0h: Disabled. 1h: Enabled.
10	IP_BYP_OUT0_EN	R/W	0x1	Enables Clock MUX to Y0 buffer. 0h: Disabled Clock MUX to Y0. 1h: Enables Clock MUX to Y0.
9	REF_CH_MUX	R/W	0x0	Selects whether input clock or PFD output is bypassed to all outputs. 0h: Input Clock is bypassed to outputs. 1h: PFD Clock is bypassed to outputs. Not recommended because duty cycle is not 50%.
8	RESERVED	R	0x0	Reserved
7:0	IP_RDIV	R/W	0x0	Reference clock divider. 0h: Doubler ON. 1h: Bypass. 2h-FFh: Divide by register value.

1.27 R26 Register (Address = 0x1A) [reset = 0x0]

R26 is shown in Table 29.

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Table 29. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13:12	RESERVED	R	0x0	Reserved
11:9	RESERVED	R	0x0	Reserved
8:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

1.28 R27 Register (Address = 0x1B) [reset = 0x1]

R27 is shown in Table 30.

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Table 30. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R	0x0	Reserved

Table 30. R27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0x0	Reserved
1:0	MASH_ORDER	R/W	0x1	Programs Sigma Delta modulator order. 0h: Integer mode. 1h: 1st Order Modulator enabled. 2h: 2nd Order Modulator enabled. 3h: 3rd Order Modulator enabled.

1.29 R28 Register (Address = 0x1C) [reset = 0x0]

R28 is shown in Table 31.

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Table 31. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.30 R29 Register (Address = 0x1D) [reset = 0x0]

R29 is shown in Table 32.

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Table 32. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13:12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7:0	RESERVED	R	0x0	Reserved

1.31 R30 Register (Address = 0x1E) [reset = 0x30]

R30 is shown in Table 33.

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Table 33. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:0	PLL_NDIV	R/W	0x30	Sets the value of the N-divider. Minimum value to be set = 24d.

1.32 R31 Register (Address = 0x1F) [reset = 0x0]

R31 is shown in Table 34.

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Table 34. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PLL_NUM_15_0	R/W	0x0	LSBs of 24 bit sigma delta numerator.

1.33 R32 Register (Address = 0x20) [reset = 0x0]

R32 is shown in Table 35.

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Table 35. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x0	Reserved
7:0	PLL_NUM_23_16	R/W	0x0	MSBs of 24 bit sigma delta numerator.

1.34 R33 Register (Address = 0x21) [reset = 0x0]

R33 is shown in Table 36.

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Table 36. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	PLL_DEN_15_0	R/W	0x0	LSBs of 24 bit sigma delta denominator.

1.35 R34 Register (Address = 0x22) [reset = 0x0]

R34 is shown in Table 37.

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Table 37. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x0	Reserved
7:0	PLL_DEN_23_16	R/W	0x0	MSBs of 24 bit sigma delta denominator.

1.36 R35 Register (Address = 0x23) [reset = 0x0]

R35 is shown in Table 38.

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Table 38. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:0	RESERVED	R	0x0	Reserved

1.37 R36 Register (Address = 0x24) [reset = 0x0]

R36 is shown in Table 39.

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Table 39. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x0	Reserved
7:0	RESERVED	R	0x0	Reserved

1.38 R37 Register (Address = 0x25) [reset = 0x0]

R37 is shown in Table 40.

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Table 40. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.39 R38 Register (Address = 0x26) [reset = 0x0]

R38 is shown in Table 41.

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Table 41. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:0	RESERVED	R	0x0	Reserved

1.40 R39 Register (Address = 0x27) [reset = 0x0]

R39 is shown in Table 42.

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Table 42. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	0x0	Reserved
7:0	RESERVED	R	0x0	Reserved

1.41 R40 Register (Address = 0x28) [reset = 0x0]

R40 is shown in Table 43.

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Table 43. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.42 R41 Register (Address = 0x29) [reset = 0x0]

R41 is shown in Table 44.

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Table 44. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SSC_EN	R/W	0x0	Enables SSC operation. 0h: Disables SSC. 1h: Enables SSC.
14:0	RESERVED	R	0x0	Reserved

1.43 R42 Register (Address = 0x2A) [reset = 0x2]

R42 is shown in Table 45.

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Table 45. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R	0x0	Reserved
5	SSC_TYPE	R/W	0x0	Selects the SSC spread Profile. 0h: Down-spread. 1h: center-spread.
4	RESERVED	R	0x0	Reserved
3:1	SSC_SEL	R/W	0x1	Selects SSC profile. 0h: 25MHz PFD, 0.25% spread. 1h: 25MHz PFD, 0.5% spread. 2h: 50MHz PFD, 0.25% spread. 3h: 50MHz PFD, 0.5% spread. Others: Do not use.
0	RESERVED	R	0x0	Reserved

1.44 R43 Register (Address = 0x2B) [reset = 0x51]

R43 is shown in Table 46.

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Table 46. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FREQ_INC_DEC_DELTA	R/W	0x51	Sets frequency step size of DCO mode.

1.45 R44 Register (Address = 0x2C) [reset = 0x0]

R44 is shown in Table 47.

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Table 47. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11:0	RESERVED	R	0x0	Reserved

1.46 R45 Register (Address = 0x2D) [reset = 0x0]

R45 is shown in Table 48.

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Table 48. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.47 R46 Register (Address = 0x2E) [reset = 0x0]

R46 is shown in Table 49.

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Table 49. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.48 R47 Register (Address = 0x2F) [reset = 0xA00]

R47 is shown in Table 50.

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Table 50. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved

Table 50. R47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12:7	PLL_CP_DN	R/W	0x14	Programming bits for DOWN current of CP. Up current and down current must be the same. 00h: 0 µA. 01h: 100 µA. 02h: 200 µA. 03h: 300 µA. 04h: 400 µA. 05h: 500 µA. 06h: 600 µA. 07h: 700 µA. 08h: 800 µA. 09h: 900 µA. 0Ah: 1000 µA. 0Bh: 1100 µA. 0Ch: 1200 µA. 0Dh: 1300 µA. 0Eh: 1400 µA. 0Fh: 1500 µA. 10h: 1600 µA. 11h: 1700 µA. 12h: 1800 µA. 13h: 1900 µA. 14h: 2000 µA. 15h: 2100 µA. 16h: 2200 µA. 17h: 2300 µA. 18h: 2400 µA. 19h: 2500 µA. 1Ah: 2600 µA. 1Bh: 2700 µA. 1Ch: 2800 µA. 1Dh: 2900 µA. 1Eh: 3000 µA. 1Fh: 3100 µA. 20h: 800 µA. 21h: 900 µA. 22h: 1000 µA. 23h: 1100 µA. 24h: 1200 µA. 25h: 1300 µA. 26h: 1400 µA. 27h: 1500 µA. 28h: 1600 µA. 29h: 1700 µA. 2Ah: 1800 µA. 2Bh: 1900 µA. 2Ch: 2000 µA. 2Dh: 2100 µA. 2Eh: 2200 µA. 2Fh: 2300 µA. 30h: 2400 µA. 31h: 2500 µA. 32h: 2600 µA. 33h: 2700 µA. 34h: 2800 µA. 35h: 2900 µA. 36h: 3000 µA. 37h: 3100 µA. 38h: 3200 µA. 39h: 3300 µA. 3Ah: 3400 µA. 3Bh: 3500 µA. 3Ch: 3600 µA. 3Dh: 3700 µA. 3Eh: 3800 µA. 3Fh: 3900 µA.

Table 50. R47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:5	PLL_PSB	R/W	0x0	Programming bits for PSB division value. 0h: Div by 4. 1h: Div by 5. 2h or 3h: Div by 6.
4:3	PLL_PSA	R/W	0x0	Programming bits for PSA division value. 0h: Div by 4. 1h: Div by 5. 2h or 3h: Div by 6.
2	RESERVED	R	0x0	Reserved
1:0	RESERVED	R	0x0	Reserved

1.49 R48 Register (Address = 0x30) [reset = 0x1A14]

R48 is shown in Table 51.

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Table 51. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:11	PLL_LF_RES	R/W	0x3	PLL loop filter resistor. 0h: 0 kΩ. 1h: 0.5 kΩ. 2h: 1 kΩ. 3h: 1.5 kΩ. 4h: 2 kΩ. 5h: 2.5 kΩ. 6h: 3 kΩ. 7h: 3.5 kΩ. 8h: 4 kΩ. 9h: 4.5 kΩ. 10h: 5.5 kΩ. 11h: 6.5 kΩ. 12h: 7.5 kΩ. 13h: Reserved. 14h: Reserved. 15h: Reserved.
10:6	PLL_LF_PCAP	R/W	0x8	PLL loop filter pole capacitor. Capacitance value (pF) = 0.87 * register value + 5.67

Table 51. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL_CP_UP	R/W	0x14	Programming bits for UP current of CP. Up current and down current must be the same. 00h: 0 µA. 01h: 100 µA. 02h: 200 µA. 03h: 300 µA. 04h: 400 µA. 05h: 500 µA. 06h: 600 µA. 07h: 700 µA. 08h: 800 µA. 09h: 900 µA. 0Ah: 1000 µA. 0Bh: 1100 µA. 0Ch: 1200 µA. 0Dh: 1300 µA. 0Eh: 1400 µA. 0Fh: 1500 µA. 10h: 1600 µA. 11h: 1700 µA. 12h: 1800 µA. 13h: 1900 µA. 14h: 2000 µA. 15h: 2100 µA. 16h: 2200 µA. 17h: 2300 µA. 18h: 2400 µA. 19h: 2500 µA. 1Ah: 2600 µA. 1Bh: 2700 µA. 1Ch: 2800 µA. 1Dh: 2900 µA. 1Eh: 3000 µA. 1Fh: 3100 µA. 20h: 800 µA. 21h: 900 µA. 22h: 1000 µA. 23h: 1100 µA. 24h: 1200 µA. 25h: 1300 µA. 26h: 1400 µA. 27h: 1500 µA. 28h: 1600 µA. 29h: 1700 µA. 2Ah: 1800 µA. 2Bh: 1900 µA. 2Ch: 2000 µA. 2Dh: 2100 µA. 2Eh: 2200 µA. 2Fh: 2300 µA. 30h: 2400 µA. 31h: 2500 µA. 32h: 2600 µA. 33h: 2700 µA. 34h: 2800 µA. 35h: 2900 µA. 36h: 3000 µA. 37h: 3100 µA. 38h: 3200 µA. 39h: 3300 µA. 3Ah: 3400 µA. 3Bh: 3500 µA. 3Ch: 3600 µA. 3Dh: 3700 µA. 3Eh: 3800 µA. 3Fh: 3900 µA.

1.50 R49 Register (Address = 0x31) [reset = 0x13]

R49 is shown in Table 52.

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Table 52. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13:11	RESERVED	R	0x0	Reserved
10:8	RESERVED	R	0x0	Reserved
7:5	RESERVED	R	0x0	Reserved
4:0	PLL_LF_ZCAP	R/W	0x13	PLL loop filter zero capacitor. Capacitance value (pF) = 27.7 * register value + 82.4

1.51 R50 Register (Address = 0x32) [reset = 0x100]

R50 is shown in Table 53.

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Table 53. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:11	RESERVED	R	0x0	Reserved
10:8	PLL_LOCKDET_WINDOW	R/W	0x1	Programmability of PFD input and output time window for lock detect. 0h: Do not Use. 1h: 1.36ns. 2h: 2.61ns. 3h: 3.94ns. 4h: 5.18ns. 5h: 6.41ns. 6h: 7.59ns. 7h: 8.9ns.
7:6	RESERVED	R	0x0	Reserved
5:3	RESERVED	R	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

1.52 R51 Register (Address = 0x33) [reset = 0x40]

R51 is shown in Table 54.

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Table 54. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	PLL_PFD_DLY_EN	R/W	0x0	Enable feedback delay generation module. Used in Dual PFD Mode. 0h: Feedback Clock Generation Disabled. 1h: Feedback Clock Generation Enabled.
9:7	RESERVED	R	0x0	Reserved
6	PLL_PFD_CTRL	R/W	0x1	Sets the PFD type. 0h: Dual PFD. 1h: Single PFD.
5:0	RESERVED	R	0x0	Reserved

1.53 R52 Register (Address = 0x34) [reset = 0x0]

R52 is shown in Table 55.

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Table 55. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:11	RESERVED	R	0x0	Reserved
10:8	RESERVED	R	0x0	Reserved
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R	0x0	Reserved
1:0	RESERVED	R	0x0	Reserved

1.54 R53 Register (Address = 0x35) [reset = 0x48]

R53 is shown in Table 56.

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Table 56. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6	PLL_NCTRL_EN	R/W	0x1	Enables Feedback Divider. 0h: Disable. 1h: Enable.
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	PLL_CP_EN	R/W	0x1	Enables Charge Pump. 0h: Disable. 1h: Enable.
2:0	RESERVED	R	0x0	Reserved

1.55 R54 Register (Address = 0x36) [reset = 0x0]

R54 is shown in Table 57.

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Table 57. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:8	RESERVED	R	0x0	Reserved
7:0	RESERVED	R	0x0	Reserved

1.56 R55 Register (Address = 0x37) [reset = 0x0]

R55 is shown in Table 58.

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Table 58. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	0x0	Reserved
9:8	PLL_LF_3_PCTRIM	R/W	0x0	PLL loop filter 3rd order pole capacitor. 0h: 1.2 pF. 1h: 2.9 pF. 2h: 4.6 pF. 3h: 8.1 pF.
7:6	PLL_LF_3_PRTRIM	R/W	0x0	PLL loop filter 3rd order pole resistor. 0h: 0 kΩ. 1h: 2 kΩ. 2h: 4 kΩ. 3h: 8 kΩ.
5:0	RESERVED	R	0x0	Reserved

1.57 R56 Register (Address = 0x38) [reset = 0x6]

R56 is shown in Table 59.

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Table 59. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CH1_MUX	R/W	0x0	Input Clock selection MUX for Integer Divider of Channel OUT1. 0h: PSA. 1h: PSB. 2h: Reserved. 3h: Input Clock.
13:0	CH1_DIV	R/W	0x6	Sets Integer Divider Division Value of Channel OUT1. 0h: Powers Down Integer Divider. Output=Input/Register Value for Other settings.

1.58 R57 Register (Address = 0x39) [reset = 0x4000]

R57 is shown in Table 60.

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Table 60. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	CH1_LPHCSL_EN	R/W	0x1	Enables LP-HCSL output buffer for Channel OUT1. 0h: Disable. 1h: Enable.
13	RESERVED	R	0x0	Reserved
12	CH1_1P8VDET	R/W	0x0	To specify Power Supply on Channel OUT1. 0h: 2.5-V/3.3-V supply. 1h: 1.8-V supply.
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	CH1_GLITCHLESS_EN	R/W	0x0	Enables Glitchless switching for Output Channel OUT1. 0h: Disable. 1h: Enable.
8:4	CH1_SYNC_DELAY	R/W	0x0	Sets additional Clock Delay when synchronization is enabled. Step size is one cycle of VCO frequency divided by prescaler. 0h: No Delay. 1h-1Fh: Register Value number of prescalar cycles.
3	CH1_SYNC_EN	R/W	0x0	Enables Synchronization for Channel OUT1. 0h: Synchronization Disabled. 1h: Synchronization Enabled.

Table 60. R57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0x0	Reserved
1	CH1_MUTE_SEL	R/W	0x0	Mute selection for Output Channel OUT1. 0h: Mute to Low. 1h: Mute to High.
0	CH1_MUTE	R/W	0x0	Mutes output clock of Channel OUT1. 0h: Un-mute. 1h: Mute.

1.59 R58 Register (Address = 0x3A) [reset = 0x0]

R58 is shown in Table 61.

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Table 61. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:12	RESERVED	R	0x0	Reserved
11:10	RESERVED	R	0x0	Reserved
9:8	RESERVED	R	0x0	Reserved
7:5	RESERVED	R	0x0	Reserved
4:0	RESERVED	R	0x0	Reserved

1.60 R59 Register (Address = 0x3B) [reset = 0x0]

R59 is shown in Table 62.

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Table 62. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CH1_LVDS_EN	R/W	0x0	Enables LVDS output on OUT1. 0h: Disable. 1h: Enable.
14	CH1_CMOSN_EN	R/W	0x0	Enables CMOS output on OUT1N. 0h: Disable. 1h: Enable.
13	CH1_CMOSP_EN	R/W	0x0	Enables CMOS output on OUT1P. 0h: Disable. 1h: Enable.
12	CH1_CMOSN_POL	R/W	0x0	Sets CMOS polarity of output OUT1N. 0h: Low Polarity. 1h: High Polarity.
11	CH1_CMOSP_POL	R/W	0x0	Sets CMOS polarity of output OUT1P. 0h: Low Polarity. 1h: High Polarity.
10	RESERVED	R	0x0	Reserved
9:7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	RESERVED	R	0x0	Reserved

1.61 R60 Register (Address = 0x3C) [reset = 0x8]

R60 is shown in Table 63.

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Table 63. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	CH1_DIFFBUF_IBIAS_TRIM	R/W	0x0	Channel 1 differential buffer current bias trim. This register sets the swing of LVDS output. Always set it to 0x6 for standard LVDS swing (single-ended). This is valid for all supply voltages. 6h: Standard LVDS swing. Others: Do not use.
11:10	CH1_LVDS_CMTRIM_INC	R/W	0x0	Channel 1 LVDS common-mode trim increment. This registers increments the common-mode of LVDS output.
9	RESERVED	R	0x0	Reserved
8:6	RESERVED	R	0x0	Reserved
5:4	CH1_LVDS_CMTRIM_DEC	R/W	0x0	Channel 1 LVDS common-mode trim decrement. This registers decrements the common-mode of LVDS output.
3:0	CH1_CMOS_SLEW_RATE_CTRL	R/W	0x8	Sets Slew rate CMOS output buffer on OUT1. 00h: Slow Mode. 10h: Normal Mode. Other combinations: Do not use

1.62 R61 Register (Address = 0x3D) [reset = 0x0]

R61 is shown in Table 64.

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Table 64. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

1.63 R62 Register (Address = 0x3E) [reset = 0x6]

R62 is shown in Table 65.

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Table 65. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CH2_MUX	R/W	0x0	Input Clock selection MUX for Integer Divider of Channel OUT2. 0h: PSA. 1h: PSB. 2h: Reserved. 3h: Input Clock.
13:0	CH2_DIV	R/W	0x6	Sets Integer Divider Division Value of Channel OUT2. 0h: Powers Down Integer Divider. Output=Input/Register Value for Other settings.

1.64 R63 Register (Address = 0x3F) [reset = 0x2000]

R63 is shown in Table 66.

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Table 66. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13	CH2_LPHCSL_EN	R/W	0x1	Enables LP-HCSL output buffer for Channel OUT2. 0h: Disable. 1h: Enable.
12	CH2_1P8VDET	R/W	0x0	To specify Power Supply on Channel OUT2. 0h: 2.5-V/3.3-V supply. 1h: 1.8-V supply.
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	CH2_GLITCHLESS_EN	R/W	0x0	Enables Glitchless switching for Output Channel OUT2. 0h: Disable. 1h: Enable.
8:4	CH2_SYNC_DELAY	R/W	0x0	Sets additional Clock Delay when synchronization is enabled. Step size is one cycle of VCO frequency divided by prescaler. 0h: No Delay. 1h-1Fh: Register Value number of prescalar cycles.
3	CH2_SYNC_EN	R/W	0x0	Enables Synchronization for Channel OUT2. 0h: Synchronization Disabled. 1h: Synchronization Enabled.
2	RESERVED	R	0x0	Reserved
1	CH2_MUTE_SEL	R/W	0x0	Mute selection for Output Channel OUT2. 0h: Mute to Low. 1h: Mute to High.
0	CH2_MUTE	R/W	0x0	Mutes output clock of Channel OUT2. 0h: Un-mute. 1h: Mute.

1.65 R64 Register (Address = 0x40) [reset = 0x0]

R64 is shown in Table 67.

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Table 67. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

1.66 R65 Register (Address = 0x41) [reset = 0x0]

R65 is shown in Table 68.

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Table 68. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:13	CH2_LVDS_CMTRIM_DEC	R/W	0x0	Channel 2 LVDS common-mode trim decrement. This registers decrements the common-mode of LVDS output.
12	RESERVED	R	0x0	Reserved

Table 68. R65 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CH2_LVDS_EN	R/W	0x0	Enables LVDS output on OUT2. 0h: Disable. 1h: Enable.
10	RESERVED	R	0x0	Reserved
9:7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	RESERVED	R	0x0	Reserved

1.67 R66 Register (Address = 0x42) [reset = 0x0]

R66 is shown in Table 69.

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Table 69. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11:9	RESERVED	R	0x0	Reserved
8:6	RESERVED	R	0x0	Reserved
5:4	CH2_LVDS_CMTRIM_INC	R/W	0x0	Channel 2 LVDS common-mode trim increment. This registers increments the common-mode of LVDS output.
3:0	CH2_DIFFBUF_IBIAS_TRIM	R/W	0x0	Channel 2 differential buffer current bias trim. This register sets the swing of LVDS output. Always set it to 0x6 for standard LVDS swing (single-ended). This is valid for all supply voltages. 6h: Standard LVDS swing. Others: Do not use.

1.68 R67 Register (Address = 0x43) [reset = 0x6]

R67 is shown in Table 70.

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Table 70. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CH3_MUX	R/W	0x0	Input Clock selection MUX for Integer Divider of Channel OUT3. 0h: PSA. 1h: PSB. 2h: Reserved. 3h: Input Clock.
13:0	CH3_DIV	R/W	0x6	Sets Integer Divider Division Value of Channel OUT3. 0h: Powers Down Integer Divider. 1h: Output=Input/Register Value for Other settings.

1.69 R68 Register (Address = 0x44) [reset = 0x2000]

R68 is shown in Table 71.

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Table 71. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved

Table 71. R68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	CH3_LPHCSL_EN	R/W	0x1	Enables LP-HCSL output buffer for Channel OUT3. 0h: Disable. 1h: Enable.
12	CH3_1P8VDET	R/W	0x0	To specify Power Supply on Channel OUT3. 0h: 2.5-V/3.3-V supply. 1h: 1.8-V supply.
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	CH3_GLITCHLESS_EN	R/W	0x0	Enables Glitchless switching for Output Channel OUT3. 0h: Disable. 1h: Enable.
8:4	CH3_SYNC_DELAY	R/W	0x0	Sets additional Clock Delay when synchronization is enabled. Step size is one cycle of VCO frequency divided by prescaler. 0h: No Delay. 1h-1Fh: Register Value number of prescalar cycles.
3	CH3_SYNC_EN	R/W	0x0	Enables Synchronization for Channel OUT3. 0h: Synchronization Disabled. 1h: Synchronization Enabled.
2	RESERVED	R	0x0	Reserved
1	CH3_MUTE_SEL	R/W	0x0	Mute selection for Output Channel OUT3. 0h: Mute to Low. 1h: Mute to High.
0	CH3_MUTE	R/W	0x0	Mutes output clock of Channel OUT3. 0h: Un-mute. 1h: Mute.

1.70 R69 Register (Address = 0x45) [reset = 0x0]

R69 is shown in Table 72.

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Table 72. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

1.71 R70 Register (Address = 0x46) [reset = 0x0]

R70 is shown in Table 73.

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Table 73. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:12	RESERVED	R	0x0	Reserved
11	CH3_LVDS_EN	R/W	0x0	Enables LVDS output on OUT3. 0h: Disable. 1h: Enable.
10	RESERVED	R	0x0	Reserved

Table 73. R70 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	RESERVED	R	0x0	Reserved

1.72 R71 Register (Address = 0x47) [reset = 0x0]

R71 is shown in Table 74.

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Table 74. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10:9	CH3_LVDS_CMTRIM_DEC	R/W	0x0	Channel 3 LVDS common-mode trim decrement. This registers decrements the common-mode of LVDS output.
8:6	RESERVED	R	0x0	Reserved
5:4	CH3_LVDS_CMTRIM_INC	R/W	0x0	Channel 3 LVDS common-mode trim increment. This registers increments the common-mode of LVDS output.
3:0	CH3_DIFFBUF_IBIAS_TRIM	R/W	0x0	Channel 3 differential buffer current bias trim. This register sets the swing of LVDS output. Always set it to 0x6 for standard LVDS swing (single-ended). This is valid for all supply voltages. 6h: Standard LVDS swing. Others: Do not use.

1.73 R72 Register (Address = 0x48) [reset = 0x6]

R72 is shown in Table 75.

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Table 75. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	CH4_MUX	R/W	0x0	Input Clock selection MUX for Integer Divider of Channel OUT4. 0h: PSA. 1h: PSB. 2h: Reserved. 3h: Input Clock.
13:0	CH4_DIV	R/W	0x6	Sets Integer Divider Division Value of Channel OUT4. 0h: Powers Down Integer Divider. Output=Input/Register Value for Other settings.

1.74 R73 Register (Address = 0x49) [reset = 0x2000]

R73 is shown in Table 76.

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Table 76. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R	0x0	Reserved
13	CH4_LPHCSL_EN	R/W	0x1	Enables LP-HCSL output buffer for Channel OUT4. 0h: Disable. 1h: Enable.

Table 76. R73 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CH4_1P8VDET	R/W	0x0	To specify Power Supply on Channel OUT4. 0h: 2.5-V/3.3-V supply. 1h: 1.8-V supply.
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	CH4_GLITCHLESS_EN	R/W	0x0	Enables Glitchless switching for Output Channel OUT4. 0h: Disable. 1h: Enable.
8:4	CH4_SYNC_DELAY	R/W	0x0	Sets additional Clock Delay when synchronization is enabled. Step size is one cycle of VCO frequency divided by prescaler. 0h: No Delay. 1h-1Fh: Register Value number of prescalar cycles.
3	CH4_SYNC_EN	R/W	0x0	Enables Synchronization for Channel OUT4. 0h: Synchronization Disabled. 1h: Synchronization Enabled.
2	RESERVED	R	0x0	Reserved
1	CH4_MUTE_SEL	R/W	0x0	Mute selection for Output Channel OUT4. 0h: Mute to Low. 1h: Mute to High.
0	CH4_MUTE	R/W	0x0	Mutes output clock of Channel OUT4. 0h: Un-mute. 1h: Mute.

1.75 R74 Register (Address = 0x4A) [reset = 0x0]

R74 is shown in Table 77.

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Table 77. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

1.76 R75 Register (Address = 0x4B) [reset = 0x0]

R75 is shown in Table 78.

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Table 78. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CH4_LVDS_EN	R/W	0x0	Enables LVDS output on OUT4. 0h: Disable. 1h: Enable.
14	CH4_CMOSP_EN	R/W	0x0	Enables CMOS output on OUT4P. 0h: Disable. 1h: Enable.
13	CH4_CMOSN_EN	R/W	0x0	Enables CMOS output on OUT4N. 0h: Disable. 1h: Enable.

Table 78. R75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	CH4_CMOSP_POL	R/W	0x0	Sets CMOS polarity of output OUT4P. 0h: Low Polarity. 1h: High Polarity.
11	CH4_CMOSN_POL	R/W	0x0	Sets CMOS polarity of output OUT4N. 0h: Low Polarity. 1h: High Polarity.
10	RESERVED	R	0x0	Reserved
9:7	RESERVED	R	0x0	Reserved
6:4	RESERVED	R	0x0	Reserved
3:0	RESERVED	R	0x0	Reserved

1.77 R76 Register (Address = 0x4C) [reset = 0x8]

R76 is shown in Table 79.

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Table 79. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:10	RESERVED	R	0x0	Reserved
9:6	CH4_DIFFBUF_IBIAS_TRIM	R/W	0x0	Channel 4 differential buffer current bias trim. This register sets the swing of LVDS output. Always set it to 0x6 for standard LVDS swing (single-ended). This is valid for all supply voltages. 6h: Standard LVDS swing. Others: Do not use.
5:4	CH4_LVDS_CMTRIM_INC	R/W	0x0	Channel 4 LVDS common-mode trim increment. This registers increments the common-mode of LVDS output.
3:0	CH4_CMOS_SLEW_RATE_CTRL	R/W	0x8	Sets Slew rate CMOS output buffer on OUT4. 00h: Slow Mode. 10h: Normal Mode. Other combinations: Do not use

1.78 R77 Register (Address = 0x4D) [reset = 0x0]

R77 is shown in Table 80.

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Table 80. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0x0	Reserved
10:6	RESERVED	R	0x0	Reserved
5:3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1:0	CH4_LVDS_CMTRIM_DEC	R/W	0x0	Channel 4 LVDS common-mode trim decrement. This registers decrements the common-mode of LVDS output.

1.79 R78 Register (Address = 0x4E) [reset = 0x1000]

R78 is shown in Table 81.

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Table 81. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12	CH0_EN	R/W	0x1	Enables CMOS output on OUT0. 0h: Disable. 1h: Enable.
11:0	RESERVED	R	0x0	Reserved

1.80 R79 Register (Address = 0x4F) [reset = 0x8]

R79 is shown in Table 82.

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Table 82. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0x0	Reserved
12:10	RESERVED	R	0x0	Reserved
9	SAFETY_1P8V_MODE	R/W	0x0	Safety switch when using 1.8-V supply. Set 1h when any channel is expected to be 1.8-V mode
8:6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:0	CH0_CMOS_SLEW_RATE_CTRL	R/W	0x8	Sets Slew rate CMOS output buffer on OUT0. 00h: Slow Mode. 10h: Normal Mode. Other combinations: Do not use

1.81 R80 Register (Address = 0x50) [reset = 0x0]

R80 is shown in Table 83.

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Table 83. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9:8	RESERVED	R	0x0	Reserved
7:4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

1.82 R81 Register (Address = 0x51) [reset = 0x0]

R81 is shown in Table 84.

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Table 84. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14:12	RESERVED	R	0x0	Reserved
11:5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	PLL_LOCK_MASK	R/W	0x0	Masks Analog Lock Delect. 0h: Digital Lock Detect AND Analog Lock Detect. 1h: Analog Lock Detect only. Set to 1 in SSC mode, because digital lock detect does not work in SSC mode.
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

1.83 R82 Register (Address = 0x52) [reset = 0x0]

R82 is shown in Table 85.

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Table 85. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0x0	Reserved
11:6	RESERVED	R	0x0	Reserved
5:3	RESERVED	R	0x0	Reserved
2:0	RESERVED	R	0x0	Reserved

1.84 R83 Register (Address = 0x53) [reset = 0x0]

R83 is shown in Table 86.

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Table 86. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.85 R84 Register (Address = 0x54) [reset = 0x0]

R84 is shown in Table 87.

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Table 87. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

1.86 R85 Register (Address = 0x55) [reset = 0x0]

R85 is shown in Table 88.

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Table 88. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	RESERVED	R	0x0	Reserved

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (July 2019) to B Revision	Page
• Updated register names	4

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