User’s Guide
LMK6x6EVM Evaluation Instructions

ABSTRACT
This user's guide applies to both LMK6E6EVM-1 and LMK6F6EVM-1 EVM modules.
The LMK6x is a lower-power clock oscillator using TI's BAW technology.

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1 Introduction

1.1 Evaluation Module Contents

The box contains:

- One LMK6E6EVM-1 board (HSDC103A), or
- One LMK6F6EVM-1 board (HSDC104A)

1.2 Evaluation Setup Requirement

The evaluation requires the following hardware:

- A DC power supply
- An oscilloscope
- A signal analyzer (optional)

1.3 Resources

See the LMK6x High-Performance BAW Oscillator data sheet for more information about the LMK6x devices.
2 Setup

2.1 Connection Diagram

Figure 2-1 shows the LMK6E6EVM (HSDC103A) connection diagram. The same connection diagram applies to LMK6F6EVM (HSDC104A).

2.2 Power Supply

Apply 4 V to the VDDin SMA connector. The maximum current consumption must not exceed 60 mA.

2.3 Clock Output

Connect P1 SMA connector to an oscilloscope. Output frequency is 24 MHz and the amplitude is about 3.3 V.

2.4 EVM Strap Options

2.4.1 J1 Header

Pin 2 of J1 is connected to the OE pin of the LMK6x device. Put the short across pin 1 and pin 2 of J1 to pull the OE pin to VDD through a resistor and enable the LMK6x device.

2.4.2 J3 Header

To use the onboard voltage regulator for the LMK6x device, put the short across pin 2 and pin 3 of J3 header. Otherwise, put the short across pin 1 and pin 2 of J3 header to use external power supply.

2.4.3 J4 Header

J4 is used to select the output voltage of the onboard voltage regulator.
3 Typical Measurement

3.1 Phase Noise

Figure 3-1 shows the phase noise for the LMK6E6EVM (HSDC103A). Similar phase noise can be obtained from LMK6F6EVM (HSDC104A).
4 Schematic

![Schematic Diagram](image)

Figure 4-1. Schematic

5 PCB Layout and Layer Stack-Up

5.1 PCB Layer Stack-Up

![Layer Stack-Up Diagram](image)

Figure 5-1. PCB Layer Stack-Up
5.2 PCB Layout

Figure 5-2. Top Layer

Figure 5-3. GND Layer

Figure 5-4. GND Layer

Figure 5-5. Bottom Layer
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