EVM User's Guide: LMK3H0102EVM

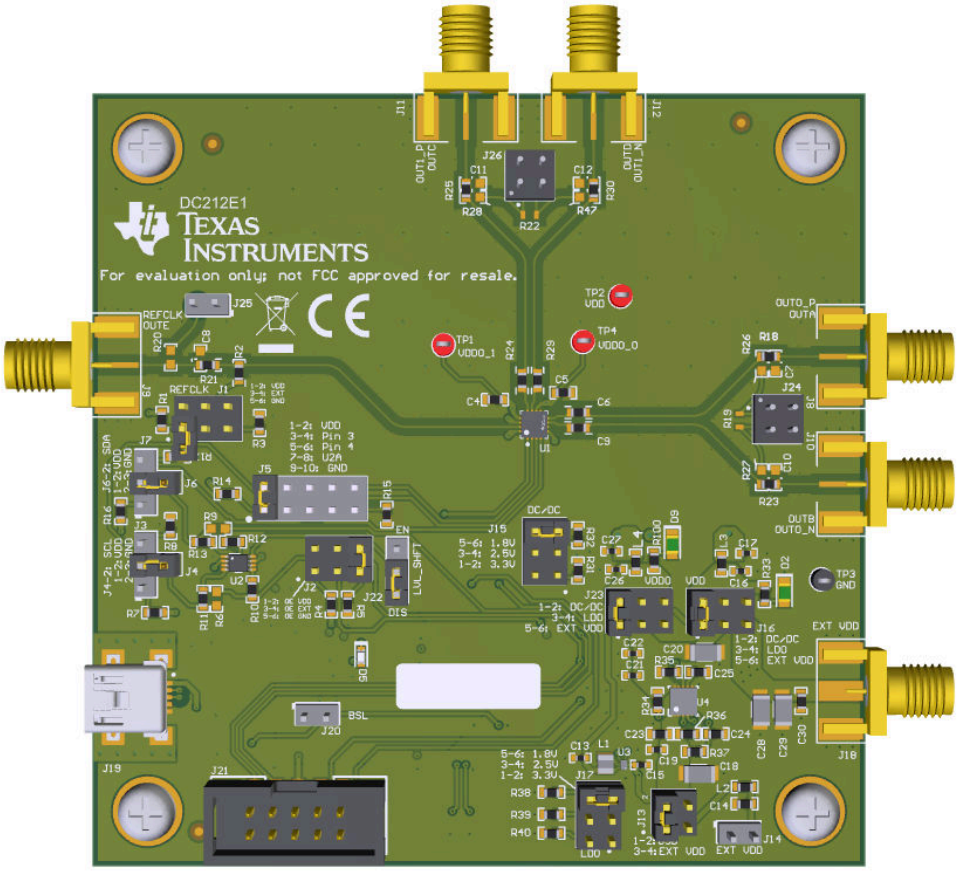
LMK3H0102 Evaluation Module

Description

The LMK3H0102EVM evaluation module provides a complete clocking platform to evaluate the clock performance, pin configuration, software configuration, and features of the Texas Instruments LMK3H0102 Clock Generator with integrated BAW-based oscillator. The LMK3H0102 is a dual-output clock generator with an internal BAW resonator and fractional output dividers, eliminating the need for an external reference clock. The EVM includes SMA connectors for all clock outputs for interfacing with 50-Ω test equipment. The EVM can be configured through the onboard USB microcontroller (MCU) interface using a PC with TI's TICS Pro software graphical user interface (GUI). TICS Pro can be used to program the LMK3H0102 registers.

Features

- Industry-first BAW-based reference-less clock generator
- Can be powered via USB only, option for external power supply
- Software support via TICS Pro for configuration generation



LMK3H0102EVM

1 Evaluation Module Overview

1.1 Introduction

The LMK3H0102EVM can be used as a flexible, multiple output clock source for compliance testing, performance evaluation, and initial system prototyping. By default, each EVM is populated with an LMK3H0102V33 device. The onboard SMA ports provide access to the LMK3H0102 clock outputs for interfacing to test equipment and other reference boards using commercially available coaxial cables, adapters, and baluns (not included). This connectivity enables integrated system level testing between TI's LMK3H0102 and third-party FPGA/ASIC/SoC reference boards. TICS Pro, a software graphical user interface (GUI), can be installed on a host PC to access the LMK3H0102 device registers via the on-board USB-to-I2C interface. TICS Pro can be used to import and export register data for in-system programming of custom device configurations.

1.2 Kit Contents

The box contains:

- One LMK3H0102EVM board (DC212)

2 Hardware

2.1 Evaluation Setup Requirement

The evaluation requires the following hardware:

- A USB B to mini USB cable
- A PC
- An oscilloscope
- A signal analyzer (optional)

2.2 Configuring the EVM

The LMK3H0102 is a highly-configurable clock generator with separate power and output clock domains. To support a wide range of evaluation use cases, the EVM was designed for maximum flexibility and has more functionality and peripheral circuitry than needed to implement frequency plans in typical customer system applications.

This section describes the jumpers and connectors on the EVM, as well as how to connect, set-up, and use of the LMK3H0102EVM. When operating the LMK3H0102EVM, Figure 2-1 shows the connection of the SMA ports to the power supply and clock outputs. These SMA ports are labeled in the top silkscreen layer.

Note

Pin 1 of the jumpers is not always in the top left. For example, J15 and J17 have Pin 1 in the bottom right. Similarly, Pin 1 of J13 is in the bottom left, with Pin 2 in the top left.

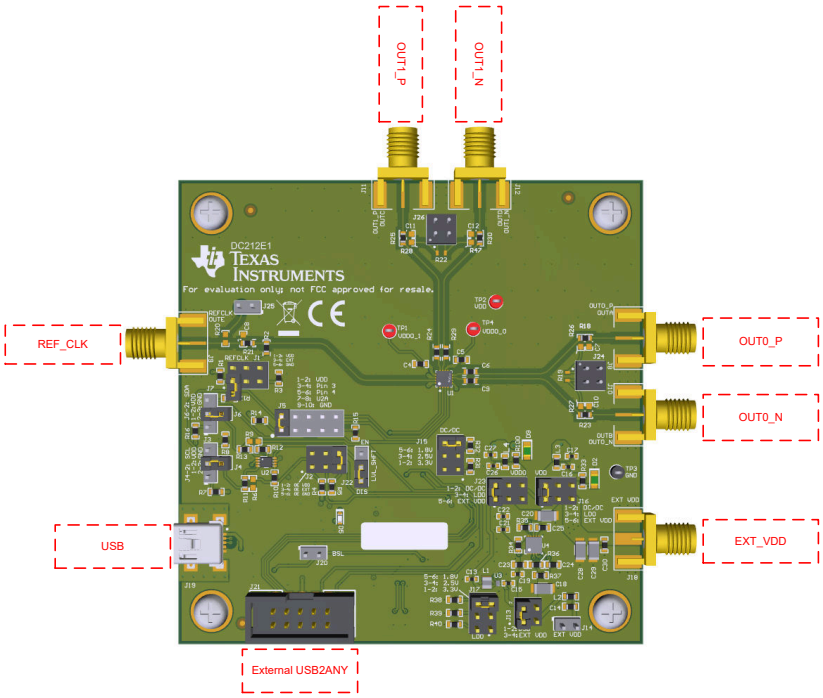


Figure 2-1. LMK3H0102 Connections

2.2.1 Configuring the Power Supply

The LMK3H102 has one VDD (analog/digital core) supply pin that operates from 1.8 V to 3.3 V (± 5%) and two VDDO (output) supply pins that operate from 1.8 V to 3.3 V (± 5%). The VDD and VDDO power planes on the EVM can be powered from a single supply or dual supplies. Each plane can be powered directly from an external supply, an on-board DC/DC converter, or an on-board LDO. Though the LMK3H0102 already has integrated LDO regulators for excellent Power Supply Ripple Rejection (PSRR), the EVM's on-board regulators (U3 & U4) allows the user to power the EVM using a higher supply voltage, such as 5 V, and enable jumper selection of the VDDO voltage. TheLMK3H0102EVM can be powered from USB without the need for an external supply, as the 5 V supply to the on-board regulators can be powered by the USB port. Figure 2-2 shows how the external supply or the on-board regulators can be independently routed to the VDD and VDDO planes by configuring the power terminals and jumpers.

Power SMA port J18 is the main power terminal block for the EVM for connecting power from an external power supply and GND. J14 provides an alternative connector style for applying external power to the LMK3H0102EVM.

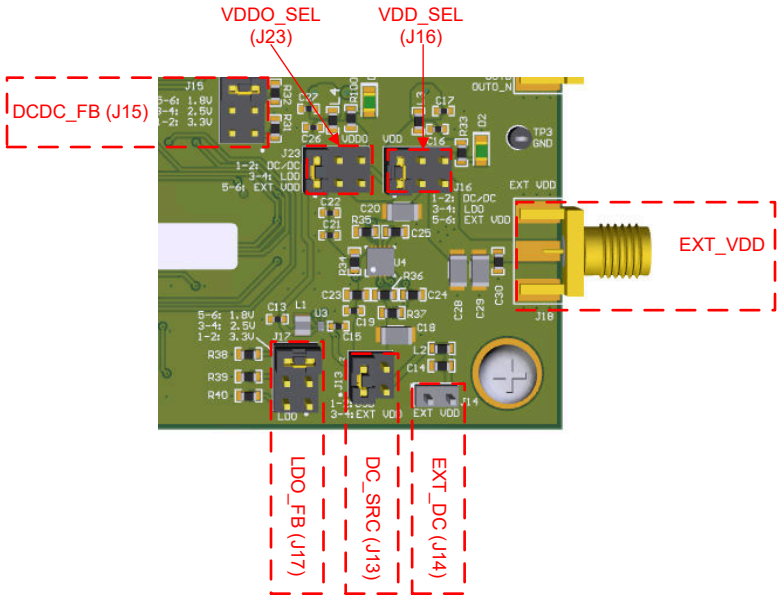


Figure 2-2. LMK3H0102EVM Power Jumpers

Table 2-1 summarizes the EVM power configurations to connect and route power to the VDD and VDDO supply domains of the LMK3H0102. Refer to Schematics for more details.

Table 2-1. Power Configurations

Connection	Name	On-Board Regulators
LMK3H0102 VDD Pins	VDD	3.3 V (Default)
LMK3H0102 VDDO Pins	VDDO_x	3.3 V (Default)
J13	DC_SRC	• Tie pins 1 and 2 (Default): Selects 5 V from USB as source for on-board regulators • Tie pins 3 and 4: Selects EXT_DC as source for on-board regulators
J14	EXT_DC	• Open (Default) • Pin 1: Connect to 5 V supply • Pin 2: Connect to GND supply
J15	DCDC_FB	• Tie pins 1 and 2: Set DC/DC output to 3.3 V • Tie pins 3 and 4: Set DC/DC output to 2.5 V • Tie pins 5 and 6 (Default): Set DC/DC output to 1.8 V
J16	VDD_SEL	• Tie pins 1 and 2 (Default): Set VDD to the DC/DC output • Tie pins 3 and 4: Set VDD to the LDO output • Tie pins 5 and 6: Set VDD to the J18 voltage
J17	LDO_FB	• Tie pins 1 and 2: Set LDO output to 3.3 V • Tie pins 3 and 4: Set LDO output to 2.5 V • Tie pins 5 and 6: Set LDO output to 1.8 V
J18	EXT_VDD	Alternative SMA connection to pin 5 of J16 and J23
J23	VDDO_SEL	• Tie pins 1 and 2 (Default): Set VDDO to the DC/DC output • Tie pins 3 and 4: Set VDDO to the LDO output • Tie pins 5 and 6: Set VDDO to the J18 voltage

2.2.2 Configuring the Control Pins

The LMK3H0102 has multiple external control pins to configure the operating mode and initial settings on POR. Figure 2-3 shows how the LMK3H0102 control pins can be configured through the jumpers.

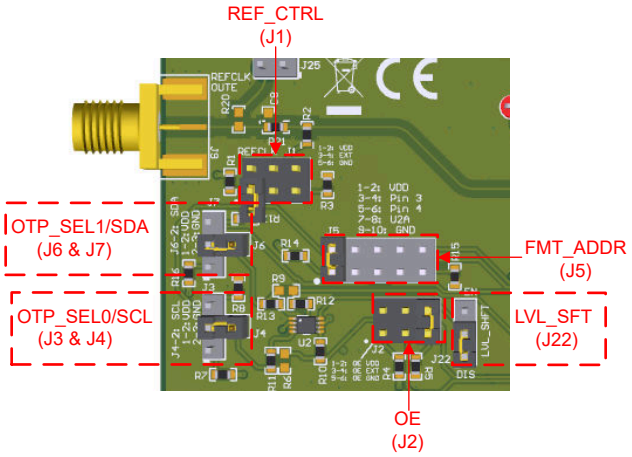


Figure 2-3. LMK3H0102EVM Control Jumpers

The REF_CTRL, OE, OTP_SEL0/SCL, and OTP_SEL1/SDA pins are all two level pins, and can be pulled high or low through the jumpers. Additionally, the REF_CTRL and OE pins can be controlled through software via TICS Pro to set the pin voltage.

The FMT_ADDR pin can be connected to VDD, GND, SCL, or SDA, in addition to being controllable via software - all of these options are available using the J5 jumper.

The LMK3H0102 control pins perform different functions depending on the mode of operation.

- For **OTP Mode**, refer to Table 2-2 for jumper descriptions.
- For **I2C Mode**, refer to Table 2-3 for jumper descriptions.

Table 2-2. OTP Mode Control Pin Behavior

Component	Name (type)	Description	
J1	REF_CTRL (2-level input)	**REF_CTRL Pin** REF_CTRL state is sampled on POR and determines the mode of operation.	
		REF_CTRL State	**Operating Mode**
		HI: Tie pins 1 & 2	**OTP Mode** OTP_SEL0 and OTP_SEL1 pins are sampled on start-up to determine the OTP page to load
		LO: Tie pins 5 & 6 Floating (Default)	**I2C Mode** FMT_ADDR pin is sampled on the first I2C transaction to determine the I2C address of the device
		SW: Tie pins 3 & 4	Pin state is controlled by software. This option can be used when using an external VDD source to set the pin state through TICS Pro to switch between I2C Mode and OTP Mode on power cycle quickly
J2	OE (2-level input)	**OE Pin** The OE pin controls the output enable, and has the same function regardless of start-up mode. The default behavior of the pin is active-low; this can be changed to active-high in the Wizard.	
		OE State	**Operating Mode**
		HI: Tie pins 1 & 2	Disable the clock outputs.
		LO: Tie pins 5 & 6 (Default)	Enable the clock outputs. If the clock outputs are disabled in software, the outputs remain disabled.
		SW: Tie pins 3 & 4	Pin state is controlled by software
J3 & J4	OTP_SEL0	**OTP_SEL0 Pin** The OTP_SEL0 and OTP_SEL1 pins control the OTP page loaded from the EFUSE into the active device registers on startup.	
		OTP_SEL1 **OTP_SEL0**	**OTP Page**
		LO: Tie J7 pins 2 & 3 LO: Tie J3 pins 2 & 3	OTP Page 0
		LO: Tie J7 pins 2 & 3 HI: Tie J3 pins 1 & 2	OTP Page 1
		HI: Tie J7 pins 1 & 2 LO: Tie J3 pins 2 & 3	OTP Page 2
		HI: Tie J7 pins 1 & 2 HI: Tie J3 pins 1 & 2	OTP Page 3
		Connect J7 pin 2 to J6 (Default) Connect J3 pin 2 to J4 (Default)	Pulled high through resistors. OTP Page 3

Table 2-2. OTP Mode Control Pin Behavior (continued)

Component	Name (type)	Description	
J5	FMT_ADDR	**FMT_ADDR Pin** The FMT_ADDR pin is ignored by default in LMK3H0102V33 default configuration. Devices with custom configurations can be populated where R9[8] = 1. In this case, the FMT_ADDR pin sets the output format for OUT[1:0].	
		FMT_ADDR State	**Output Format**
		HI: Tie J5 pins 1 & 2 (Default)	LP-HCSL 85-Ω Termination
		LO: Tie J5 pins 9 & 10	LP-HCSL 100-Ω Termination
		Software: Tie J5 pins 7 & 8	Pulled to HI or LO using TICS Pro
		OTP_SEL0: Tie J5 pins 3 and 4	Matches state of OTP_SEL0 pin
		OTP_SEL1: Tie J5 pins 5 and 6	Matches state of OTP_SEL1 pin
J6 & J7	OTP_SEL1	**OTP_SEL1 Pin** See OTP_SEL0 Pin	
J22	LVL_SFT	Tie J22 pins 2 & 3 together in OTP Mode.	

Table 2-3. I2C Mode Control Pin Behavior

Component	Name (type)	Description	
J1	REF_CTRL (2-level input)	**REF_CTRL Pin** REF_CTRL state is sampled on POR and determines the mode of operation.	
		REF_CTRL State	**Operating Mode**
		HI: Tie pins 1 & 2	**OTP Mode** OTP_SEL0 and OTP_SEL1 pins are sampled on start-up to determine the OTP page to load
		LO: Tie pins 5 & 6 Floating (Default, internal pulldown resistor)	**I2C Mode** FMT_ADDR pin is sampled on the first I2C transaction to determine the I2C address of the device
		SW: Tie pins 3 & 4	Pin state is controlled by software This option can be used when using an external VDD source to set the pin state through TICS Pro to switch between I2C Mode and OTP Mode on POR quickly
J2	OE (2-level input)	**OE Pin** The OE pin controls the output enable, and has the same function regardless of start-up mode. The default behavior of the pin is active-low; this can be changed via software to active-high.	
		OE State	**Operating Mode**
		HI: Tie pins 1 & 2	Disable the clock outputs.
		LO: Tie pins 5 & 6 (Default)	Enable the clock outputs. If the clock outputs are disabled in software, the outputs remain disabled.
		SW: Tie pins 3 & 4	Pin state is controlled by software

Table 2-3. I2C Mode Control Pin Behavior (continued)

Component	Name (type)	Description	
J3 & J4	SCL	**SCL Pin** The SCL and SDA pins control the I2C interface of the device. If VDD is 1.8 V, then use J22 to level-shift the logic high voltage down to 1.65 V to prevent device damage. SCL is the I2C clock, and SDA is the I2C data.	
		SCL **SDA**	**I2C Configuration**
		Connect J3 pin 2 to J4 (Default) Connect J7 pin 2 to J6 (Default)	SCL connected to the USB2ANY SDA connected to the USB2ANY
		All other states	I2C disconnected
J5	FMT_ADDR	**FMT_ADDR Pin** In I2C mode, the I2C address is latched based on the state of the FMT_ADDR pin at the first I2C transaction.	
		FMT_ADDR State	**I2C Address**
		HI: Tie J5 pins 1 & 2 (default)	0x69
		LO: Tie J5 pins 9 & 10	0x68
		SCL: Tie J5 pins 3 and 4	0x6A
		SDA: Tie J5 pins 5 and 6	0x6B
		SW: Tie J5 pins 7 and 8	I2C address controlled by software, latched on first I2C transaction
J6 & J7	SDA	**SDA Pin** See SCL Pin	
J22	LVL_SFT	**I2C Level Shift Pin** The state of this pin determines whether or not the I2C level shifter is enabled. R6 and R9 are depopulated by default.	
		LVL_SFT State	**Level Shift Operation**
		HI: Tie J22 pins 1 and 2 (Default)	Level shifter is active
		LO: Tie J22 pins 2 and 3 together	Level shifter is inactive R6 and R9 must be populated

2.2.3 Configuring the Clock Outputs

The clock output pairs of the LMK3H0102 are routed via 50-Ω single-ended traces to SMA ports (OUT[1:0]_P/OUT[1:0]_N). These outputs have series resistor (0-Ω populated) options. The default output configuration for the LMK3H0102EVM is AC-coupled LP-HCSL for OUT0 and DC-coupled LP-HCSL for OUT1. Each of these outputs can be configured for AC-LVDS, DC-LVDS, LP-HCSL, and LVCMOS output formats per the Output Format Types section of the LMK3H0102 data sheet.

The REF_CTRL pin of the LMK3H0102 can be configured as an additional LVCMOS clock, REF_CLK, allowing for up to five LVCMOS clock outputs. The REF_CLK output is routed to the REFCLK SMA port through a 33-Ω series resistor, with the option for a 10 pF capacitor to GND.

The output high level of the OUT0 and OUT1 LVCMOS outputs are set by the voltage on the VDDO plane. The output high level of the REF_CLK output is set by the voltage on the VDD plane.

2.2.4 Using the USB Interface Connection

The on-board MSP430F5529 USB microcontroller (U7) provides an I2C host interface to the LMK3H0102 peripheral device. The device registers can be controlled via USB using the TICS Pro software running on a host PC. J21 can be used with an external USB2ANY as an alternative to using the on-board USB2ANY.

If the USB2ANY firmware needs to be updated, the J20 header serves as the BSL pin. Connect the jumper on J20 between pins 1 and 2 to mimic pressing the BSL button of an external USB2ANY. Disconnect the jumper after updating the firmware.

2.2.5 EVM Quick Start Guide

The following guide allows the user to quickly configure the LMK3H0102EVM to evaluate the pre-programmed I2C or OTP configurations.

1. If using software to program the device registers using I2C, install the TICS Pro software.
2. Confirm the EVM default power configuration is set per Figure 2-2/Table 2-1 to power the LMK3H0102 using the on-board DC/DC converters with VDD = VDDO = 3.3 V.
3. Set the control pin jumpers to select the desired start-up mode, as well as the other pin configuration settings, according to Table 2-2 for OTP Mode or Table 2-3 for I2C Mode. The default configuration is for I2C Mode.
   a. For OTP mode, Table 2-4 shows the default settings of the different OTP pages for the LMK3H0102V33 preprogrammed device configuration.
4. Connect the micro-B USB cable to the micro-B USB port of the EVM, and connect the USB-A end to a PC.
5. Observe any active clock on the OUT[1:0] SMA ports.
   a. OUT0 is AC-coupled, and OUT1 is DC-coupled.
   b. REF_CTRL is DC-coupled to the SMAs with a 33-Ω termination resistor in series.
   c. Use 50-Ω coax cables to connect the test equipment to the output SMA ports. If making a single-ended measurement on a differential output, terminate the unused SMA port with a 50-Ω load.
   d. To minimize output clock switching noise from affecting jitter-sensitive measurements, terminate any unused active output clock pair using 50-Ω SMA loads; otherwise, power-down unused output clocks via register programming.

Table 2-4. LMK3H0102 Start-up Settings

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
OUT0 Frequency	100 MHz	100 MHz	100 MHz	100 MHz
OUT0 Output Format	100-Ω LP-HCSL	100-Ω LP-HCSL	100-Ω LP-HCSL	100-Ω LP-HCSL
OUT0 Enable	Enable	Enable	Enable	Enable
OUT0 Slew Rate	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns
OUT0 Amplitude	755 mV (typical)	755 mV (typical)	755 mV (typical)	755 mV (typical)
OUT0 Disable Behavior	GND	GND	GND	GND
OUT1 Frequency	100 MHz	100 MHz	100 MHz	100 MHz
OUT1 Output Format	100-Ω LP-HCSL	100-Ω LP-HCSL	100-Ω LP-HCSL	100- LP-HCSL
OUT1 Enable	Enable	Enable	Enable	Enable
OUT1 Slew Rate	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns	2.3 to 3.4 V/ns
OUT1 Amplitude	755 mV (typical)	755 mV (typical)	755 mV (typical)	755 mV (typical)
OUT1 Disable Behavior	GND	GND	GND	GND
REF_CTRL Behavior	CLK_READY	CLK_READY	CLK_READY	CLK_READY
FOD0 Frequency	200 MHz	200 MHz	200 MHz	200 MHz
FOD1 Frequency	200 MHz	200 MHz	200 MHz	200 MHz
SSC Enable	Disable	Disable	Disable	Disable
SSC Modulation Type	Down-spread	Down-spread	Down-spread	Down-spread
SSC Modulation Depth	0%	–0.1%	–0.3%	–0.5%

2.3 Modes of Operation

The LMK3H0102 can be configured to start-up in one of two modes upon power-on/reset (POR). The mode of operation and associated control pins determine which on-chip memory type and memory page settings are used to initialize the active registers for configuring the Fractional Output Dividers (FODs), Output, and Device Control blocks for full operation:

1. **I2C Mode** (EVM default): Loads all registers with the settings stored on OTP Page 0, defined in Table 2-4. The I2C interface is available in this mode for configuring the device registers as desired.
2. **OTP Mode**: Loads all registers from one of the four OTP page settings defined in Table 2-4. All four pages are "hard-coded" with predefined register settings by TI and cannot be overwritten. The I2C interface is not available in this mode.

Once the LMK3H0102 starts up in I2C mode, the I2C interface is enabled to provide (optional) access to all device registers for full control of the LMK3H0102 settings. For convenience, a USB-to-I2C interface is integrated on-board and can be controlled by TICS Pro.

3 Software

3.1 Using TICS Pro with the LMK3H0102EVM

The TICS Pro profile for the LMK3H0102 can be accessed by performing the following steps:

1. Open the TICS Pro software
2. Navigate to Select Device > Referenceless Clock Generators > LMK3H0102

3.1.1 Using the LMK3H0102 Wizard

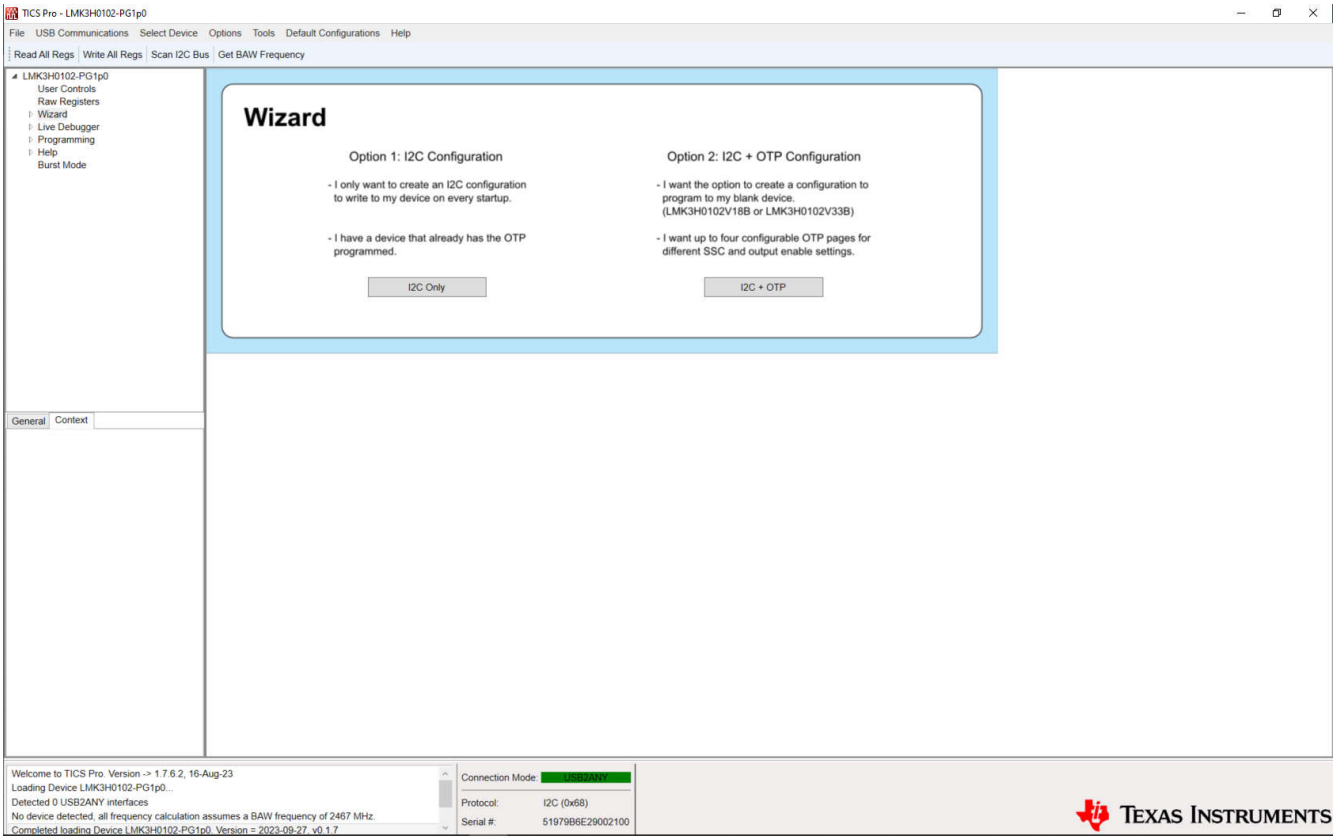


Figure 3-1. LMK3H0102 Wizard Start Page

Figure 3-1 shows the opening page, the *Wizard* page, for the TICS Pro profile for the LMK3H0102. The *Wizard* page allows for selecting one of two programming methods:

1. **I2C Configuration**: This is for users that intend to create an I2C configuration to write on start-up every time. If the device needs to start up with a specific configuration other than the device default, this option must not be selected.
2. **I2C + OTP Configuration**: This is for users that plan to place the part into a system and start up with predefined settings without additional programming. This option is intended exclusively for sending a configuration file to TI for creating an OTP configuration. Use E2E for sending custom configuration files, exported using the *Design Report* page.

Clicking on the I2C or I2C + OTP opens the *Output Frequency Plan* page. If I2C Configuration is selected, then the option to configure the various OTP pages is automatically skipped.

3.1.1.1 Frequency Plan

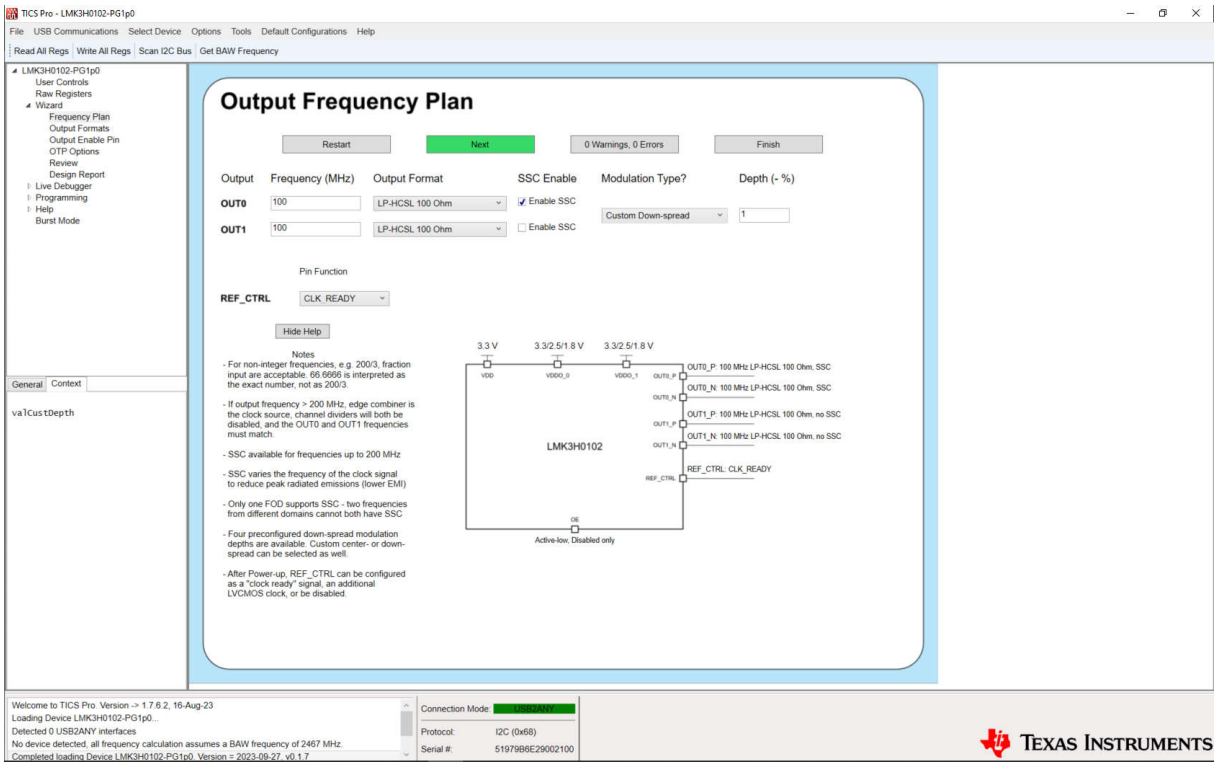


Figure 3-2. LMK3H0102 Wizard Output Frequency Plan Page

The *Output Frequency Plan* page allows for configuring the outputs required for a system. Set each output's clock to the desired frequency and the wizard determines the FOD selection, the channel dividers, and so on for generating the frequency plan. Each output can have the format set on this page, with additional details on the format configuration provided on the *Output Formats* page.

SSC can be individually enabled/disabled on this page. If either output frequency exceeds 200 MHz, then SSC cannot be used. If SSC is enabled for a specific output, then the modulation type can be set to one of the preconfigured down-spread configurations, a custom down-spread configuration, or a custom center-spread configuration. The custom modulation depth fields accept both positive and negative numbers, so there is no need to worry about specifying the sign of the value.

If the REF_CTRL pin is configured as a REF_CLK output, then options appear for setting the REF_CLK frequency. If only one FOD is used, then any arbitrary frequency between 12.5 MHz and 100 MHz without SSC can be generated, and a text box appears for inputting the desired frequency. If both FODs are in use, then a drop-down menu appears that displays the available frequencies.

The block diagram representation of the LMK3H0102 updates based on the settings that have been selected during configuration generation, and is presented as an aid for visualizing the configuration of the pins on each wizard page.

Clicking the *Next* button navigates to the next page if there are no errors on the page. If there is an entry that causes an error, then the field is highlighted in red, an error message appears in the status bar at the bottom of the page, a tooltip is added to the field displaying the error message, and the "0 Warnings, 0 Errors" button turns red and updates the error count. If an entry creates a warning, then the same actions occur, but instead the highlight is yellow, and the warning count is updated. Clicking on the Warning/Error button at the bottom displays all of the current errors that exist in the configuration.

Clicking the *Restart* button clears all fields on all pages that have been entered, and returns to the *Wizard* page.

Clicking the *Finish* button assumes the device defaults for all remaining configuration options, and navigates to the *Design Review* page, where the full configuration can be viewed before writing to the device.

3.1.1.2 Output Formats

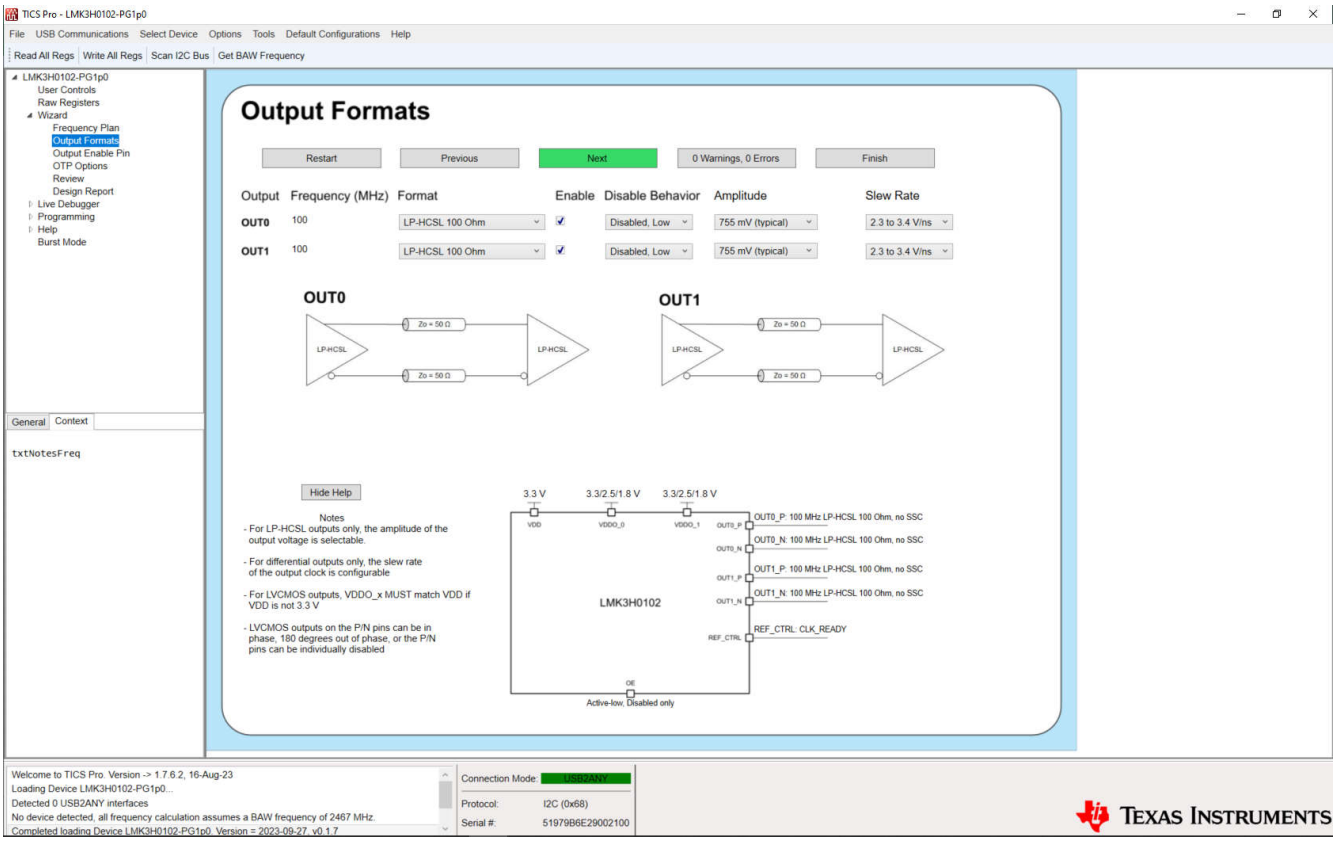


Figure 3-3. LMK3H0102 Wizard Output Formats Page

The *Output Formats* page allows for configuring the formats of the device outputs. For each output type selected, the images in the GUI change to provide a visual aid. For differential outputs, these are diagrams showing the termination required. For single-ended outputs, these are diagrams showing the behavior of the P and N pins of the output.

If an LP-HCSL output is selected, *Amplitude* field sets the typical LP-HCSL amplitude. If an LVDS output is selected, then this field is hidden as the settings do not apply to LVDS. For LVCMOS outputs, the phase is selectable, and the field changes to a *Phase* field. The OUTx_P and OUTx_N pins can be individually enabled, in phase, or opposite phase.

For all differential outputs, the output slew rate can be configured using the *Slew Rate* field. For single-ended outputs, the phase and LVCMOS voltages are selectable, and the *Slew Rate* field changes to an *LVCMOS Voltage* field. The *LVCMOS Voltage* is not register-backed, but instead is meant to provide a visual by displaying the pin voltage in the block diagram.

Each output can be individually enabled or disabled on this page. A disabled output can be pulled to GND internally or tr-istated. By default, any disabled outputs are pulled to GND.

3.1.1.3 Output Enable Pin

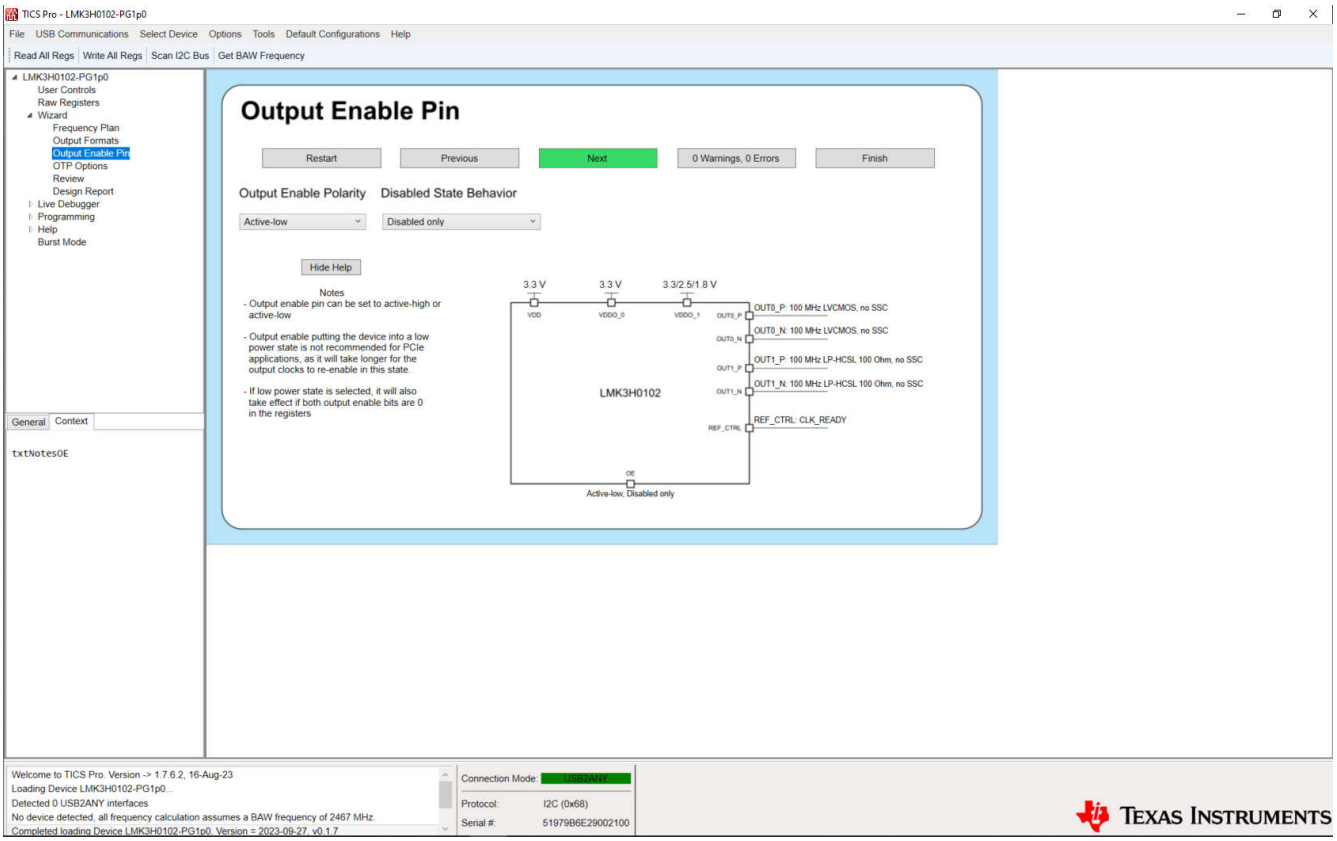


Figure 3-4. LMK3H0102 Wizard Output Enable Pin Page

The *Output Enable Pin* page allows for configuration of the OE pin behavior. By default, the pin is configured as an active-low pin. The pin can be configured to active-high, where connecting the OE pin to GND disables the outputs.

The disabled state behavior can be set such that, on disable, the device enters a power-down mode with only I2C accessible. This is not recommended for applications where the clocks need to re-enable quickly, such as PCIe applications, as the device must power up again prior to the output clocks being ready.

3.1.1.4 OTP Options

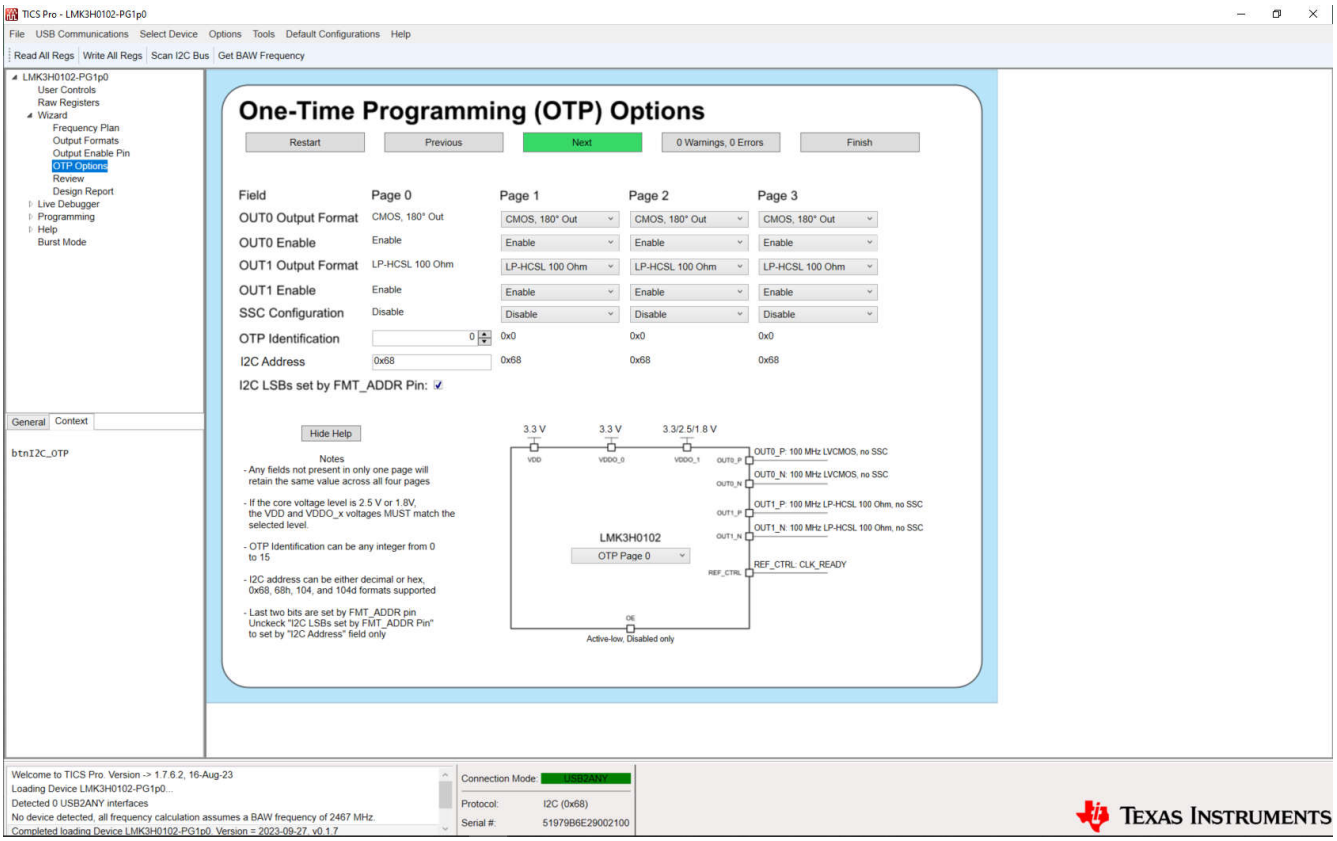


Figure 3-5. LMK3H0102 Wizard OTP Options Page

The *OTP Options* page allows for configuration of the additional OTP pages that are not present in the live registers. If using the wizard in I2C Mode, then this page is skipped by default, and the options on the page are greyed out if the page is manually navigated to. The format of the output clocks, the output enables, and the SSC on FOD0 can all be modified across the different OTP pages. The Page 0 settings are specified based on the prior wizard pages. Changing the page 0 fields requires navigating to the previous pages.

The *OTP Identification* and *I2C Address* fields are all shared between the four OTP pages. *OTP Identification* is a four-bit field that can be set to any integer value between 0 and 15. The *I2C Address* is a 7-bit field that can be set to any value between 0 and 127 allowed by the I2C standard. The two least significant bits of the I2C address are set by the state of the FMT_ADDR pin on start-up.

When in the I2C + OTP Configuration mode, the block diagram on the *OTP Options* and *Review* pages has a dropdown that allows for showing the pin configuration for the specified OTP page.

3.1.1.5 Review

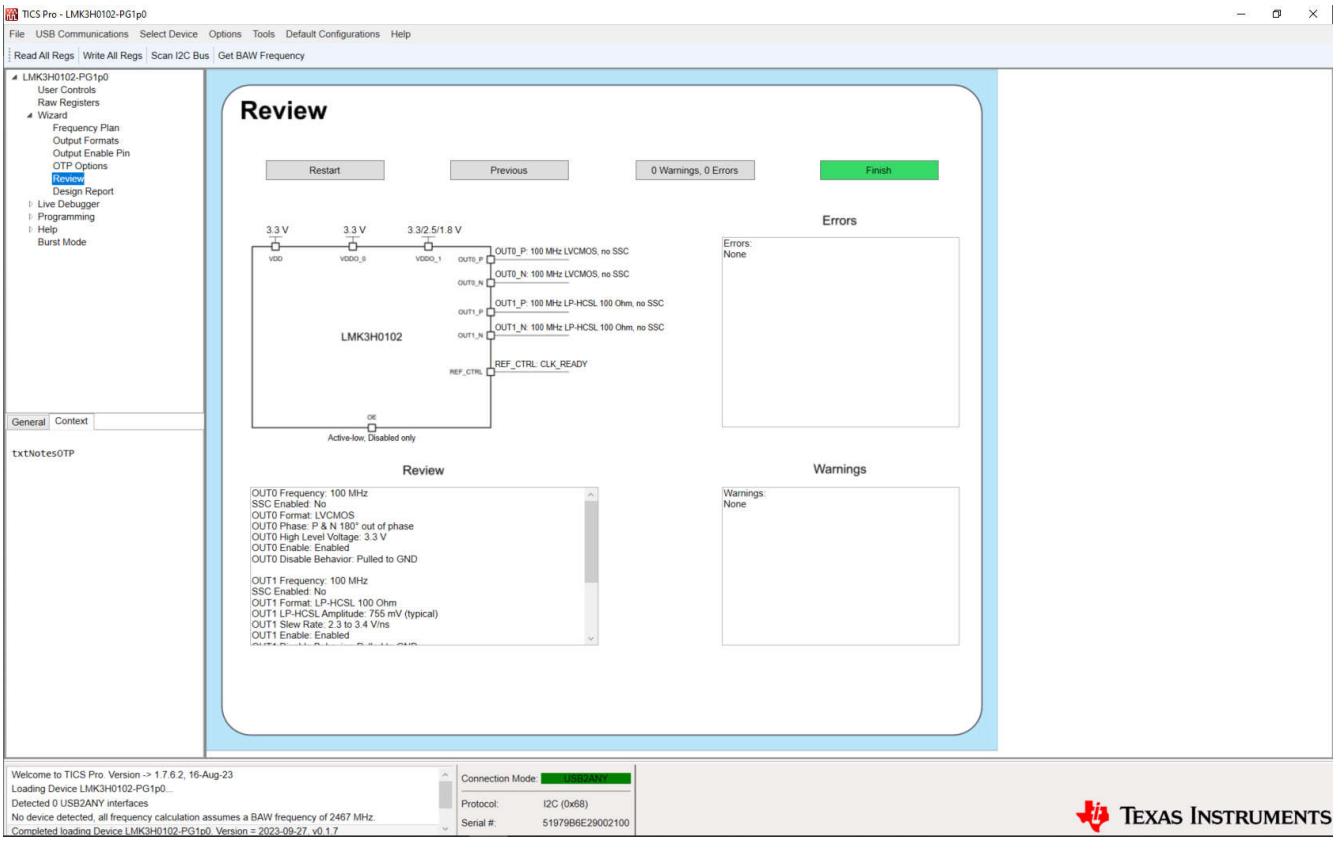


Figure 3-6. LMK3H0102 Wizard Review Page

The *Review* page is a high-level overview of the options that have been selected in the wizard. Any errors prevent configuration generation and must be resolved on their respective pages before the wizard allows device writing.. Warnings are informational only, and do not prevent configuration generation. If there are no errors and the configuration is as desired, then click the "Finish" button to proceed to the design report.

3.1.1.6 Design Report

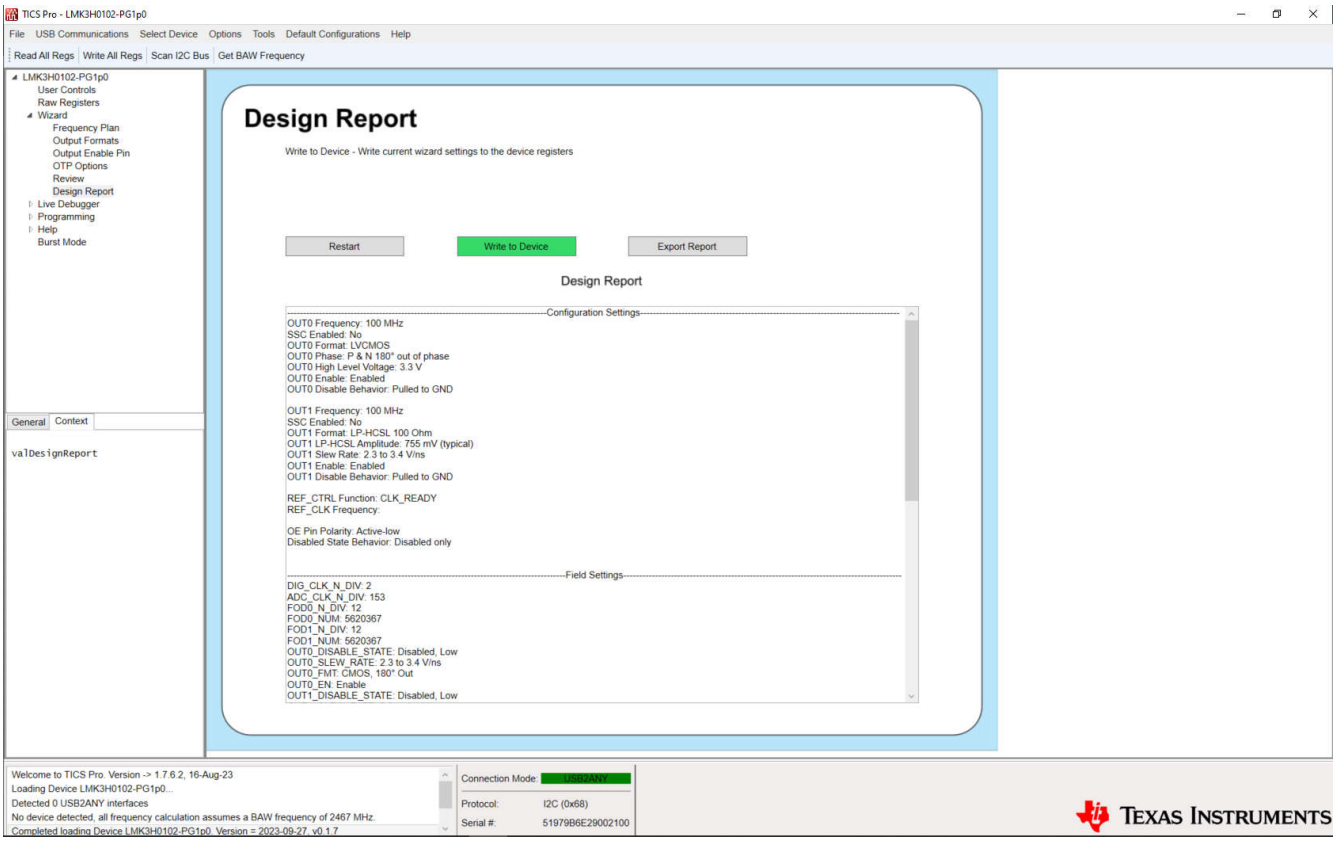


Figure 3-7. LMK3H0102 Design Report Page

The *Design Report* page allows for writing the LMK3H0102 registers based on the settings selected on the previous wizard pages.

The "Write to Device" button takes the current configuration, and writes to the registers of the device. The "Export Report" button exports the text of the Design Report window to a text file for sending to TI when requesting a new custom OTP configuration. Submit all new configuration requests on E2E.

The text under the "Design Report" label is populated with a full design report, including:

- The configuration settings
- The value of each device field
- The OTP pages, if configuring an OTP configuration
- The register settings

3.1.2 Live Debugger

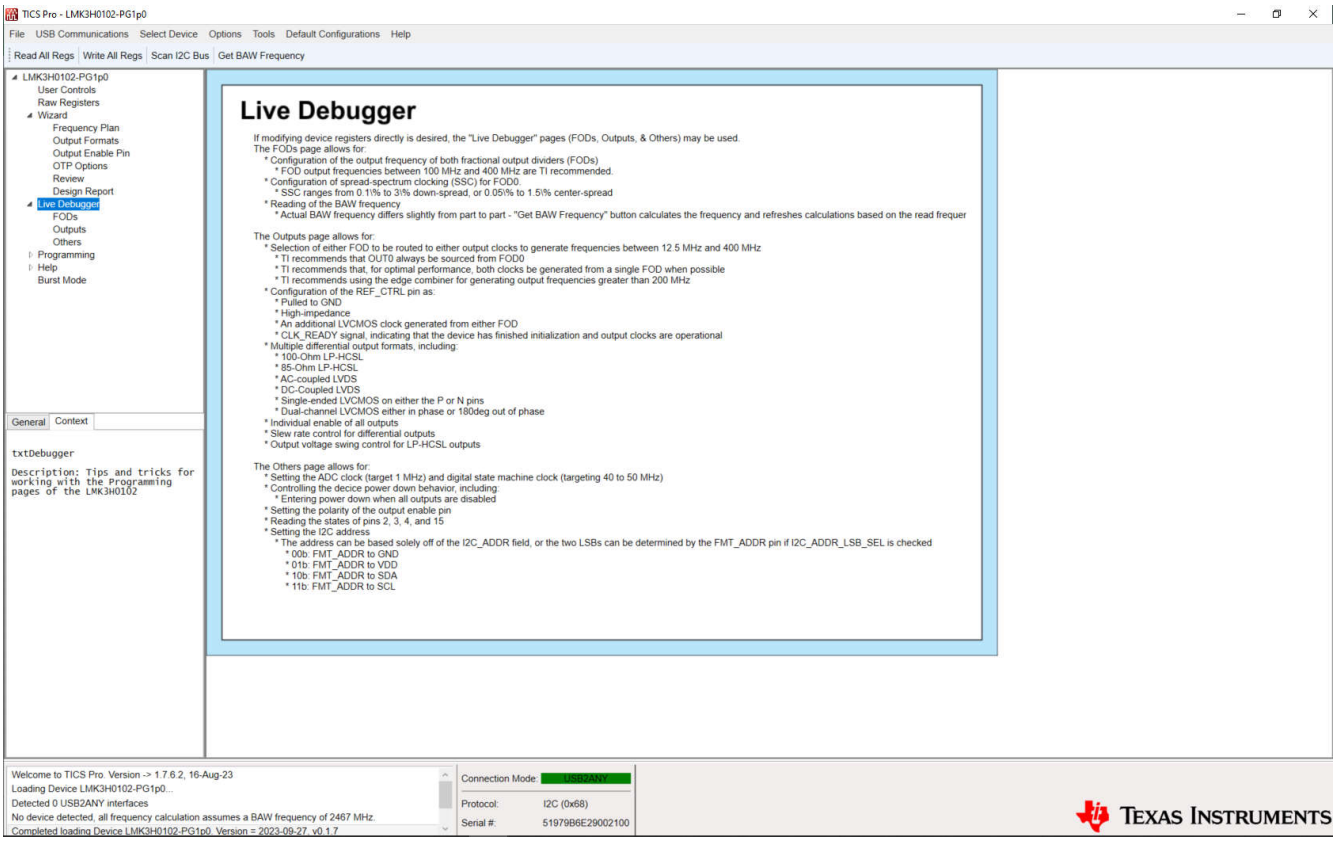


Figure 3-8. LMK3H0102 Live Debugger Page

The *Live Debugger* page provides an overview of how to use the *FODs*, *Outputs*, and *Others* pages. This serves as an in-GUI reference with TI recommendations, as to prevent having to alternate between the GUI and the data sheet or User's Guide.

3.1.2.1 FODs

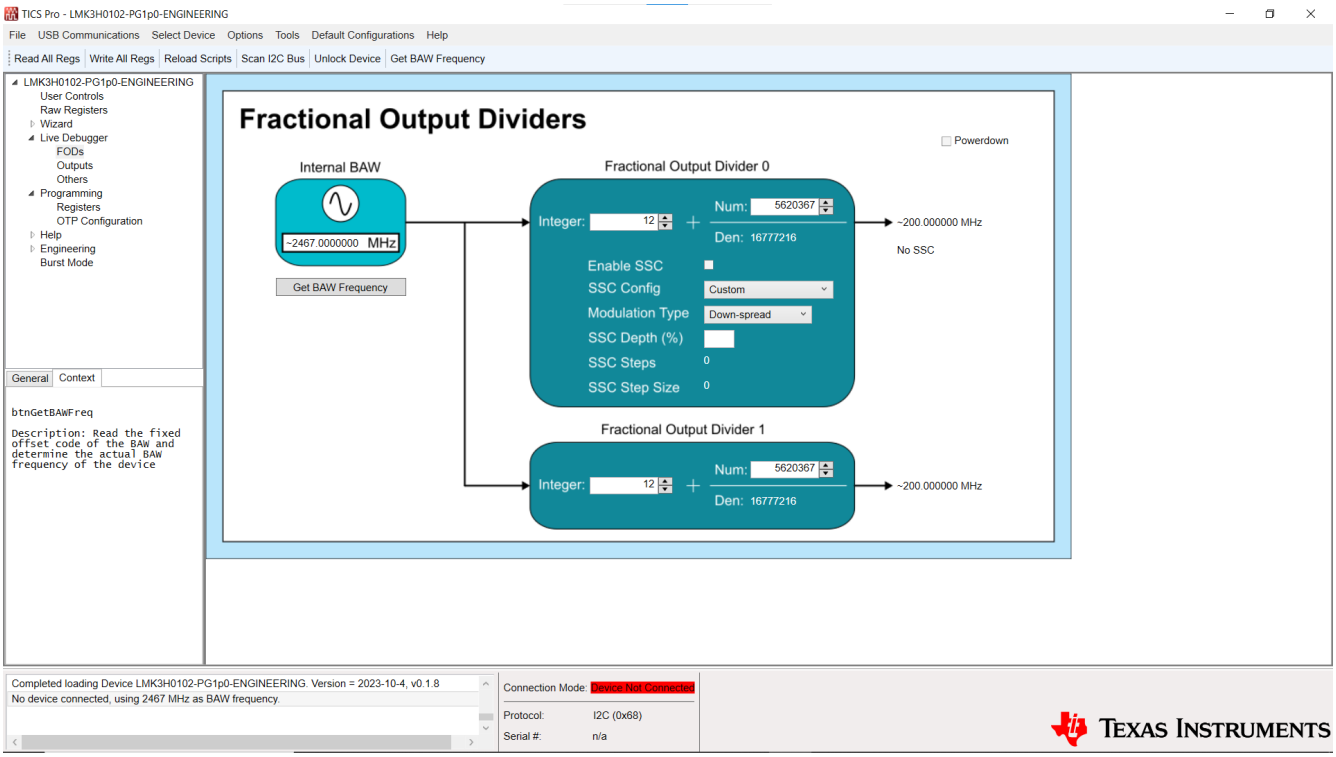


Figure 3-9. LMK3H0102 FODs Page

The *FODs* page allows for manipulation of the FODs of the device. Before modifying the FOD settings, read the BAW frequency from the device by clicking the *Get BAW Frequency* button. This populates the field with the approximate BAW frequency of the connected device, and keeps the value internally for frequency calculation. If there is not a device connected, then the nominal frequency of 2467 MHz is used for all GUI frequency calculations, including the wizard. As the BAW frequency changes from device to device, reading the frequency before continuing with the GUI usage is imperative. If the device registers are read at startup of the profile, or if the *Read All Regs* button in the toolbar is pressed, then the BAW frequency is read from the device and updated in the GUI.

Before modifying any settings on this page, click the *Powerdown* check box, change the settings, then click the *Powerdown* checkbox again. Both FODs consist of an integer and fractional divider. The output of the fractional divider is given by the frequency of the BAW divided by the total divide value of the FOD. FOD0 exclusively has the option for SSC on the output, meaning that any outputs requiring SSC must be sourced from FOD0. The down-spread SSC settings are configured before and can be selected. If a different depth or center-spread are required, then the GUI automatically calculates the SSC_STEPS and SSC_STEP_SIZE fields based on the desired depth and modulation type.

3.1.2.2 Outputs

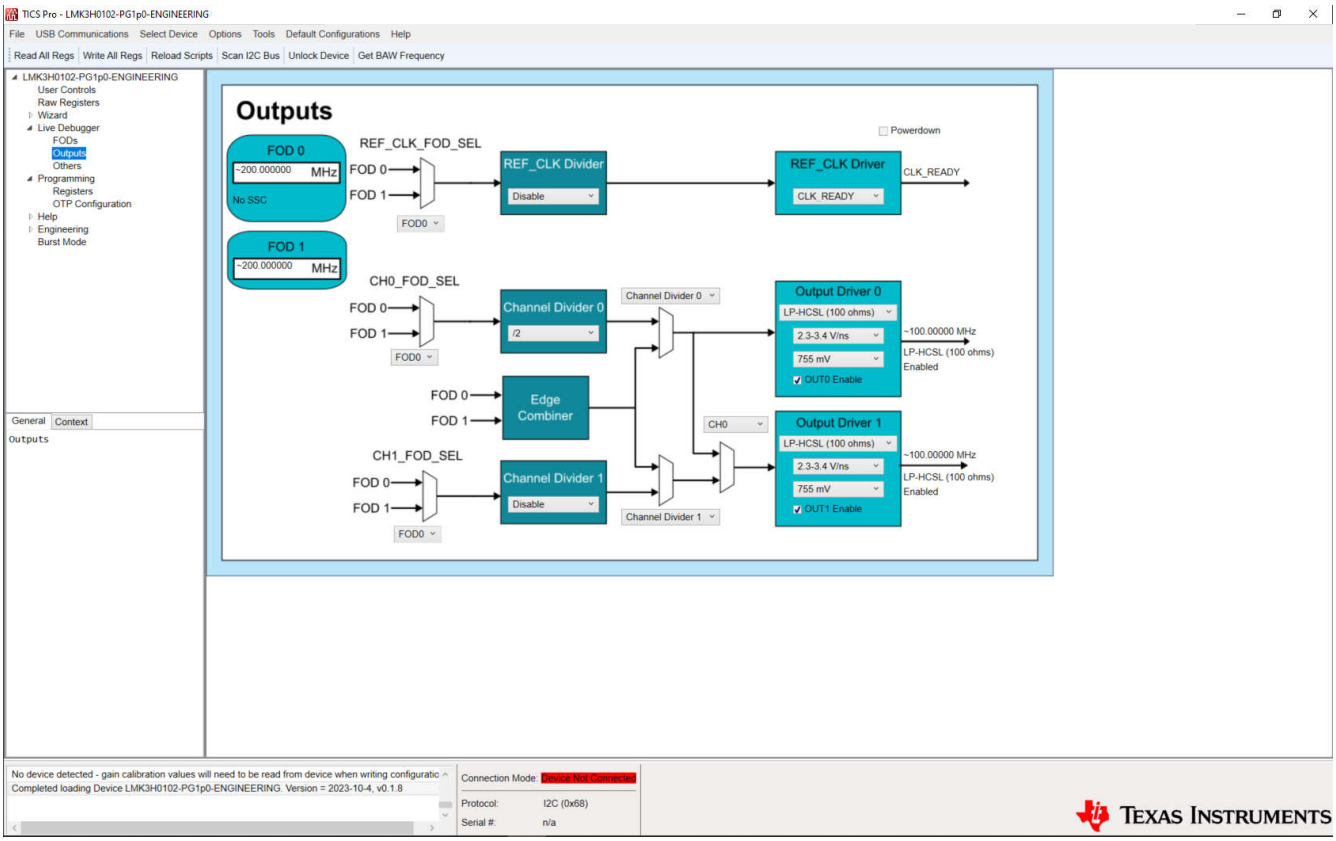


Figure 3-10. LMK3H0102 Outputs Page

The *Outputs* page allows for configuration of the channel dividers and output drivers. Before changing any settings on this page, click the *Powerdown* checkbox, modify the desired settings, then click the *Powerdown* checkbox again. Either channel divider can be driven from either FOD. Each output driver can be sourced from the respective channel divider, or the Edge Combiner. Output Driver 1 can be sourced from either channel divider output, allowing for power savings if OUT0 and OUT1 are the same frequency. The REF_CTRL pin can be configured as a CLK_READY signal, pulled low, high impedance, or an additional LVCMOS clock sourced from either FOD.

For LP-HCSL outputs, the output swing is adjustable between 625 mV and 950 mV depending on the application requirements. The output can be AC-coupled and used to mimic AC-coupled versions of other clock formats, such as LVPECL. All differential output formats have adjustable slew rate control. LVCMOS clock outputs can be individually enabled, in phase, or 180 degrees out of phase - TI recommends keeping the P and N outputs out of phase unless necessary for improved performance. The text to the right of each output driver summarizes the output frequency, the enable state of the output, and the output format.

3.1.2.3 Others

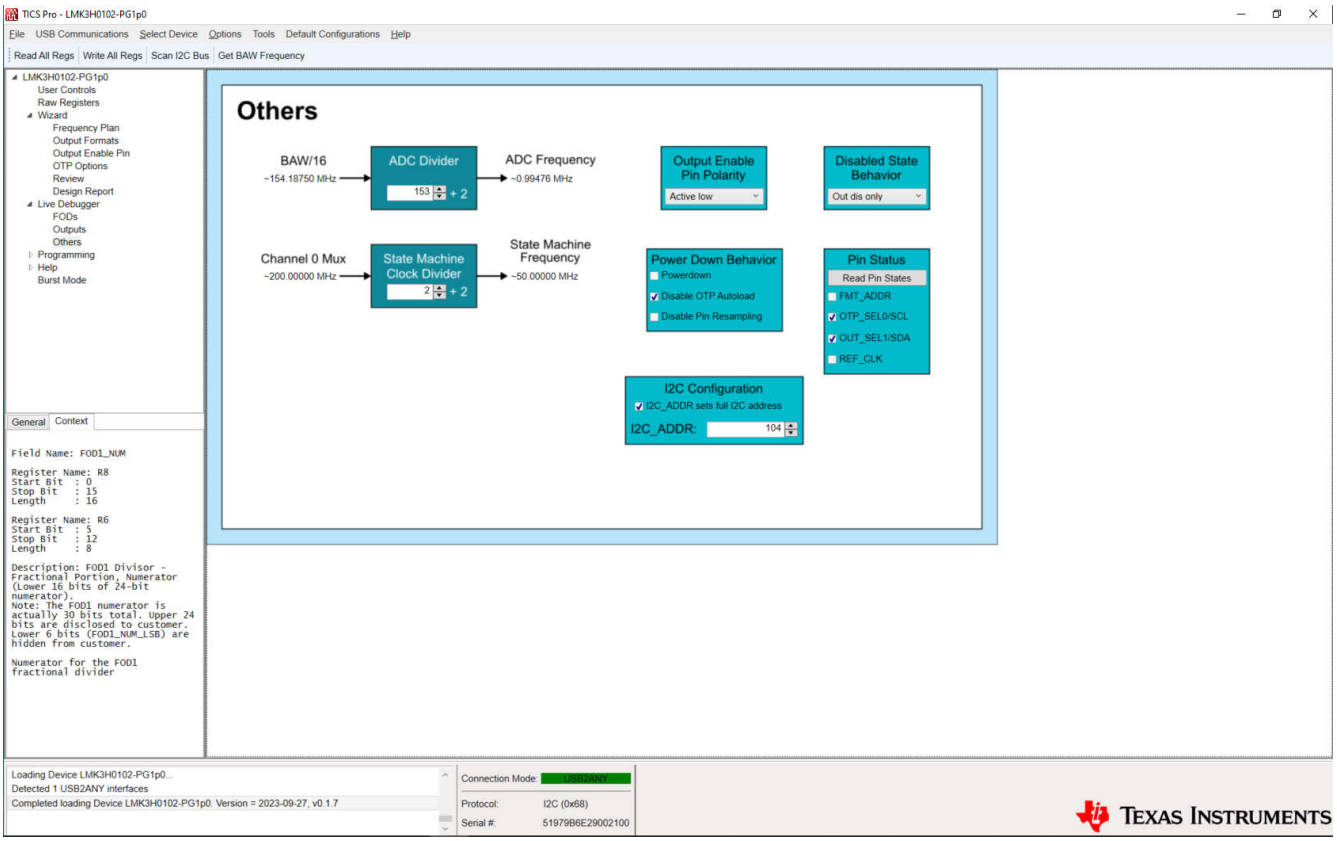


Figure 3-11. LMK3H0102 Others Page

The *Others* page allows for modification of remaining miscellaneous device fields. The ADC Divider is fixed at 153 - TI does not advise changing this value. The State Machine Clock Divider must be set so that the State Machine Frequency is as close as possible to 45 MHz. The polarity of the Output Enable Pin, as well as the behavior of the device when put into a disabled state, are both adjustable here. The *Read Pin States* button reads R10 from the device and populates the checkboxes below the button with the live pin states. The I2C configuration fields are used for configuring the I2C address - unlocking device in the *User Controls* page must be done prior to modifying these fields (User Controls → Customer: Controls, Pin setting, and Status → 0x5B to UNLOCK_PROTECTED_REG).

The *Disable OTP Autoload* checkbox disables loading of OTP Page 0 into the live device registers when the device comes out of a low power state. If changing the configuration of the device, this box must be checked to prevent the OTP autoload function, and can only be set while the *Powerdown* checkbox is checked. The *Powerdown* checkbox places the device into a low power state, within which the settings on the Section 3.1.2.1 and Section 3.1.2.2 pages can be modified. If the State Machine Clock Divider needs to change, then check this box, modify the divider, and clear this box. The *Disable Pin Resampling* checkbox, when cleared, allows for resampling of the device pins when coming out of a low power state. This can be used to transition from I2C mode to OTP mode by changing the state of the device pins, followed by toggling the *Powerdown* checkbox from cleared → checked → cleared. Transitioning from OTP mode back to I2C mode requires a power cycle of the device.

3.1.3 Programming

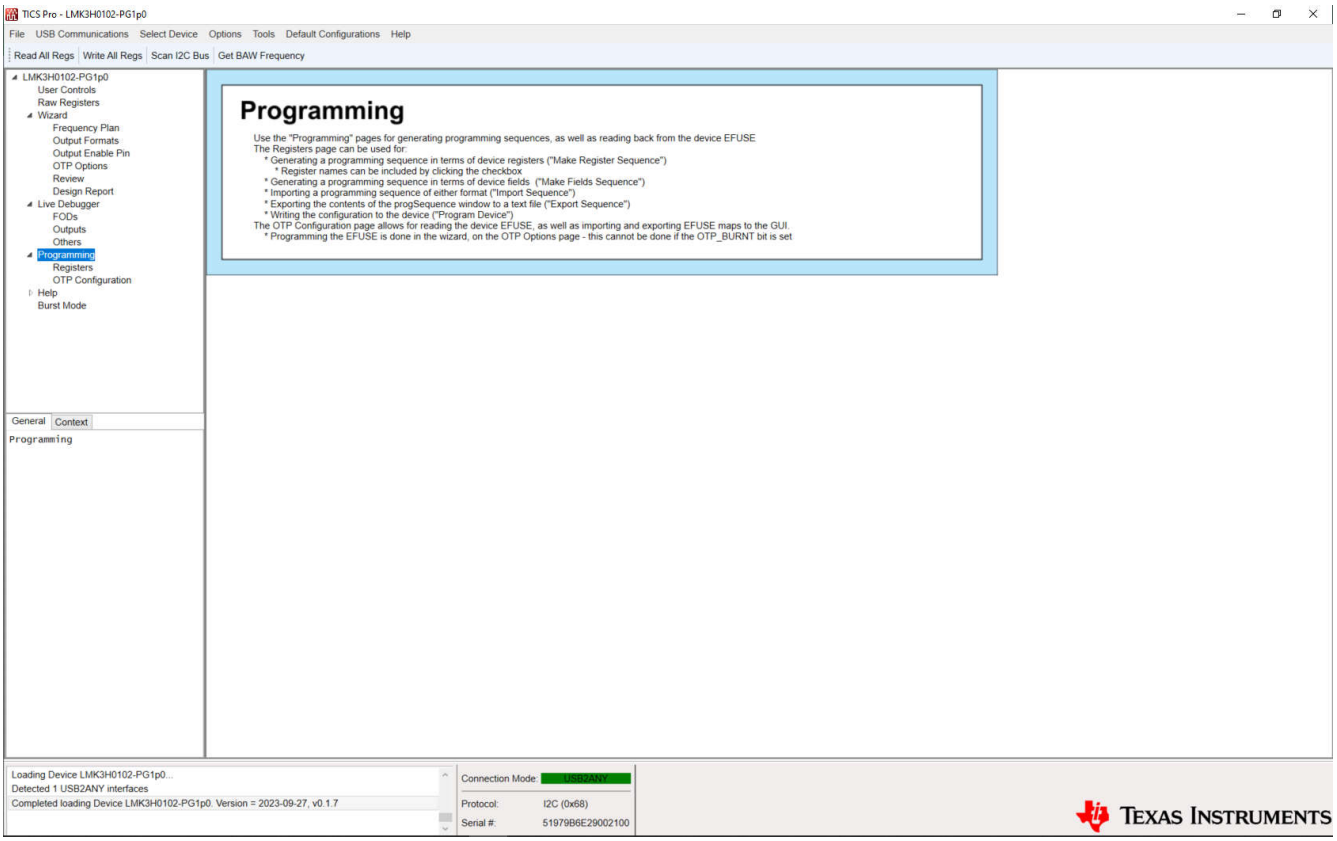


Figure 3-12. LMK3H0102 Programming Page

The *Programming* page serves as a reference for using the *Registers* and *OTP Configuration* pages.

3.1.3.1 Registers

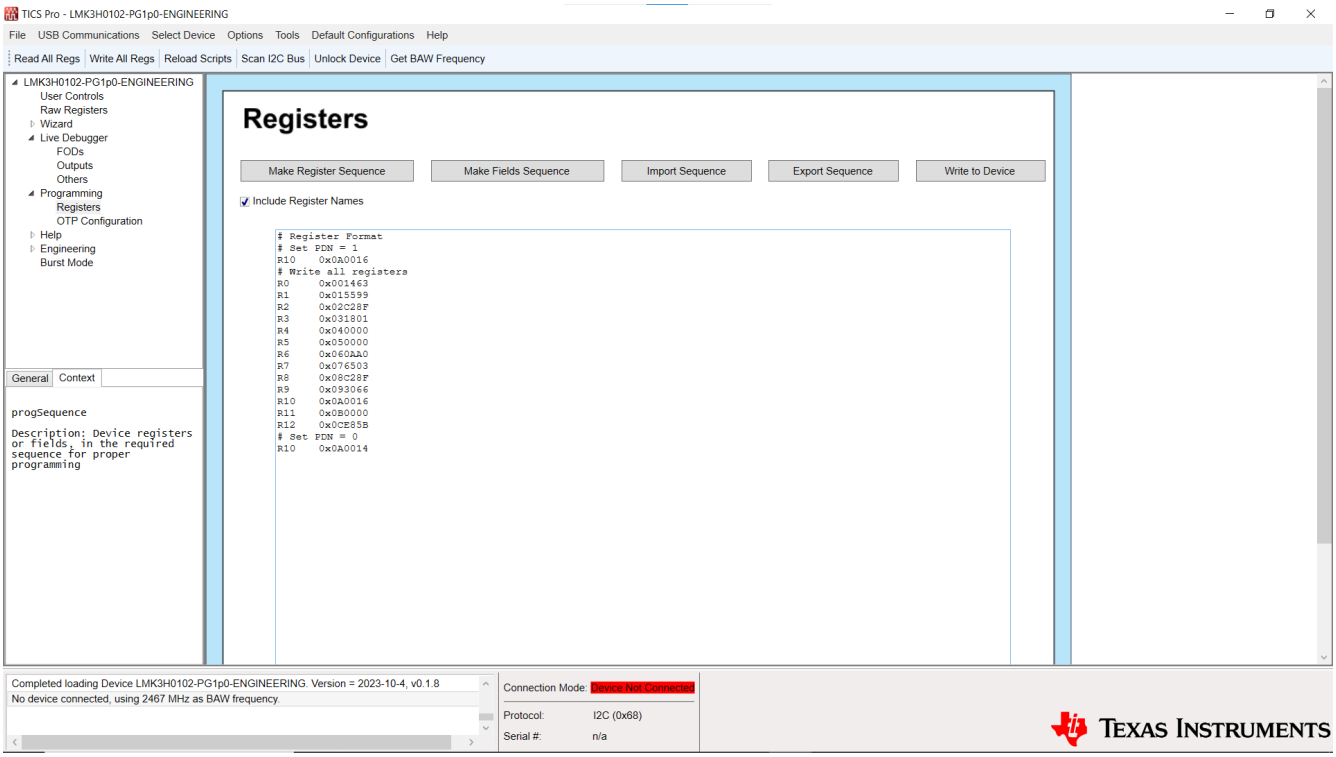


Figure 3-13. LMK3H0102 Registers Page

The *Registers* page allows for bulk reading and writing of the device registers. The *Make Register Sequence* button generates a register sequence for writing all required registers to the device. This includes setting the PDN bit to a '1' before modifying registers, and setting the bit to a '0' afterward. The *Include Register Names* checkbox inserts the register name before the register data, separated by a tab. The registers can be written field-by-field using the *Make Fields Sequence* button. Sequences can be imported into and exported from the GUI using the *Import Sequence* and *Export Sequence* buttons. The contents of the *progSequence* field below the buttons can be written to the device using the *Write to Device* button.

Custom data can be written to the device using the *progSequence* and *Write to Device* buttons. The requirements for custom data are as follows:

- Empty lines are ignored.
- Comments must start with the '#' character.
- Registers can be data only, or register name and data. If register name and data, these must be separated by a tab or a single space.
- Field names and data can be specified. If so, these must be separated by a tab or a single space.

3.1.3.2 OTP Configuration

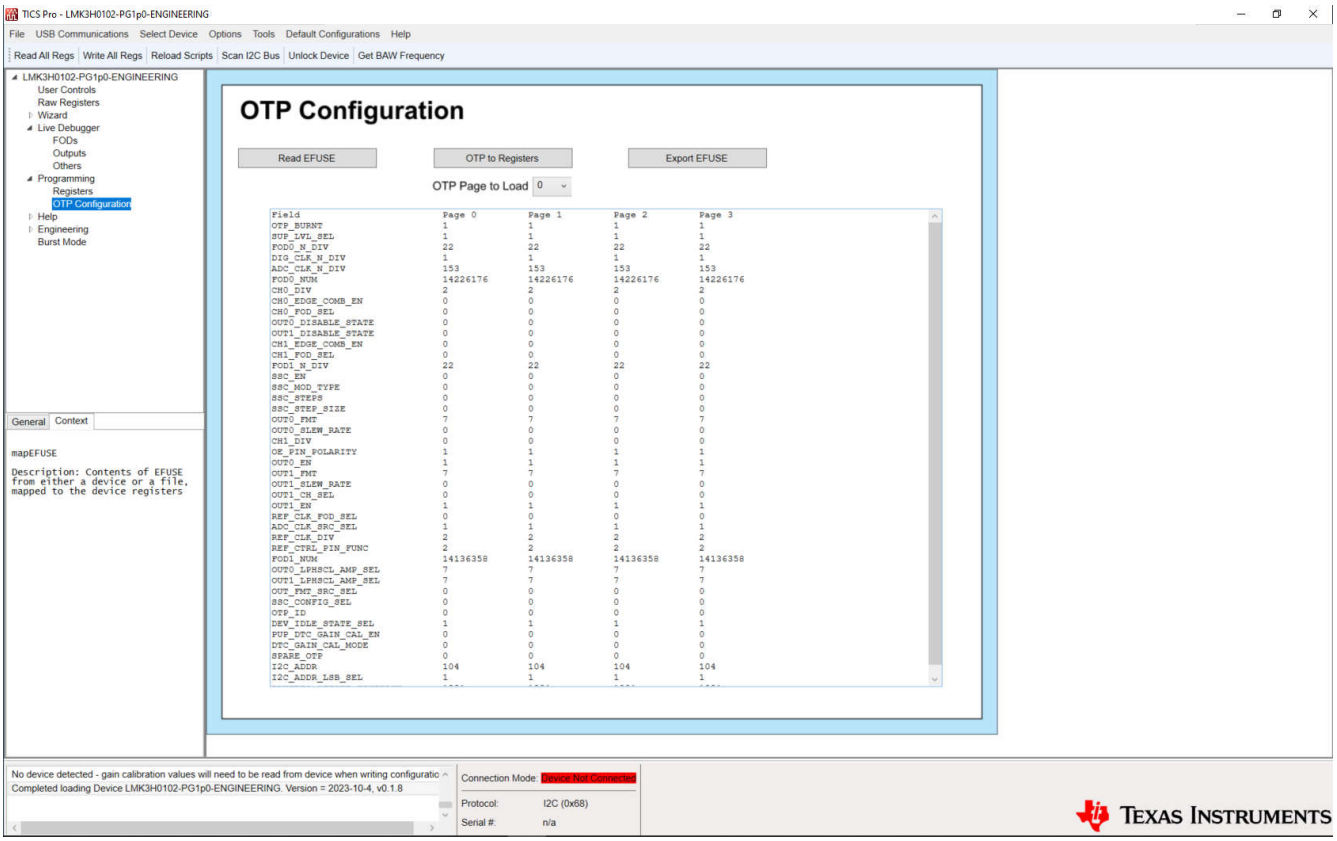
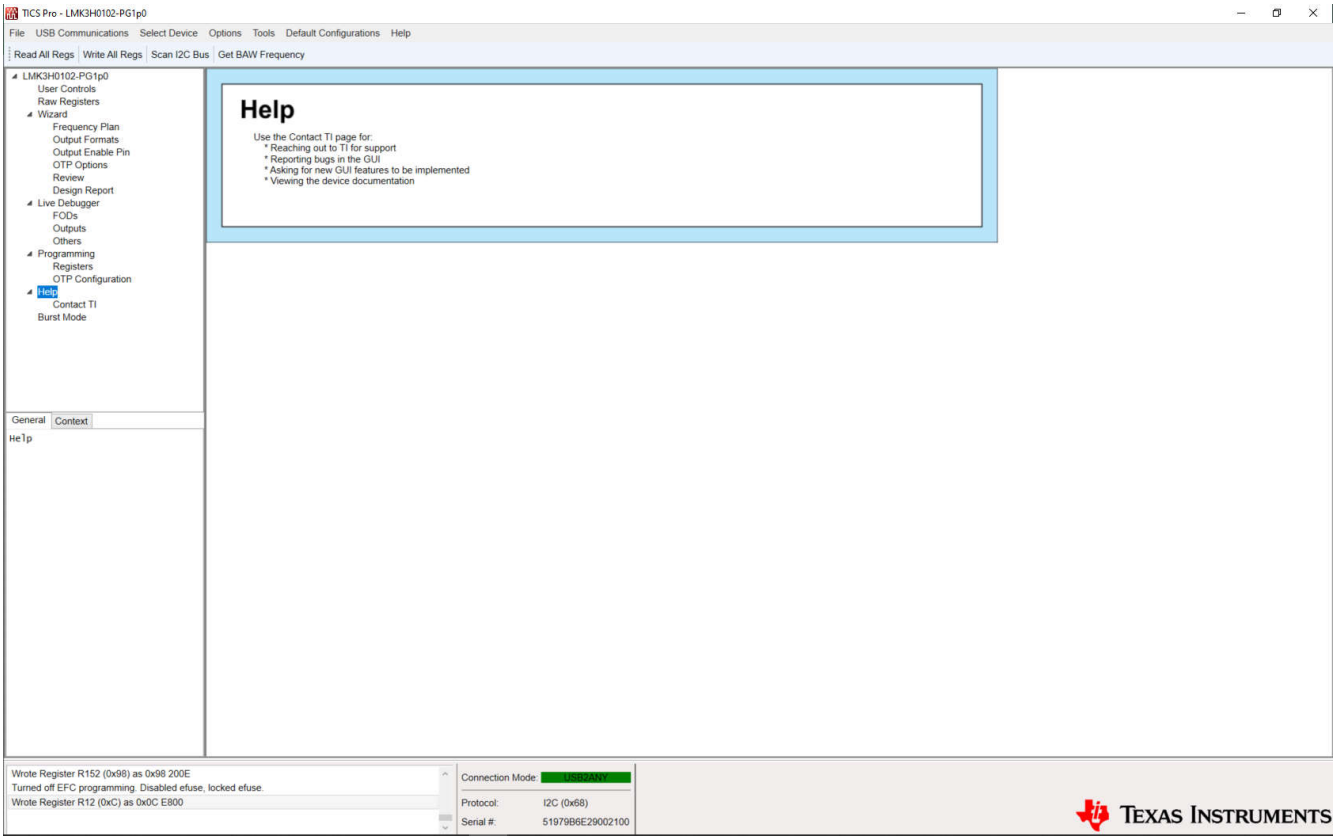


Figure 3-14. LMK3H0102 OTP Configuration Page

The *OTP Configuration* page is used for reading the EFUSE of the device. The *Read EFUSE* button reads the entirety of the EFUSE, and populates the relevant contents to the window below. The *OTP to Registers* button loads an OTP page to the active device registers. The page loaded is selected by the drop-down menu below the *OTP to Registers* button. The *Export EFUSE* button stores the contents of the window to a text file for future referencing, or providing to TI for analysis. Click the *I2C + OTP* button on the *Wizard* page to enable these GUI fields.

3.1.4 Help

Figure 3-15. LMK3H0102 Help Page



The *Help* page serves as a reference for the *Contact TI* page.

3.1.4.1 Contact TI

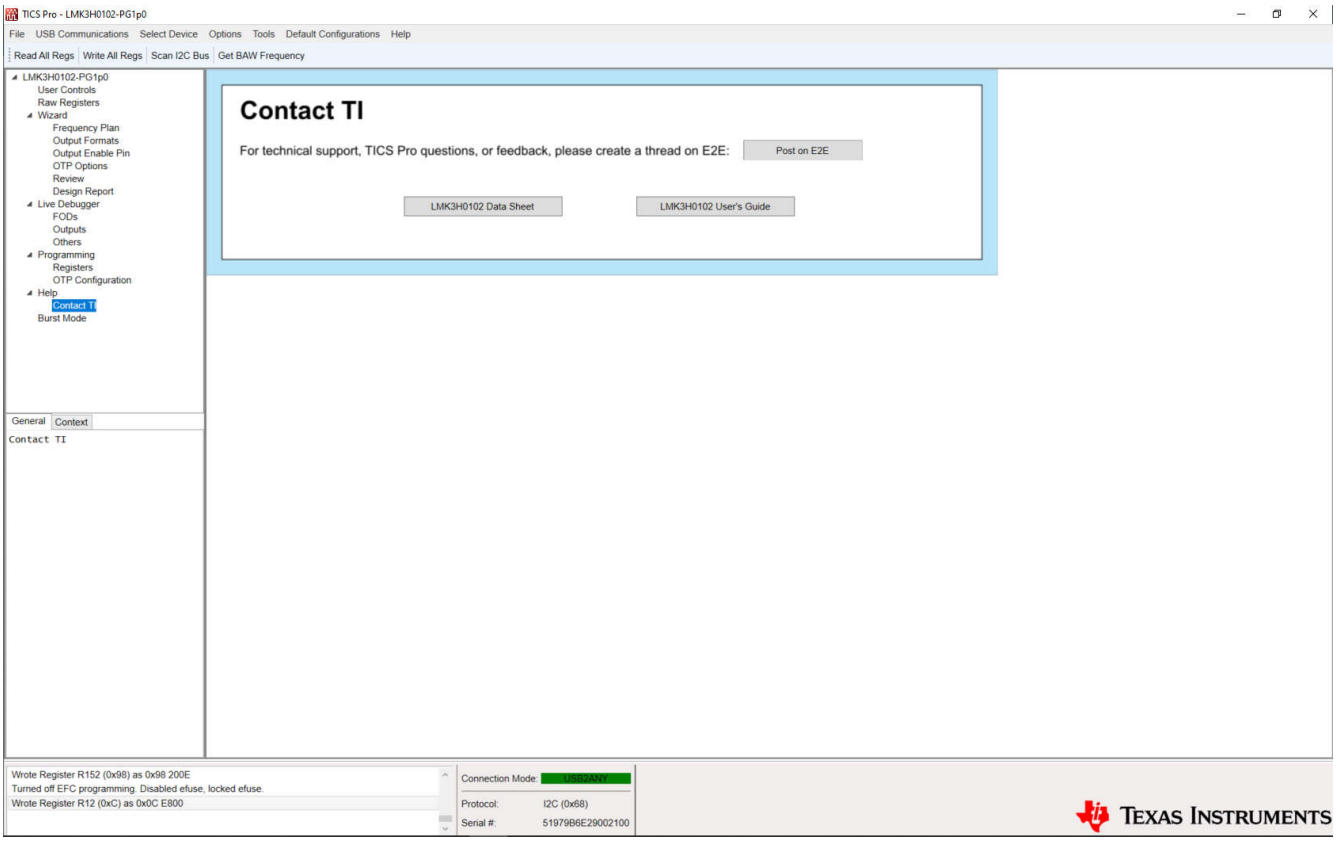


Figure 3-16. LMK3H0102 Contact TI Page

Use the *Contact TI* page for receiving additional support when using the GUI, reporting issues, or referencing the Data Sheet of Users' Guide. The "Post on E2E" page will, if logged in to E2E, open the default browser and navigate to creating a new post on E2E. The remaining two buttons open the *LMK3H0102 Data Sheet* and *LMK3H0102EVM User's Guide* in the default browser.

3.2 Using TI's USB2ANY Module for In-System Programming of the LMK3H0102

When designing in the LMK3H0102 into a system application board, TI recommends to use a dedicated header to access the I2C lines of the device to support external programming from Texas Instruments' USB2ANY module (see Figure 3-17). The USB2ANY module can be very useful to support in-system programming of the initial clock configuration. For example, before the system software/firmware is enabled) and rapid clock prototyping, optimization, and debugging.

Figure 3-17. USB2ANY Module

Since the USB2ANY module implements the same MSP430-based USB-to-I2C interface and firmware as the one integrated on the LMK3H0102EVM, the TICS Pro software can be used to easily program the device in-system.

Once the user's system software and firmware are enabled and can provide reliable configuration of the LMK3H0102, then the provisional I2C header can be removed or superseded in the next iteration of the hardware design.

3.2.1 USB2ANY Board Connections

The USB2ANY has four interface connectors: one USB 2.0 connector (J2) and three I/O connectors (J3, J4, and J5). The USB connector is a standard ‘A’ type mini USB receptacle. The I/O connectors are standard dual-row, 0.1” center, pin headers.

The I/O connectors J3 and J5 are 8-pin type and J4 is a 10-pin type. The I/O connectors are configured such that the I/O connectors accept either individual cable connections or a single 30-pin connection.

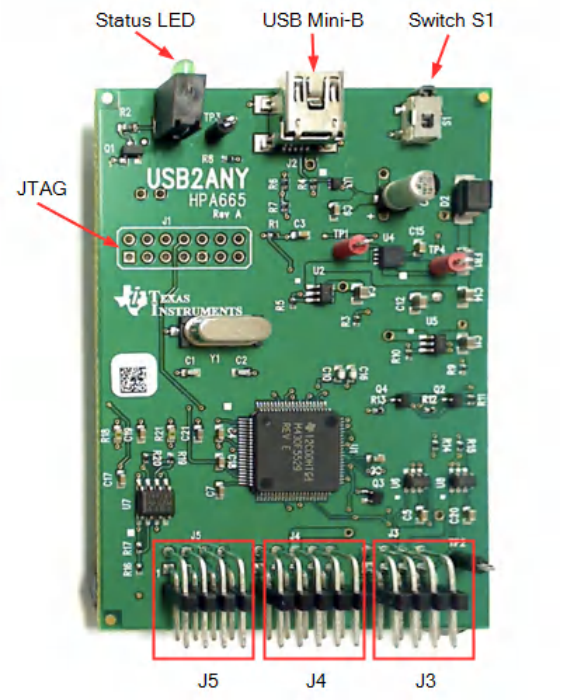


Figure 3-18. USB2ANY Board Connections

The standard USB2ANY Kit (HPA665-001) includes both a 10-pin cable and a 30-pin cable. The 10-pin cable is intended to be connected to J4. J4 provides the SDA, SCL, and GND connections of interest.

Note

J5 and J6 supply other connections that are NOT required and therefore, outside the scope of this document.

When the USB2ANY board is in the enclosure, there is a key notch above J4 that prevents the cable connector from being plugged in upside-down. With the notch at the top, pin 1 of the 10-pin cable connector is located at the upper-right corner.

The 10-pin cable is about 6 inches in length and has a keyed female 10-pin IDC connector on each end. Figure 3-19 shows the connection of the cable to the USB2ANY board (the key must be facing up, away from the board). The opposite end of the cable must be connected to the target board. Figure 3-20 shows the indicator for pin 1, the red stripe on the cable.

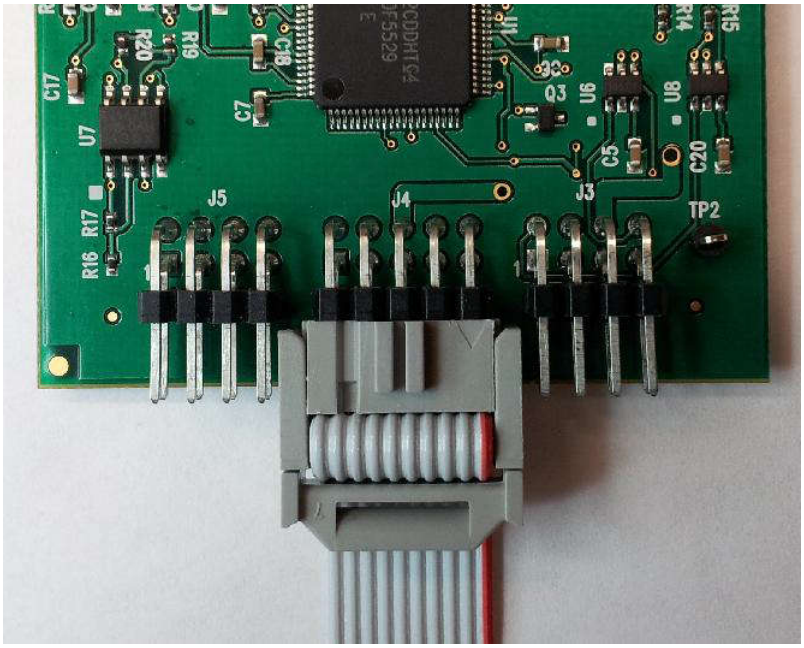


Figure 3-19. 10-pin Cable Connection to J4

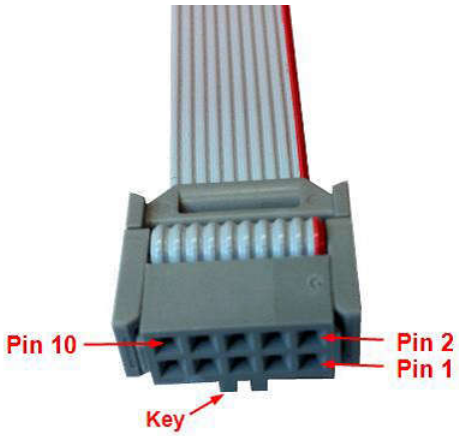


Figure 3-20. 10-pin Cable Pinout

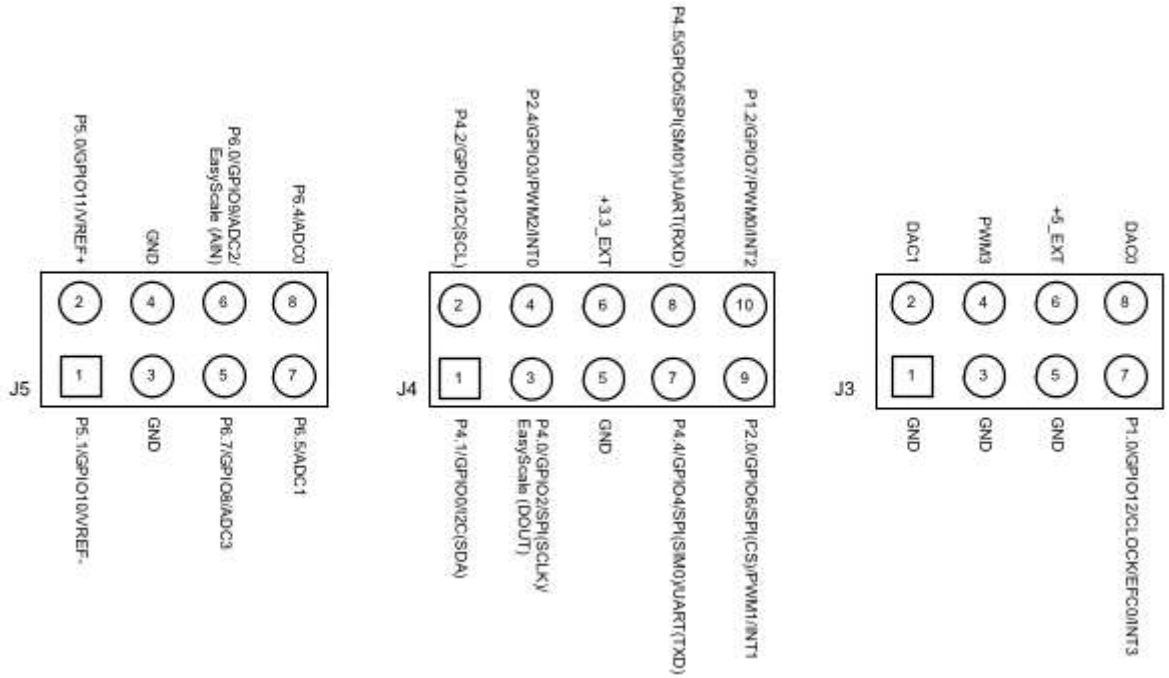


Figure 3-21. USB2ANY Board Connector Pinout Diagram

Table 3-1. USB2ANY Board Connector J4 and 10-pin Cable Pinouts

Pin Name	J4 Pin #	Cable Pin #	Description
P4.1/GPIO0/I2C(SDA)	1	10	I2C Data
P4.2/GPIO1/I2C(SCL)	2	9	I2C Clock
P4.0/GPIO2/SPI(SCLK)	3	8	General-purpose digital I/O (not required)
P2.4/GPIO3	4	7	General-purpose digital I/O (not required)
GND	5	6	Common Ground
+3.3_EXT	6	5	+3.3V output power supply (100 mA limit)
P4.4/GPIO4/SPI(SIM0)	7	4	General-purpose digital I/O (not required)
P4.5/GPIO5/SPI(SM01)	8	3	General-purpose digital I/O (not required)
P2.0/GPIO6/SPI(CS)	9	2	General-purpose digital I/O (not required)
P1.2/GPIO7	10	1	General-purpose digital I/O (not required)

Instead of using the 10-pin header and supplied cable, a board designer can alternatively choose to use a 3-pin *I2C header* on the application board and 3 jumper wires to connect the SDA, SCL, and GND signals from J4 of USB2ANY to the I2C header.

3.2.2 Ordering a USB2ANY Module

To order a USB2ANY module, submit a request to clock_support@list.ti.com with the following information:

1. Request/Reason: 1 USB2ANY module for LMK3H0102 in-system programming/prototyping
2. Company Name
3. Application/End-Equipment
4. LMK3H0102 Est. Annual Volume/Year
5. Ship-To Address

4 Hardware Design Files

4.1 Schematics

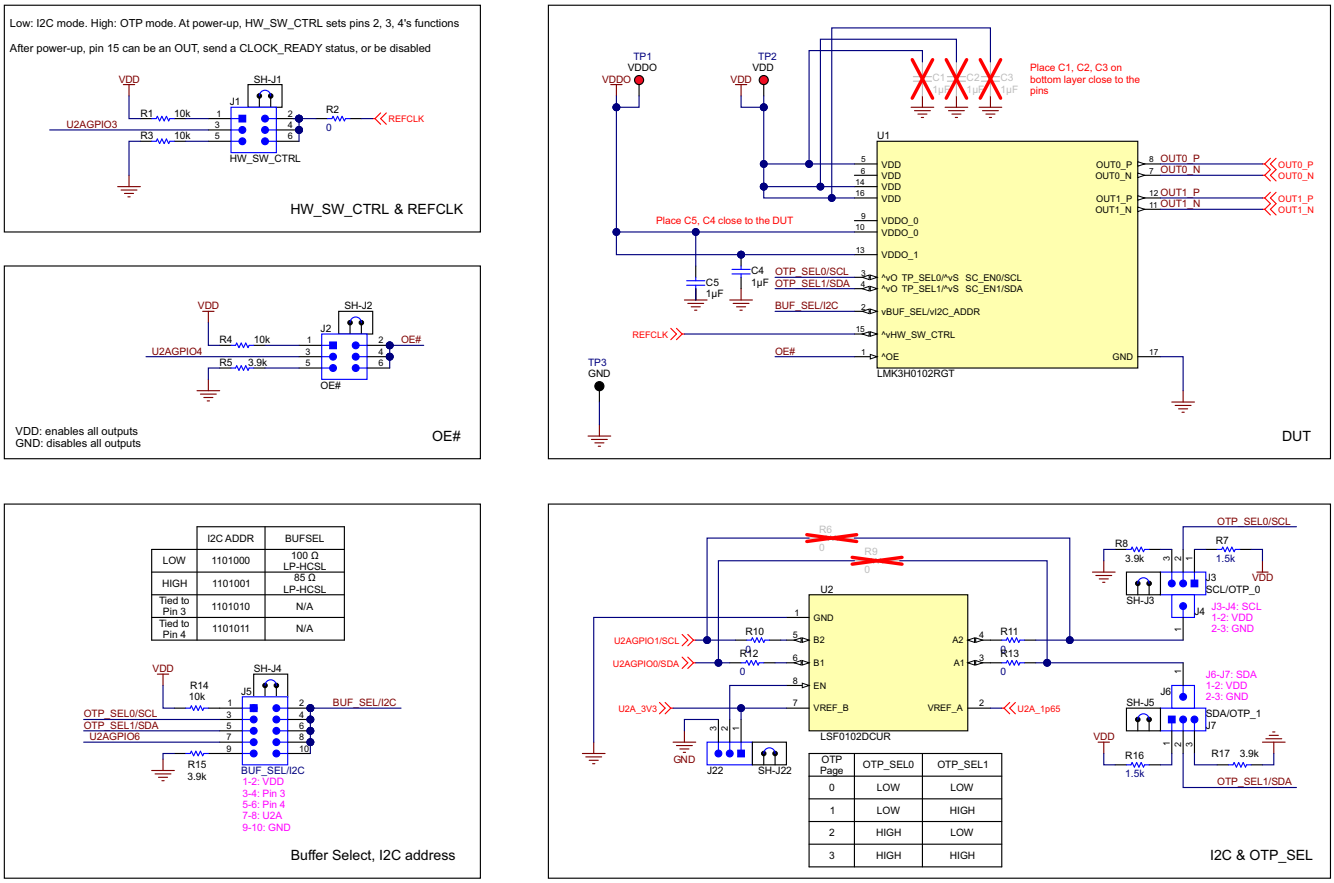


Figure 4-1. LMK3H0102 & Control Pins

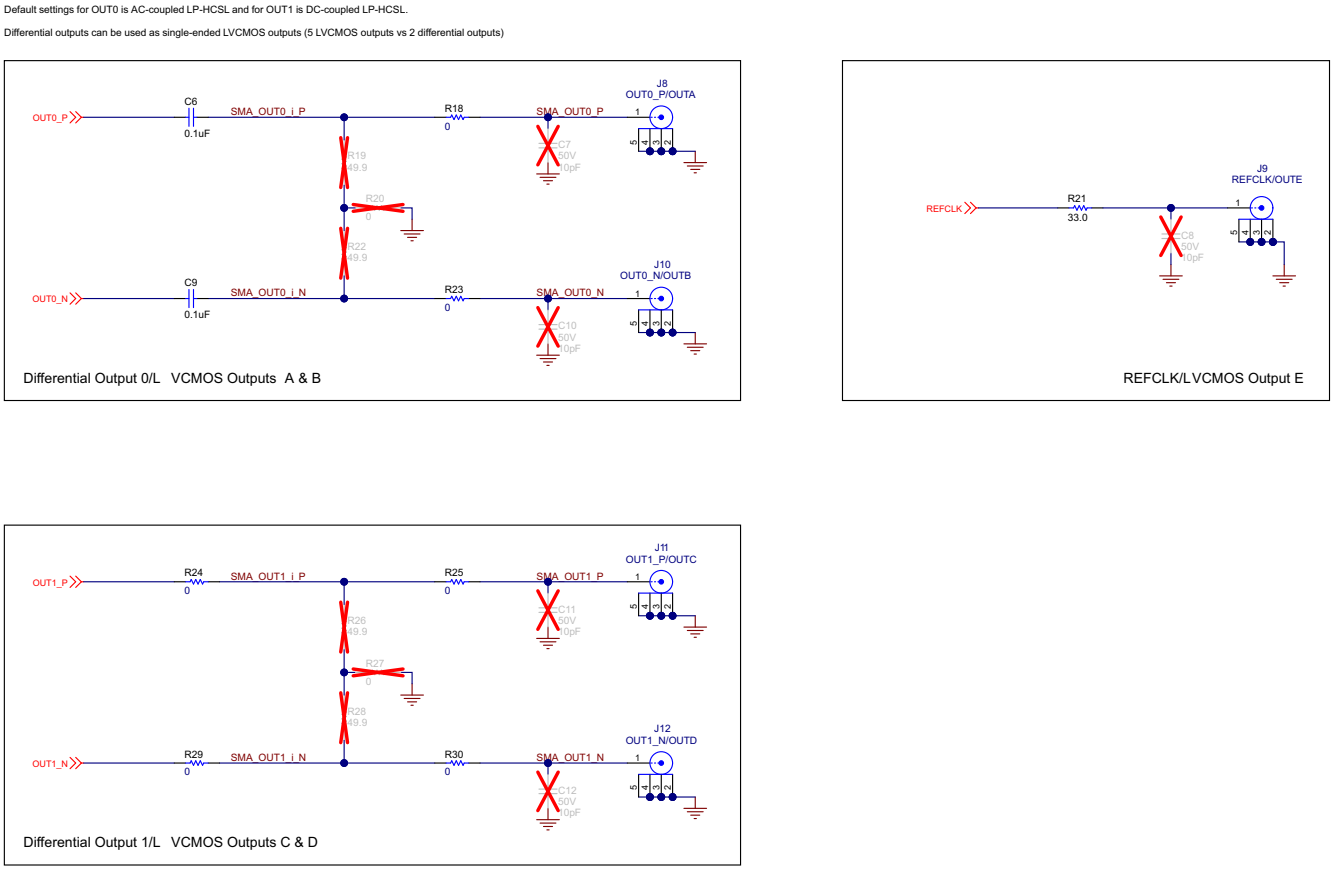


Figure 4-2. Output Connections

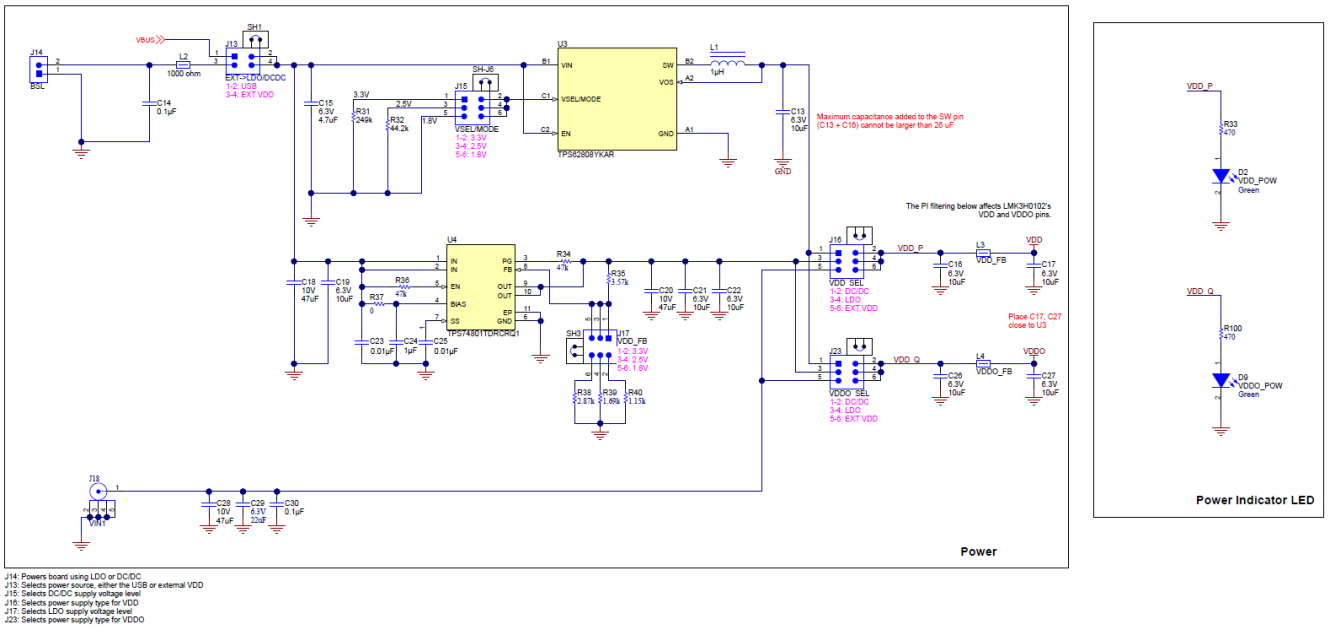


Figure 4-3. Power Connections

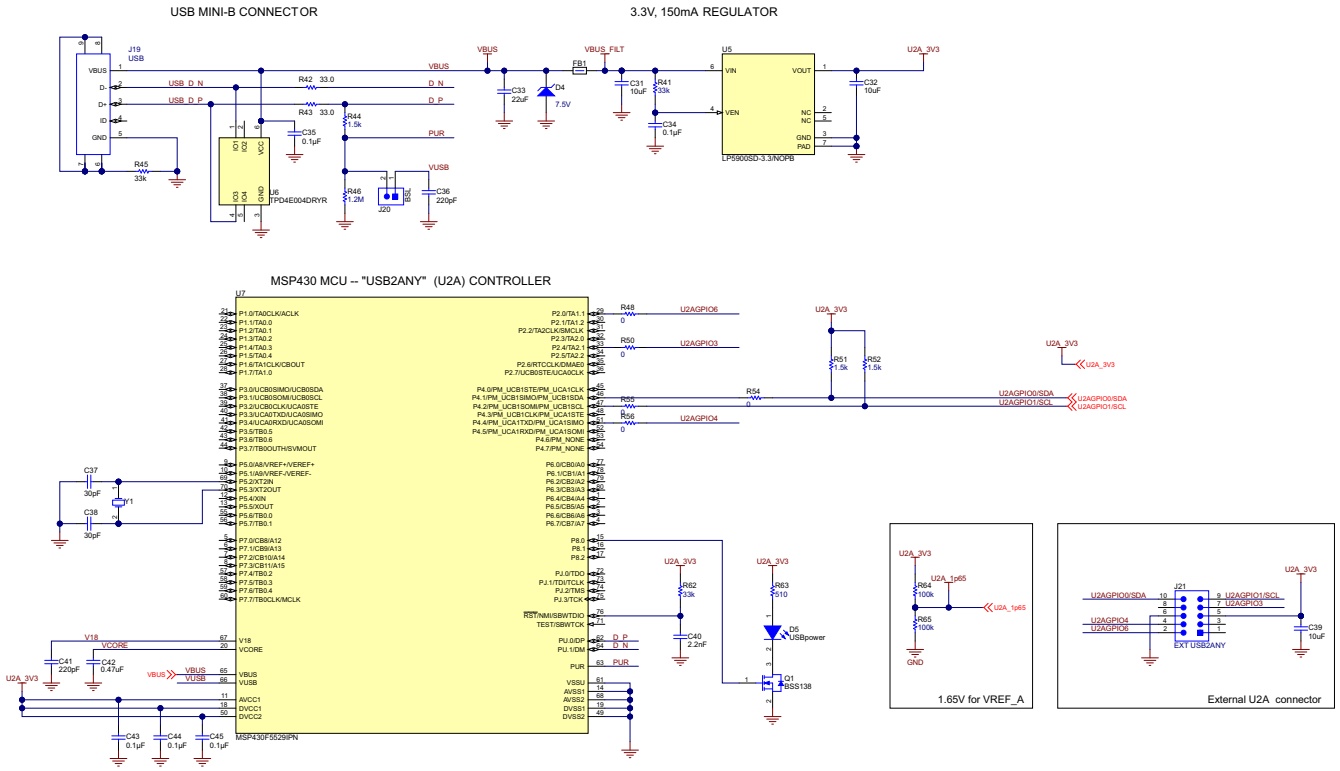


Figure 4-4. USB Connections

4.2 PCB Layout

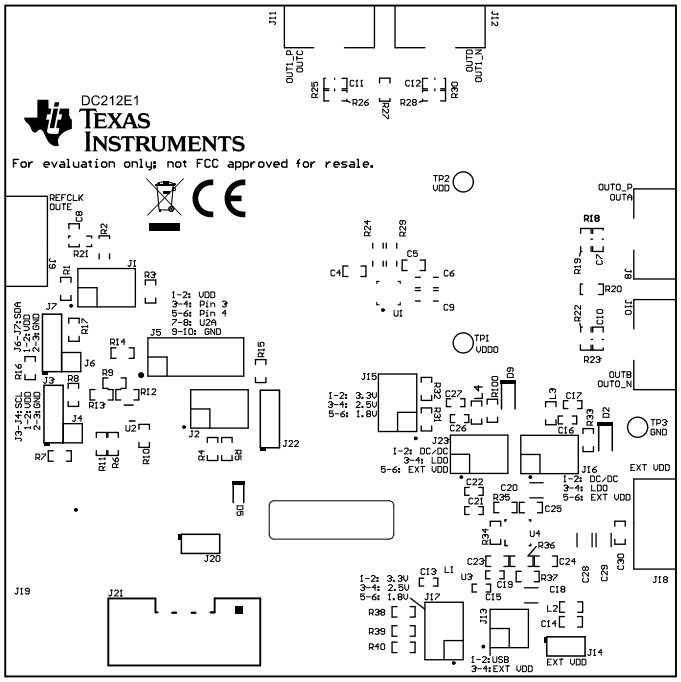


Figure 4-5. Top Overlay

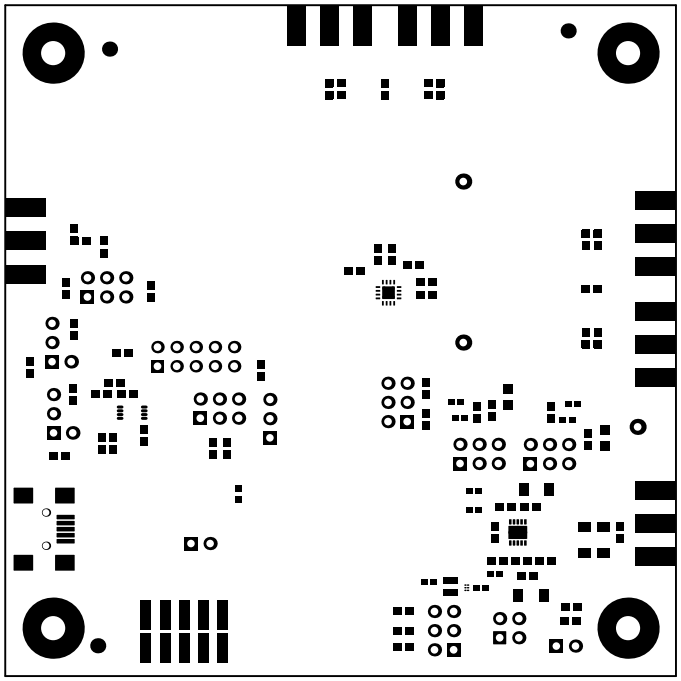


Figure 4-6. Top Solder Mask

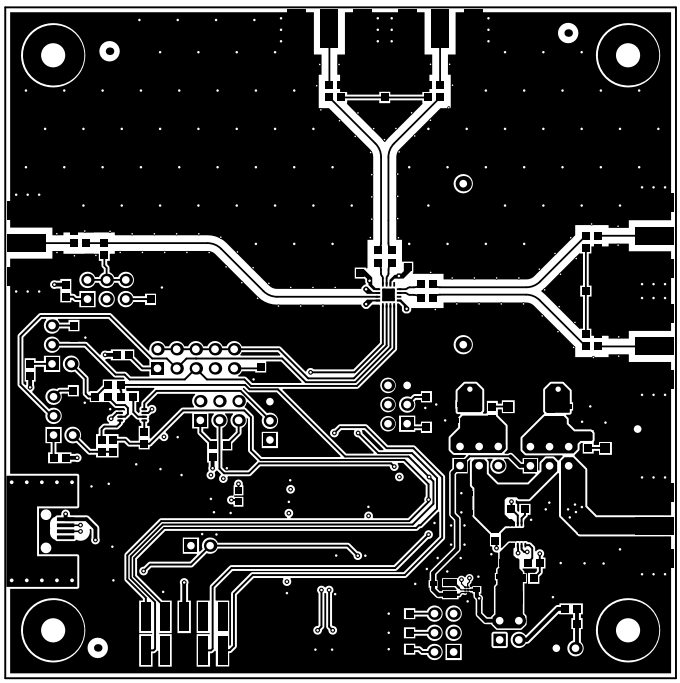


Figure 4-7. Layer 1 (Top Side)

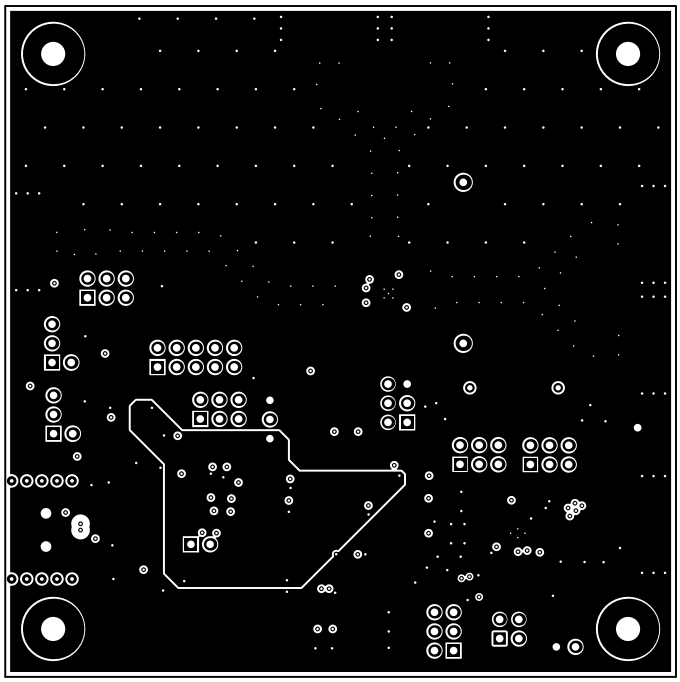


Figure 4-8. Signal Layer 1

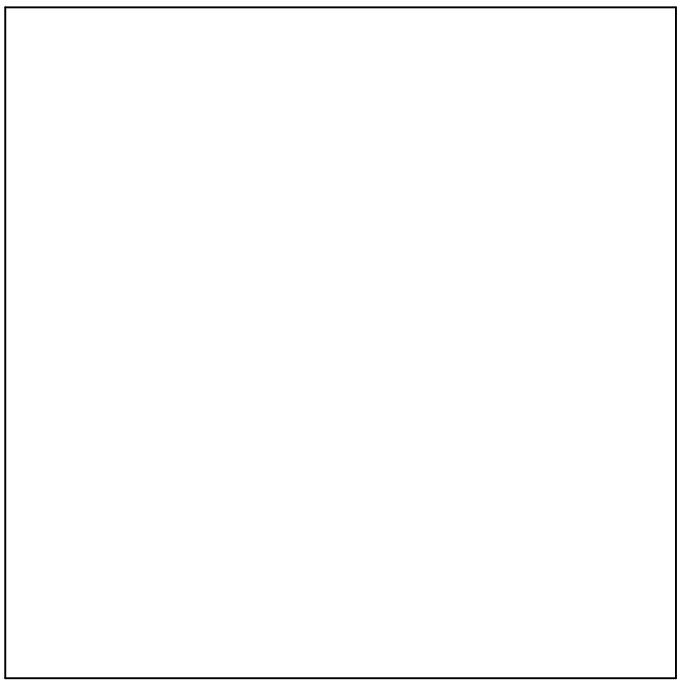


Figure 4-9. Signal Layer 2

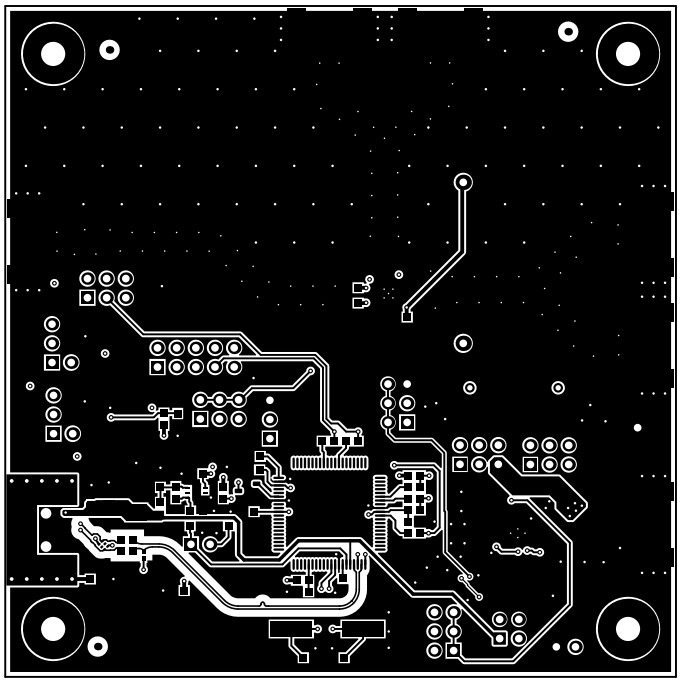


Figure 4-10. Bottom Layer (View from Top)

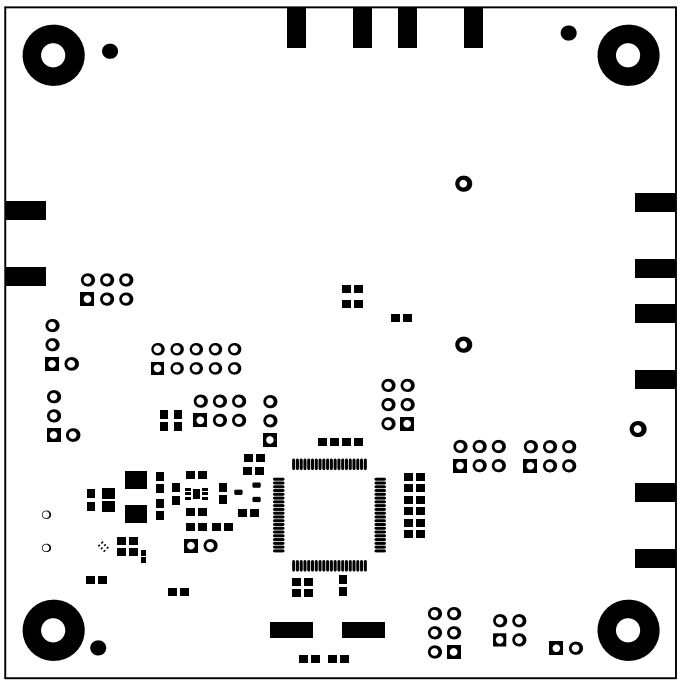


Figure 4-11. Bottom Solder Mask

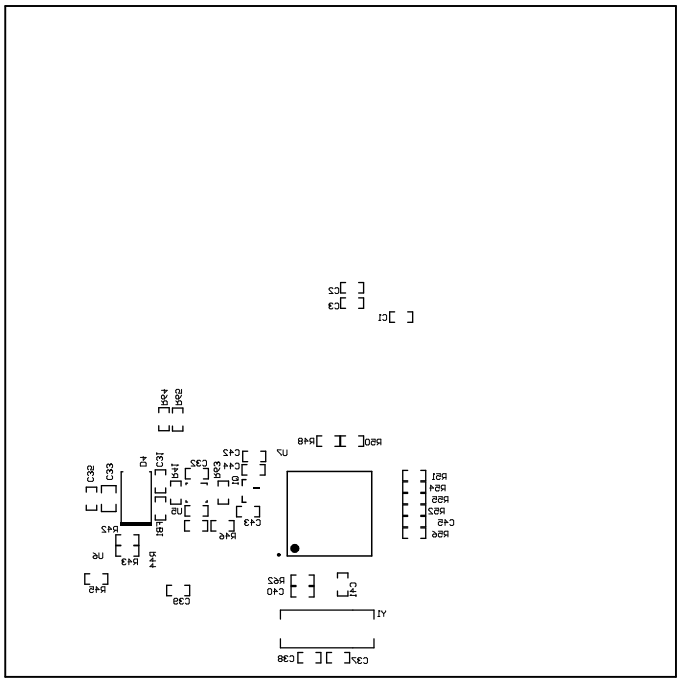
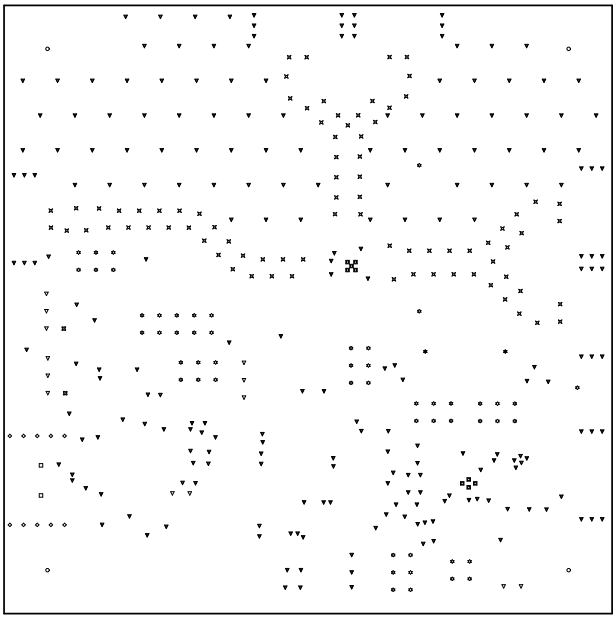


Figure 4-12. Bottom Overlay



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
□	2	35.43mil (0.900mm)	NPTH	Round	Top Layer - Bottom Layer	
▣	9	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
⌑	82	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	
▽	225	13.00mil (0.330mm)	PTH	Round	Top Layer - Bottom Layer	
◇	10	19.69mil (0.500mm)	PTH	Round	Top Layer - Bottom Layer	
✱	2	28.00mil (0.711mm)	PTH	Round	Top Layer - Bottom Layer	
▽	13	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer	
☼	53	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	2	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
○	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	
	402 Total					

Figure 4-13. Drill Drawing

4.3 Bill of Materials

Table 4-1. Bill of Materials

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
C4, C5	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, 0603	TDK	C1608X7R1E105K080AE	2
C6, C9	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	Kemet	C0603C104J4RACTU	2
C13, C16, C17, C19, C21, C22, C26, C27, C46, C47	CAP, CERM, 10 uF, 6.3 V, +/- 20%, X5R, 0402	MuRata	GRM155R60J106ME15D	10
C14, C30, C34, C35, C43, C44, C45	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206046	7
C15	CAP, CERM, 4.7 uF, 6.3 V, +/- 20%, X5R, 0402	MuRata	GRM155R60J475ME47D	1
C18, C20, C28	CAP, CERM, 47 uF, 10 V, +/- 10%, X5R, AEC-Q200 Grade 1, 1206	MuRata	GRT31CR61A476KE13L	3
C23, C25	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206040	2
C24	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206052	1
C29	CAP, CERM, 22 uF, 6.3 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	TDK	CGA5L1X7R0J226M160AC	1
C31, C32, C39	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	TDK	C1608X5R1A106M080AC	3
C33	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	Taiyo Yuden	LMK212BJ226MG-T	1
C36, C41	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	AVX	KGM15ACG1H221FT	2
C37, C38	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C2A300JA01D	2
C40	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206036	1
C42	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603	MuRata	GRM188R71A474KA61D	1
D2, D9	LED, Green, SMD	Lite-On	LTST-C171GKT	2
D4	Diode, Zener, 7.5 V, 550 mW, SMB	ON Semiconductor	1SMB5922BT3G	1
D5	LED, Green, SMD	Lite-On	LTST-C190GKT	1
FB1	Ferrite Bead, 60-Ω @ 100 MHz, 3.5 A, 0603	TDK	MPZ1608S600ATAH0	1
H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	4
HS1, HS2, HS3, HS4	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
J1, J2, J15, J16, J17, J23	Header, 100mil, 3x2, Gold, TH	Samtec	TSW-103-07-G-D	6
J3, J7, J22	Header, 100mil, 3x1, Tin, TH	TE Connectivity	5-146278-3	3
J4, J6	Conn Unshrouded Header HDR 1 POS Solder ST Thru-Hole	Samtec	TSW-101-07-L-S	2
J5	Header, 100mil, 5x2, Tin, TH	Sullins Connector Solutions	PEC05DAAN	1
J8, J9, J10, J11, J12, J18	Connector, End launch SMA, 50-Ω, SMT	Cinch Connectivity	142-0701-851	6
J13	Header, 100mil, 2x2, Gold, TH	Samtec	TSW-102-07-G-D	1
J14, J20, J25	Header, 100mil, 2x1, Tin, TH	TE Connectivity	5-146278-2	3
J19	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2	1

Table 4-1. Bill of Materials (continued)

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
J21	Header (shrouded), 100mil, 5x2, Gold, SMT	FCI	52601-S10-8LF	1
J24, J26	Header, 100mil, 2x2, Tin, TH	Sullins Connector Solutions	PEC02DAAN	2
L1	Inductor, Shielded, Metal Composite, 1 µH, 2.7 A, 0.057-Ω, SMD	MuRata	DFE201610E-1R0M=P2	1
L2	Ferrite Bead, 1000-Ω @ 100 MHz, 0.6 A, 0603	MuRata	BLM18HE102SN1D	1
L3, L4, L5	Ferrite Bead, 750-Ω @ 100 MHz, 0.4 A, 0603	Wurth Elektronik	742792656	3
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
Q1	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	Fairchild Semiconductor	BSS138	1
R1, R3, R4, R14	RES, 10 k, 5%, 0.1 W, 0603	Yageo	RC0603JR-0710KL	4
R2, R10, R11, R12, R13, R18, R23, R24, R25, R29, R30, R37, R48, R50, R54, R55, R56	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3GEY0R00V	17
R5, R8, R15, R17	RES, 3.9 k, 5%, 0.1 W, 0603	Yageo	RC0603JR-073K9L	4
R7, R16, R51, R52	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K50JNEA	4
R21, R42, R43	RES, 33.0, 1%, 0.1 W, 0603	Yageo	RC0603FR-0733RL	3
R31	RES, 249 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603249KFKEA	1
R32	RES, 44.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060344K2FKEA	1
R33, R100	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603470RJNEA	2
R34, R36	RES, 47 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060347K0JNEA	2
R35	RES, 3.57 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06033K57FKEA	1
R38	RES, 2.87 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06032K87FKEA	1
R39	RES, 1.69 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K69FKEA	1
R40	RES, 1.15 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K15FKEA	1
R41, R62	RES, 33 k, 5%, 0.1 W, 0603	Yageo	RC0603JR-0733KL	2
R44	Res Thick Film 0402 1.5-KΩ 5% 1/10W ±200ppm/°C Molded SMD Punched Carrier T/R	Panasonic	ERJ-2GEJ152X	1
R45	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060333K0JNEA	1
R46	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031M20JNEA	1
R63	RES, 510, 5%, 0.1 W, 0603	Yageo	RC0603JR-07510RL	1
R64, R65	RES, 100 k, 0.5%, 0.1 W, 0603	Yageo America	RT0603DRE07100KL	2
SH1, SH2, SH3, SHJ23, SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J22	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G	11
TP1, TP2, TP4	Test Point, Miniature, Red, TH	Keystone Electronics	5000	3
TP3	Test Point, Miniature, Black, TH	Keystone Electronics	5001	1

Table 4-1. Bill of Materials (continued)

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
U1	Dual Output Reference-less PCIe Gen 1 to Gen 6 Clock Generator	Texas Instruments	LMK3H0102RGT	1
U2	Dual Bidirectional Multi-Voltage Level Translator, DCU0008A (VSSOP-8)	Texas Instruments	LSF0102DCUR	1
U3	600-mA, Ultra-Low IQ Step-Down Converter, YKA0006ACAC (DSBGA-6)	Texas Instruments	TPS62808YKAR	1
U4	Single Output LDO, 1.5 A, Adjustable 0.8 to 3.6 V Output, 0.8 to 5.5 V Input, with Programmable Soft Start, 10-pin SON (DRC), -40 to 105 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS74801TDRCRQ1	1
U5	150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	Texas Instruments	LP5900SD-3.3/NOPB	1
U6	4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	Texas Instruments	TPD4E004DRYR	1
U7	25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	Texas Instruments	MSP430F5529IPN	1
Y1	Crystal, 24.000 MHz, 20 pF, SMD	ECS Inc.	ECS-240-20-5PX-TR	1
C1, C2, C3	CAP, CERM, 1 µF, 25 V,+/- 10%, X7R, 0603	MuRata	GRJ188R71E105KE11D	0
C7, C8, C10, C11, C12	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H100JA01D	0
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
R6, R9, R20, R26, R27, R28, R47	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Panasonic	ERJ-3GEY0R00V	0
R19, R22	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100RJNEA	0

5 Additional Information

Trademarks

All trademarks are the property of their respective owners.

6 Related Documentation

For more information about the LMK3H0102 device, refer to the *LMK3H0102 Dual Output Reference-less PCIe Gen 1 to Gen 6 Clock Generator* data sheet.

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