DS90UR907Q-EVK
FPD-Link to FPD-Link II Converter
Evaluation Kit

Rev 0.1
April, 2010

General Description

The DS90UR907Q-EVK converts FPD-link to FPD-Link II. It translates four LVDS data/control streams and one LVDS clock pair into a high-speed serialized interface over a single pair. It is backward compatible for operation with older generation deserializer devices.

The DS90UR907Q-EVK board has a space saving 20-position wall header as the FPD-Link input, and a Rosenberger Automotive HSD Connector as the output. USB or SMA connectors can also be configured as the output, based on the type of the cable to be used.

Features

- 5 – 65 MHz support (140 Mbps to 1.82 Gbps Serial Link)
- 5-channel (4 data + 1 clock) FPD-Link receiver inputs
- AC Coupled STP Interconnect up to 10 meters in length
- Integrated output termination
- @ Speed link BIST Mode and reporting pin
- Optional I2C compatible Serial Control Bus
- RGB888 + VS, HS, DE serialized to 1 pair
- Power down Mode minimizes power dissipation
- Randomizer/Scrambler – DC-balanced data stream
- Low EMI FPD-Link input
- Selectable output VOD and adjustable de-emphasis
- 1.8V or 3.3V compatible control bus interface
- Automotive grade product: AEC-Q100 Grade 2 qualified
- >8 kV HBM and ISO 10605 ESD rating
- Backward compatible mode for operation with older generation devices

Applications

- Automotive Displays for Navigation
- Automotive Display for Entertainment

Ordering Information

PART: DS90UR907QSQ
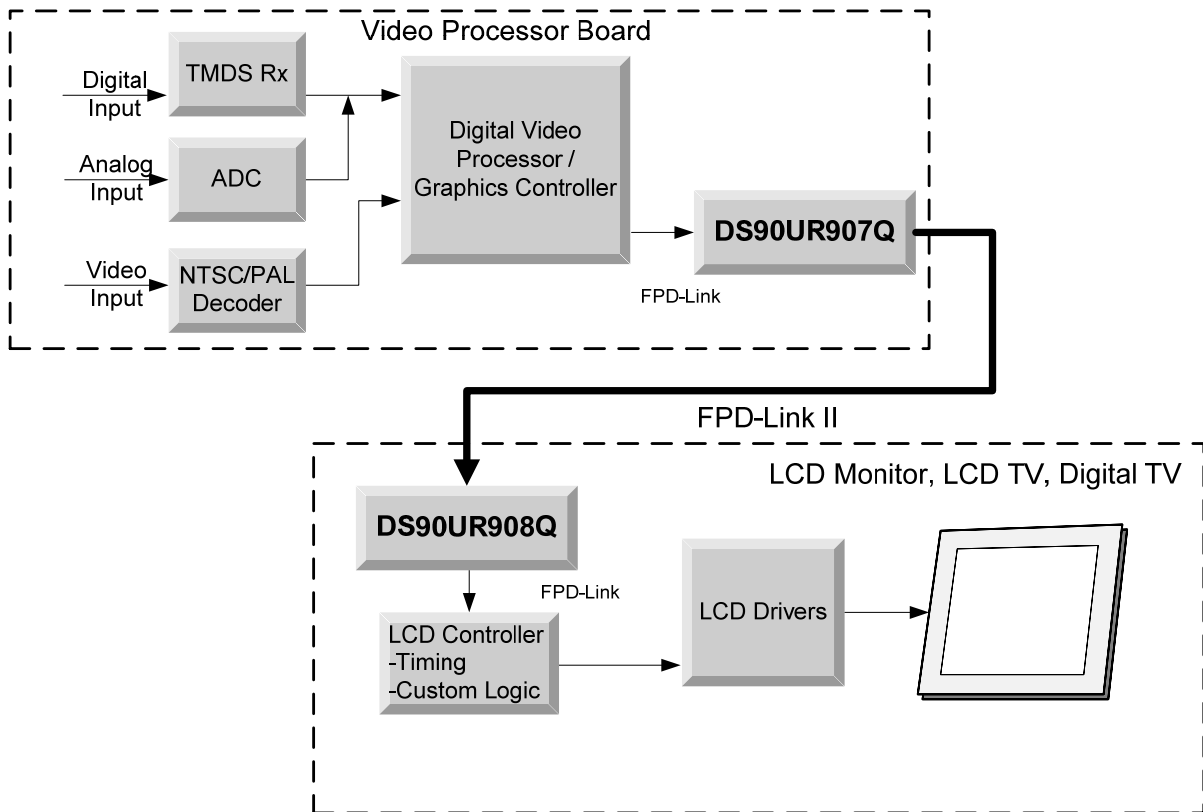**Demo board:** DS90UR907Q-EVK

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Typical Configuration

Quick Start Guide:

1. Connect 3.3V DC power and ground of the board to the JP1 from the power supply. Connect 1.8V DC power and ground of the board to the J3 and J4 from the power supply.
2. Attach an applicable cable (not supplied) to this TX board (DS90UR907Q) output to an RX board (DS90UR908Q) input.
3. From the Video Decoder board, connect a flat cable (not supplied) to this TX board and connect another flat cable (not supplied) from the RX board to the panel.
4. Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the board. See text on Configuration Settings and datasheet for more details.
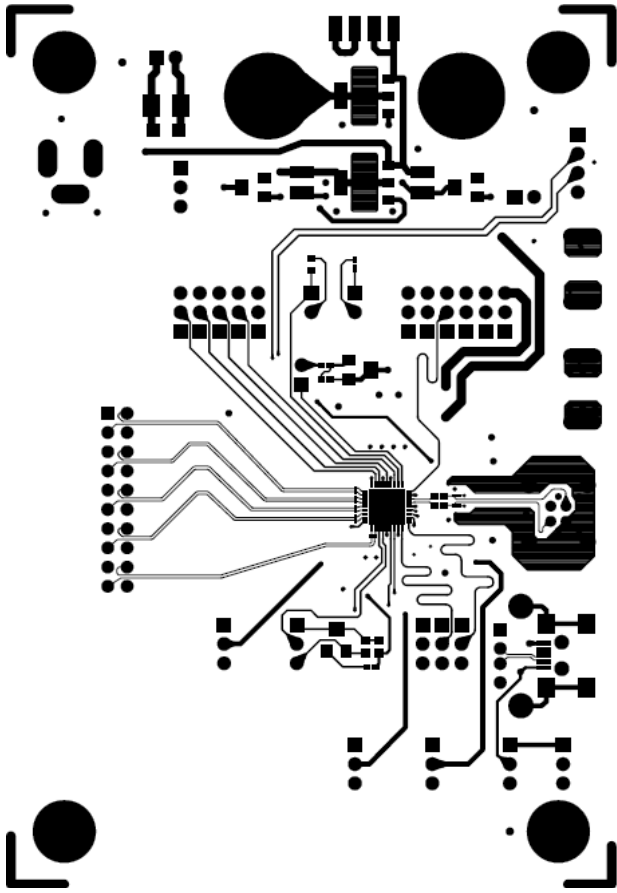
Configuration Settings

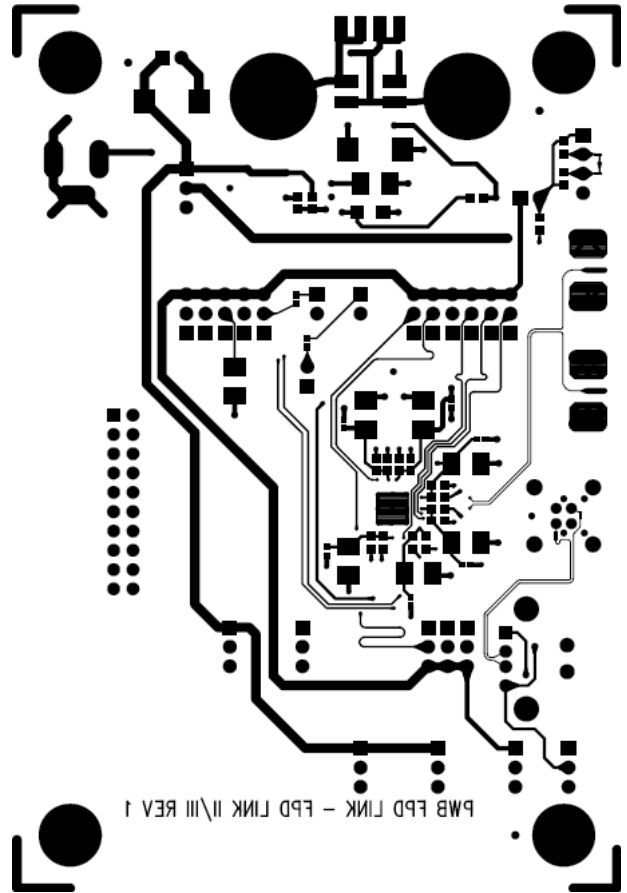| Component	Name	Function
Power Connections		
J3	1.8V DC	1.8V VDD Power.
JP1	3.3V DC	3.3V VDD Power.
J4	VSS	Ground.
JP2	VDDI	Always connect to 3.3V.
JP18	VDDL	Always connect to 1.8V.
JP23	VDDP	Always connect to 1.8V.
JP24	VDDHS	Always connect to 1.8V.
Input and Output Connections		
J1	20 position wall header	Connect to FPD-Link input.
P1	Automotive HSD Connector	Connect to FPD-Link II output (default).
J7 and J8	SMA Connectors	Connect to FPD-Link II output. (When using these connectors, R8 and R9 should be placed with 0Ω resistors, the traces from R8 and R9 to the P1 should be cut).
P3	USB Connector	Connect to FPD-Link II output. (When using this connector, P1 should be removed, and R26 and R27 should be placed with 0Ω resistors).
JP25 and JP26	Power Wire in USB cable through P3	Connect to VSS is recommended.
Control Connections		
JP4	MAPSEL	Connect it to "L" or "H" for the FPD Link mapping select. See datasheet for detail information.
JP5	TESTEN	NSC test mode. Always connect it to "L" or leave it unconnected.
JP6	PDB	Connect it to "L" for the power down mode. Connect it to "H" for the enable mode. See datasheet for detail information.
JP7	BISTEN	Connect it to "H" for the BIST enable mode. See datasheet for detail information.
JP8	VODSEL	Connect it to "L" or "H" for the FPD-Link II VOD level select. See datasheet for detail information.
JP21 and JP22	CONFIG	Configuration select. See datasheet for detail information.
JP17 and VR3	DEEMPH	Leave JP17 unconnected to disable the FPD-Link II output de-emphasis feature. Connect JP17, Adjust VR3 value to select de-emphasis level.
JP19 and VR4	ID[x]	Connect JP19 to VSS to have the default device PHY address (h'EC). Connect JP19 to VR4; then adjust VR4 value to select desired device PHY address. See datasheet for detail information.
JP3 and J6	I2C Interface	Connect JP3 if the I2C power is not supplied on J6. Otherwise, leave it unconnected.

Bill of Material

Item	Quantity	Reference	Comments	Digi-key P/N	Part number
1	2	C1,C13	CAPACITOR TANT 2.2UF 20V 10% SMD	399-3714-1-ND	T491B225K020AT
2	2	C2,C14	CAP .10UF 50V CERAMIC X7R 1206	399-1249-1-ND	C1206C104K5RACTU
3	4	C3,C4,C7,C8	CAP TANTALUM 10UF 16V 20% SMD. Optional.	493-2365-1-ND	F931C106MBA_open
4	2	C5,C6	CAP CERAMIC .1UF25V X5R 0402	445-4964-1-ND	C1005X5R1E104K
5	2	C9,C12	CAP TANTALUM 22UF 25V 20% SMD	493-2391-1-ND	F931E226MNC
6	2	C10,C11	CAP CERAMIC 5.0PF 25V NP0 0201	PCC2107CT-ND	ECJ-ZEC1E050C
7	7	C15,C20,C23,C24,C27,C30, C32	CAP .1UF ±10% 25V CERAMIC X7R 0603	PCC2277CT-ND	ECJ-1VB1E104K
8	7	C16,C17,C18,C19,C28,C33, C34	CAPACITOR TANT 22UF 16V 20% SMD	399-3835-1-ND	T494B226M016AT
9	6	C21,C22,C25,C26,C29,C31	CAP CERAMIC .01UF 100V X7R 0603	399-3189-1-ND	C0603C103K1RACTU
10	3	JP1,JP3,JP17	CONN HEADER VERT .100 2POS 30AU	A26542-ND	87220-2
11	14	JP2,JP4,JP5,JP6,JP7,JP8, JP18,JP19,JP21,JP22,JP23, JP24,JP25,JP26	CONN HEADER VERT .100 3POS 15AU	A26545-ND	87224-3
12	1	J1	CONN HEADER 20 POS STRGHT GOLD.	MHC20K-ND	N2520-6002RB
13	1	J2	CONN POWER JACK 2.1MM. Optional.	CP-002A-ND_open	PJ-002A_open
14	2	J3,J4	BANANA-female (non-insulated)	J147-ND	108-0740-001
15	1	J5	CONN HDR DUAL 8POS .100 SRT AU. Optional.	WM26808-ND	10-89-7082_open
16	1	J6	CONN HEADER 4POS .100 VERT GOLD End Launch Jack Receptacle - Tab Contact.	WM2702-ND	22-11-2042
17	2	J7,J8	Optional.	J658-ND_open	142-0701-851_open
18	1	P1	Automotive HSD Conn - Right Angle Plug Optional.		D4S20B-40ML5-Y_open
19	1	P2	CONN RECEPT MINI USB2.0 5POS. Optional.	H2959CT-ND	UX60-MB-5ST_open
20	1	P3	CONN USB RECEPT R/A TYPE A 4POS.	A31726-ND	292303-1
21	1	R1	RES 1.50K OHM 1/16W 1% 0402 SMD	P1.50KLCT-ND	ERJ-2RKF1501X
22	2	R2,R12	RES ZERO OHM 1/16W 5% 0402 SMD. Optional.	P0.0JTR-ND_open	ERJ-2GEJ0R00X_open
23	5	R3,R4,R5,R6,R7	RES 100 OHM 0201 SMD. 1/20W .5%	RR03P100DCT-ND	RR0306P-101-D
24	2	R8,R9	RES 0 OHM 0201 SMD. Optional.	P0.0AGCT-ND	ERJ-1GE0R00C
25	1	R10	RES 100K OHM 1/10W 1% 0603 SMD. Optional.	P100KHCT-ND_open	ERJ-3EKF1003V_open
26	1	R11	RES 10.0K OHM 1/10W 1% 0603 SMD	P10.0KHCT-ND	ERJ-3EKF1002V
27	2	R13,R14	RES 4.7K OHM 1/10W 5% 0603 SMD	P4.7KGCT-ND	ERJ-3GEYJ472V
28	2	R15,R16	RES 82.5 OHM 1/10W 1% 0603 SMD. Optional.	P82.5HCT-ND	ERJ-3EKF82R5V_open
29	1	R17	RES 100 OHM 1/10W 1% 0603 SMD. Optional.	P100HCT-ND	ERJ-3EKF1000V_open
30	7	R18,R20,R21,R22,R23,R24, R25	RES ZERO OHM 1/16W 5% 0402 SMD	P0.0JTR-ND	ERJ-2GEJ0R00X
31	2	R26,R27	RES 0.0 OHM 1/20W 5% 0201 SMD	P0.0AGCT-ND	ERJ-1GE0R00C
32	1	U1	DO NOT PURCHASE, National will supply.		DS90UR907
33	2	U2,U3	IC REG ADJ 800MA LDO SOT-223.	LM1117IMP-ADJ/NOPB	LM1117IMP-ADJ/NOPB_open
34	2	VR1,VR2	TRIMPOT 100 OHM 4MM TOP ADJ SMD.	3214W-101ETR-ND	3214W-1-101E_open
35	1	VR3	11-Turn Trimming Potentiometer; Top Adjust	3224W-203ECT-ND	3224W-1-203E
36	1	VR4	11-Turn Trimming Potentiometer; Top Adjust	3224W-1-104ECT-ND	3224W-1-104E

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Schematics

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Document Number: DS90UR907 Tx Demo Board

Date: Friday, August 07, 2009

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Rev B
Size B

OPTIONAL External 3.3V input

VDD3.3V

JP1

C9 22uF
C1 2.2uF
C2 0.1uF

VSS

VDDIO=3.3V (external)
VDDIO=VDD (1.8V)

JP2

VDD3.3V
VDDI
VDD

VDDI

R20 0 Ohm/0402

VDDIO >> VDDIO

C17 22uF Place near pin 22 of U1
C20 0.1uF
C21 0.01uF

VSS

VDDL=3.3V (external)
VDDL=VDD (1.8V)

JP18

VDD3.3V
VDDLc
VDD

VDDLc

R23 0 Ohm/0402

VDDL >> VDDL

C33 22uF Place near pin 5 of U1
C32 0.1uF
C31 0.01uF

VSS

VDDHS=3.3V (external)
VDDHS=VDD (1.8V)

JP24

VDD3.3V
VDDHSc
VDD

VDDHSc

R24 0 Ohm/0402

VDDHS >> VDDHS

C28 22uF Place near pin 14 of U1
C27 0.1uF
C26 0.01uF

VSS

VDD >> VDDTX

R22 0 Ohm/0402

VDD

C19 22uF Place near pin 17 of U1
C24 0.1uF
C25 0.01uF

VSS

VDDRX >> VDDRX

R21 0 Ohm/0402

VDD

C18 22uF Place near pin 24 of U1
C23 0.1uF
C22 0.01uF

VSS

VDDIO=1.2V (external)
VDDL=VDD (1.8V)

JP23

VDD3.3V
VDDPc
VDD

VDDPc

R25 0 Ohm/0402

VDDP >> VDDP

C34 22uF Place near pin 11 of U1
C30 0.1uF
C29 0.01uF

VSS

DIRECT
1.8V INPUT
POWER
CONNECTOR

J3
BANANA
J4
BANANA

VDD >> VDD

C12 22uF
C13 2.2uF
C14 0.1uF

VSS

iiiWARNINGiii
Input power thru J2 OR J3 OR J4
ONLYii
Input power thru only one connector!!

SVR100_open
VSS
VR2

OPTIONAL
5V to 1.8V
INPUT POWER
REGULATOR

LM1117IMP-ADJ/SOT223_open

U2
INPUT Tab/Vout OUTPUT
ADJ/GND

R15 825ohm_open

1.8V

C7 10uF_open
C8 10uF_open

VSS

OPTIONAL
5V to 3.3V
INPUT POWER
REGULATOR

VDD3.3V
VR1
SVR100_open
VSS

R17 100ohm_open

LM1117IMP-ADJ/SOT223_open

U3
INPUT Tab/Vout OUTPUT
ADJ/GND

R16 825ohm_open

3.3V

C3 10uF_open
C4 10uF_open

VSS

J5
2x4 pin jumper_open

VSS

J2
CONN JACK PWR_open

OPTIONAL
5V INPUT POWER
CONNECTOR

VSS

FEATURES/OPTIONS ON THE DEMO BOARD:
- R33, R34, R37, R38, R39 series 0402 size pads
  1) Provided for easy separation of each VDD domain (not a user requirement).
     This will allow individual IDD current measurements. (Loaded with 0 ohm resistors)
  2) This also allows insertion of series inductor in each VDD domain (not a user requirement),
     for noise reduction experimentation.
- C13-C27 decoupling capacitors 0603 and B size pads
  1) It is not a requirement that the user must have all these capacitors and power separations in the user layout.
     The extra capacitors and power separations are provided for ease of experimentation.
     It is easier to un-populate than to add capacitors and pads after the fact.
  2) See "Typical Connection Diagram Tx - User Reference" for recommended minimum power grouping and decoupling.

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POWERWISE

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Reference Layout

Top Layer

Bottom Layer

IMPORTANT NOTICE