LMK00101 User's Guide

This user guide describes how to set up and operate the LMK00101 evaluation board kit (EVK). The LMK00101 is a high performance, low noise, low voltage CMOS fanout buffer. The core voltage can be 2.5 or 3.3 volts, while the power supply for the outputs can be selected from: 1.5 V, 1.8 V, 2.5 V, or 3.3 V, provided that it does not exceed the core supply voltage .

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Trademarks

1 Introduction

This user guide describes how to set up and operate the LMK00101 evaluation board kit (EVK). The LMK00101 is a high performance, low noise, low voltage CMOS fanout buffer. The core voltage can be 2.5 or 3.3 volts, while the power supply for the outputs can be selected from: 1.5 V, 1.8 V, 2.5 V, or 3.3 V, provided that it does not exceed the core supply voltage .

Table 1. Part Description

BUFFER	IC	PACKAGE
U1	LMK00101	LLP-32

2 Quick Start

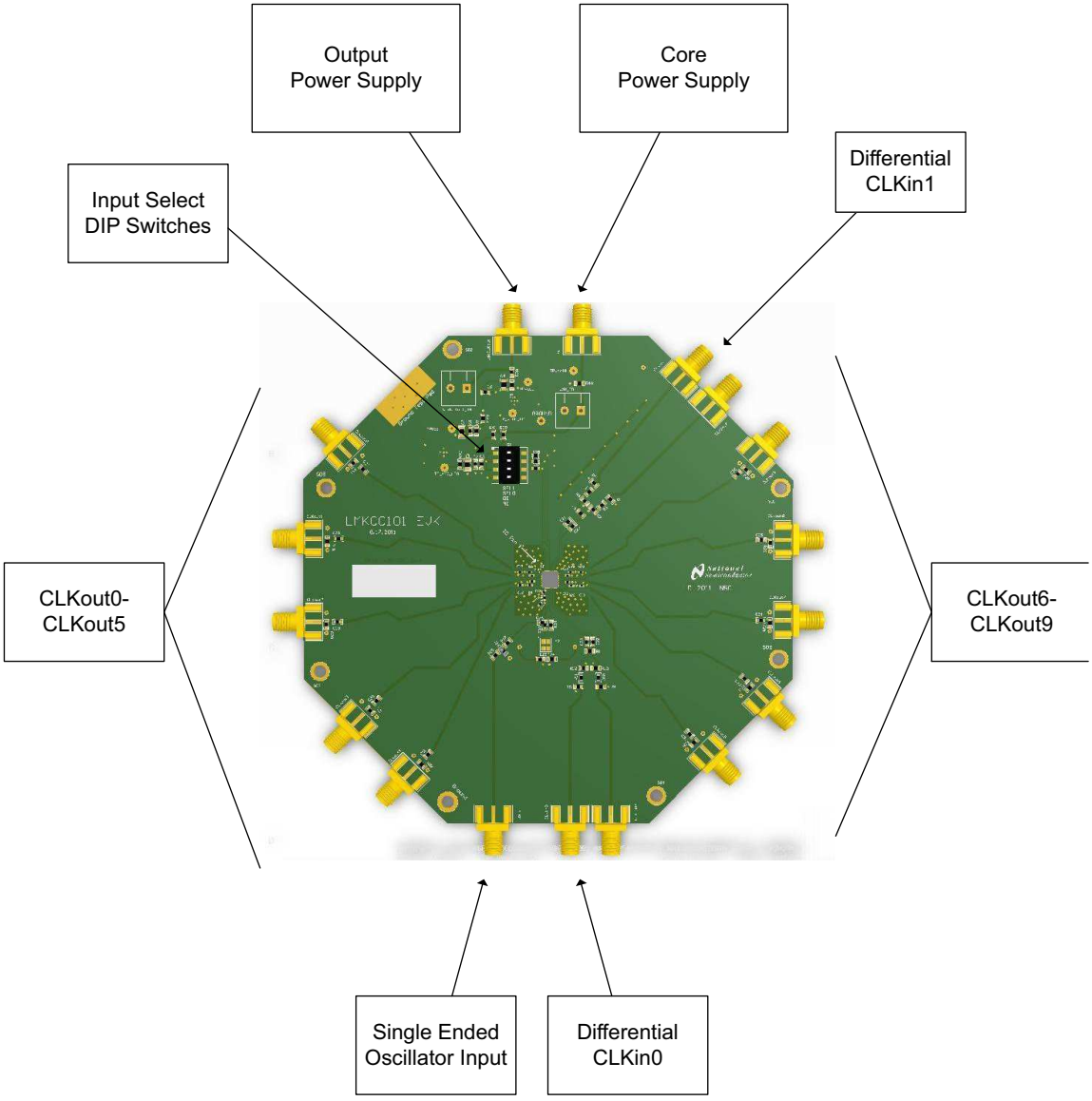

Figure 1. LMK00101 Quick Start Setup

2.1 Quick Start Description

The LMK00101 EVK allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1.

1. Verify the output mode control switches, S1[1:4], match the states shown in Table 2 to reflect the default output clock interfaces configured on the EVK.

Table 2. Default Clock Output Modes / Interfaces

SW POSITION/NAME	SW STATE
S1[1] / SEL1	0 (OFF)
S1[2] / SEL0	1 (ON)
S1[3] / OE	1 (OFF)
S1[4] / NC	Unused

2. Connect the Vdd SMA from the board to a 3.3 V source. This powers the non-output portions of the LMK00101.
3. Connect the Vdd CLKout SMA from the board to a 3.3 V source. This powers the output drivers of the LMK00101.
4. Set the desired clock input using the input selection control switches, S1[1:2], per Table 3. A differential clock source can be connected to SMAs **CLKin0/0*** or **CLKin1/1***.

   Note: CLKin0/0 and CLKin1/1* paths are configured by default to receive a differential clock as the input. The SMA inputs are DC coupled to the device inputs and terminated with 100 Ω differential. Refer to the Clock Inputs section to configure the EVK for a single-ended input.*

Table 3. Input Selection (0=SW OFF, 1=SW ON)

SELECTED INPUT	DEFAULT INPUT MODE	S1[1]CLKin_Sel0 State	S1[2] CLKin_Sel1 State
CLKin0/0*	Differential clock	0	0
CLKin1/1*	Differential clock	0	1
OSCin	Select OSCin	1	Don't Care

5. Connect and measure any clock output SMA labeled **CLKoutX** to an oscilloscope or other test instrument using SMA cable(s). The output clock will be level-translated/buffered copy of the selected clock input or crystal oscillator. Note: All output clocks are AC-coupled to the SMA connectors to ensure safe use with RF instruments.

   Note: Switching noise from one or more un-terminated outputs may impair the signal quality of the measured output(s). To minimize switching noise and EMI, properly terminate any unused output path using an SMA load or the component options near the SMA outputs, or alternatively, remove the 0 Ω series resistor nearest the unused output pin.

3 Signal Path and Control Switches

The LMK00101 supports single-ended or differential clocks on CLKin0 and CLKin1. A third input, OSCin, has an integrated crystal oscillator interface that supports a fundamental mode, AT-cut crystal or an external single-ended clock. The three-input multiplexer is pin-controlled. To achieve the maximum operating frequency and lowest additive jitter, it is recommended to use a differential clock with high input slew rate (>1 V/ns) and DC-coupling to either CLKin0 or CLKin1 port.

All control pins are configured with the control switch, S3. The output enable logic is shown in Table 4.

Table 4. Output Enable Selection (0=OFF, 1=ON)

CLKout ENABLE MODE	S1[3]-OE
Disabled/Hi-Z	0
Enabled	1

4 Power Supplies

By default, Vdd and VddCLKout are supplied by two external power supplies. To modify the EVK with a different power supply configuration, populate the resistor options as shown in Table 5.Then, apply the appropriate voltage(s) to the EVK power input(s).

Decoupling capacitors and 0 Ω resistor footprints, which can accommodate ferrite beads, can be used to isolate the EVK power input(s) from the device power pins. Do not disconnect or ground any of the VddCLKout pins as they are all internally connected inside the device.

Table 5. Power Supply Configuration

	DUAL EXTERNAL INPUTS (DEFAULT)	SINGLE EXTERNAL INPUT 3.3 V
Vdd input	Apply 3.3 V	Apply 3.3 V ± 5%
VddCLKout input	Apply Voltage ≤Vdd	Not used
R38	0 Ω	DNP
R39	0 Ω	0 Ω
R43	DNP	0 Ω

5 Clock Inputs

The SMA inputs labeled CLKin0 & CLKin0* and CLKin1 & CLKin1* are configured to receive a differential clock or single ended clock. Best performance is achieved with DC-coupled differential input clock.

5.1 Crystal Oscillator Interface

The LMK00101 has an integrated crystal oscillator interface (OSCin/OSCout) that supports a fundamental mode, AT-cut crystal. If the crystal input is selected, an optional onboard crystal on either footprint Y1 or Y2 will start-up and the oscillator clock can be measured on any enabled output.

A crystal with the HC49 footprint can be populated on the bottom side of the PCB. Alternatively, a 3.2 x 2.5 mm crystal can be populated on Y2, located on the top side. Only one crystal footprint should be used at a time.

The values of C42 and C25(C_{EXT}) depend on the load capacitance (C_L) specified for the crystal. The OSC input capacitance (C_{IN}) of the device is 1 pF differential, and the trace capacitance (C_{TRACE}) of OSCin and OSCout is around 1 pF. If the selected crystal is specified for C_L of 18 pF, the C_{EXT} is calculated as follows:

$$C_{EXT} = (C_L - C_{IN} - C_{TRACE}/2) * 2 \quad (1)$$

$$C_{EXT} = (18\ pF - 1\ pF - 1\ pF/2) * 2 \quad (2)$$

$$C_{EXT} = 33\ pF \quad (3)$$

5.2 Configuring OSCin for a Crystal Mode

To configure the board to use crystal mode remove C26 to disconnect the OSCin Port. Install 0 Ω resistors on R33 and R34. Install a crystal in either footprint (Y1 or Y2) and install the proper load capacitors in C24 and C25.

6 Clock Outputs

All clock outputs are LVCMOS. In the case that not all outputs are used, any unused outputs should be left floating.

7 Schematics

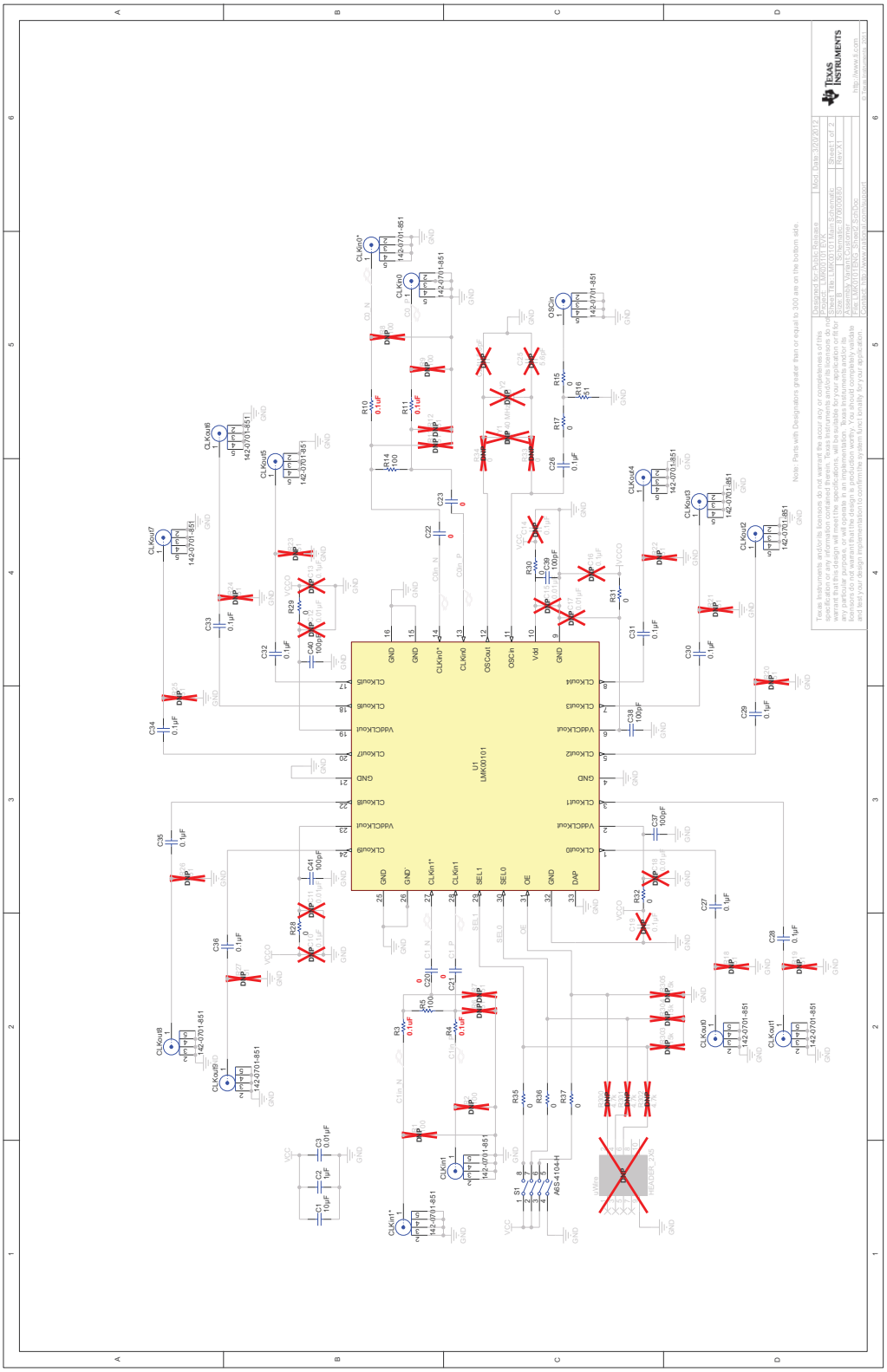

Figure 2. Schematic Sheet 1

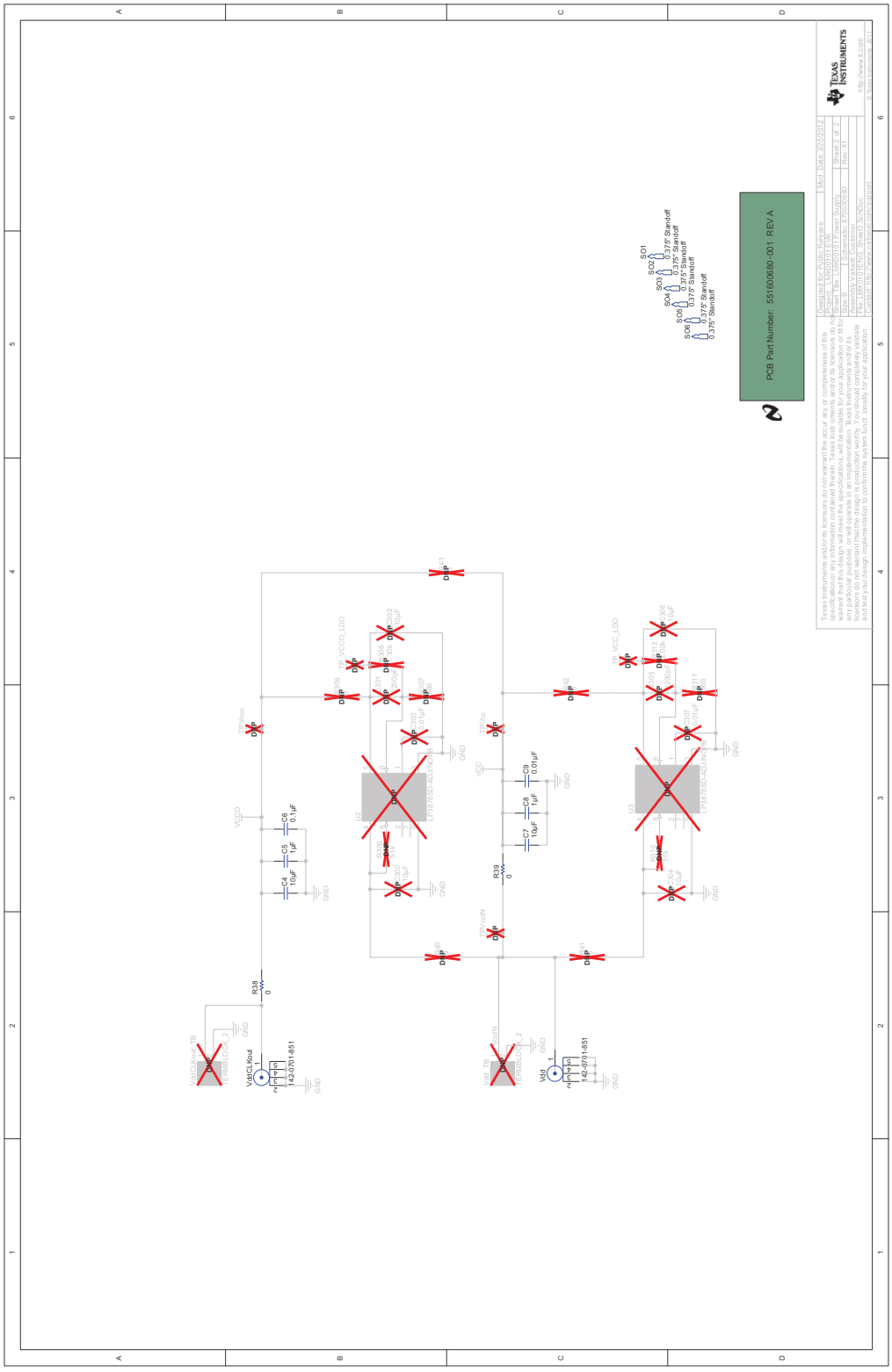

Figure 3. Schematic Sheet 2

8 PCB Layout

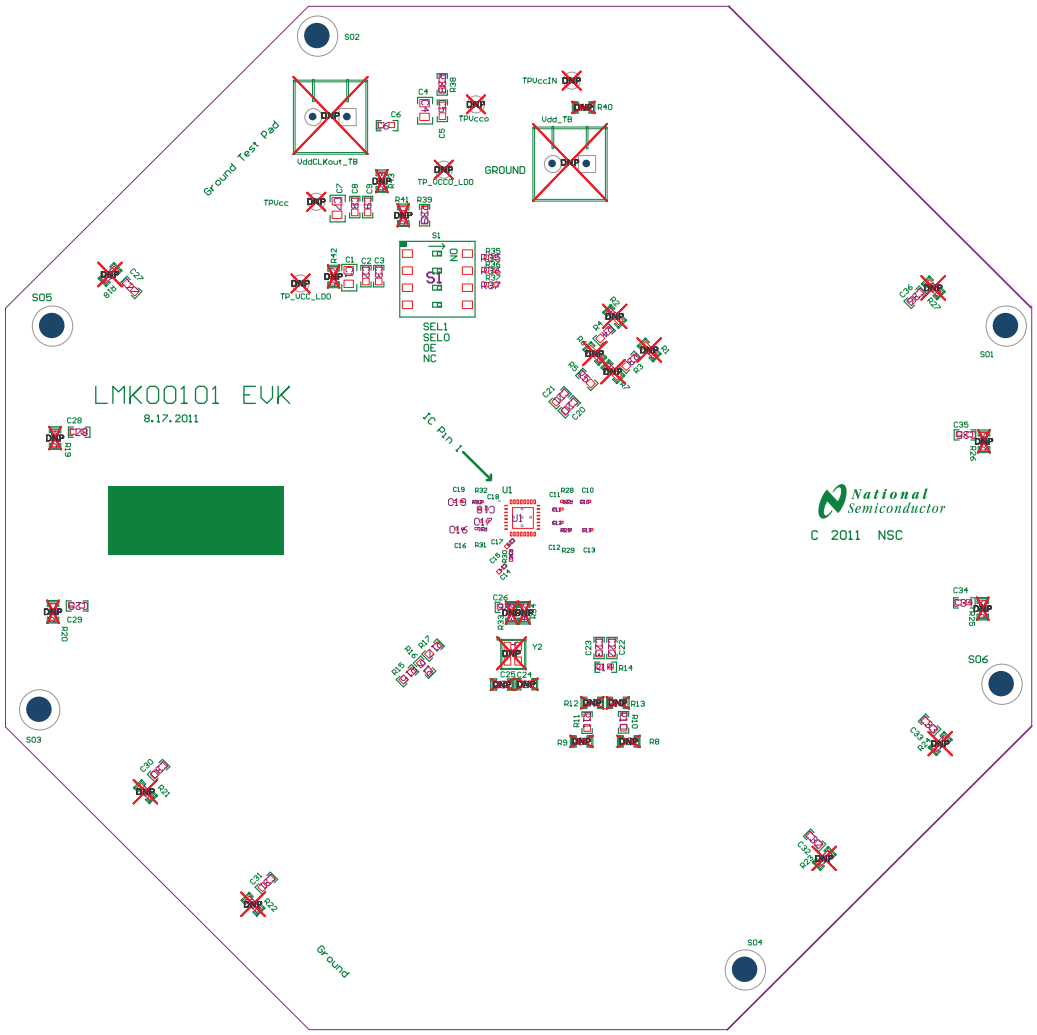

Figure 4. PCB Top

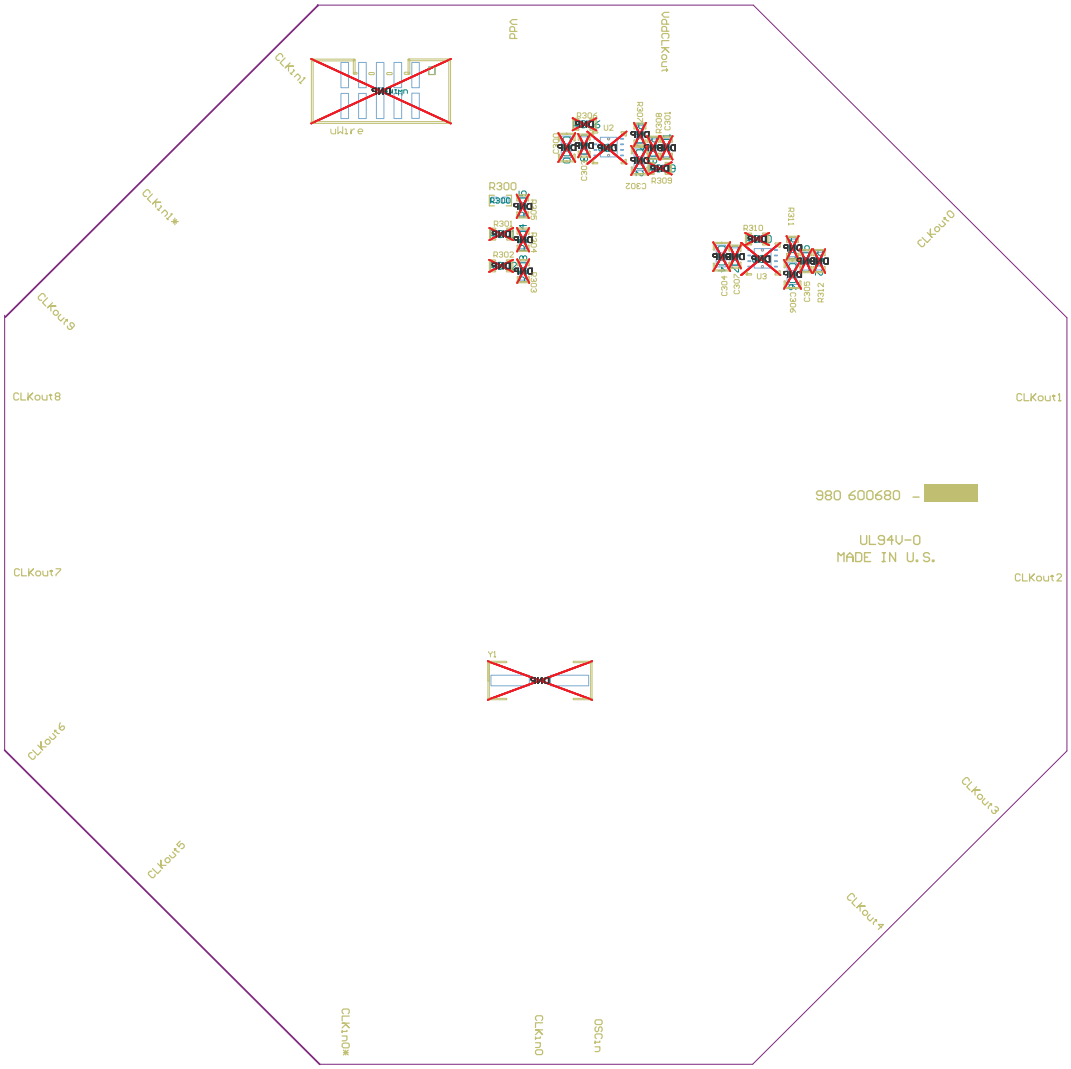

Figure 5. Bottom Side (Layer Inverted, Not to Scale)

9 Bill of Materials

Table 6. Bill of Materials

Item	DESCRIPTION	QTY	DESIGNATOR	MANUFACTURER	PART NUMBER
1	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	3	C1, C4, C7	MuRata	GRM21BR61A106KE19L
2	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	3	C2, C5, C8	TDK	C1608X7R1C105K
3	CAP, CERM, 0.01uF, 100V, +/-5%, X7R, 0603	2	C3, C9	Kemet	C0603C103J1RACTU
4	CAP, CERM, 0.1uF, 16V, +80/-20%, Y5V, 0603	1	C6	TDK	C1608Y5V1C104Z
5	RES, 0 ohm, 5%, 0.1W, 0603	11	C20, C21, C22, C23, R15, R17, R35, R36, R37, R38, R39	Vishay-Dale	CRCW06030000Z0EA
6	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	15	C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, R3, R4, R10, R11	TDK	C1608X7R1C104K
7	CAP, CERM, 100pF, 25V, +/-5%, C0G/NP0, 0402	5	C37, C38, C39, C40, C41	MuRata	GRM1555C1E101JA01D
8	Connector, SMT, End launch SMA 50 ohm	17	CLKin0, CLKin0*, CLKin1, CLKin1*, CLKout0, CLKout1, CLKout2, CLKout3, CLKout4, CLKout5, CLKout6, CLKout7, CLKout8, CLKout9, OSCin, Vdd, VddCLKout	Emerson Network Power Connectivity	142-0701-851
9	RES, 100 ohm, 5%, 0.1W, 0603	2	R5, R14	Vishay-Dale	CRCW0603100RJNEA
10	RES, 51 ohm, 5%, 0.1W, 0603	1	R16	Vishay-Dale	CRCW060351R0JNEA
11	RES, 0 ohm, 5%, 0.063W, 0402	5	R28, R29, R30, R31, R32	Vishay-Dale	CRCW04020000Z0ED
12	DIP Switch, 4 position slide actuator, SPST, SMD	1	S1	Omron Electronic Components	A6S-4104-H
13	0.375" Standoff	6	SO1, SO2, SO3, SO4, SO5, SO6		
14	LMK00101	1	U1	Texas Instruments	LMK00101
15	CAP, CERM, 0.1uF, 16V, +80/-20%, Y5V, 0402	0	C10, C13, C14, C16, C19	TDK	C1005Y5V1C104Z
16	CAP, CERM, 0.01uF, 25V, +/-10%, X7R, 0402	0	C11, C12, C15, C17, C18	TDK	C1005X7R1E103K
17	CAP, CERM, 5.6pF, 50V, +/-5%, C0G/NP0, 0603	0	C24, C25	AVX	06035A5R6CAT2A
18	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	0	C300, C302, C304, C306	MuRata	GRM21BR61A106KE19L
19	CAP, CERM, 2200pF, 100V, +/-5%, X7R, 0603	0	C301, C305	AVX	06031C222JAT2A
20	CAP, CERM, 0.01uF, 25V, +/-5%, C0G/NP0, 0603	0	C303, C307	TDK	C1608C0G1E103J
21	RES, 100 ohm, 5%, 0.1W, 0603	0	R1, R2, R8, R9	Vishay-Dale	CRCW0603100RJNEA
22	RES, 51 ohm, 5%, 0.1W, 0603	0	R6, R7, R12, R13, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27	Vishay-Dale	CRCW060351R0JNEA
23	RES, 0 ohm, 5%, 0.1W, 0603	0	R33, R34, R40, R41, R42, R43, R309	Vishay-Dale	CRCW06030000Z0EA
24	RES, 4.7k ohm, 5%, 0.1W, 0603	0	R300, R301, R302	Vishay-Dale	CRCW06034K70JNEA

Table 6. Bill of Materials (continued)

Item	DESCRIPTION	QTY	DESIGNATOR	MANUFACTURER	PART NUMBER
25	RES, 15k ohm, 5%, 0.1W, 0603	0	R303, R304, R305	Vishay-Dale	CRCW060315K0JNEA
26	RES, 51k ohm, 5%, 0.1W, 0603	0	R306, R310	Vishay-Dale	CRCW060351K0JNEA
27	RES, 866 ohm, 1%, 0.1W, 0603	0	R307, R311	Vishay-Dale	CRCW0603866RFKEA
28	RES,1.30k ohm, 1%, 0.1W, 0603	0	R308	Vishay-Dale	CRCW06031K30FKEA
29	RES, 2.00k ohm, 1%, 0.1W, 0603	0	R312	Vishay-Dale	CRCW06032K00FKEA
30	Testpoint	0	TP_VCC_LDO, TP_VCCO_LDO, TPVcc, TPVccIN, TPVcco		
31	Micropower800mA Low Noise "Ceramic Stable" Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP, Pb-Free	0	U2, U3	Texas Instruments	LP3878SD-ADJ/NOPB
32		0	uWire, Vdd_TB, VddCLKout_TB		
33	Crystal, xxxMHz, xxpF, [MountType]	0	Y1		
34	Crystal, Citizen CS325, XXMHz	0	Y2		

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2012) to A Revision	Page
• Changed document throughout.	2

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