

DS250DF810EVM User's Guide

The DS250DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. It is used to extend the reach and robustness of long, lossy, crosstalk-impaired high-speed serial links while achieving a bit error rate (BER) of 10-15 or less. Each channel of the DS250DF810 independently locks to serial data rates in a continuous range from 20.6 Gbps to 25.8 Gbps or to any supported sub-rate (÷2 and ÷4), including key data rates such as 10.3125 Gbps and 12.5 Gbps. Integrated physical AC coupling capacitors (TX and RX) eliminate the need for external capacitors on the PCB. The DS250DF810 has a single power supply and minimal need for external components. These features reduce PCB routing complexity and BOM cost. The advanced equalization features of the DS250DF810 include a low-jitter 3-tap transmit finite impulse response (FIR) filter, an adaptive continuous-time linear equalizer (CTLE), and an adaptive decision feedback equalizer (DFE). This enables reach extension for lossy interconnect and backplanes with multiple connectors and crosstalk. The integrated CDR function is ideal for front-port optical module applications to reset the jitter budget and retime the high-speed serial data. The DS250DF810 implements 2x2 cross-point on each channel pair, providing the host with both lane crossing and fanout options.

The DS250DF810 can be configured via the default SMBus slave mode or with an external EEPROM. Up to 16 devices can share a single EEPROM. A non-disruptive on-chip eye monitor and PRBS generator and checker functions allow for in-system diagnostics. With this kit, users can quickly evaluate the DS250DF810 retimer performance.



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1 Hardware Description and Setup

The general procedure for setting up and testing with the DS250DF810 Evaluation Module (DS250DF810EVM) hardware is as follows:

- 1. Check the EVM jumper settings to ensure they match Figure 1 below.
- 2. Connect the EVM to a PC using the provided USB cable.
- 3. Connect 3.3V power (2A max) as shown below. The EVM has an on-board 3.3V-to-2.5V regulator to supply the Retimer with the required 2.5V.



Figure 1. DS250DF810EVM, Showing Necessary Connections for Power, Signal, and USB Communications

4. Connect the EVM to the system under test.

The default EVM configuration has four differential RX inputs and four differential TX outputs accessible to the user. Connect the RX and TX signals to the test channel using Huber+Suhner 1x8 MXP cable assemblies (See Section 6 for ordering information).

NOTE: All TX and RX channels are AC coupled with physical 220 nF capacitors on the package of the device, so external AC coupling capacitors are not needed when using this EVM.

2 Software Description

2.1 Setup

SigCon Architect Installer

The **one-time** procedure for installing the GUI software is as follows:

- 1. Download and install the TI SigCon Architect GUI. The steps for installing the software are as follows:
 - 1. Go to www.ti.com/tool/sigconarchitect and download the latest version of SigCon Architect. At the time this document was written, the latest version of SigCon Architect is 2.0.0.4.

SIGCON ARCHITEC	Г											
(ACTIVE) SIGCONARCHITECT												
Description &	Features	Technical Documents	5	🚨 Support & C	ommunity	📜 Order Now						
Description												
The Texas Instruments SigCon Architect utility tool provides a simple to use and robust system for interaction with several different high speed signal conditioning Ti devices. This software provides an interview GUI for supported devices to access device features via SMBus and SPI communications.												
SigCon Architect is a LabView-based GUI, and for proper operation, LabView Run-Time Engine (RTE) is installation prerequisites. Please select from the following installation options:												
SigCon Architect Installer (Run-Time En	gine NOT embed	ided):										
For users who already have LabVie	w RTE installed											
 For users who do not have LabView active Internet connection 	/ RTE but will be i	nstalling SigCon Architect on a PC v	with an									
SigCon Architect Installer wRTE (Run-Ti	me Engine embe	dded):										
 For users who do not have LabView without an active internet connection 		installing SigCon Architect on a PC										
Important Notes:												
SigCon Architect has only been vali	dated for use wit	h Windows 7										
For scripting utility options within S	igCon Architect, F	ython v2.7 is required.										
Order Now												
Part Number	Buy from	Texas Instruments or Third Party	Status	Current Version	Version Date							
SICCONADCHITECT:	Downloa	d	ACTIVE	V2.0.0.0	05-MAY-2015							

Figure 2. Download SigCon Architect from www.ti.com

- 2. Extract the executable file (.EXE) from the downloaded file and run the executable.
- 3. Follow the installation wizard's instructions to install SigCon Architect.
- 4. Download the DS250DF810 profile file from the TI SigCon Architect page.
- 5. Extract the executable file (.EXE) from the downloaded file and run the executable.

- 2. Run the SigCon Architect software.
 - 1. Start the software by double-clicking its icon on the desktop.
 - 2. On the "Selection" panel, the DS250DF810 should appear.
 - 3. If DS250DF810 is not listed:
 - 1. Go to "Device" tab and choose "Manage Devices".
 - 2. Click on "+" icon and then select the "DS250DF810" device model.
 - 3. Fill in the "New Device Name, DS250DF810 is recommended.
 - 4. Select the slave address as configured on EVM (typical setting is 0x30).
 - 5. Click "OK".
 - 4. Navigate to the "Configuration" page of DS250DF810 via the "Selection" panel. Choose "Slave Address" "0x30" from the drop down menu. Verify the "USB2ANY Details" specify "USB2ANY 0", and click "Apply". Successful connection is indicated by the green "CONNECTED" indicator on the bottom of the application.

SigCon Architect			– – ×
File Script Device Help			
and the second	SigCon Archit	Demo Mode	
Selection DS125DF1610 Configuration Configuration Configuration Des250DF10 DS250DF10 DS250DF10 DS250DF10 Configuration Configuratio	Device Model # of Channel Slave Address DS250DF810 8 0x30	USB2ANY Details USB2ANY 0 • Toggle LED Apply DS250DF810 Datasheet: SNLS495	Î
 High level Page 	DS250DF810 25 Gbps Mult	DS250DF810EVM User's Guide: SNLUxxx i-Rate 8-Channel Retimer	
	 Octal-Channel Multi-Rate Retimer with Integrated Signal G All Channels Lock Independently from 20.6 to 25.8 Gbps (i Ultra Low latency: < 500 ps Single Power Supply, No Low-Jitter Reference Clock Requires Routing Complexity and BOM Cost Integrated 2x2 Cross Point Adaptive Continuous Time Linear Equalizer (CTLE) Adaptive Decision Feedback Equalizer (DFE) 		-
-	Low-litter Transmitter with 3-Tan FIR Filter	Online Documentation	n
Idle		LabVIEW 12.0.1	NSTRUMENTS

Figure 3. Sigcon Architect Start-Up Screen



Software Description

www.ti.com

😒 SigCon Architect										
File Script Device Help										
	SigCon Architect	🗖 Demo Mode								
Selection	The Manage Devices)								
 ◆ DS125DF1610 → Configuration → Configuration → Expe Monitor Page → Experimentation → Configuration → Low Level Page → Experimentation 	List of Loaded Devices DS125DF1610 DS250DF810 Device Model DS250DF810 Slave Address × 30	USB2ANY Details USB2ANY 0 Toggle LED Apply DS250DF810 Datasheet: SNLS495 DS250DF810EVM User's Guide: SNLUxxx								
	•	e 8-Channel Retimer								
	OK CANCEL	ning Sub-Rates like 10.3125 Gbps, 12.5 Gbps, and more)								
×	Ultra Low latency: < 500 ps Single Power Supply, No Low-Jitter Reference Clock Required, and Integrated AC Coupling Capacitors to Reduce Board Routing Complexity and BOM Cost Integrated 2x2 Cross Point Adaptive Continuous Time Linear Equalizer (CTLE) Adaptive Decision Feedback Equalizer (DFE) I ow-litter Transmitter with 3-Tan FIR Filter Online Documentation									
Idle		Labview 12.0.1 CONNECTED 🛷 Texas Instruments								

Figure 4. Capture Illustrating the "Manage Devices" Pop-Up Window for Adding New Part Numbers to the "Selection" Panel

3. Once connection is successfully established, users can read and write various settings to the device in real-time, using the functional pages.

2.2 Functional Pages

2.2.1 Low-Level Page

The low-level page allows the user to read and write to all registers on the DS250DF810. To access it, navigate to the "Low Level Page", as shown below.

- The user may click "Read All" to load the data in each register from the device to the "Register Map."
- The user may access the Shared, Global or Channel registers via "Block Select."
- To Read a register:
 - Type the readable address in the "Current Address" text box or select a register from the Register Map.
 - Click "Read Register". The data in this register will appear in the "Data" text box.
- To Write a register:
 - Type the writeable address in the "Current Address" text box or select a register from the Register Map.
 - The user may either type the data value (in HEX) to write to this address in the "Data" text box, or check/uncheck boxes as desired for individual bits within the register. Then click "Write Register."
 - If Broadcast is selected for channel register writes, the specified write will be performed to all channels in the device.



File Script Device Help							
		SigC	Con Architec	"When in Demo Mode, click "Apply" or	n the profile Configuratio	Demo M n Page to enable access to other p	
Selection	Block Select Shared Registers Quadrant 0 • Register Map Block/ Register Name • Shared Registers Quadrant 1 • Global Registers • Channel 0 • Channel 1 • Channel 1 • Channel 3 • Channel 5 • Channel 6 • Channel 7	Expand All	Collapse All ize Data ize Data ixe 0 Data × Write Regist Broadcast Read All Read All Reset Devic Load Config Save Config Save Config Note: Load Con will Overwrite a Registers. *	er Field Description Field Name	Access	Mask Value x FF	
Idle					CONNECTED	🔱 Texas Instrume	NTS

Figure 5. Low-Level Page Capture Illustrating the Different Block Select Options

				Sig	gC	on /	٩r	chitect	hen in Demo Mode, click "Apply" or	n the profile Con	iguration Page to enable access to of
ion ^	Block Select										
Configuration		•									
ow Level Page	Register Map		Ex	pand All		Collapse	All				
ye Monitor Page	Block / Register Name	Address	Default	Mode	Size	Data	1				Mask Value
ligh level Page	0x6E	0x6E	0x00	RAV	8	0x00	-1^	Current Address	Mask Register Data		
1219	0x6F	0x6E	0x00	RAV	8	0x00		× 78	7 RESERVED[1		× 0
onfiguration	0x70	0×70	0x03	RAV	8	0x03			6 RESERVED[0		
ow Level Page igh level Page	0x71	0x71	0x00	RAV	8	0x20		Data	5 📄 🛛 V SD_STATUS		
ve Monitor Page	0x72	0x72	0x00	RAV	8	0x00		× 30	4 📄 🛛 V CDR_LOCK_		
,	0x73	0x73	0x00	RAV	8	0x00			3 CDR_LOCK_	INT[0]	
	0x74	0x74	0x00	RAV	8	0x00		Write Register	2 SD_INT[0]		
	0x75	0x75	0x00	RAV	8	0x00				E_LIMIT_ERR	OR[0]
	0x76	0×76	0x22	RAV	8	0x22		Broadcast	0 HEO_VEO_IN	IT[0]	
	0x77	0x77	0x1A	RAV	8	0x1A		Read Register	Field Description		
	0x78	0x78	0x00	R	8	0x30		Redu Register			Description
	0x79	0x79	0x10	RAV	8	0x30		Read All	Field Name	Access	Description
	0x7A	0x7A	0x00	RM	8	0x00			RESERVED[7:6]	R	RESERVED
	0x7B	0×7B	0x00	RAV	8	0x00			SD_STATUS[5:5]	R	Primary observation point for
	0x7C	0x7C	0x00	R	8	0x00		Reset Device			signal detect status
	0x7D	0x7D	0x48	R/W R/W	8 8	0x48			CDR_LOCK_STATUS[4:4]	R	Primary observation point for
	0x7E 0x7F	0x7E 0x7F	0x13 0x3A	RAV	8	0x13 0x2A		Load Config			CDR lock status
	0x7F	0x7F 0x80	0x3A 0x00	R	8	0x2A 0x36		Save Config	CDR_LOCK_INT[3:3]	R	Requires that channel
	0x81	0x81	0x00	R	8	0xE5		Save coming			register 0x79[1] be set.
	0x82	0×82	0x00	RAV	8	0x00	=	Notes I and Oracle			1: Indicates CDR has achieved lock, lock goes from
	0x83	0x83	0x00	R	8	0x00	=	Note: Load Config will Overwrite all			LOW to HIGH. This bit is
	0x84	0x84	0x00	R	8	0x00		Registers.			cleared after reading. This bit
	0x85	0x85	0x00	R	8	0x00		itegisters.			will stay set until it has been
	0x86	0x86	0x00	R	8	0x00					cleared by reading.
	0x87	0x87	0x00	R	8	0x00			SD_INT[2:2]	R	Requires that channel
	0x88	0x88	0x00	R	8	0x00					register 0x79[0] be set.
	0x89	0x89	0x00	R	8	0x00					1: Indicates signal detect
	0x8A	0x8A	0x00	R	8	0x00					status has changed. This will
	0x8B	0x8B	0x00	RAV	8	0x00	-				trigger when signal detect

Figure 6. Low-Level Page Capture After Selecting Access to an Individual Register



2.2.2 Eye Opening Monitor (EOM) Page

The Eye monitor page allows the user to visualize DS250DF810 eye plots, a means of assessing received signal quality after equalization.

- Select the channel for eye plotting. Note that plots can only be generated for a given channel if "CDR Locked" is indicated.
- The EOM_SEL_VRANGE pull-down allows the user to adjust the vertical scale for eye plots.
- The user may perform a "Single Capture" of eye monitor plot, or select "Continuous Capture" to accumulate multiple plots over a period of time.
- The Horizontal Eye Opening (HEO) and Vertical Eye Opening (VEO) may be read on the Eye Monitor page.
- If the user desires to do their own analysis or post-processing of the EOM data, the "Export Raw Data" and "Export Density" buttons respectively generate an Excel spreadsheet containing the 63x63 eye monitor values matrix.



Figure 7. Eye Monitor Page for DS250DF810 Profile



2.2.3 EEPROM Page

The SigCon Architect EEPROM page allows the user to either: create a DS250DF810 Hex file that is programmable to an EEPROM, or configure a DS250DF810 device based on values from an existing DS250DF810 Hex file.

			Si	igCon	Arch	itect	'hen in Demo Moo	de, click "Apply" o	on the profile Co	nfiguration Pa	age to enable access	Dem to oth
on 250DF810 Configuration Low Level Page Eye Monitor Page										oad From Hex File	Write EEPRON	
Page Page	No. of Device EEPR		bbA	ress	EEPROM Data							
	1 🖨 1024	Bytes -								30	0x00	+
									0x		0x00	- 8
										32	0x00	+
										33	0x00	+
			Slot Update	Details	Ad	dress/Slot list	Selection		Ox	34	0x00	-
						evice Address	Slot#		0x	35	0x00	-
	CERRON Usedas		Slot #	0 🌲		0x30	0		Ox	36	0x00	
	EEPROM Header		All Slots						0x	37	0x00	
	Common Channel?		C All Sidis							38	0x00	
	Address Map Enabled	2								39	0x00	_
			Update SI	lot From Device	e					3A	0x00	_
	EEPROM > 256?				_				0x		0x00	-
	Enable CRC?		Update De	evice From Slo	t			-		3C 3D	0x00 0x00	⊢.
	Major Channel Settings : Slot	t 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7		1	
	Parameters ADAPT MODE	<u></u>		0x00		0x00	0x00		-			_
	EQ_BST0	0x00 0x00	0x00 0x00	0x00	0x00 0x00	0x00	0x00 0x00	0x00 0x00	0x00 0x00			
	EQ_BST0	0x00	0x00 0x00	0x00	0x00	0x00	0x00	0x00	0x00			-
	EQ_BST2	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00			-
				0000	0100	0.00		0.00	0.00		1 1	

Figure 8. EEPROM Page for DS250DF810 Profile

The user may choose to update the EEPROM page settings based on values read from the DS250DF810 device by clicking "Update Slot from Device". To create the programmable hex file, click "Write to EEPROM Hex". Note that the evaluation module does not include an EEPROM, but an external EEPROM can be used. SigCon Architect cannot directly program the EEPROM. The EEPROM Hex File can be burned on the EEPROM via I²C communication (i.e. AARDVARK or equivalent interface adapter). The EEPROM control settings are described in greater detail below.

- Common Channel: If this box is checked, all channels receive the same configuration. Different devices can receive different configurations, but within one device, all channels will receive the same configuration. If this box is unchecked, then the EEPROM will store the configuration as unique channel configurations. Each of the four channels can receive a unique configuration.
- EEPROM>256:
 - This setting must be enabled if there are more than 4 EEPROM slots.
 - When this box is checked, the "EEPROM Size" drop down menu is automatically populated by 512 Bytes if previously populated by 256 Bytes.
 - When this box is unchecked, the "EEPROM Size" drop down menu is automatically populated by 256 Bytes. Up to 4 EEPROM slots can be programmed.
- Enable CRC: If enabled, each device will have a CRC value specific to the base header, address map header, and data. If disabled, the CRC is not computed.
- Slot Update Details: The number of slots refers to the total number of unique SMBus register settings to load from the EEPROM. The user can choose to update all slots, or which slot # to update the SigCon Architect EEPROM page from.



- EEPROM Size: The EEPROM size must be set to 256, 512, or 1024 bytes. A single external EEPROM can be used by up to 16 DS250DF810 devices.
 - The first 3 bytes of EEPROM data is the base header. The base header contains the CRC enabled, address map header enabled, EEPROM<256 bytes, device count, and maximum EEPROM burst size settings.
 - If multiple devices are programmed, an address map header is needed for each device. The address map header specifies the CRC value and the Device EEPROM Start Address.
 - EEPROM Size ≤ 256 Bytes:
 - EEPROM Size = 3 Bytes (Base Header) + # of devices * 8 Bytes/device (Address Header) + # of slots * 66 Bytes/slot (Data)
 - EEPROM Size > 256 Bytes:
 - EEPROM Size = 3 Bytes (Base Header) + # of devices * 12 Bytes/device (Address Header) + # of slots * 66 Bytes/slot (Data)

2.2.4 High-Level Page

2.2.4.1 Overview

The High-Level Page on the Selection Panel enables the user to easily configure and/or check the status of the DS250DF810 high-speed data path functional blocks: Clock and data recovery (CDR), Receiver equalization, Transmitter output driver, PRBS generator and checker, and cross-point. The figure below shows the landing page after uses selects "High-Level Page on the Selection Panel. The first button option is the "Block Diagram", an illustrative page highlighting the DS250DF810's functional stages. The configuration features for the additional tabs within the High-Level Page are described further in the next sub-sections.

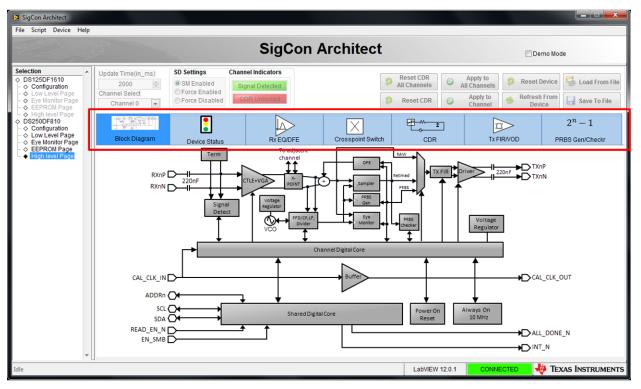


Figure 9. High-Level Page, with Block Diagram Tab Selected



2.2.4.2 Device Status

In order to view a real-time high-level summary of the current device status and control settings, navigate to the "High Level Page", and choose the "Device Status" tab. Click "Refresh From Device" to ensure the settings shown are from the device. The settings on this page are not editable.

- Signal Detect Status: For each channel the device status is displayed as "Signal Not Detected" if there is no detectable signal present at the RX side of this channel or "Signal Detected" if there is a signal present at the RX side of this channel.
- CDR Locked: For each channel the CDR lock status is displayed. Note that each channel's CDR status and configuration is independent from the others.
- EQ Boost: This field displays the Rx Continuous-Time Linear Equalizer (CTLE) boost value as a four digit figure. Each digit corresponds to one of the four CTLE stages, and each can have a value from 0 to 3.
- DFE Taps: The boost values in mV for each of the five Decision Feedback Equalizer (DFE) taps are displayed here.
- HEO and VEO: The HEO and VEO values in mV are displayed for each of the retimer channels.
- Tx FIR filter taps: The Device Status tab displays the current decimal value and polarity for the FIR pre-cursor, main-cursor and post-cursor taps for each of the channels. The coefficient sum (i.e. absolute sum of the FIR tap values) is also displayed. Finally, the page displays approximate values for the effective post-cursor and pre-cursor de-emphasis based on the channel's current FIR tap settings.

				S	igC	on Ar	chite)emo Mode, clic	k "Apply" on the profile	e Configuration F	Demo Page to enable access to othe
n 1218 onfiguration	Update Time(in_ms)	SD Settin SM En		inel Indicat					set CDR Channels	Apply to All Channels	Rese	t Device 💆 Load Fror
w Level Page gh level Page e Monitor Page 5DF1610	Channel Select Channel 3 💌	 Force I Force I 	Enabled	CDR Lock					eset CDR	Apply to Channel	Refre	sh From evice Save To F
iguration Level Page Monitor Page						>	X	<u>`</u>		ŧ		$2^{n} - 1$
l Page I Page I 0	Block Diagram		vice Status		Rx EQ/D	FE	Crosspo	int Switch	CDR		Tx FIR/VOD	PRBS Gen/Cheo
ation el Page itor Page		anal Detected		Boost -	3	DFE Taps 1	+ 0		+26	Main Cursor	1.15	Approx. VOD(V p-p)
M Page el Page		OR Locked		(mV) +	0	DFE Taps 2 DFE Taps 3	+ 0 +0	DFE Taps 5 Pre-Cursor	+0	Post-Cursor Co efficient Sum	0	Approx. Pre DEM(dB) Approx. Post DEM(dB)
		anal Detected	·	Boost -	3	DFE Taps 1	+ 0	DFE Taps 4	+26	Main Cursor	1.15	Approx. VOD(V p-p)
	Citaliner 4	R Locked)(UI) + (mV) +	0	DFE Taps 2 DFE Taps 3	+ 0	DFE Taps 5 Pre-Cursor	+0	Post-Cursor Co efficient Sum	0	Approx. Pre DEM(dB) Approx. Post DEM(dB)
			0000 EQ I	Boost -	3	DFE Taps 1	+ 0	DFE Taps 4	+26	Main Cursor	1.15	Approx. VOD(V p-p)
	Channer 5	gnal Detected OR Locked)(UI) +	0	DFE Taps 2 DFE Taps 3	+ 0		+0	Post-Cursor	0	Approx. Pre DEM(dB)
			0.125 VEO	(111) +	U	UPE Taps 3	+0	Pre-Cursor	26	Co efficient Sum	0	Approx. Post DEM(dB)
	Channel 6	gnal Detected	0000 EQ E	Boost -	3 0	DFE Taps 1	+ 0		+26	Main Cursor	1.15	Approx. VOD(V p-p)
		R Locked		(mV) +	0	DFE Taps 2 DFE Taps 3	+ 0	DFE Taps 5 Pre-Cursor	+0	Post-Cursor Co efficient Sum	0	Approx. Pre DEM(dB) Approx. Post DEM(dB)

Figure 10. High-Level Page, with Device Status Tab Selected



2.2.4.3 Rx EQ/DFE

The Rx EQ/DFE tab provides the user with full status and control capability of the DS250DF810 Rx equalization functions. The figure below illustrates the Rx EQ page functions, which are described below in more detail.

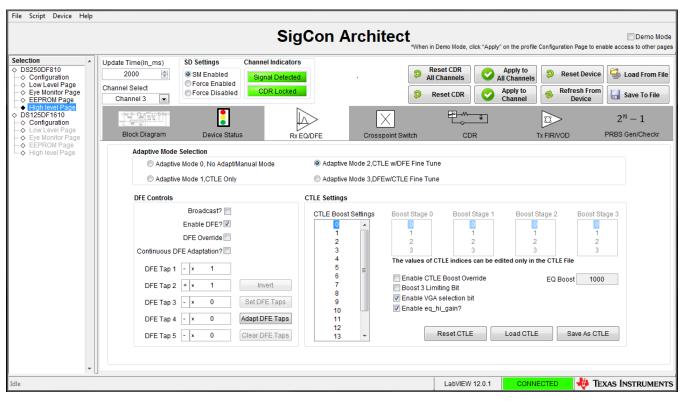


Figure 11. Rx EQ/DFE Tab

- Adapt Mode
 - Upon landing on the Rx EQ page, the GUI will display the current status for the retimer adapt mode for the channel selected in the Channel Select pull-down.
 - The Rx EQ page allows the user to set the DS250DF810 device to any of the four available adapt modes. To do so, the user should click on the desired adapt mode then click "Apply to Channel" to configure a specific retimer channel. Alternatively the user may broadcast the new adapt mode setting by clicking on "Apply to all channels."
- CTLE Settings
 - Select the desired channel on Channel Select pull-down.
 - The GUI will display the current CTLE boost value on the EQ Boost field of the CTLE Settings section.
 - If the user wishes to manually set the EQ value:
 - Adapt Mode 0 may be selected (i.e. no adaption mode).
 - Check the "Enable CTLE Boost Override" option.
 - Click on "Reset CDR" button on the top right of page.
 - Boost 3 Limiting bit
 - When checked, this option configures the last CTLE boost stage to have a limiting output.
 - VGA (Variable Gain Amplifier) gain bit
 - When checked, it enables the Rx VGA block.
 - EQ Hi gain mode bit
 - When checked, the EQ is set to the high-gain mode of operation. This bit is enabled by default.



- EQ boost table If the user wishes to customize the sixteen value CTLE boost table:
 - The user can enter the desired values individually on the "CTLE Boost Settings".
 - After entering all of the CTLE table values, the user should click on "Save as CTLE" button to save the file.
 - This CTLE table file can be loaded for use with new devices by clicking "Load CTLE" and selecting the file from its location.
- DFE Controls
 - Upon landing on the "Rx EQ" tab, the" DFE Controls" section will display the current weight values and polarities for the five DFE taps for the selected channel.
 - The user may check the "DFE Override" box to manually configure the DFE tap values.
 - The user may enable continuous DFE adaption by checking the corresponding box on the "DFE Controls" section.

2.2.4.4 Cross-Point Switch

The cross-point tab allows the user to easily configure the 2x2 cross-point implemented for each of the adjacent channel pairs of the DS250DF810 retimer.

- With the "Pair Select" pull-down, the user can choose which cross-point pair to configure (0-1, 2-3, 4-5, or 6-7.)
- The cross-point mode is selected using the "Crosspoint Configuration" pull-down.
- The cross-point channels mappings are illustrated on the "Crosspoint Settings" table on the page, and the displayed color matches the current cross-point mode.

There are three cross-point configuration modes selectable via the "Crosspoint Configuration" pull-down:

- Default
 - The transmitter for a given channel obtains data from its own receiver.
- Fanout
 - Upon selecting the "Fanout" option on the pull-down, the user will be asked to select a channel on the "Broadcast Channel" pull-down.
 - After the user selects the broadcast channel and clicks on "Broadcast", the received data for the selected channel will be output both on its Tx output and also on the Tx output of its cross-point pair channel.
- Lane Crossing
 - Upon selecting the "Lane Crossing" option, the GUI will automatically configure the cross-point pair in question such that the Tx output of a given channel obtains its data from the Rx of its adjacent cross-point pair channel



Software Description

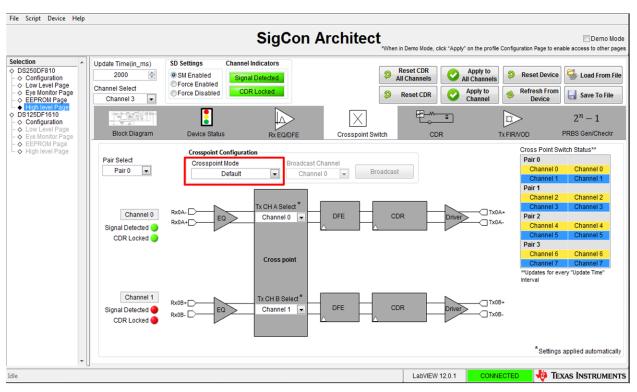


Figure 12. Cross-Point Tab, Default Mode Selected

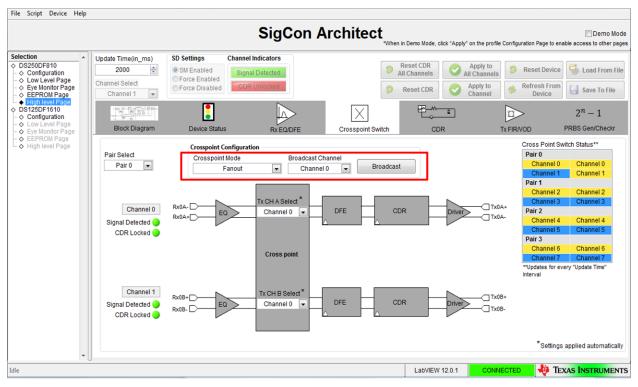


Figure 13. Cross-Point Tab, Fanout Mode Selected



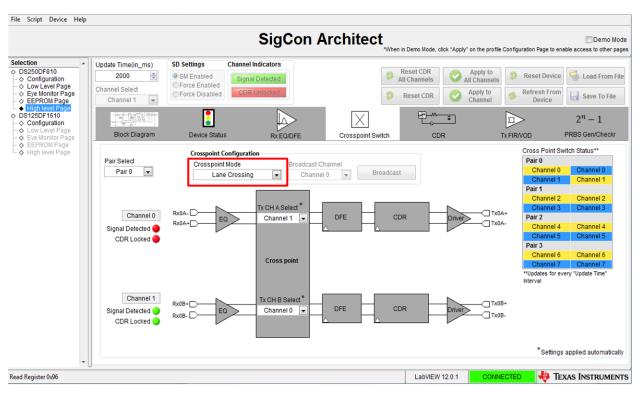


Figure 14. Cross-Point Tab, Lane Crossing Mode Selected

2.2.4.5 CDR (Clock and Data Recovery)

The CDR tab provides a quick way to configure the DS250DF810 retimer to operate at the desired data rates and sub-rates. The DS250DF810 channels must each be pre-programmed for the expected data rate(s) to ensure CDR lock. On the CDR tab the user can select between the Standard and Manual modes of CDR lock configuration.

- Upon landing on the CDR tab, the page will automatically display the mode that the retimer is currently set to, along with the data rate setting and also the divider setting (in the case of Manual Mode.)
- Standard Mode allows the user to program the retimer rate/sub-rate to one of within a set of predefined standard values.
 - Select the desired channel on Channel Select pull-down.
 - The user first clicks on the "Standard Mode" option on the page.
 - The user then selects the desired rate within the "Standard Data Rate Selection" Options.

NOTE: The default settings for the DS250DF810 are "Standard Mode", and "100Gb Ethernet" (i.e 25.78125 Gb/s data rate per channel).

• Manual Mode allows the user to manually program a retimer channel to CDR lock to a specific data rate. This function is intended for applications requiring a data rate that exists within the VCO range, but that are not listed within the "Standard Data Rate Selection" options.

- To configure a channel via "Manual Mode":
 - Select the desired channel on Channel Select pull-down.
 - Select "Manual Mode" option on the page; the user will then see the manual mode input fields become adjustable.
 - Select the desired divider setting from the "Divider Configuration" pull-down.
 - Select "divide-by-1" when data rate > 13 Gbps.
 - Select "divide-by-2" when 13 Gbps ≥ data rate > 6.5 Gbps.
 - Select "divide-by-4" for data rate \leq 6.5 Gbps.
 - Enter desired Data Rate for group 0 then click "Write Rate Regs". The GUI defaults to max PPM tolerance.
 - Enter desired Data Rate for for group 1 then click "Write Rate Regs". The GUI defaults to max PPM tolerance.

 Click "Res 	set CDR".
--------------------------------	-----------

File Script Device Help							
			SigCon Ar	chitect	n in Demo Mode, click "Apply" o	on the profile Configuration Page	Demo Mode to enable access to other pages
Selection ↓ ↓ Configuration ↓ Configuration ↓ Low Level Page ↓ High level Page ↓ SEPEDF101 ↓ Configuration ↓ Level Page ↓ EEPROM Page ↓ EEPROM Page ↓ Bez50DF810 ↓ Configuration ↓ Configuration ↓ Low Level Page ↓ Bez50DF810 ↓ Computed ↓ Computed ↓ EEPROM Page ↓ EEPROM Page ↓ EEPROM Page	@ S	SD Settings Channel Inc SM Enabled Signal D Force Enabled Signal D CDR L Device Status Selection* tandard Mode Manual Mo ard Data Rate Selection*	Rx EQ/DFE Divider Configu		All Channels All	Apply to Channels Refresh Channel Refresh Channel Trick Refresh Device Trick Construction Tx FIR/VOD	From El Save Te File
	© 1	n Data Rate Selection n Data Rate Selection	ops 💿 12.5 Gbps	Reserved	© 25.0 Gbps	.78125 Gbps 💿 Uns	el
		Group 0 Manual Mode Set	5.78125 Gbps Rate Regs 4074			6.78125 Gbps Rate Regs 4074 (F	ettings applied automalically
Idle							Texas Instruments

Figure 15. CDR Tab, Standard Mode Selected



File Script Device Help									
			Sig	Con Arch	itect	in Demo Mode, click "Aj	pply" on the profile Conf	figuration Page to ena	Demo Mode ble access to other pages
Selection ◇ LIMH1218 → Configuration → Configuration → Low Level Page → High level Page → Stj2SDF1610 → Configuration → Low Level Page → Stj2SDF1610 → Configuration → Low Level Page → Eye Nonitor Page → Eye Nonitor Page → EperROM Page → High level Page	Update Time(in_n 5000 Channel Select Channel 3 Block Diage	SM Enabled Force Enable Force Disable		D/DFE Cro		Reset CDR III Channels Reset CDR	Apply to Channel	Refresh From Device	Load From File Save To File $2^n - 1$ PRBS Gen/Checkr
 ♦ DS250DF810 ♦ Configuration ♦ Low Level Page ♦ Eye Monitor Page ♦ EFROM Page ♦ High revel Page 		Mode Selection* Standard Mode Manual Mode Standard Data Rate Selection* 		Divider Configuration* PDIQ_SEL_DIV Divide by 1 12.5 Gbps Reserved		© 25.0 Gbps @ 25.78125 G		© Unsel	
		Group 0 M	anual Mode Settings ata Rate 25.78125 Write Rate Re Count to x 4074 Count to 0x64[7:4] 0x0,0xF	Gbps	C	VCO Count to 0x63/0x62		ops	
•									applied automatically
Idle							CONNEC	ted 🚽 🐺 Te	xas Instruments

Figure 16. CDR Tab, Manual Mode Selected



2.2.4.6 TX FIR/VOD

The TX FIR tab allows the user to configure the FIR tap settings for each of the retimer channels, to set the output to specific voltage amplitude and/or realize specific transmit pre-cursor and post-cursor equalization ratios.

File Script Device Help								
SigCon Architect When in Demo Mode, click "Apply" on the profile Configuration Page to enable access to other pages								
Selection ▲ ◇ LUMH1218 ▲ ◇ ○onfiguration → Configuration → Low Level Page ○ Stabular → Sige Monitor Page > Stabular ○ Low Level Page → Configuration - Configuration - Low Level Page → Low Level Page - Eye Monitor Page - EPROM Page → Ever ROM Page - EPROM Page - EPROM Page	Update Time(in_ms) 5000 😴 Channel Select Channel 3 💌	SD Settings SM Enabled Force Enabled Force Disabled	Channel Indicators Signal Detected CDR Locked	\$	All Chaimeis	Apply to All Channels Apply to Channel	Reset Device	
	Block Diagram	Device Status	Rx EQ/DFE	Crosspoint Switch		1	Tx FIR/VOD	2^n-1 PRBS Gen/Checkr
 			Transmitter FIR/VOD Settings					
				Broadcast? 🕅				
High level Page			Pre Cursor Tap	+0 🔺	Read Taps			
			Main Cursor	+26	Set Taps			
			Post Cursor Tap	+0 💌				
			Co efficient abs Sum	26				
			Approx. VOD	1.15 Vp-p				
			Approx. Pre de-emphasis	0 dB				
			Approx. Post de-emphasis	0 dB				
·								
Idle						CON	INECTED 🦊	Texas Instruments

Figure 17. TX FIR Tab

- Upon landing on the TX FIR tab, the page will display the current decimal values and polarity for the main-cursor, post-cursor and pre-cursor FIR taps.
- In addition, the page also displays approximate values for the voltage output differential (VOD) and the de-emphasis for both pre-cursor and post-cursor.
- The user may adjust the FIR tap values, by clicking on the up/down arrows for each field. After entering the desired value(s), the user can click on "Set Taps" to make the entries effective.
- At any point the user can click on "Read Taps".

2.2.4.7 PRBS Tab

The PRBS tab within the High-Level page allows the user to configure the PRBS generator or Checker functions on any of the channels of the DS250DF810 retimer.

- To enable PRBS Generator on a channel:
 - Select the desired channel using the "Channel Select" pull-down.
 - Select the desired pattern using the "Pattern Type" pull-down.
 - Set desired Polarity via pull-down, Non-Invert or Invert.
 - Click "Enable" button.

File Script Device Help								
Demo Mode "When in Demo Mode, click "Apply" on the profile Configuration Page to enable access to other pages								
Selection → LiMH1218 → Configuration → Low Level Page → High level Page → Eye Monitor Page → Scripturation → Low Level Page → Configuration → Low Level Page → Eye Monitor Page	Update Time(in_ms) 5000 🗭 Channel Select Channel 0 💌	SD Settings (SM Enabled Force Enabled Force Disabled	Channel Indicators Signal Detected CDR Locked	X	Reset CDR All Channels Reset CDR Reset CDR	Apply to All Channels Apply to Channel	Reset Devi Refresh Fro Device	
-	Block Diagram	Device Status	Rx EQ/DFE	Crosspoint Sw	vitch CDF	२	Tx FIR/VOD	PRBS Gen/Checkr
♦ DS250DF810	PRBS Generator Config	gurations	PRBS Checker					
Configuration Low Level Page Eye Monitor Page EEPROM Page EEPROM Page High level Page High level Page	Enable* Pattern Type PRBS 15 Polarity Non - Invert		Mode Selection Standard Mode Capture Period Hour Finite 0 1- 1000000- 00-	Group 0 💌	Datarate 25.7812 Gbp ype Polarity letect Non - Im			in) Bit Count d 0E+0 Turn OFF ror Count
			-1-¦ 3:59:59.000 PM 12/31/1903 Error Count Graph	3:59:59.500 PM 12/31/1903	4:00:00.000 PM 12/31/1903 Time(in minutes)	4:00:00.500 PM 12/31/1903	4:00:01.(12/31/	Reset Checker Clear Checker
-							*Setting	s applied automatically
Idle						CON		Texas Instruments

Figure 18. PRBS Tab, PRBS Generator Configuration

Software Description

- To enable PRBS Checker on a channel:
 - Select the desired channel using the "Channel Select" pull-down.
 - Set the "Capture Period".
 - Set pull-down to "Infinite" if it desired to run extended duration test without time limit.
 - If "Finite" period is desired, set the pull-down to "Finite" and enter the desired test duration via the "Hours" and/or the "Mins(Minutes)" input fields.
 - Click "Turn ON".
 - The user may clear the counter fields by clicking "Clear Checker," or reset the PRBS checker settings by clicking "Reset Checker".
 - To turn off the checker and return to default settings, click on "Turn OFF".

File Script Device Help		
		SigCon Architect
Selection Cull High 2 Selection Configuration Configuration Cull Level Page DS125DF1610 Configuration Cull Level Page EEPROM Page Low Level Page Cull Level Page EEPROM Page EEPROM Page High Level Page Configuration Low Level Page High Level Pag	Update Time(in_ms) 5000	Channel Indicators Image: Signal Detected Image: Apply to Apply to All Channels Image: Apply to Channels <t< th=""></t<>
	PRBS Generator Configurations Enable* Pattern Type Custom Pattern PRBS 7 b 0 Polarity Non - Invert	PRBS Checker Mode Selection Group Selection Datarate Error Count(bits) Error Rate(bits/min) Bit Count Manual Mode Group 0 25.7812 Gbps d 0 d 0 d 7.73438E+11 Capture Period Hours Mins Pattern Type Polarity Infinite 0 : 1 PRBS 15 Non - Invert Turn OFF Error Count Free Error Count Free Error Density
		-1- 2:13:04.789 PM 2:13:10.000 PM 2:13:15.000 PM 2:13:20.000 PM 2:13:25.000 PM 2:13:29.7 10/7/2015 10/72015 10/72000 10/72000 10/72000 10/72000 10/7200000000000000000000000000000000000

Figure 19. PRBS Tab, PRBS Checker Configuration



3 Best Practices and Usage Tips

The following is a general procedure that should be followed when using the DS250DF810EVM in a system.

- 1. Set up your data source (either BERT TX or ASIC TX) to generate a PRBS pattern of the desired data rate.
 - Not all BERT TX sources have FIR capabilities. The DS250DF810 receiver usually does not need much de-emphasis applied by the link partner transmitter (i.e. the BERT TX or ASIC TX). Typically 3dB of de-emphasis or 0-15% post-cursor will be adequate. If the BERT/ASIC TX has pre-cursor capabilities, then 0-15% pre-cursor should be adequate. Most links should be operable without any TX de-emphasis.
- 2. Connect the EVM in to the system. Typically this will consist of the following topology: BERT TX or ASIC TX \rightarrow SMA cables \rightarrow channel_1 \rightarrow Huber+Suhner cables \rightarrow DS250DF810 EVM RXn \rightarrow DS250DF810 EVM TXn \rightarrow Huber+Suhner cables \rightarrow channel_2 \rightarrow SMA cables \rightarrow BERT RX or ASIC RX
 - 1. After making your data rate selection, push the "Initialize Channel" button on the Receiver tab. You only need to press this once, provided you do not change data rate or adapt mode. If you want to re-lock the CDR, simply press the "Reset channel CDR" button.
 - 2. Check the Signal Detect, CDR lock, and Adapt Complete status indicators to see if the link is established.
 - 3. If the CDR is in lock, the corresponding lock LED on the EVM will light up.
- 3. Check the Horizontal Eye Opening (HEO) and Vertical Eye Opening (VEO) by clicking on the Acquire HEO/VEO "On" button.
- 4. Check the Retimer Receiver's bit error rate by launching the PRBS pattern checker from the Receiver tab. If necessary, tune the link partner transmitter's FIR settings to achieve the target BER.
- 5. Tune the Retimer TX FIR settings. It is best to demonstrate that the return path (Retimer TX to BERT/ASIC RX) is working first before trying to optimize the Retimer RX parameters. One way to do this would be to test over a simple channel_1 first to prove that the Retimer can drive data error-free into the BERT/ASIC (optimizing the Retimer TX FIR as needed) then switch to the more difficult channel_1 while keeping channel_2 unchanged.

Things to watch for:

- 1. At 25-28Gbps data rates, small imperfections in the channel can be problematic. Ensure that cables are properly torqued (not over-torqued), paddle cards are properly mated with backplane connectors, and the BERT RX is properly aligned to the incoming data stream.
- 2. When adding up the total channel loss, do not forget to include the loss of the test fixture and cables. For example, the DS250DF810 EVM board plus Huber+Suhner cables have ~4dB of insertion loss from the device output to the Huber+Suhner cable end; and another ~4dB from the Huber+Suhner cable end to the device input.

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Test Case Examples

www.ti.com

4 Test Case Examples

The following is an example test case with results collected using this EVM.

- Data Rate: 25.78125Gbps
- Data pattern: PRBS31
- Backplane insertion loss: -35dB @ 12.9GHz
- Crosstalk at victim RX: 4.1 mV RMS (24.1 mVppd)
- Victim TX amplitude: 1200mVppd
- Victim TX FIR: C(-1)=-4, C(0)=24, C(+1)=-3
- Adapt mode: 2
- Adapted RX CTLE: [3,0,0,0]
- Adapted DFE: [-0x14, +0x2, +0x1, -0x2, 0x0]

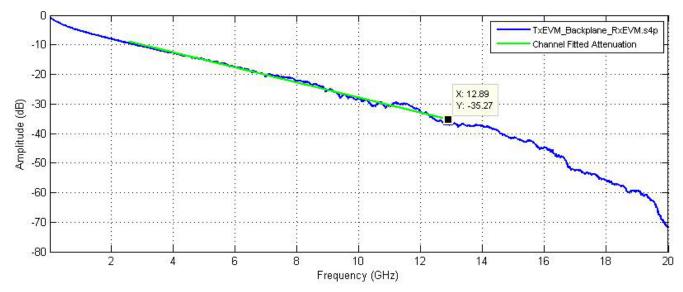


Figure 20. SDD21 Loss Characteristic of Example Test Case

Results:

- Error count = 0, BER < 1E-13
- Horizontal eye opening (HEO): 0.44UI @ 1.5E-5
- Vertical eye opening (VEO): 190mV @ 1.5E-5
- Eye plot:

-1.000 -0.750 -0.500 -0.250 0 +0.250 +0.500 +0.750 +1.000 +300.0 +290.6 +281.3+271.9+262.5 +253.1 +243.8 ++ +234.4+++225.0 +++ +215.6 ++-+206.3 +++ +196.9 ++-+187.5 +178.1 +168.8 +159.4

+150.0	+++++++++++++++++++++++++++++++++++++++
+140.6	+++++++++++++++++++++++++++++++++++++++
+131.3	***************************************
+121.9	+++++++++++++++++++++++++++++++++++++++
+112.5	***************************************
+103.1	*****
+93.8	+++++++++++++++++++++++++++++++++++++++
+84.4	***************************************
+75.0	*****
+65.6	+++++++++++++++++++++++++++++++++++++++
+56.3	+++++++++++++++++++++++++++++++++++++++
+46.9	+++++++++++++++++++++++++++++++++++++++
+37.5	*****
+28.1	+++++++++++++++++++++++++++++++++++++++
+18.8	+++++++++++++++++++++++++++++++++++++++
+9.4	+++++++++++++++++++++++++++++++++++++++
+0.0	+++++++++++++++++++++++++++++++++++++++
-9.4	+++++++++++++++++++++++++++++++++++++++
-18.8	+++++++++++++++++++++++++++++++++++++++
-28.1	+++++++++++++++++++++++++++++++++++++++
-37.5	+++++++++++++++++++++++++++++++++++++++
-46.9	+++++++++++++++++++++++++++++++++++++++
-56.3	+++++++++++++++++++++++++++++++++++++++
-65.6	***************************************
-75.0	***************************************
-84.4	***************************************
-93.8	***************************************
-103.1	***************************************
-112.5	***************************************
-121.9	+++++++++++++++++++++++++++++++++++++++
-131.3	+++++++++++++++++++++++++++++++++++++++
-131.5	++++++++++++++******++++
-140.0	+++++++++++++++++++++++++++++++++++++++
-150.0	+++++++++++++++++++++++++++++++++++++++
-159.4	
	+++++++++++++++++++++++++++++++++++++++
-178.1	*****
-187.5	++++++++++++**************************
-196.9	+++++++++++****************************
-206.3	+++++++++++++++++++++++++++++++++++++++
-215.6	+++++++++++****************************
-225.0	+++++++********************************
-234.4	++++*+*+**************+++++++++++++++++
-243.8	+*+*********************+++++++++++++++
-253.1	***************************************
-262.5	***************************************
-271.9	***************************************
-281.3	***************************************
-290.6	***************************************
	++
-	1.000 -0.750 -0.500 -0.250 0 +0.250 +0.500 +0.750 +1.000

5 Supplemental Documents

All the EVM design, layout, and other files which are relevant to this EVM are listed below:

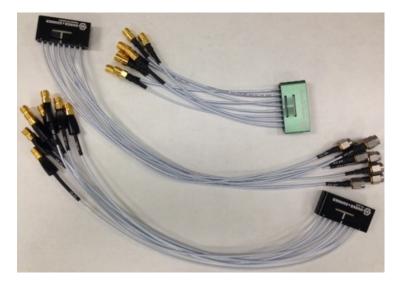
FILE DESCRIPTION	FILE NAME
Schematic PDF	DS280DF810_MW_Rev3-01-23-2015.pdf
Board layout file	DS280XX810_EVM_BRD_REVC_15-0024_PCB_030615-1.brd
Board Gerbers	DS280XX810_EVM_BRD_REVC_15-0024_GBR_031915-1.zip
Board s-parameters folder	EVM/s_parameters/



www.ti.com

6 EVM Cable Assemblies

The DS250DF810EVM uses Huber+Suhner 1x8 MXP cable assemblies.



To inquire about purchasing cable assemblies from Huber+Suhner, contact:

Info.us@hubersuhner.com HUBER+SUHNER Inc. 8530 Steele Creek Place Drive, Suite H Charlotte-NC- 28273 +1 704-790-7300

There are three part numbers that TI suggests using with this EVM:

- 1. 85014420, MF53/1x8A_21MXP/21SMA/152: "MXP-15 cable assembly". This is a lower cost cable assembly compared to the MXP-40, but the SI performance is very good and more than adequate for 25Gbps operation.
- 2. 84099607, MF53/1x8A_21MXP/11SK/305: "MXP-40 cable assembly". This cable assembly is designed specifically for 40+ GHz. It features a male cable end and longer cable length options.
- 3. 84098900, MF53/1x8A_21MXP/21SK_ergo/305: "MXP-40 cable assembly". This cable assembly is designed specifically for 40+ GHz. It features a female cable end and longer cable length options.

Huber+Suhner brochure available here.



Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Ch	anges from Original (October 2015) to C Revision	Pag	е
•	Initial Public Release		3

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