1 Overview

The DS90LV047-48AEVM is an evaluation module designed for performance and functional evaluation of the Texas Instruments DS90LV047A 3-V LVDS Quad CMOS Differential Line Driver and DS90LV048A 3-V LVDS CMOS Differential Line Receiver. With this kit, users can quickly evaluate the output waveform characteristics and signal integrity supported by the DS90LV047A and DS90LV048A. Header pins allow access to the DS90LV047A and DS90LV048A inputs and outputs and also facilitate connection to lab equipment or user systems for performance evaluation.

Figure 1. DS90LV047-48AEVM
2 Features

DS90LV047A:
• Converts Single-Ended LVCMOS to Differential LVDS
• >400 Mbps (200 MHz) Switching Rates
• Single Supply Operation: VDD = 3.3 V ± 5%
• ± 350 mV LVDS Signaling
• Low Power (13 mW at 3.3 V Static)

DS90LV048A:
• Converts Differential LVDS to Single-Ended LVCMOS
• >400 Mbps (200 MHz) Switching Rates
• Single Supply Operation: VDD = 3.3 V ± 5%
• Accepts Small ±35 mV Differential Signaling
• Low Power Design (40 mW at 3.3 V Static)

3 Applications

• Wireless/Telecom Infrastructure
• Medical/Health
• Multi-Function Printers
• Factory Automation and Control
• EPOS/ECR/Cash Drawer

4 Ordering Information

<table>
<thead>
<tr>
<th>EVM ID</th>
<th>Device ID</th>
<th>Device Package</th>
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<tr>
<td>DS90LV047-48AEVM</td>
<td>DS90LV047A, DS90LV048A</td>
<td>SOIC</td>
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</table>
5 Setup

The DS90LV047A is a LVDS Quad CMOS Differential Line Driver, and the DS90LV048A is a LVDS Quad CMOS Differential Line Receiver. When operating the DS90LV047-48AEVM, jumper setting definitions can be referenced in Table 1, while signal input and output connection descriptions can be found in Figure 2 and Figure 3. When using the DS90LV047A and DS90LV048A together, the typical configuration is to connect the DS90LV047A outputs (J4) such that they drive the inputs of the DS90LV048A (J1).

Table 1. Description of Jumper Settings

<table>
<thead>
<tr>
<th>Component</th>
<th>Name</th>
<th>Comments</th>
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<tr>
<td>J8</td>
<td>GND</td>
<td>GND power supply</td>
</tr>
<tr>
<td>J7</td>
<td>VDD</td>
<td>3.3 V VDD power supply</td>
</tr>
<tr>
<td>J3</td>
<td>ENABLE1</td>
<td>Leave Pins 1 and 2 open, and tie Pins 3 and 4 to enable DS90LV048A.</td>
</tr>
<tr>
<td>J6</td>
<td>ENABLE2</td>
<td>Leave Pins 1 and 2 open, and tie Pins 3 and 4 to enable DS90LV047A.</td>
</tr>
</tbody>
</table>

Figure 2. DS90LV047-48AEVM Input and Output Diagram
5.1 Hardware Description and Setup

For hardware setup and connections, reference the diagrams in Figure 3 and Figure 4.

1. Connect a 3.3 V DC power supply (30 mA max) to the EVM.
   • Connect J7: VIN = 3.3 V and J8: GND.

2. Install the default shunt jumpers for appropriate operation, as shown in Figure 4.
   • Install a shunt jumper on J3 Pins 3-4 to tie DS90LV048A NEN to GND.
   • Install a shunt jumper on J6 Pins 3-4 to tie DS90LV047A NEN to GND.

3. Apply a high-speed 3.3 V LVCMOS signal to the DS90LV047A inputs on header J5.

4. The DS90LV047A LVDS output signals can be measured differentially on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J4 to measure the differential signal across the 100 $\Omega$ termination resistors R15-R18. The expected output waveform is a ±350 mV LVDS signal.

5. Apply a high-speed ±350 mV (700 mVpp differential) LVDS signal to the DS90LV048A inputs on header J1. If desired, the LVDS inputs can be provided by connecting the LVDS outputs on header J4 to the desired LVDS input pins on header J1. If this is done, remove resistors R15-R18 to avoid double-termination.

6. The DS90LV048A LVCMOS output signals can be measured on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J2.
Figure 4. DS90LV047-48AEVM Setup Configuration

In order to measure LVDS signals properly, a 100 Ω termination resistor must be present across each differential pair at the point of measurement. However, if multiple 100 Ω termination resistors are placed across a differential pair between the transmitter and receiver, the signal becomes double terminated. Double termination should be avoided, since this reduces the output amplitude and noise margin.

By factory default, the DS90LV047-48AEVM comes with stuffed termination resistors R1-R4 on the DS90LV048A inputs and stuffed termination resistors R15-R18 on the DS90LV047A outputs.

Remove R15-R18...
- if the DS90LV047A output interfaces with a DS90LV048A input by connecting J4 to J1.
- if the DS90LV047A output interfaces with an external load that has an appropriate 100 Ω differential termination.

Populate R15-R18 with 100 Ω termination resistors (or leave R15-R18 populated)...
- if the DS90LV047A output is measured by a high-impedance differential probe.
- if the DS90LV047A output interfaces with an external load that does not have an appropriate 100 Ω differential termination.
5.2 DS90LV047-48AEVM Performance Plots

The following plots show typical waveforms measured on the DS90LV047-48AEVM inputs and outputs using the hardware setup in Figure 4. For these measurements, the following parameters were used:

- Operating Frequency: 200 MHz (400 Mbps)
- DS90LV047A Input: 3.3 V LVCMOS sine wave to DIN1
- DS90LV047A Output: Measured with 100 Ω termination resistor R15 populated across DOUT1±
- DS90LV048A Input: LVDS signal to RIN1± from DS90LV047A output DOUT1±. 100 Ω termination resistor R15 removed
- DS90LV048A Output: Measured at ROUT1

Figure 5. DS90LV047A 3.3 V LVCMOS Input
Figure 6. DS90LV047A Differential LVDS Output
Figure 7. DS90LV047A Single-Ended LVDS Output
Figure 8. DS90LV048A LVCMOS Output
# Bill of Materials

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<th>Part Number</th>
<th>Description</th>
<th>Designator</th>
<th>Footprint</th>
<th>Quantity</th>
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<tr>
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<td>C1, C2</td>
<td>0402</td>
<td>2</td>
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<td>GRM188R61A106ME69</td>
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<td>LED_SML-LX0603GW</td>
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<tr>
<td>Fiducial</td>
<td>Fiducial mark. There is nothing to buy or mount.</td>
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<td>Fiducial10-20</td>
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<td>NY PMS 440 0025 PH</td>
<td>Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead</td>
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<td>NY PMS 440 0025 PH</td>
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<td>ERJ-2GEO00X</td>
<td>RES, 0, 5%, 0.063 W, 0402</td>
<td>R5, R6, R7, R8</td>
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<td>SNT-100-BK-G</td>
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<td>3V LVDS Quad CMOS Differential Line Receiver, 16-pin Narrow SOIC, Pb-Free</td>
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<td>M16A_N</td>
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Figure 9 and Figure 10 show the DS90LV047-48AEVM layout. The DS90LV047A and DS90LV048A inputs and outputs can be accessed via header pins.
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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

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This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:
(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

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