EVM User's Guide: DS320PR410-RSC-EVM

DS320PR410-RSC-EVM Evaluation Module

Description

The DS320PR410-RSC-EVM evaluation module provides a complete high-bandwidth platform for evaluating the signal conditioning features of the Texas Instruments DS320PR410 Four-Channel PCI-Express 5.0 Linear Redriver. This evaluation board can be used for standard compliance testing, performance evaluation, and initial system prototyping.

Get Started

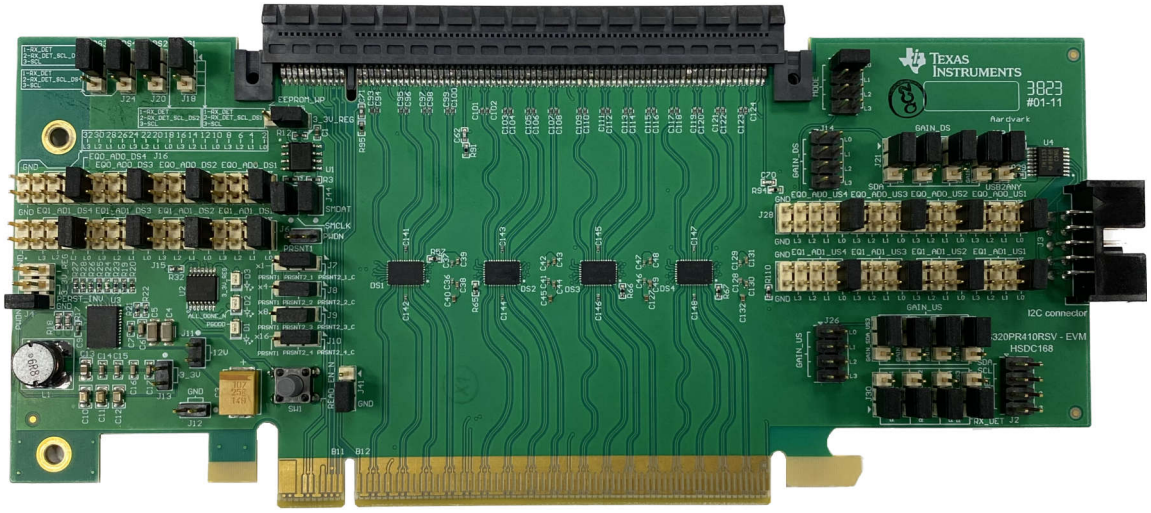
1. Order the DS320PR410-RSC-EVM on ti.com
2. Read through the instructions provided in this User's Guide to understand the jumper options provided on the DS320PR410-RSC-EVM and for instructions to configure the EVM.
3. For EEPROM or SMBus / I^2C programming, visit the TI SigCon Architect download page to install the Texas Instruments SigCon Architect GUI. To download the DS320PR410 SigCon Architect GUI profile, please contact your TI representative or create a request using TI E2E.

Features

- PCIe x16 Riser Card option with eight 4-channel unidirectional linear redrivers operating at rates up to 32Gbps
- Linear equalization for seamless support of link training and PCIe channel extension
- CTLE boosts up to 22 dB at 16 GHz
- Programmable device configuration through EEPROM, GPIO, I^2C, or SMBus
- Onboard 12-V to 3.3-V, 2-A step-down DC/DC converter
- Industrial temperature range: –40°C to 85°C
- Flow-through layout in 4 mm × 6 mm, 40-pin, lead-less WQFN 0.4-mm pitch package

Applications

- PCI Express Gen-1, 2, 3, 4, and 5
- High-speed interfaces up to 32Gbps
- Enterprise server motherboard, workstation
- Enterprise storage
- Enterprise add-in card, end-point



DS320PR410-RSC-EVM – Top Side View

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1 Evaluation Module Overview

1.1 Introduction

The DS320PR410-RSC-EVM evaluation module features eight DS320PR410 linear redrivers that can extend the transmission distance of a PCIe Gen-5 x16 bus. The evaluation module can directly be plugged into a PCIe slot on a server or PC motherboard using one end of the board, and paired up with a PCIe add-in card using the straddle mount connector attached to the other end of the board.

This user's guide describes the characteristics, operation, and use of the DS320PR410-RSC-EVM evaluation module. The user's guide details how to set up and configure hardware and reviews various aspects of the software operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the DS320PR410-RSC-EVM. This user's guide also provides information on the operating procedure, input and output connections, an electrical schematic, printed circuit board (PCB) layout drawings, and a Bill of Materials (BOM) for the EVM.

1.2 Kit Contents

The EVM kit contains one (1) DS320PR410-RSC-EVM. Contact the Texas Instruments Product Information Center nearest you if any components are missing. TI highly recommends that users check the TI website at ti.com to verify that the latest versions of the related software is being used.

1.3 Specification

The DS320PR410-RSC-EVM is targeted for applications where PCI-Express riser card slots (up to x16) are available for test. Figure 1-1 shows the DS320PR410-RSC-EVM used with a system motherboard with a PCI-Express Gen5.0 capable CPU and an Add-In Card Endpoint.

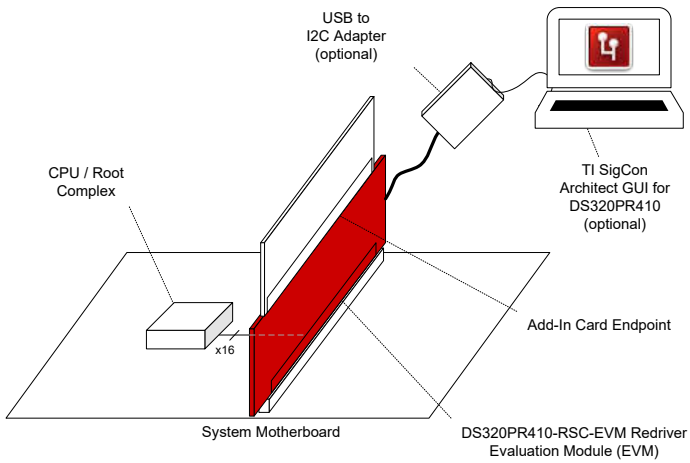

Figure 1-1. DS320PR410-RSC-EVM Example Application Diagram

1.4 Device Information

The DS320PR410 is a four-channel low-power high-performance linear redriver designed to support PCI-Express Gen5.0, CXL 2.0, UPI 2.0, and other interfaces up to 32Gbps. Each device is pin-strap, EEPROM, or I^2C / SMBus configurable.

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2 Hardware

The Hardware section details DS320PR410-RSC-EVM hardware control features, the SMBus / I^{2}C control interface, and quick-start guidelines.

2.1 DS320PR410 5-Level I/O Control Inputs

Each DS320PR410 features 5-level input pins (MODE, GAIN, RX_DET, EQ0 / ADDR0, and EQ1 / ADDR1) that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the four valid levels to provide a wider range of control settings.

Table 2-1. Five-Level Control Pin Settings

PIN LEVEL	PIN SETTING
L0	1 kΩ to GND
L1	8.25 kΩ to GND
L2	24.9 kΩ to GND
L3	75 kΩ to GND
L4	Float

2.2 DS320PR410 Modes of Operation

Each DS320PR410 can be configured to operate in either Pin Mode, SMBus with I^{2}C Primary Mode (EEPROM Mode), or SMBus with I^{2}C Secondary Mode. The mode of operation of the DS320PR410 is determined by the pin strap setting on the MODE pin as shown in Table 2-2.

Table 2-2. Modes of Operation

MODE PIN LEVEL	MODE OF OPERATION
L0	Pin Mode
L1	SMBus Mode or I^{2}C Primary Mode (EEPROM Mode)
L2	SMBus Mode or I^{2}C Secondary Mode
L3	RESERVED
L4	RESERVED

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2.3 DS320PR410 SMBus or I²C Register Control Interface

Each DS320PR410 internal registers can be accessed through standard SMBus protocol. The DS320PR410 features one bank of channels, Channels 0–3. The SMBus secondary address pairs (one for each device) are determined at power up based on the configuration of the EQ0 / ADDR0 and EQ1 / ADDR1 pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

There are 16 unique SMBus secondary addresses that can be assigned to the device by placing external resistor straps on the EQ0 / ADDR0 and EQ1 / ADDR1 pins as shown in Table 2-3. When multiple DS320PR410 devices are on the same SMBus interface bus, each device must be configured with a unique SMBus secondary address.

Table 2-3. DS320PR410 SMBus Address Map

ADDR1 Pin Level	ADDR0 Pin Level	DS320PR410 7-Bit Address [HEX]
L0	L0	0x18
L0	L1	0x1A
L0	L2	0x1C
L0	L3	0x1E
L0	L4	Reserved
L1	L0	0x20
L1	L1	0x22
L1	L2	0x24
L1	L3	0x26
L1	L4	Reserved
L2	L0	0x28
L2	L1	0x2A
L2	L2	0x2C
L2	L3	0x2E
L2	L4	Reserved
L3	L0	0x30
L3	L1	0x32
L3	L2	0x34
L3	L3	0x36
L3	L4	Reserved

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2.4 DS320PR410 Equalization Control

Each channel of the DS320PR410 features a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. Table 2-4 shows available equalization boost through EQ control pins (EQ1 and EQ0) when in Pin Control mode (MODE = L0).

Table 2-4. Equalization Control Settings

EQ INDEX	EQ1 PIN LEVEL	EQ0 PIN LEVEL	CTLE BOOST AT 8 GHz (dB)	CTLE BOOST AT 16 GHz (dB)
0	L0	L0	For CTLE boost values at 8 GHz, please reference the DS320PR410 data sheet (SNLS739).	For CTLE boost values at 16 GHz, please reference the DS320PR410 data sheet (SNLS739).
1	L0	L1		
2	L0	L2		
5	L1	L0		
6	L1	L1		
7	L1	L2		
8	L1	L3		
9	L1	L4		
10	L2	L0		
11	L2	L1		
12	L2	L2		
13	L2	L3		
14	L2	L4		
15	L3	L0		
16	L3	L1		
17	L3	L2		
18	L3	L3		
19	L3	L4		

The equalization gain of each channel of each device can also be set by writing to SMBus / I^2C registers in I^2C Mode. Refer to the *DS320PR410 Programming Guide* for details.

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2.5 DS320PR410 RX Detect State Machine

Each DS320PR410 deploys an RX Detect state machine that governs the RX detection cycle as defined in the PCI Express specification. At power up or after a manually triggered event, the redriver determines whether or not a valid PCI Express termination is present at the far end of the link. When the DS320PR410 is in Pin Mode (MODE = L0), the RX_DET pin of DS320PR410 provides additional flexibility to system designers to appropriately set the device in their desired mode, according to Table 2-5.

Table 2-5. Receiver Detect State Machine Settings

PD PIN LEVEL	RX_DET PIN LEVEL	DS320PR410 Channel RX Common-mode Impedance	DESCRIPTION
L	L0	Always 50 Ω	PCI Express RX detection state machine is disabled. Recommended for non-PCI Express use cases.
L	L1	Pre Detect: Hi-Z Post Detect: 50 Ω	Outputs poll until 3 consecutive valid detections.
L	L2	Pre Detect: Hi-Z Post Detect: 50 Ω	Outputs poll until 2 consecutive valid detections.
L	L3	N/A	Reserved
L	L4 (Float)	Pre Detect: Hi-Z Post Detect: 50 Ω	TX polls approx. every 150 µs until valid termination is detected. Rx CM impedance held at Hi-Z until detection. Reset by asserting PD high for 200 µs then low.
H	X	Hi-Z	Reset all DS320PR410 channels signal path and set their Rx impedance state to Hi-Z.

The RX Detect state of each channel of each device can also be set by writing to SMBus / I^2C registers in Secondary or Primary Modes. Refer to the *DS320PR410 Programming Guide* for details.

2.6 DS320PR410 DC Gain Control

When operating in Pin Mode (MODE = L0), the GAIN pin can be used to set the overall data-path flat gain (DC and AC) of the DS320PR410 for channels 0-3 as shown in Table 2-6.

Table 2-6. GAIN Control

GAIN/SDA PIN LEVEL	GAIN SETTING
L0	–6 dB (-5.6dB actual)
L1	–4 dB (-3.8dB actual)
L2	-2 dB (-1.2dB actual)
L3	+2 dB (+2.6dB actual)
L4 (Float)	0 dB (+0.6dB actual - recommended for most use cases)

The DC gain of each channel of each device can also be set by writing to SMBus / I^2C registers in Secondary or Primary Modes. Refer to the *DS320PR410 Programming Guide* for details.

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2.7 DS320PR410 EVM Global Controls

Table 2-7 shows DS320PR410-RSC-EVM global controls that affect all devices on the board.

Table 2-7. EVM Global Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J1	4x2 Header	MODE control tied to MODE pins of all eight DS320PR410 devices on the EVM L0: All devices set to Pin Mode (**Default**) L1: All devices set to SMBus / I²C Primary Mode (EEPROM Mode) L2: SMBus / IC Secondary Mode L3: Reserved L4: Reserved
J2	4x2 Header	RX_DET control tied to RX_DET pins of all eight DS320PR410 devices on the EVM L0: RX Detect state machine disabled on all devices L1: RX Detect state machine enabled on all devices (3 valid detections needed) L2: RX Detect state machine enabled on all devices (2 valid detections needed) L3: Reserved L4: RX Detect state machine enabled on all devices (1 valid detection needed) - **Default**
J3	5x2 Header	SMBus / I²C interface. All eight DS320PR410 devices on the EVM are on the same bus and can be accessed through this interface.
J4	3x2 Header	PWDN control tied to PD pins of all eight DS320PR410 devices on the EVM. **Remove shunt on J6 when using J4 to control PWDN.** PWDN tied to GND: All devices enabled (**Default**) PWDN tied to PERST_INV: All device PD pins controlled by inverted PCIe Reset (PERST#) PWDN tied to 3.3V_REG: All devices disabled. PWDN floating: Tie PCIe system PRSNT signal to PWDN using J6 for the PWDN control (optional for PCIe use case)
J5	3x1 Header	Access point to the WP (write protect) pin of the onboard EEPROM devices. WP tied to GND: I²C Access to the EEPROM enabled WP floating: I²C Access to the EEPROM disabled (**Default**)
J6	2x1 Header	Alternative PWDN Control. **Remove shunt on J4 when using J6 to control PWDN.** PWDN floating: Use J4 for the PWDN control (**Default**) PWDN tied to PRSNT: PRSNT signal controls PWDN (optional for PCIe use case).
J7, J8, J9, J10	3x1 Headers	PCIe PRSNT Signal Controls Tie pins 1-2 on J7, J8, J9, and J10: Allow support any PCIe bus width (**Default**) Tie pins 2-3 of J7, leave J8, J9, and J10 floating: Force x1 PCIe bus width. Tie pins 2-3 of J8, leave J7, J9, and J10 floating: Force x4 PCIe bus width. Tie pins 2-3 of J9, leave J7, J8, and J10 floating: Force x8 PCIe bus width. Tie pins 2-3 of J10, leave J7, J8, and J9 floating: Force x16 PCIe bus width.
J11	2x1 Header	Onboard regulator input. Apply 12 V when using the EVM as a standalone system. DO NOT APPLY power if plugging the EVM into a system as the power is provided through the gold finger connector (CONN1).
J12	2x1 Header	Access point to the GND reference.
J13	2x1 Header	Onboard 3.3 V output.
J38	3x1 Header	Select I²C adapter to plug into Connector J3. Tie pins 1-2 for TI USB2ANY Adapter Tie pins 2-3 for Aardvark Adapter (**Default**) **Select the appropriate jumper position for the selected adapter to avoid damaging the EVM.**
J41	3x1 Header	READ_EN_N select Tie pins 1-2 to tie READ_EN_N to GND and initiate EEPROM read (EEPROM mode only) - **Default** Tie pins 2-3 to tie READ_EN_N to disable EEPROM read
J44	2x1 Header	SMDAT header to connect global SMBus Data line (Pin 1) to local SMDAT/SDA (Pin 2). Remove shunt to disconnect global SMDAT from local SMDAT/SDA.
J45	2x1 Header	SMCLK header to connect global SMBus Clock line (Pin 1) to local SMCLK/SCL (Pin 2). Remove shunt to disconnect global SMCLK from local SMCLK/SCL.

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2.8 DS320PR410-RSC-EVM Downstream Devices Control

Table 2-8 shows the DS320PR410-RSC-EVM downstream device controls that affect DS1, DS2, DS3, and DS4 devices on the board.

Table 2-8. EVM Downstream Devices Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J14	4x2 Header	Gain Controls tied to GAIN pins of all downstream device banks (GAIN_DS) L0: –6 dB Gain Setting L1: –4 dB Gain Setting L2: -2 dB Gain Setting L3: +2 dB Gain Setting L4: 0 dB Gain Setting (**Default**)
J15	17x2 Header	Pin Mode (**Default**): EQ1 controls for each downstream device and device bank. Use pins 1–8 for configuring EQ1 pin of DS1 device. Use pins 9–16 for configuring EQ1 pin of DS2 device. Use pins 17–24 for configuring EQ1 pin of DS3 device. Use pins 25–32 for configuring EQ1 pin of DS4 device. SMBus, I^2C Modes: ADDR1 controls for each downstream device. Use pins 1–8 for configuring ADDR1 pin of DS1 device. Use pins 9–16 for configuring ADDR1 pin of DS2 device. Use pins 17–24 for configuring ADDR1 pin of DS3 device. Use pins 25–31 for configuring ADDR1 pin of DS4 device. Install a shunt to achieve L0, L1, L2 or L3 level on the pin. Leave floating to achieve L4 level on the pin.
J16	17x2 Header	Pin Mode (**Default**): EQ0 controls for each downstream device and device bank. Use pins 1–8 for configuring EQ0 pin of DS1 device. Use pins 9–16 for configuring EQ0 pin of DS2 device. Use pins 17–24 for configuring EQ0 pin of DS3 device. Use pins 25–32 for configuring EQ0 pin of DS4 device. SMBus, I^2C Modes: ADDR0 controls for each downstream device. Use pins 1–8 for configuring ADDR0 pin of DS1 device. Use pins 9–16 for configuring ADDR0 pin of DS2 device. Use pins 17–24 for configuring ADDR0 pin of DS3 device. Use pins 25–31 for configuring ADDR0 pin of DS4 device. Install a shunt to achieve L0, L1, L2 or L3 level on the pin. Leave floating to achieve L4 level on the pin.
J17	3x1 Header	GAIN / SDA Dual Function Pin Provision for DS1 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J18	3x1 Header	RX_DET / SCL Dual Function Pin Provision for DS1 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J19	3x1 Header	GAIN / SDA Dual Function Pin Provision for DS2 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J20	3x1 Header	RX_DET / SCL Dual Function Pin Provision for DS2 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J21	3x1 Header	GAIN / SDA Dual Function Pin Provision for DS3 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J22	3x1 Header	RX_DET / SCL Dual Function Pin Provision for DS3 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes

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Table 2-8. EVM Downstream Devices Controls (continued)

COMPONENT	NAME	FUNCTION / DESCRIPTION
J23	3x1 Header	GAIN / SDA Dual Function Pin Provision for DS4 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J24	3x1 Header	RX_DET / SCL Dual Function Pin Provision for DS4 Device Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes

2.9 DS320PR410-RSC-EVM Upstream Devices Control

Table 2-9 shows DS320PR410-RSC-EVM upstream devices controls that affect US1, US2, US3, and US4 devices on the board.

Table 2-9. EVM Upstream Devices Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J26	4x2 Header	Gain Controls tied to GAIN pins of all downstream device banks (GAIN_US) L0: –6 dB Gain Setting L1: –4 dB Gain Setting L2: -2 dB Gain Setting L3: +2 dB Gain Setting L4: 0 dB Gain Setting (**Default**)
J27	17x2	Pin Mode (**Default**): EQ1 controls for each downstream device and device bank. Use pins 1–8 for configuring EQ1 pin of US1 device. Use pins 9–16 for configuring EQ1 pin of US2 device. Use pins 17–24 for configuring EQ1 pin of US3 device. Use pins 25–32 for configuring EQ1 pin of US4 device. SMBus, I^2C Modes: ADDR1 controls for each downstream device. Use pins 1–8 for configuring ADDR1 pin of US1 device. Use pins 9–16 for configuring ADDR1 pin of US2 device. Use pins 17–24 for configuring ADDR1 pin of US3 device. Use pins 25–31 for configuring ADDR1 pin of US4 device. Install a shunt to achieve L0, L1, L2 or L3 level on the pin. Leave floating to achieve L4 level on the pin.
J28	17x2 Header	Pin Mode (**Default**): EQ0 controls for each downstream device and device bank. Use pins 1–8 for configuring EQ0 pin of US1 device. Use pins 9–16 for configuring EQ0 pin of US2 device. Use pins 17–24 for configuring EQ0 pin of US3 device. Use pins 25–32 for configuring EQ0 pin of US4 device. SMBus, I^2C Modes: ADDR0 controls for each downstream device. Use pins 1–8 for configuring ADDR0 pin of US1 device. Use pins 9–16 for configuring ADDR0 pin of US2 device. Use pins 17–24 for configuring ADDR0 pin of US3 device. Use pins 25–31 for configuring ADDR0 pin of US4 device. Install a shunt to achieve L0, L1, L2 or L3 level on the pin. Leave floating to achieve L4 level on the pin.
J29	3x1 Header	GAIN / SDA Dual Function Pin Provision for US1 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J30	3x1 Header	RX_DET / SCL Dual Function Pin Provision for US1 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J31	3x1 Header	GAIN / SDA Dual Function Pin Provision for US2 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes

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Table 2-9. EVM Upstream Devices Controls (continued)

COMPONENT	NAME	FUNCTION / DESCRIPTION
J32	3x1 Header	RX_DET / SCL Dual Function Pin Provision for US2 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J33	3x1 Header	GAIN / SDA Dual Function Pin Provision for US3 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J34	3x1 Header	RX_DET / SCL Dual Function Pin Provision for US3 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J35	3x1 Header	GAIN / SDA Dual Function Pin Provision for US4 Device. Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes
J36	3x1 Header	RX_DET / SCL Dual Function Pin Provision for US4 Device Install shunt across pins 1-2 for operation in Pin Mode (**Default**) Install shunt across pins 2-3 for operation in SMBus, I^2C Modes

2.10 Quick-Start Guide (Pin Mode)

Check that the shunts are at the following positions as follows:

1. The redrivers are configured to operate in Pin Mode (MODE pins tied to L0 using J1 header).
2. RX Detect state machine of all redrivers is enabled by leaving J2 open (L4 - floating).
3. The redrivers are enabled (PWDN pins tied to GND by placing a shunt between pins 5-6 on the J4 header). Alternatively, for PCIe sideband signal control, the PWDN pins can be driven by PCIe Present (PRSNT1#) signal by leaving J4 open and placing a shunt across pins 1 and 2 of J6, or by inverted PCIe Reset (PERST#) signal by placing a shunt between pins 3-4 on J4 and by leaving J6 open.
4. The redrivers are connected to RX_DET and GAIN using the dual function pins at headers J17-J24 and J29-J36 in Table 2-7. Set the shunts for these headers to connect pins 1-2.
5. The board is configured for any PCIe bus width (PRSNTx# signal controls set as 'default' in Table 2-7 using J7, J8, J9 and J10 headers). Shunts need to be placed between pins 1-2 on headers J7, J8, J9, and J10.
6. DC Gain of all redrivers is set to 0 dB by leaving J14 open for the downstream redrivers and by leaving J26 open for the upstream redrivers.
7. EQ level of the RX CTLEs of all redrivers is set to 10 dB at 16 GHz by using J15 and J16 for the downstream redrivers and J27 and J28 for the upstream redrivers (EQ1 = L2, EQ0 = L0).
8. If necessary, adjust EQ levels of the downstream redrivers, or upstream redrivers, or both, by arranging shunts on J15 and J16 for downstream redrivers and J27 and J28 for the upstream redrivers.
9. Plug the EVM into a PCIe x16 server motherboard slot. Make sure the motherboard is powered down before installing the EVM or configured for hot-plug operation.
10. Install a compatible PCIe endpoint card into the straddle connector of the EVM.
11. Power-up the motherboard.

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2.11 Quick-Start Guide (SMBus / I²C Secondary Mode)

1. Configure all devices to operate in the SMBus Secondary Mode by setting their MODE pins to the L2 level. This is accomplished by placing a shunt on J1 L2 location.
2. Set a unique SMBus Secondary address for each device by placing shunts in the following arrangement:
   - On J15 connector, place shunts in L0 locations for all downstream devices (DS1, DS2, DS3, and DS4) to set the ADDR1 level for each downstream DS320PR410.
   - On J16 connector, place shunts in L0 location for DS1, L1 location for DS2, L2 location for DS3, and in L3 location for DS4 to set the ADDR0 level for each downstream DS320PR410.
   - On J27 connector, place shunts in L1 locations for all upstream devices (US1, US2, US3, and US4) to set the ADDR1 level for each upstream DS320PR410 device.
   - On J28 connector, place shunts in L0 location for US1, L1 location for US2, L2 location for US3, and in L3 location for US4 to set the ADDR0 level for each upstream DS320PR410.
   - The above arrangement sets the 7-bit SMBus secondary addresses of the DS320PR410 devices as:
     - DS1: 0x18
     - DS2: 0x1A
     - DS3: 0x1C
     - DS4: 0x1E
     - US1: 0x20
     - US2: 0x22
     - US3: 0x24
     - US4: 0x26
3. Move shunts from pins 1-2 to pins 2-3 on J17-J24, J29-J36 to connect the dual function redriver pins to the SMBus / I²C bus. Please reference Table 2-7 for guidance on the dual function pins.
4. Make sure all devices by pulling their PWDN pins to GND. This is accomplished by placing a shunt on J4 between pins 5-6 (PWDN and GND). Alternatively, for PCIe sideband signal control, the PWDN pins can be driven by PCIe Present (PRSNT1#) signal by leaving J4 open and placing a shunt across pins 1 and 2 of J6, or by inverted PCIe Reset (PERST#) signal by placing a shunt between pins 3-4 on J4 and by leaving J6 open.
5. Select the appropriate adapter using J38 (shunt position 1-2 for USB2ANY or 2-3 for Aardvark). Please make sure that the correct shunt setting is selected for your adapter. Otherwise, there is risk of damage to the EVM.
6. Connect a USB2ANY Adapter or Aardvark Adapter to J3 (Note that neither is not supplied with the DS320PR410-RSC-EVM).
7. Install the latest SigCon Architect application and the DS320PR410 profile. Please contact a local FAE for download instructions.
8. Plug the EVM into a PCIe x16 server motherboard slot. Make sure the motherboard is powered down before installing the EVM or configured for hot-plug operation.
9. Install a compatible PCIe endpoint card into the straddle connector of the EVM.
10. Power-up the motherboard.
11. Start the SigCon Architect application.
12. Select the DS320PR410 Configuration Page and click the *Apply* box to enable the device profile. If necessary, edit the devices SMBus addresses in the *Edit Device Addresses* box, then click *Apply*.
13. In the DS320PR410 High Level Page, select *Block Diagram* as shown in Figure 2-1.
14. Select the desired EQ Settings.
15. Select devices you want to apply the selected settings and click *Apply to All Channels*.

Note

To observe the effects of programmed DS320PR410 EQ settings on PCIe lane performance (lane margin, BER, etc.), the PCIe link must be re-trained by toggling PERST# or by performing a warm reset (without removing power to the DS320PR410).

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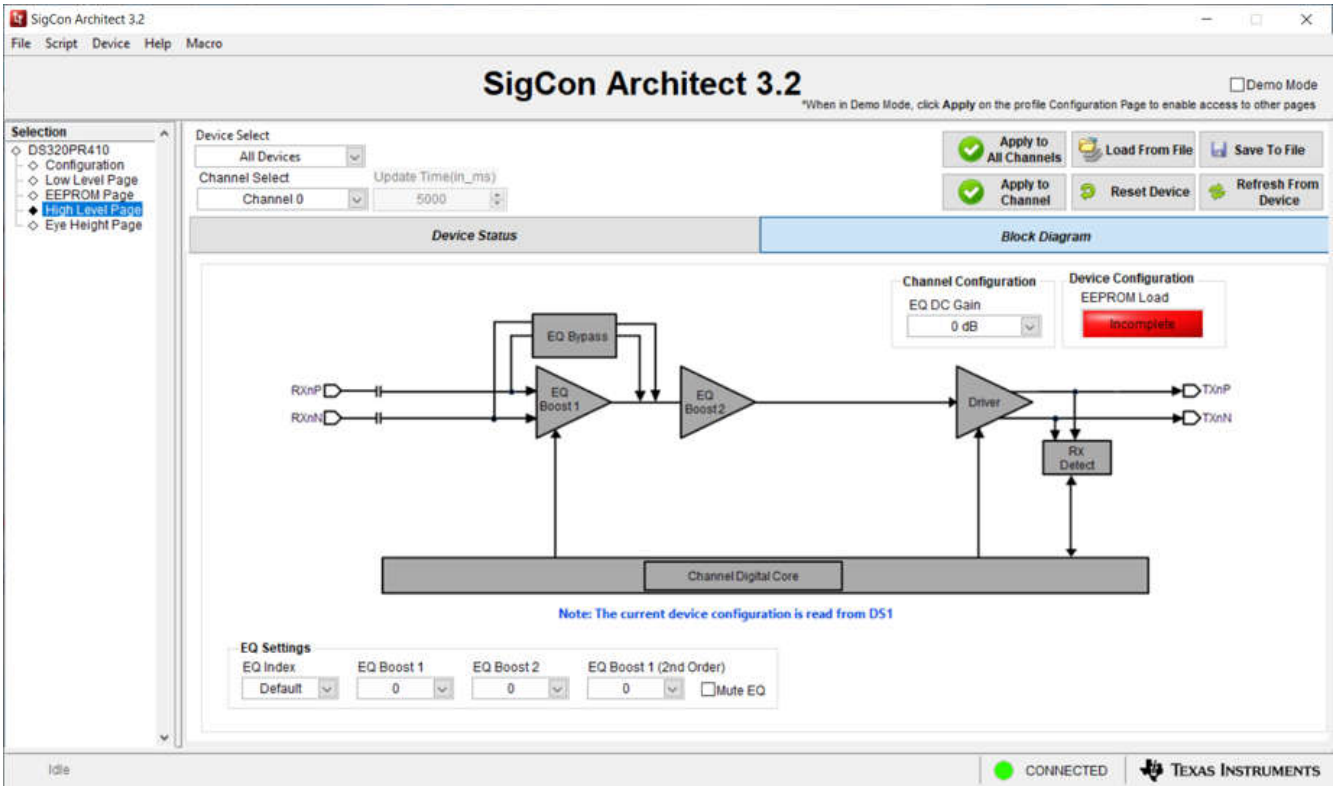

Figure 2-1. SigCon Architect DS320PR410 High-Level Page

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3 Implementation Results

3.1 Test Setup and Results

Figure 3-1 shows a typical system setup with the DS320PR410-RSC-EVM placed between a CPU on a server motherboard and a PCIe end point (Network Interface Card or NIC). Additional *Extender* cards are inserted to increase the channel loss and demonstrate the ability of the redriver to extend the reach.

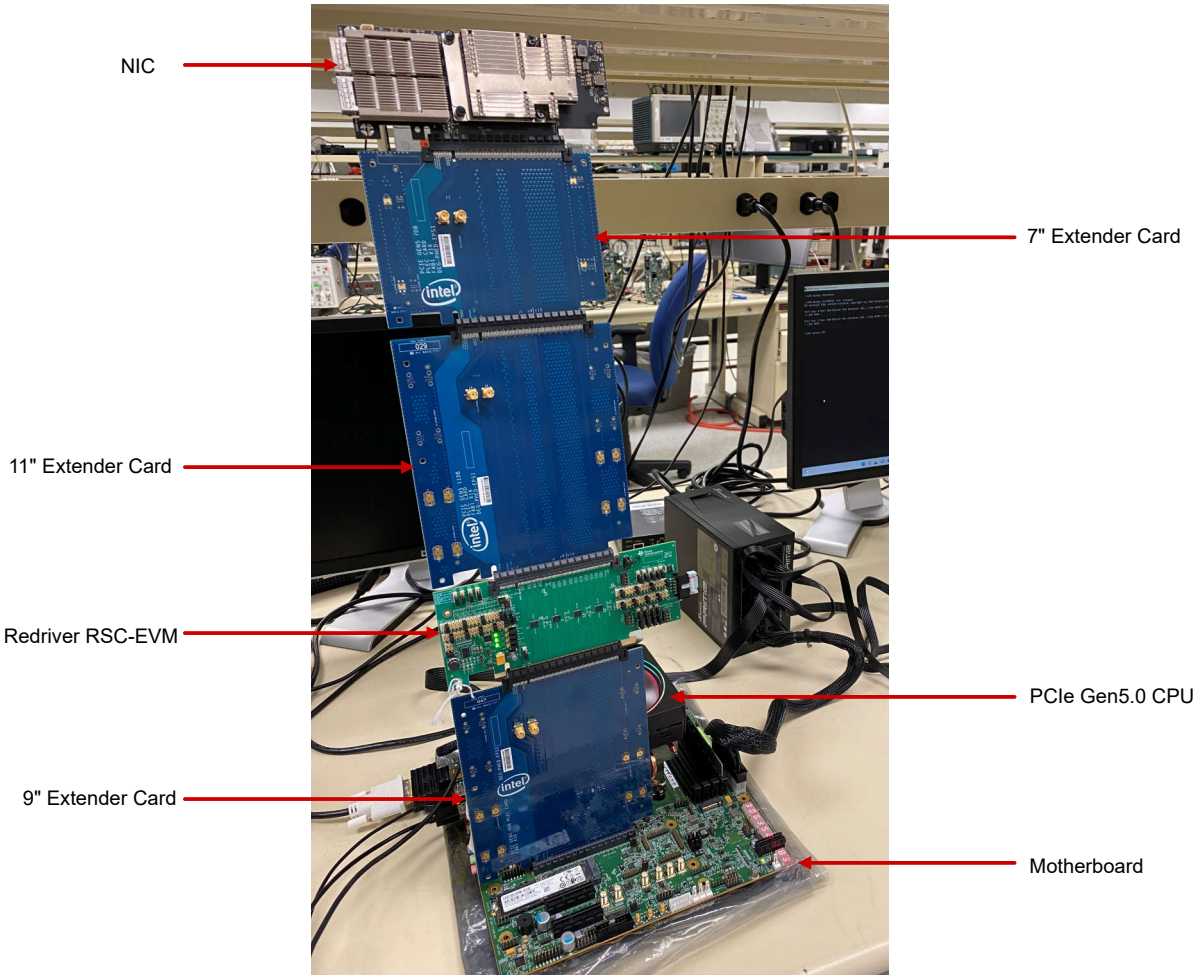

Figure 3-1. Example Test Setup

Figure 3-2 is a typical test result achieved with a system shown in Figure 3-1. As the result indicates, the end point (Nvidia / Mellanox NIC) with the DS320PR410-RSC-EVM placed in the data path achieves a stable Gen5, x16 PCIe link.

```
C:\AMD Xpress IO>AMDXIO -i=2 -listport
AMD XpressIO TOOL version 4.0.45.0, Copyright (c) 2023 Advanced Micro Devices, Inc.

Port Num: 0 Bus: 0x0 Device: 0x1 Function: 0x1 | Link Width = x16 |  Link Speed = 5
 | LINK NAME :

Port Num: 1 Bus: 0x0 Device: 0x1 Function: 0x2 | Link Width = x4 |  Link Speed = 4
 | LINK NAME :


C:\AMD Xpress IO>
```

Figure 3-2. Example Test Results

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4 Hardware Design Files

4.1 Schematics

Figure 4-1 through Figure 4-7 illustrate the EVM schematics.

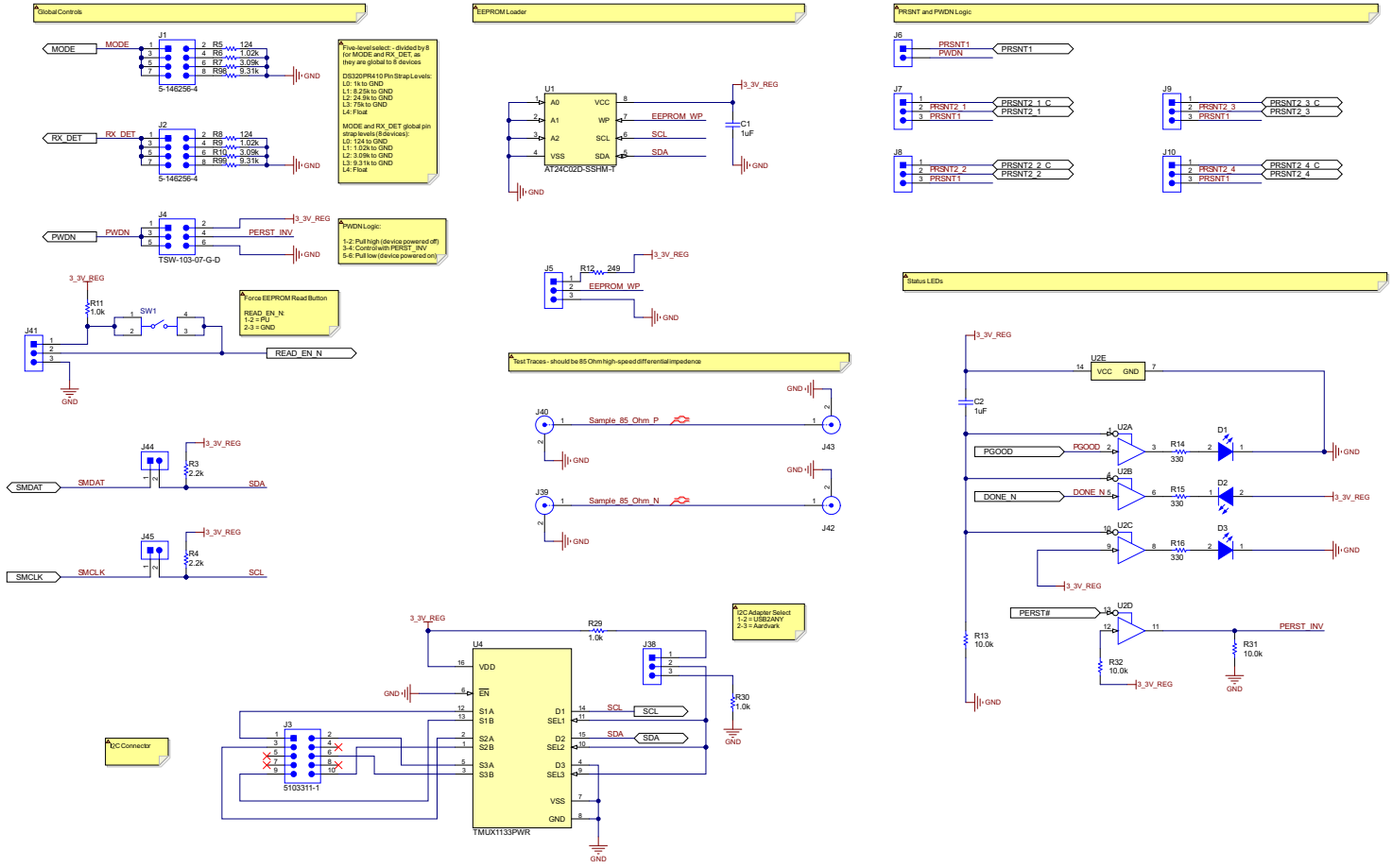

Figure 4-1. Control and Status Schematic Page

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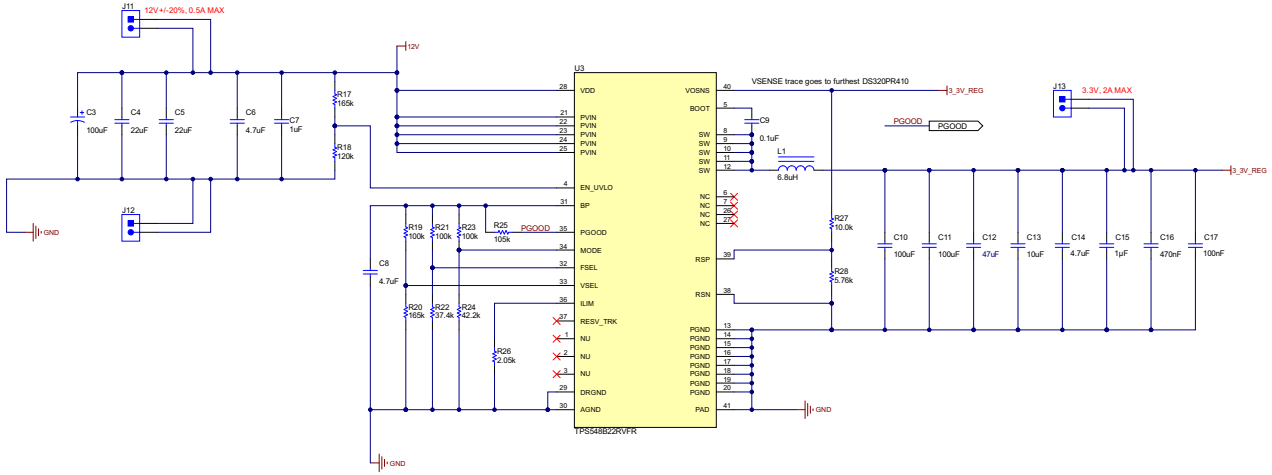

Figure 4-2. Voltage Regulator Schematic Page

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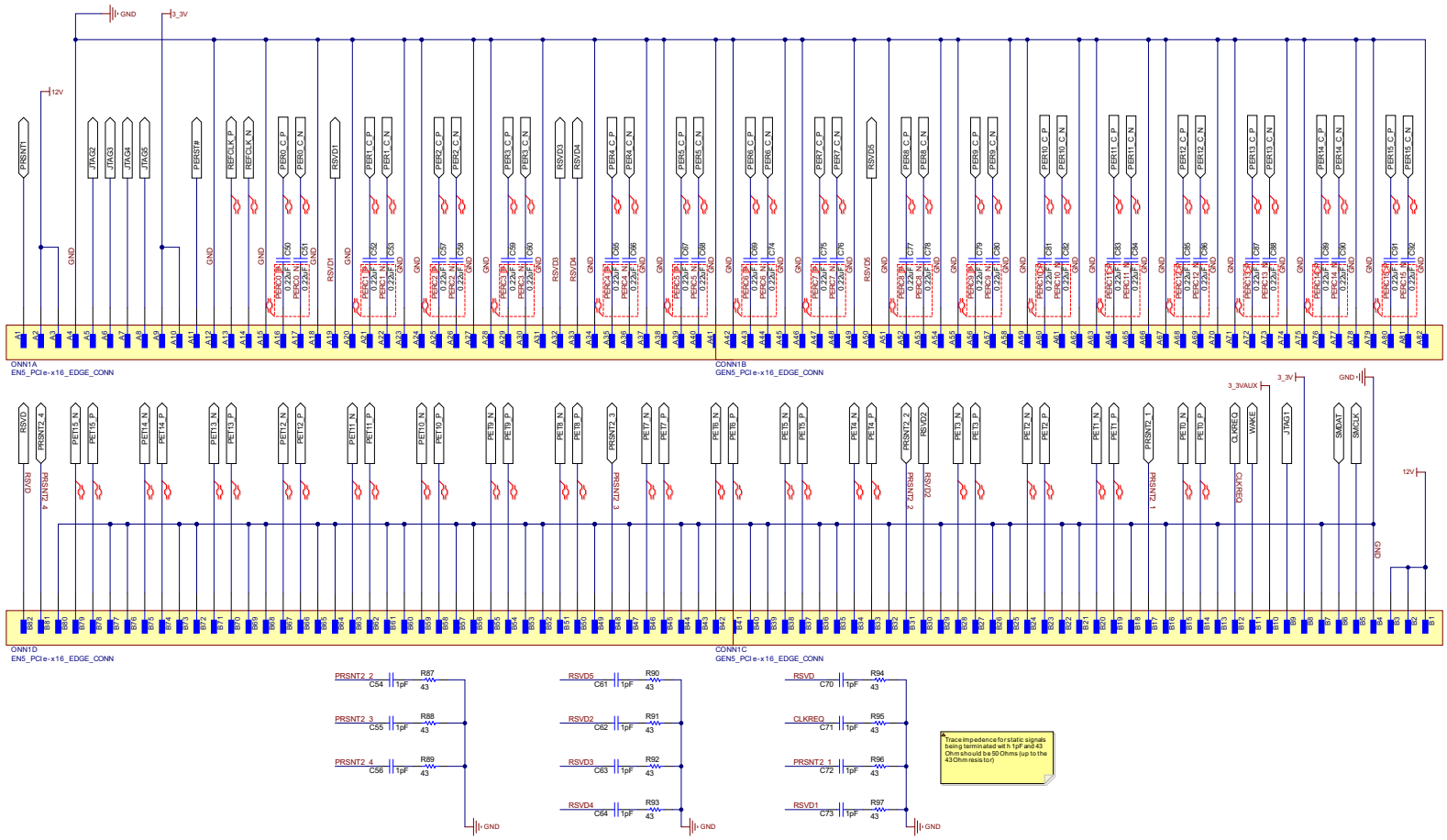

Figure 4-3. Gold Finger Connector Schematic Page

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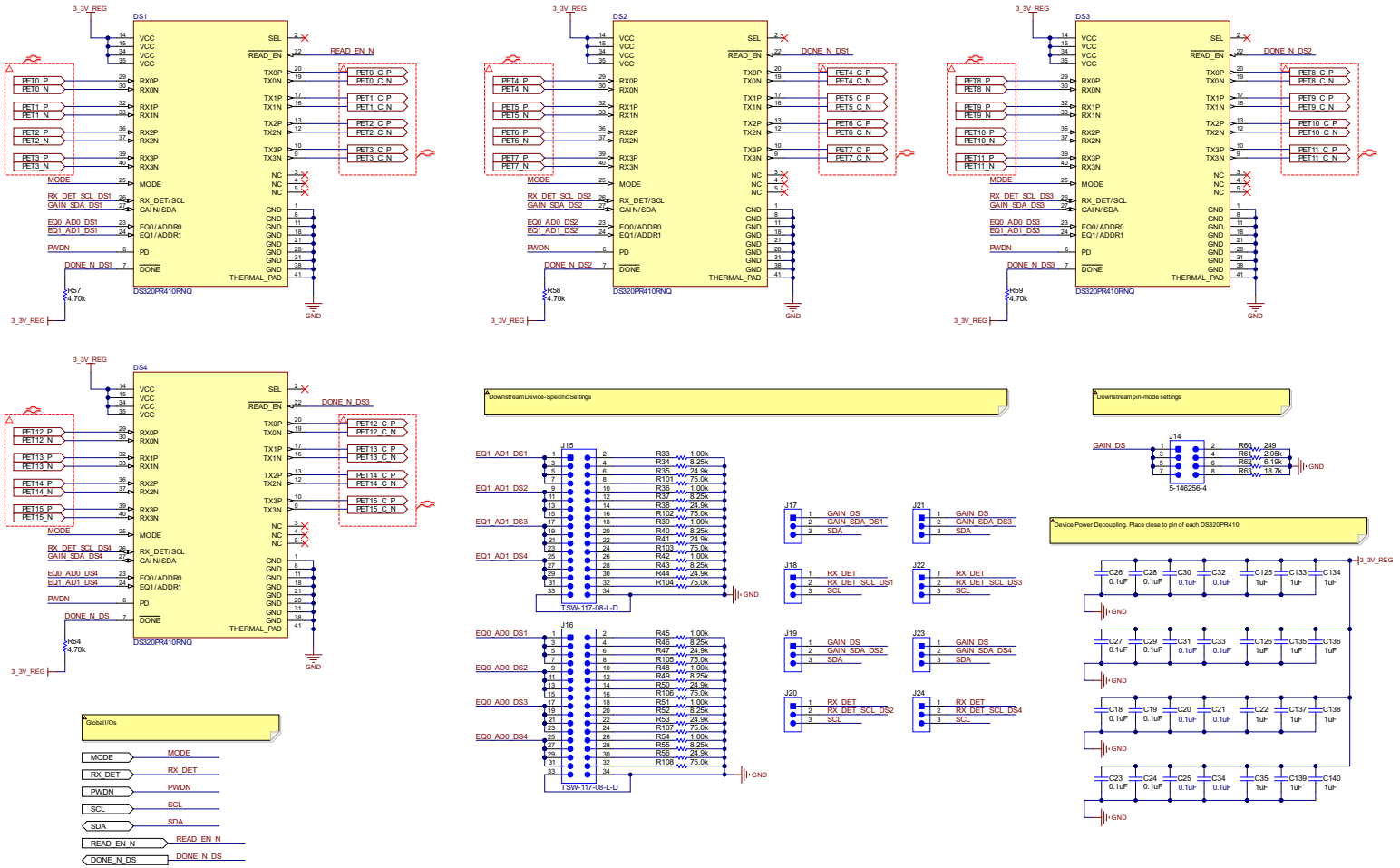

Figure 4-4. Downstream Devices Schematic Page

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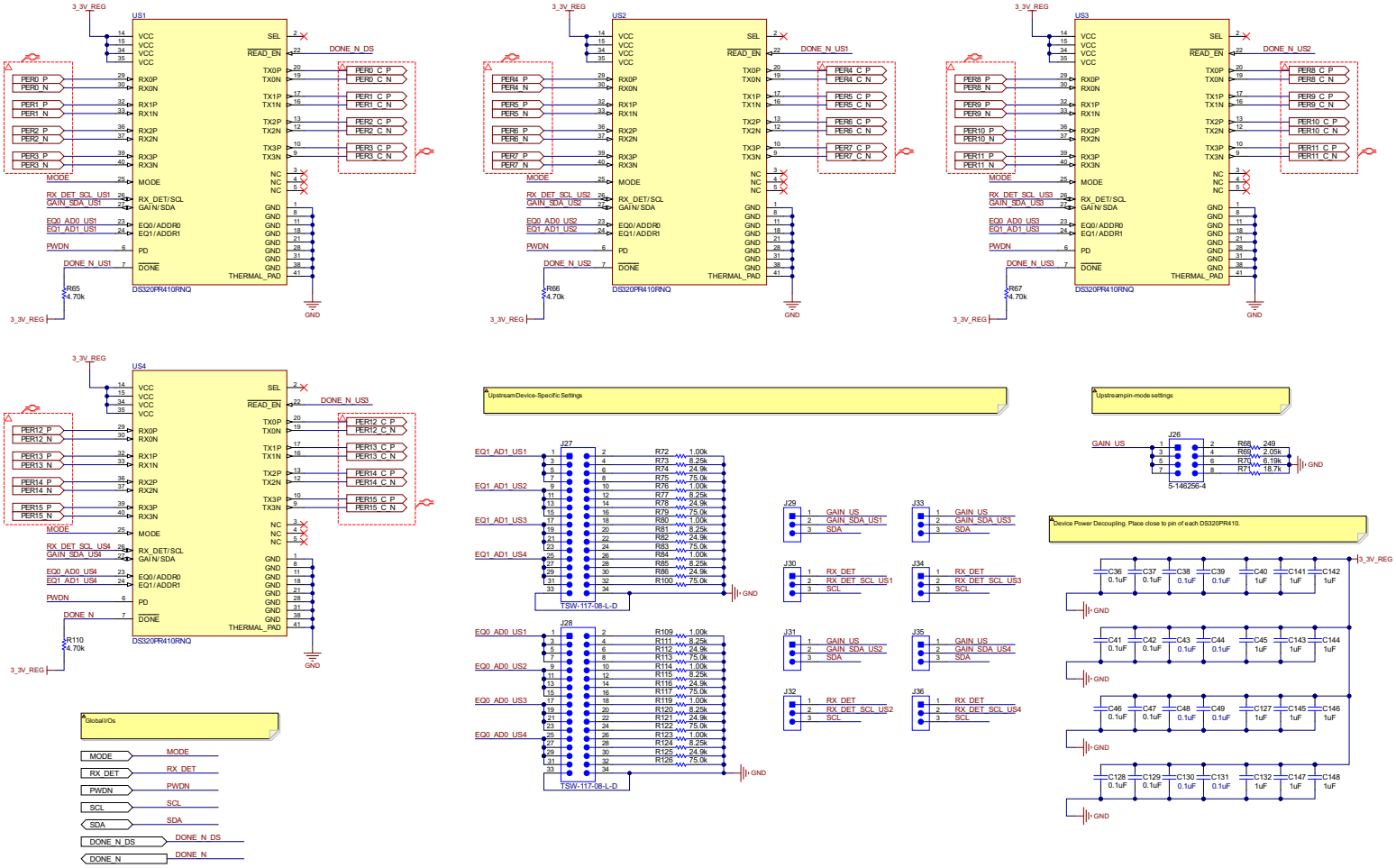

Figure 4-5. Upstream Devices Schematic Page

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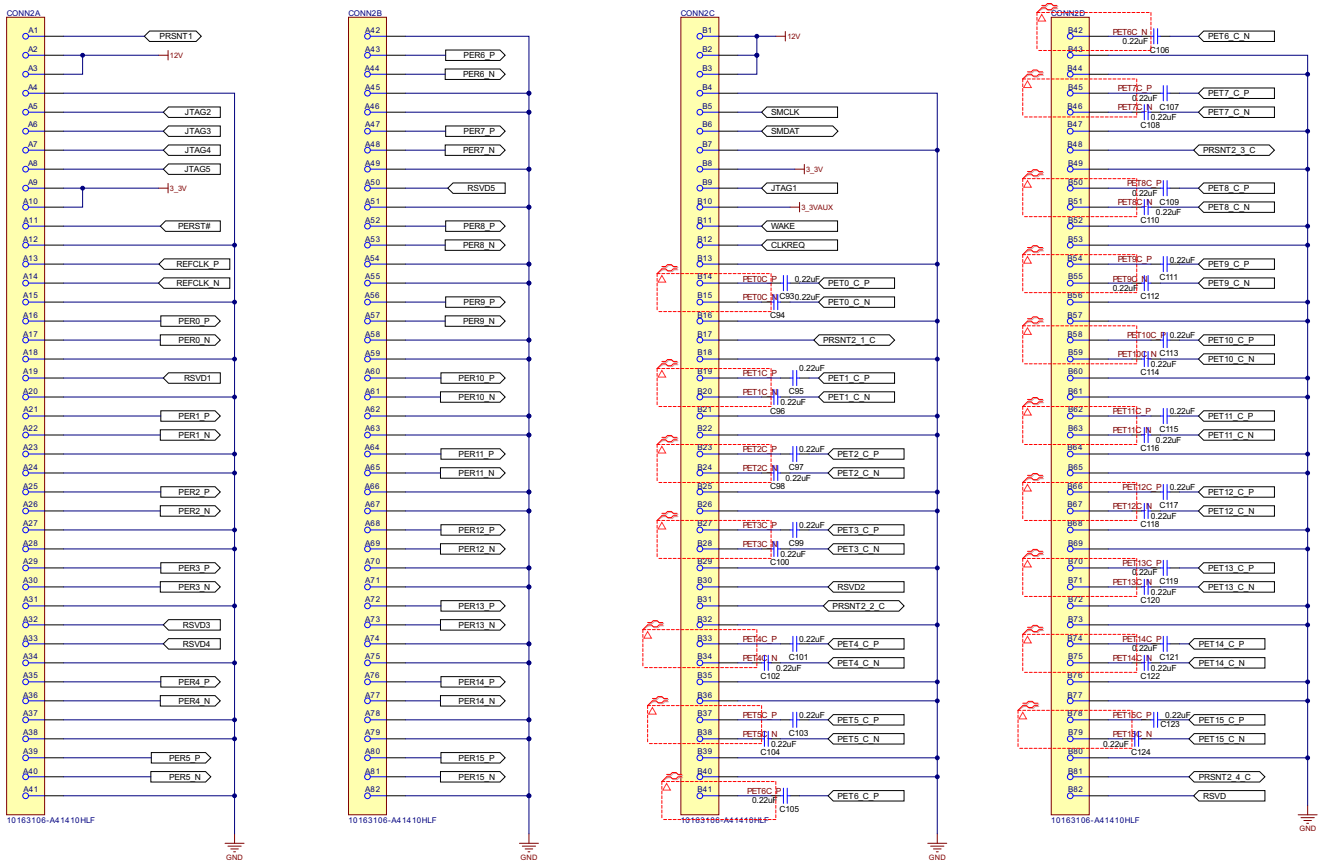

Figure 4-6. Straddle Connector Schematic Page

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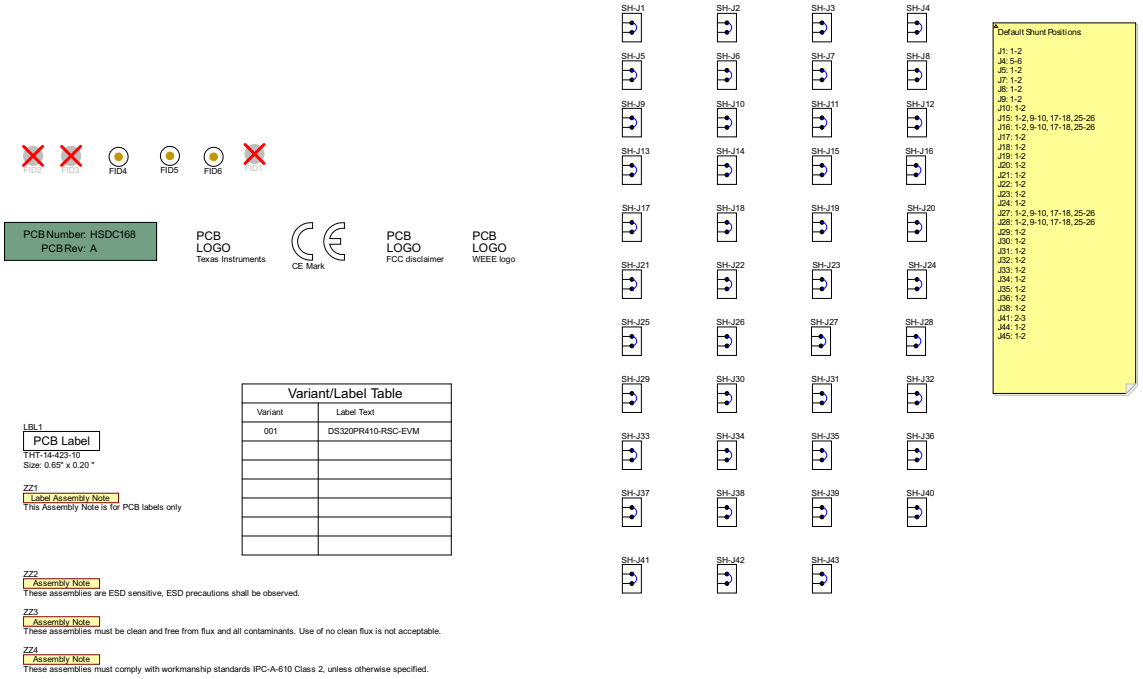

Figure 4-7. Hardware Page

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4.2 Board Layout

Figure 4-8 and Figure 4-9 illustrate the EVM board layouts.

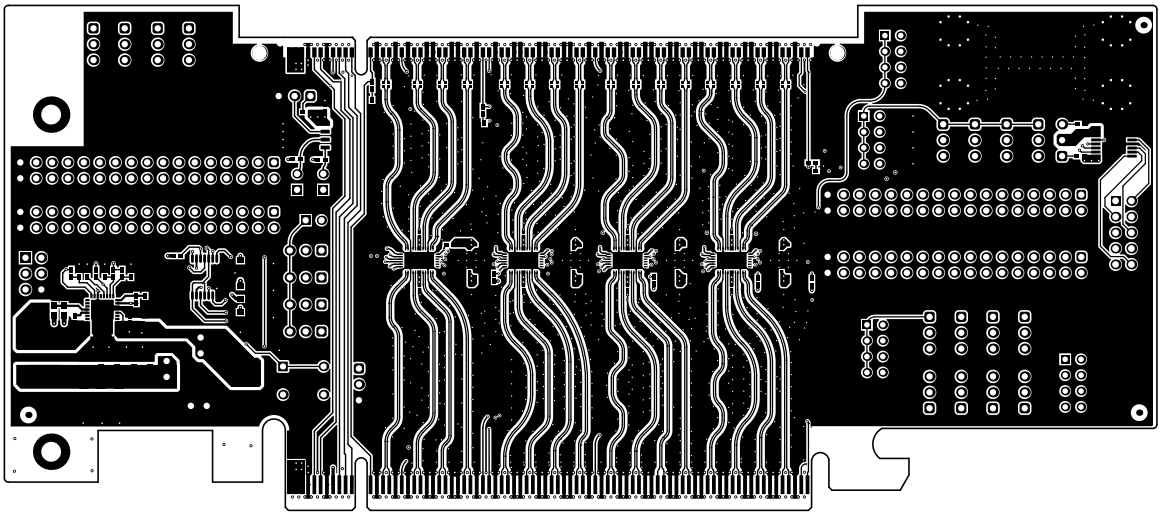

Figure 4-8. Top Layer

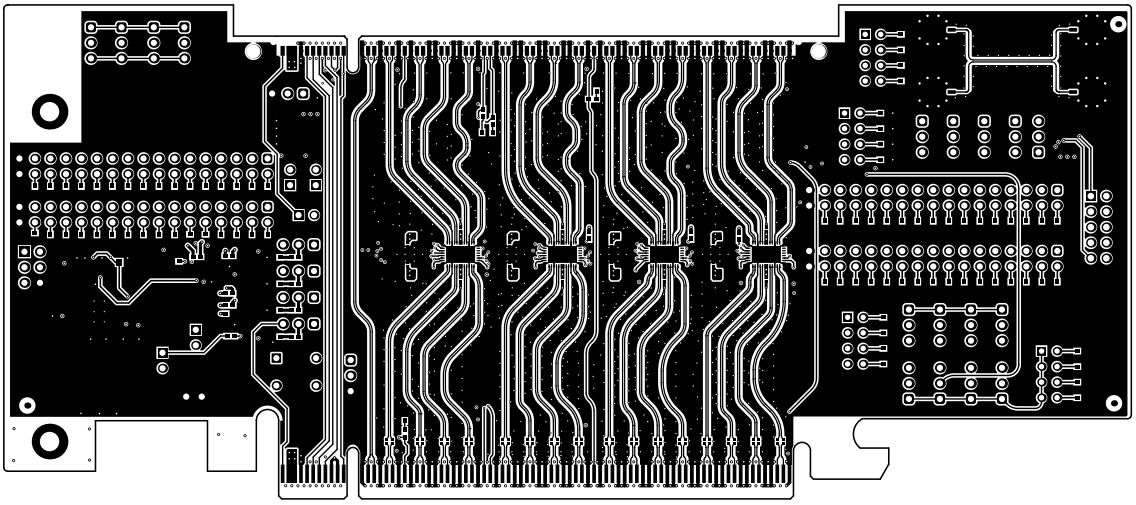

Figure 4-9. Bottom Layer

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4.3 Bill of Materials

Table 4-1 lists the EVM bill of materials.

Table 4-1. Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		HSDC168	Any
C1, C2, C7	3	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK
C3	1	100uF	CAP, TA, 100 uF, 25 V, +/- 10%, 0.1 ohm, SMD	7360-38	T495E107K025ATE100	Kemet
C4, C5	2	22uF	CAP, CERM, 22 uF, 25 V, +/- 20%, X5R, 1206_190	1206_190	TMK316BBJ226ML-T	Taiyo Yuden
C6, C8	2	4.7uF	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X6S, 0603	0603	GRM188C81E475KE11D	MuRata
C9	1	0.1uF	CAP, CERM, 0.1 uF, 35 V, +/- 10%, X5R, 0402	0402	GMK105BJ104KV-F	Taiyo Yuden
C10, C11	2	100uF	CAP, CERM, 100 uF, 6.3 V, +/- 20%, X5R, 0805	0805_HV	GRM21BR60J107M	MuRata
C12	1	47uF	CAP, CERM, 47 uF, 6.3 V, +/- 20%, X5R, 0805	0805_HV	GRM219R60J476ME44D	MuRata
C13	1	10uF	CAP, CERM, 10 uF, 6.3 V, +/- 10%, X5R, 0805	0805_HV	C0805C106K9PAC	Kemet
C14	1	4.7uF	CAP, CERM, 4.7 uF, 6.3 V, +/- 10%, X5R, 0603	0603	C0603C475K9PACTU	Kemet
C15	1	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C16	1	0.47uF	CAP, CERM, 0.47 uF, 6.3 V, +/- 10%, X7R, 0603	0603	C0603C474K9RACTU	Kemet
C17	1	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603	0603	C0603C104K8RACTU	Kemet
C18, C19, C23, C24, C26, C27, C28, C29, C36, C37, C41, C42, C46, C47, C128, C129	16	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X5R, 0201	0201_033	GRM033R60J104KE84D	MuRata
C20, C21, C25, C30, C31, C32, C33, C34	8	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X5R, 0402	0402	C1005X5R0J104K050BA	TDK
C22, C35, C40, C45, C125, C126, C127, C132	8	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X5R, 0402	0402S	C1005X5R1E105K050BC	TDK
C38, C39, C43, C44, C48, C49, C130, C131	8	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, +/- 10%, X5R, 0402	0402S	C1005X5R0J104K050BA	TDK

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Table 4-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C50, C51, C52, C53, C57, C58, C59, C60, C65, C66, C67, C68, C69, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124	64	0.22uF	CAP, CERM, 0.22 uF, 10 V, +/- 20%, X5R, 0201	0201_033	LMK063BJ224MP-F	Taiyo Yuden
C54, C55, C56, C61, C62, C63, C64, C70, C71, C72, C73	11	1 pF	CAP, CERM, 1 pF, 50 V, +/- 10%, C0G/NP0, 0402	0402	GJM1555C1H1R0BB01D	MuRata
C133, C134, C135, C136, C137, C138, C139, C140, C141, C142, C143, C144, C145, C146, C147, C148	16	1uF	CAP CER 1UF 10 V X5R 0201	0201	CL03A105KP3NSNC	Samsung Electro-Mechanics
CONN1	1		PCIE GEN5 STRADLLE MOUNT	FP-GEN5_PCIe-x16_EDGE_CONN_CONN_PCIE_EDGE-MFG	GEN5_PCIe-x16_EDGE_CONN	Amphenol
CONN2	1		PCI Express/PCI Connectors GEN 5 Straddle Mount	FP-10163106A41410HLF_CONN_PCI-164-MFG	10163106-A41410HLF	Amphenol-FCI
D1, D2, D3	3	Green	LED, Green, SMD	LG_M67K_Green	LG M67K-G1J2-24-Z	OSRAM
DS1, DS2, DS3, DS4, US1, US2, US3, US4	8		Four-Channel Linear Redriver for PCIe 5.0, CXL 2.0	RNQ0040A-MFG	DS320PR410RNQ	Texas Instruments
FID4, FID5, FID6	3		Fiducial mark. There is nothing to buy or mount.	Fiducial10-20	N/A	N/A
J1, J2, J14, J26	4		Header, 100mil, 4x2, Gold, TH	TE_5-146256-4	5-146256-4	TE Connectivity
J3	1		Connector, Header, Lo-Pro R/A 10-Pos (5x2), 100-mil Pitch, Gold plated, TH	TE_5103311-1	5103311-1	TE Connectivity
J4	1		Header, 100mil, 3x2, Gold, TH	TSW-103-07-G-D	TSW-103-07-G-D	Samtec
J5, J7, J8, J9, J10, J17, J18, J19, J20, J21, J22, J23, J24, J29, J30, J31, J32, J33, J34, J35, J36, J38, J41	23		Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	TSW-103-07-G-S	Samtec
J6, J11, J12, J13, J44, J45	6		Header, 100mil, 2x1, Gold, TH	CONN_5-146261-1	5-146261-1	TE Connectivity
J15, J16, J27, J28	4		Header, 2.54mm, 17x2, Gold, TH	Samtec_TSW-117-08-x-D	TSW-117-08-L-D	Samtec
J39, J40, J42, J43	4		Plug, 50 Ohm, Straight, SMT	Molex_0853050232	0853050232	Molex
L1	1	6.8uH	Inductor, Drum Core, Ferrite, 6.8 uH, 3.2 A, 0.04 ohm, SMD	SDR0805	SDR0805-6R8ML	Bourns
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Label_650x200	THT-14-423-10	Brady
R3, R4	2	2.2k	RES, 2.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20JNED	Vishay-Dale

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Table 4-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R5, R8	2	124	RES, 124, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402124RFKED	Vishay-Dale
R6, R9	2	1.02k	RES, 1.02 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K02FKED	Vishay-Dale
R7, R10	2	3.09k	RES, 3.09 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K09FKED	Vishay-Dale
R11, R29, R30	3	1.0k	RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00JNED	Vishay-Dale
R12, R60, R68	3	249	RES, 249, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF2490X	Panasonic
R13, R31, R32	3	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	AC0402FR-0710KL	Yageo America
R14, R15, R16	3	330	RES, 330, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402330RJNED	Vishay-Dale
R17	1	165k	RES, 165 k, 1%, 0.1 W, 0603	0603	RC0603FR-07165KL	Yageo
R18	1	120k	RES, 120 k, 1%, 0.1 W, 0603	0603	RC0603FR-07120KL	Yageo
R19, R21, R23	3	100k	RES, 100 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07100KL	Yageo America
R20	1	165k	RES, 165 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1653X	Panasonic
R22	1	37.4k	RES, 37.4 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040237K4FKED	Vishay-Dale
R24	1	42.2k	RES, 42.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040242K2FKED	Vishay-Dale
R25	1	105k	RES, 105 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402105KFKED	Vishay-Dale
R26, R61, R69	3	2.05k	RES, 2.05 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K05FKED	Vishay-Dale
R27	1	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America
R28	1	5.76k	RES, 5.76 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04025K76FKED	Vishay-Dale
R33, R36, R39, R42, R45, R48, R51, R54, R72, R76, R80, R84, R109, R114, R119, R123	16	1.00k	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00FKED	Vishay-Dale
R34, R37, R40, R43, R46, R49, R52, R55, R73, R77, R81, R85, R111, R115, R120, R124	16	8.25k	RES, 8.25 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04028K25FKED	Vishay-Dale
R35, R38, R41, R44, R47, R50, R53, R56, R74, R78, R82, R86, R112, R116, R121, R125	16	24.9k	RES, 24.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040224K9FKED	Vishay-Dale
R57, R58, R59, R64, R65, R66, R67, R110	8	4.70k	RES, 4.70 k, 1%, 0.063 W, 0402	0402	CRG0402F4K7	TE Connectivity
R62, R70	2	6.19k	RES, 6.19 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04026K19FKED	Vishay-Dale

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Table 4-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R63, R71	2	18.7k	RES, 18.7 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040218K7FKED	Vishay-Dale
R75, R79, R83, R100, R101, R102, R103, R104, R105, R106, R107, R108, R113, R117, R122, R126	16	75.0k	RES, 75.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040275K0FKED	Vishay-Dale
R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97	11	43	RES, 43, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040243R0JNED	Vishay-Dale
R98, R99	2	9.31k	RES, 9.31 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04029K31FKED	Vishay-Dale
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19, SH-J20, SH-J21, SH-J22, SH-J23, SH-J24, SH-J25, SH-J26, SH-J27, SH-J28, SH-J29, SH-J30, SH-J31, SH-J32, SH-J33, SH-J34, SH-J35, SH-J36, SH-J37, SH-J38, SH-J39, SH-J40, SH-J41, SH-J42, SH-J43	43	1x2	Shunt, 100mil, Flash Gold, Black	SPC02SYAN	SPC02SYAN	Sullins Connector Solutions
SW1	1		Tactile Switch SPST-NO Top Actuated Through Hole	FP-PTS645SH95-2LFS_PTH4_6MM0_6MM0-MFG	PTS645SH95-2LFS	C&K Components
U1	1		I2C-Compatible (2-wire) Serial EEPROM 2-Kbit (256 x 8), SOIC-8	SOIC-8	AT24C02D-SSHM-T	Atmel
U2	1		Quadruple Bus Buffer Gate With 3-State Outputs, PW0014A, LARGE T&R	PW0014A_N	SN74LVC125APWRG3	Texas Instruments
U3	1		1.5-V to 16-V VIN, 4.5-V to 22-V VDD, 25-A SWIFT Synchronous Step-Down Converter with Full Differential Sense, RVF0040A (LQFN-CLIP-40)	RVF0040A_SMD_NV	TPS548B22RVFR	Texas Instruments
U4	1		3 Circuit IC Switch 2:1 4Ohm 16-TSSOP	PW0016A-MFG	TMUX1133PWR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial10-20	N/A	N/A

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5 Additional Information

Trademarks

All trademarks are the property of their respective owners.

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6 References

For references, see the following:

1. Texas Instruments, *DS320PR410 Four-Channel Linear Redriver for PCI-Express 5.0, CXL 2.0* data sheet.
2. Texas Instruments, *DS320PR410 Programming Guide*

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STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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