National Semiconductor
Paul Grohe
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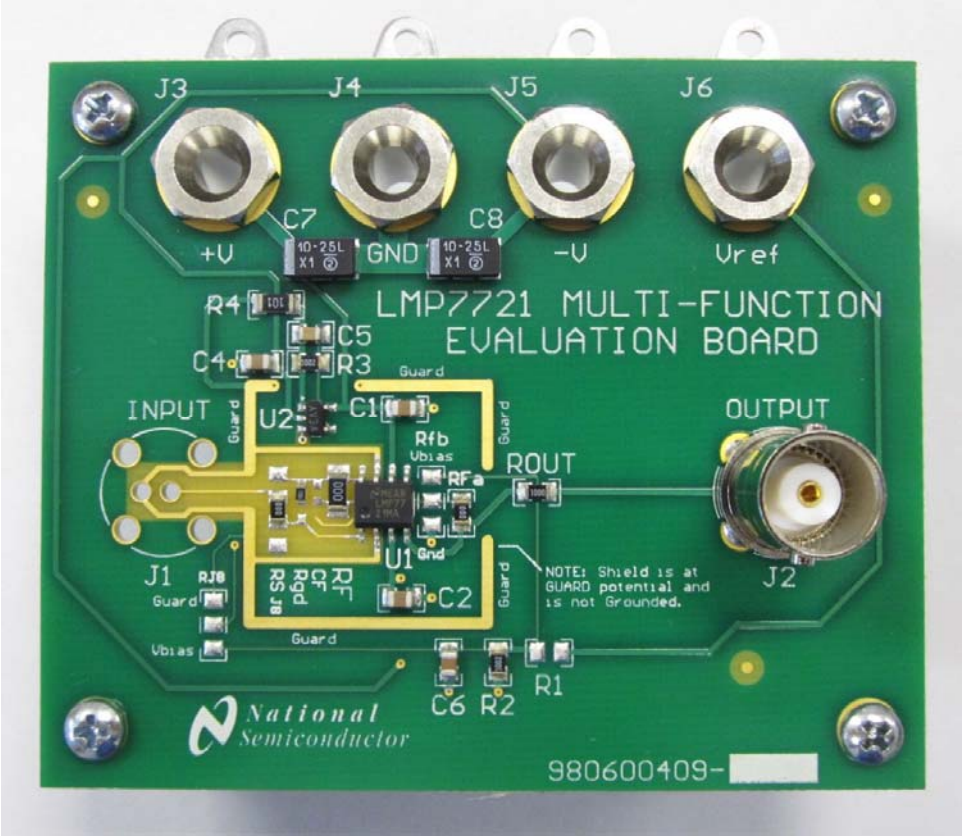
LMP7721 Multi-Function Evaluation Board Users' Guide



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1.0 Overview

The LMP7721 Evaluation Board provides a platform to test the performance of the LMP7721 Ultra-low input bias current operational amplifer.

The LMP7721 amplifier is optimized for ultra low input bias current applications by utilizing internal guarding techniques and a special package pin-out to isolate the amplifier's inputs from its power supply and output pins. This pinout also allows room for proper guarding around the input pins and feedback circuitry.

The LMP7721 Multi-Function Evaluation board may be used to evaluate the LMP7721 in the inverting, non-inverting and Transimpedance ('TIA' or 'I to V') configurations. The layout has been optimized for sub-picoamp operation using conventional FR4 materials through careful layout and guarding techniques.

A second LMP7715 precision amplifier (U2) acts as a guard driver to provide active guarding to the input circuits. The LMP7715 buffer samples the voltage on the LMP7721's summing node and drives the guard traces to an identical potential.

2.0 Board Assembly

The LMP7721 Evaluation Board comes assembled with all components pre-installed for the non-inverting buffer configuration. The J1 input connector is included in the kit as a standard BNC, but is not mounted on the board. This allows the user to configure the input for other purposes. See Section 4.2.3 for details about the input connector options.

Other configurations will require component modification by the user. Refer to Section 4 to determine which components need to be installed.

3.0 Cleaning

Cleaning of the board is ultra-critical to provide the expected sub-picoamp performance. Properly cleaning the board takes a few extra steps over conventional methods. Leftover flux, moisture, fingerprints and cleaning residues will severely degrade low current performance. The board must be cleaned when received to achieve the best low current performance as the board has only undergone standard cleaning after assembly. Section 3.1 describes the extended cleaning procedure.

The following items are required for proper cleaning:

1. Fresh Isopropyl Alcohol ("Rubbing Alcohol" or "IPA").
2. Acid brushes with bristles trimmed to 1cm (push bristles up into handle or cut short).
3. Disposable low-lint cleaning wipes (small "Kimwipes").
4. Compressed Air (spray duster cans or shop CDA with air gun).
5. Heat Gun, ~200°C (Hairdryers are generally not hot enough, but can be used).

After cleaning, only handle the board by the edges and do not touch anything inside the guard area. Avoid breathing on the board, as the saline moisture in the breath severely degrades performance. The use of "no clean" spray flux removers and conformal coatings is not recommended. The board should be re-cleaned after any rework to components within the guarded sections.

3.1 Cleaning Procedure

1. Wash the board per normal cleaning procedures to remove flux, fingerprints and other major contaminates (water wash).
2. While holding the board with a pair of long pliers or forceps, slowly move the board in front of the heat gun for a minute or two to evaporate any remaining moisture (no less than 5cm from the nozzle).
3. Let the board cool to room temperature and flood board with fresh, clean isopropyl alcohol. Allow the alcohol to soak for a few seconds.
4. Immediately scrub the board using an acid brush, particularly the areas around and in-between the U1 pins and RS mounting pads. The critical area is the "bare" area inside the guard trace area

which should be cleaned and scrubbed thoroughly. Dab the entire board with a towlette and soak up most of the excess alcohol. Don't forget the bottom of the board.

5. Flush the area again with fresh alcohol, and dab up as much excess alcohol as possible with a fresh towelette. Immediately blow the remaining alcohol off the board using the compressed air, starting with the input area and working outward. Do NOT use water. Blow air around and under U1 to get as much residue as possible out from under U1 and around the J1 Input connector pins. Moisture can hide under the SMT devices.
6. Immediately after blowing off the board, dab/wipe it with a fresh towlette to remove any remaining alcohol residue. Wipe both the top and bottom of the board with a fresh towlette.
7. Repeat step 2 with the heat gun to dissipate any remaining alcohol. If any white residue is seen, go back to step 2 and repeat. If the white spots persist, the alcholol is contaminated with water.
8. Store the board in an airtight container when not in use. Pack the board with desiccant pack. If desiccant is not available, wrap two tablespoons of dry, uncooked rice in a folded tissue (Kimwipe).

4.0 Hardware Configuration Overview

The Evaluation Board allows for several configurations using one board.

Unconventional component mounting techniques are used to combine both jumpers and resistor selection. Resistors and/or jumpers are soldered between combinations of pads rather than dedicated pads. This minimizes the number of pads required and reduces the overall input surface area. A good example is the four-pad "RS" layout. The following sections will explain the use of these pads.

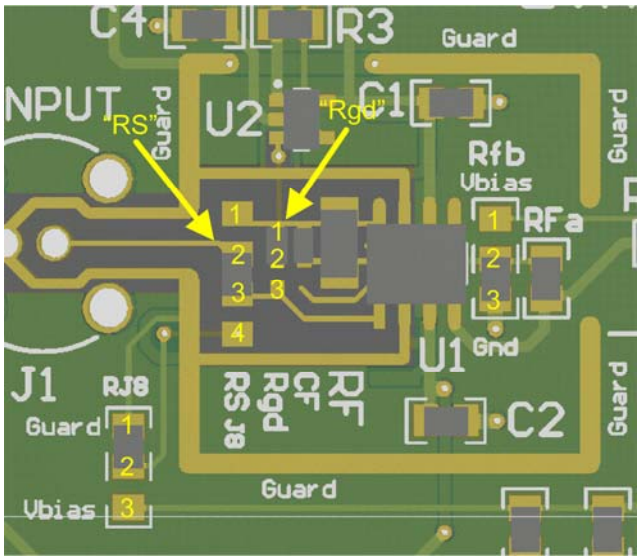

Figure 1. Jumper Resistor Pad Locations

Viewing the board from the top, the pads are numbered top to bottom.

4.1.1 Non-Inverting Configuration (Factory Configuration)

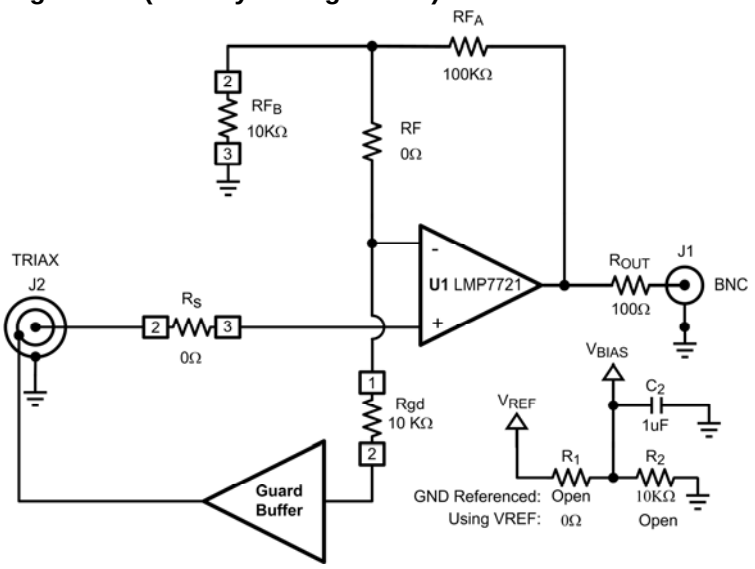

Figure 2. Simplified Non-Inverting Schematic

The evaluation board comes pre-configured in the non-inverting buffer configuration.

A jumper resistor (0Ω) is mounted between pads 2 and 3 of the "RS" pads to connect the J_1 input to the LMP7721 non-inverting input. A jumper is also soldered across the large "RF" pads since this location is not used in this configuration.

RS can be zero ohms, but it is usually a good idea to provide a little series resistance on a direct-coupled input to provide current limiting in case the input exceeds the rails (limiting ESD diode clamp current) should the input go beyond the rails. Recommended value is 100Ω to 1KΩ.

For buffer applications, Rfb is left open and RFa is a value between 0Ω and 100KΩ.

If gain is desired, the gain is set by the ratio of RFa ("R_F") and Rfb ("R_S") resistors.

Gain = 1+ (RFa / Rfb)

Rfb has the option of having it's reference end tied to GND (2-3) or to the Vbias line (1-2) to set the output zero level. See section 4.2.1.

Rgd is soldered between the pads 1 and 2 to tie the guard buffer input to the inverting input node.

RJ8 is soldered between pads 1 and 2. This resistor ties the J8 exposed pad inside the guard area to guard potential, minimizing leakage from the input to the unused J8 pad. Recommended value is 0Ω.

See section 4.2.1 for explanations and configuration of R1, R2, C6, Vbias and Vref lines.

4.1.2 Inverting Configuration

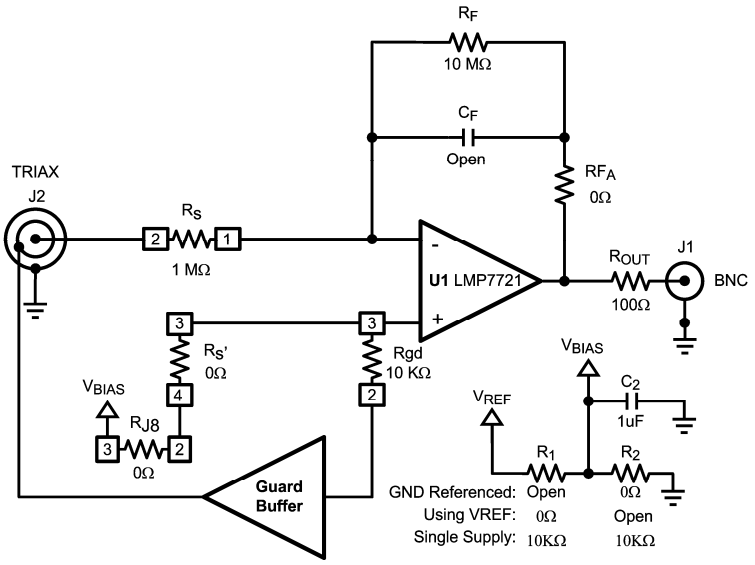

Figure 3. Simplified Inverting Schematic

To configure the board for inverting applications, RS is soldered between pads 1 and 2.

A second jumper resistor RS' (0Ω) is placed between the two lower RS pads (3-4) to provide the DC bias to the non-inverting input from the J8 jumper. RJ8 is connected between pins 2 and 3 to connect to the Vbias line. R1 and R2 determine the bias on the non-inverting input.

The feedback resistor RF is mounted on the large RF pads, and a zero ohm resistor is mounted on RFa. Rfb is not used and is left open.

Gain = - (RF / RS)

Rgd is soldered between pads 2 and 3 to tie the guard buffer input to the non-inverting input node. The exact value of this resistor is not critical. The suggested value is 10kΩ.

RJ8 connects the non-inverting input to the Vbias line. The recommended value is 0Ω. RJ8 has the option of having it's reference end tied to GND (1-2) or to the Vbias line (2-3) to set the output zero level.

Feedback resistor multiplication is also possible utilizing RFa and Rfb in a "Tee" feedback configuration. See the Transimpedance Configuration with "Tee" Feedback section 4.1.4 for more details.

4.1.3 Transimpedance Configuration

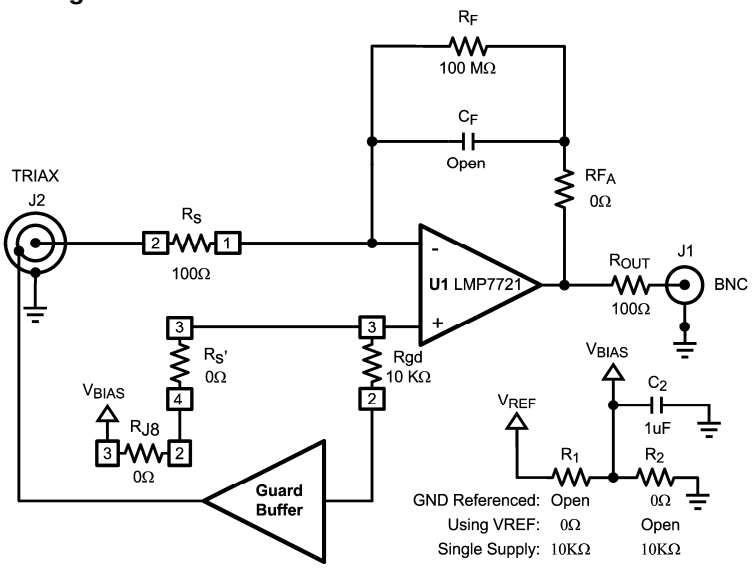

Figure 4. Simplified Transimpedance (TIA) Schematic

Figure 4 shows the classic “Transimpedance Amplifier” (“TIA”) or “Current to Voltage” (I to V) converter circuit.

Vout = -I / RF

The setup is similar to the Inverting configuration, except for the RS value. It is recommended that RS should not be less than 100 ohms, otherwise, if the input is grounded, the feedback path will be lost and the output will rail.

Larger “1206” sized RF pads are provided to accommodate the physically larger high-value (>1GΩ) resistors that are generally used in this position. As of this writing, values up to 10TΩ are currently available in 1206 surface mount devices. Note that many of these high value resistors contain exotic materials in their construction and may require special solder and soldering precautions. Check the resistor datasheet for warnings.

If a leaded resistor is required, it is possible to solder one lead to the input terminal and the other lead to the lower RF pad. Care should be taken so that the body of the resistor does not touch any other components and clears the guards. It should be mounted “up in the air” for best results.

4.1.4 Transimpedance Configuration with “Tee” Feedback

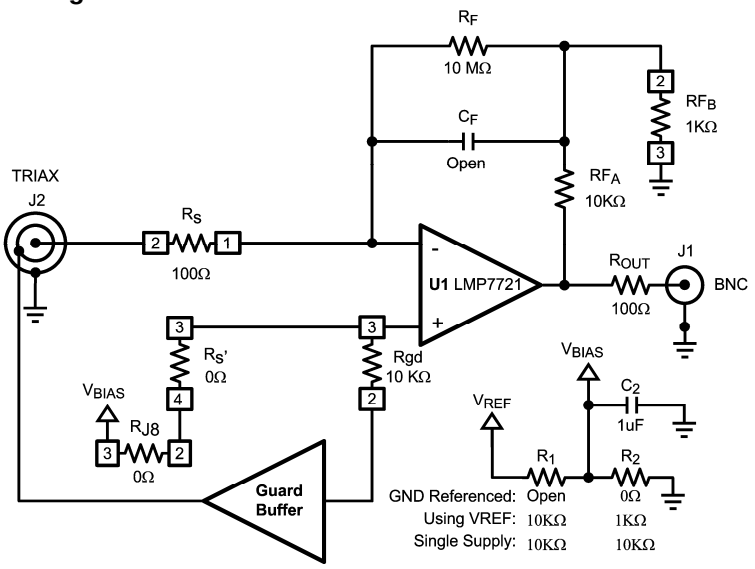

Figure 5. Simplified Transimpedance with "Tee" Feedback

Figure 5 shows how to it is possible to multiply the effective value of the feedback resistor by adding two resistors, RFa and Rfb into the feedback path. A 10MΩ resistor can be made to look like a 100MΩ with this "trick". This comes in handy when larger value resistors are not available or too expensive. It is also possible to change the sensitivity by simply changing the Rfb value.

Vout = - I / (RF * (RFa / Rfb))

RFa and Rfb attenuate the output feedback signal going to the RF resistor, effectively multiplying the size of the feedback resistor by the attenuation ratio. In Figure 5, the RFa and Rfb resistors, with a 10:1 ratio, make the 10MΩ now look like a 100MΩ resistor. The circuit will now have a sensitivity of 10nA/V instead of 100nA/V without changing the feedback resistor.

However, this trick comes at several costs. Adding the “attenuation” is actually adding noise gain, so this circuit has all the side effects one would associate with an standard inverting amplifier (offset voltage and input noise will be multiplied, closed loop bandwidth will be reduced).

The bias point voltage applied to the non-inverting input will also be multiplied by the non-inverting noise gain [1+ (RFa / Rfb)].

This trick also multiplies the effect of CF (and also any stray capacitance around RF). CF must be now reduced by the RFa/Rfb ratio. In the above example, if a 10pF capacitor was chosen for 10MΩ, it now must be 1pF for the “100MΩ” resistor. This places a lower limit on the reductions since stray capacitance is generally around 0.25pF. As one can guess, using high ratios can lead to absurdly low capacitor values – well below the natural stray capacitance, and the stray capacitance will now eat up a large portion of the bandwidth. It is possible to place a capacitor around RFa to counteract the effects – but the details are beyond the scope of this appnote.

With R1/R2 ratio equal to the RFa/Rfb ratio, a standard “subtractor” circuit can be built to set the bias point using the Vref input.

4.2.0 Power Supply Connections

Connectors J3, J4 and J5 are the power supply connections. The power supply can be a single supply with a range 1.8 to 5.5 volts. Also, a split supply voltage can be used with the condition that 1.8V ≤ (+V) - (-V) ≤ 5.5V.

For single supply operation, J4 and J5 are connected together and J4 is the ground connection. The positive supply voltage connection is J3.

For split-supply operation, the negative supply voltage is connected to J5. The positive supply voltage is connected to J3 and the ground (or common) connection of the supplies is connected to J4.

4.2.1 Vref and Vbias

The LMP7721 evaluation board can be configured as a transimpedance, inverting or a non-inverting amplifier. In each case, it may be required to provide a level shift voltage to keep the output voltage within a specified range. This is accomplished by using the Vref input connection.

Vref is connected to the top end of the voltage divider R1 and R2.

Vbias is developed from the R1+ R2 voltage divider center tap and is supplied to the RJ8 and Rfb pads.

For dual supply setups, Vbias is usually at ground. In this case, R2 is jumpered and R1 is left open.

To use an external Vref voltage without modification, R_1 is shorted and R_2 is open. R2 can be used as a generator termination resistor if needed.

For single supply setups, R1 and R2 comprise a voltage divider to provide the needed bias voltage. The Vref input can be connected to the positive supply.

The source impedance of the Vbias line is the parallel combination of R1 and R2. (Zbias = R1 || R2). C6 provides an AC ground, and the low frequency pole is determined by the total impedance (R1 || R2 || Rfb) and C6.

If the bias voltage is applied to the “bottom” side of Rfb (using pads 1 and 2), the parallel combination of R1 and R2 must be added in series with Rfb, otherwise there will be a gain error caused by the addition of these resistors. The equivalent “RG” gain set resistor is Rfb plus the parallel combination of R1+R2. C6 should be removed if the resistors are added together, otherwise AC and DC gains will be different.

“RG” = Rfb + (R1 || R2)

4.2.2 Guards and Shields

Guards are important concepts in sub-picoamp current designs. The guard creates an equal potential zone around the input pins, preventing external leakages from reaching the input. Input leakages “leak” to an equivilent voltage resulting in much smaller current flows. External currents “leak” to the low impedance guard instead of the input traces.

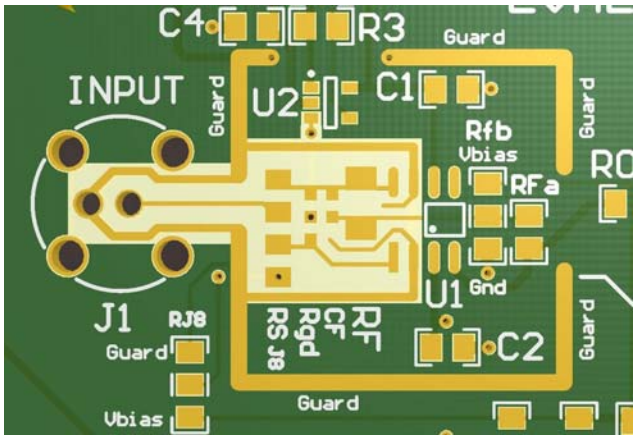

Figure 6. Input guard traces

On the board, the input traces and all the sensitive feedback components are located within the perimeter of the guard traces. The solder mask has also been removed from this area to reduce surface charge accumulation.

The LMP7715 guard driver (U2) drives the input guard traces to the same potential as the expected input signal. Rgd selects the reference node.

In the inverting and transimpedance modes, the guard is driven to the same potential as the non-inverting input node by placing Rgd between pads 2 and 3. Generally this node will be GND or the Vbias potential.

In the non-inverting mode, the guard is driven to the same potential as the inverting input node. This node follows the input signal through the feedback action of the LMP7721. A buffered duplicate of the input signal will appear on the guards.

The bandwidth of the guard driver circuit is determined by R1 and C5. The default R1 and C5 values are 10K and 1000pF, which creates a 16 KHz driver bandwidth. For higher bandwidths, these values can be decreased down to 100Ω and 82pF. But some bandwidth limiting should be used to prevent peaking of the buffer at high frequencies, which could cause instability of the entire system

The exact value of Rgd is not critical, but it does provide some capacitive isolation to the non-inverting node (prevents LMP7721 from peaking). Too large of a Rgd value will create a pole with the input capacitance of the buffer driver amplifier (~12pF), reducing the guard effectiveness at higher frequencies by introducing extra phase lag. Too low of a Rgd value will add the LMP7715’s input capacitance to the LMP7721 summing node, causing ”peaking” at high frequencies. The suggested value for Rgd is 10k.

R4 is for current limiting and capacitive load isolation. 100Ω is the recommended value.

Since the guard is essentially “bootstrapping” the input, the effective input capacitance from the guard traces to the input traces is cancelled (including any cable capacitance when the guard drives the shield adjacent to the input conductor).

For the LMP7721 board, the board input capacitance drops from 13pF to 11pf due to the guarding. The cancellation is effective over the flat bandwidth of the guard driver. The guard does NOT cancel out the capacitance of the LMP7721’s internal input stage (about 10pF).

The guard buffer gain should always be limited to less than one, otherwise positive feedback may occur. Any peaking on the buffer output may cause the gain to go greater than one, so R3 and C5 should always be used to control the buffer bandwidth. R4 should be no less than 100Ω to prevent guard driver output peaking due to capacitive loading and to provide short circuit protection.

The LMP7721's No Connect ("N/C") pins, pins 2 and 7, are tied to the guard traces. This provides input guarding all the way into the package down to the lead frame level. Pins 2 and 7 are not connected internally and will not interfere with amplifier operation. It is recommended that these pins be tied to the guard traces whenever possible.

The wide, bare traces around the guarded area provide for optional metal shields that can be soldered in place to provide full electrostatic shielding. Note that the metallic shields are not tied to ground, but to the guard voltage. Be careful to not short the shields to ground or to inadvertently use them as grounding test points for test equipment.

The pads are laid out for the 0.75 X 0.75 X 0.25 (top) and 0.5 X 1.0 X 0.25 (bottom) prefabricated metal shields from FotoFab, Inc (see B.O.M.). During prototyping, only tack-solder two opposite corners to ease removal.

For the upper shield, a simple modification must be done to prevent the shield from shorting to the input trace. Two small vertical cuts are made and pliers used to bend the metal flap up and away from the input trace. The recommended shield is made of thin plated brass and is easy to work with. Bending the flap out should create a little "awning" over the input trace. See Figure 7.

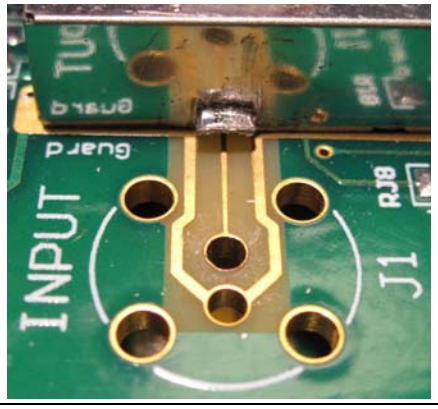

Figure 7. Shield modification to clear input trace

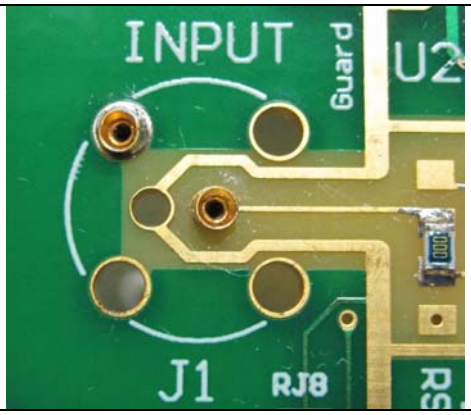

Figure 8. Pin sockets used instead of connectors

4.2.3 Input and output connectors

The J1 input is designed for a Trompeter CBJR70 series Triaxial connector. A Triax connector is similar to a BNC connector, but includes a guard shield between the center conductor and the outer shell. Note that the recommended connector has 3 index lugs and is not compatible with standard BNC connectors.

Since Triaxial connectors are expensive, the mounting holes and center pin have been slightly enlarged to allow a standard PCB mount BNC connector to be fitted for less demanding applications. Teflon (PTFE) dielectric BNC connectors are recommended.

A standard BNC (similar to J2) is provided with the board, but is not installed. This is to allow the user to configure the input for their own use and to prevent damage to the board if the user does not want the connector.

If a coax input is not desired, a single-pin PCB mount socket can be fitted into the input mounting holes to provide connection to wire leads. See Figure 8.

The J2 output is a standard BNC connector and is the output of the LMP7721 amplifier. ROUT provides capacitive isolation (to prevent oscillations and peaking when driving coax) and short circuit current limiting. The recommended value for ROUT is 100Ω.

5.0 Evaluation Board Specifications

Board Size:	2.5" x 3.0" (6.35 cm x 7.62 cm)
Power Requirements:	+/- 2.5V or +5V @ 3mA

6.0 Hardware Schematics

6.1 Hardware Schematic – Non-Inverting Configuration

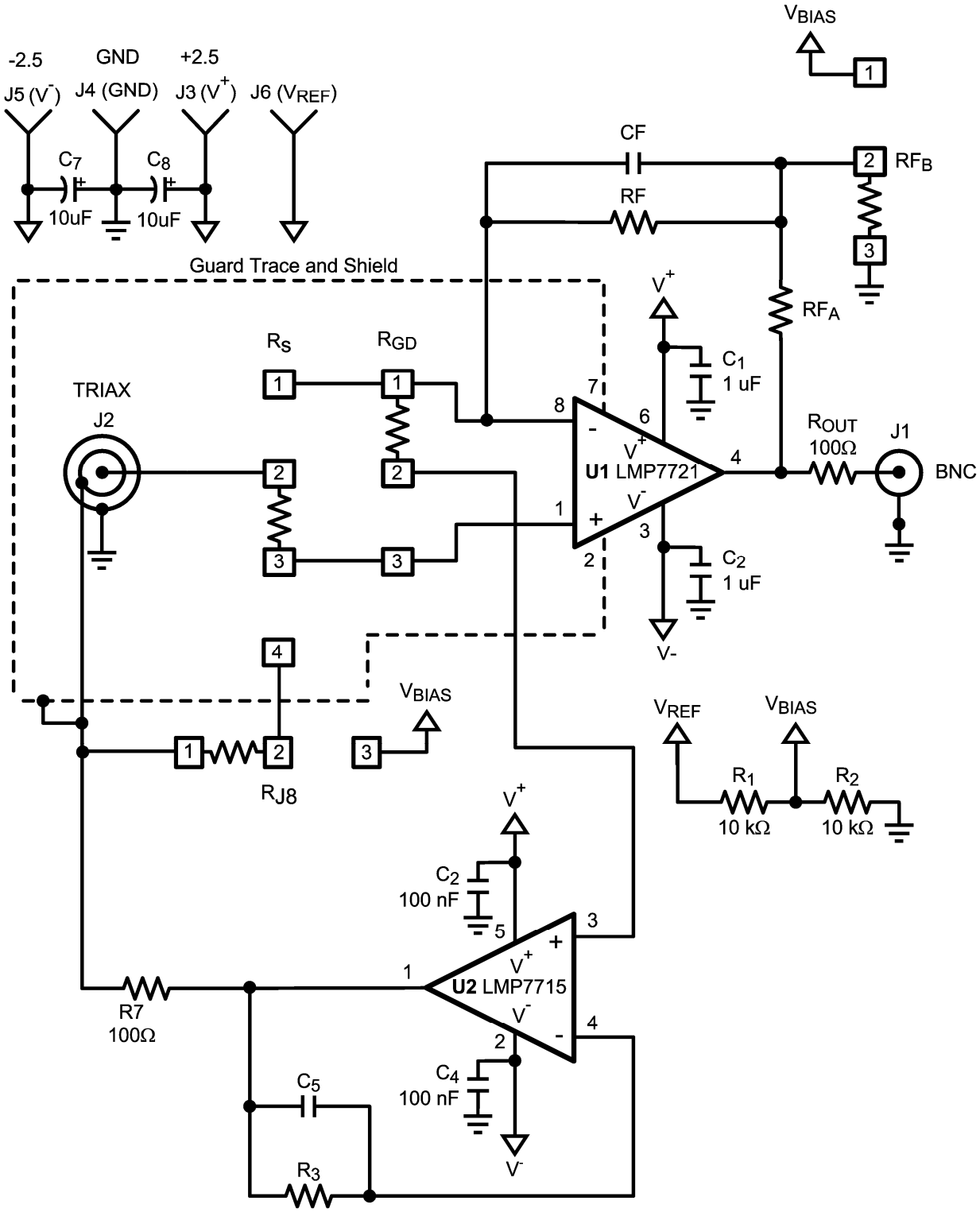

Figure 9. LMP7721 Multi-Function Evaluation Board Schematic (GND Referenced)

6.2 Hardware Schematic – Inverting Configuration

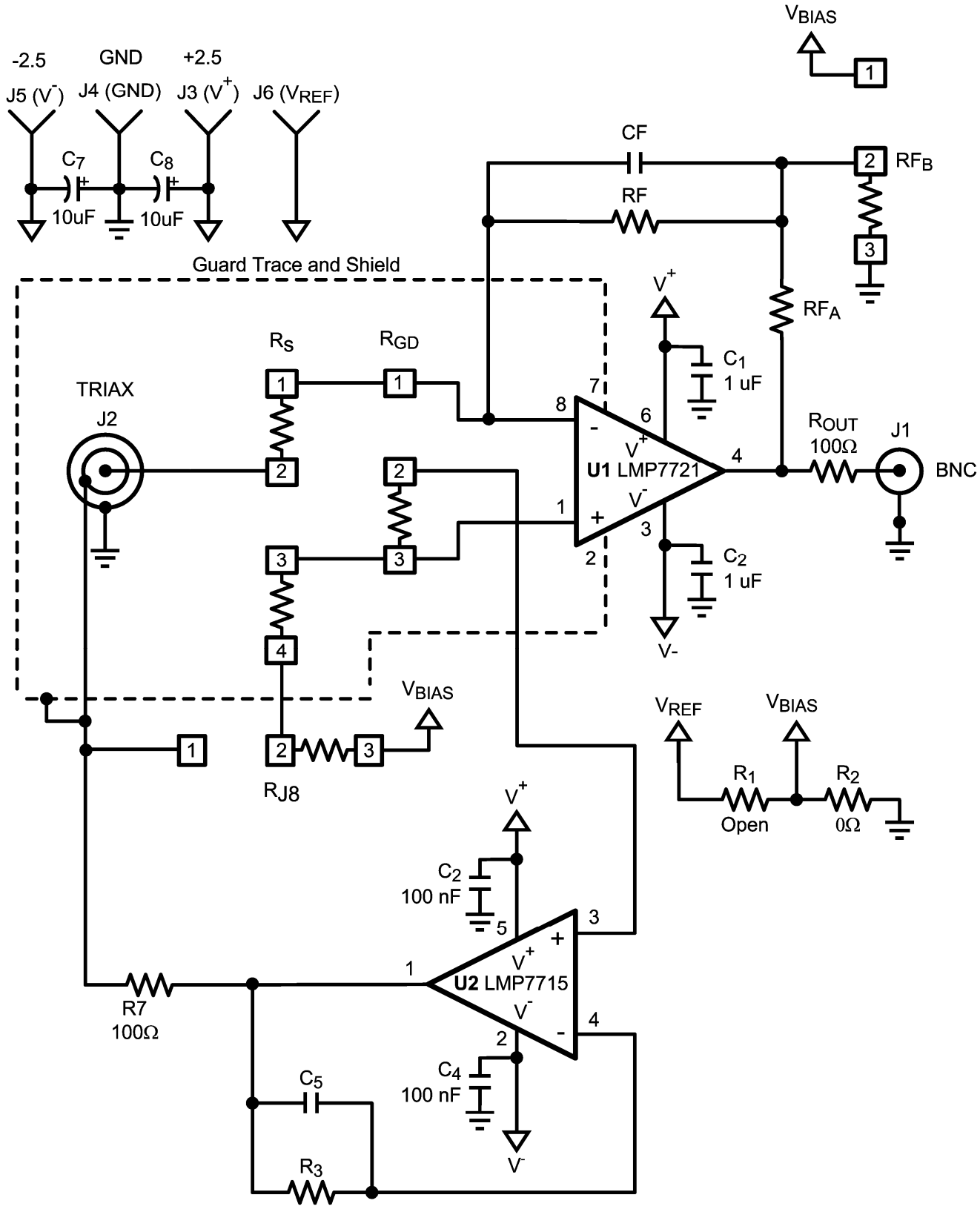

Figure 10. LMP7721 Inverting Configuration Schematic (GND referenced)

6.3 Hardware Schematic – Transimpedance Configuration

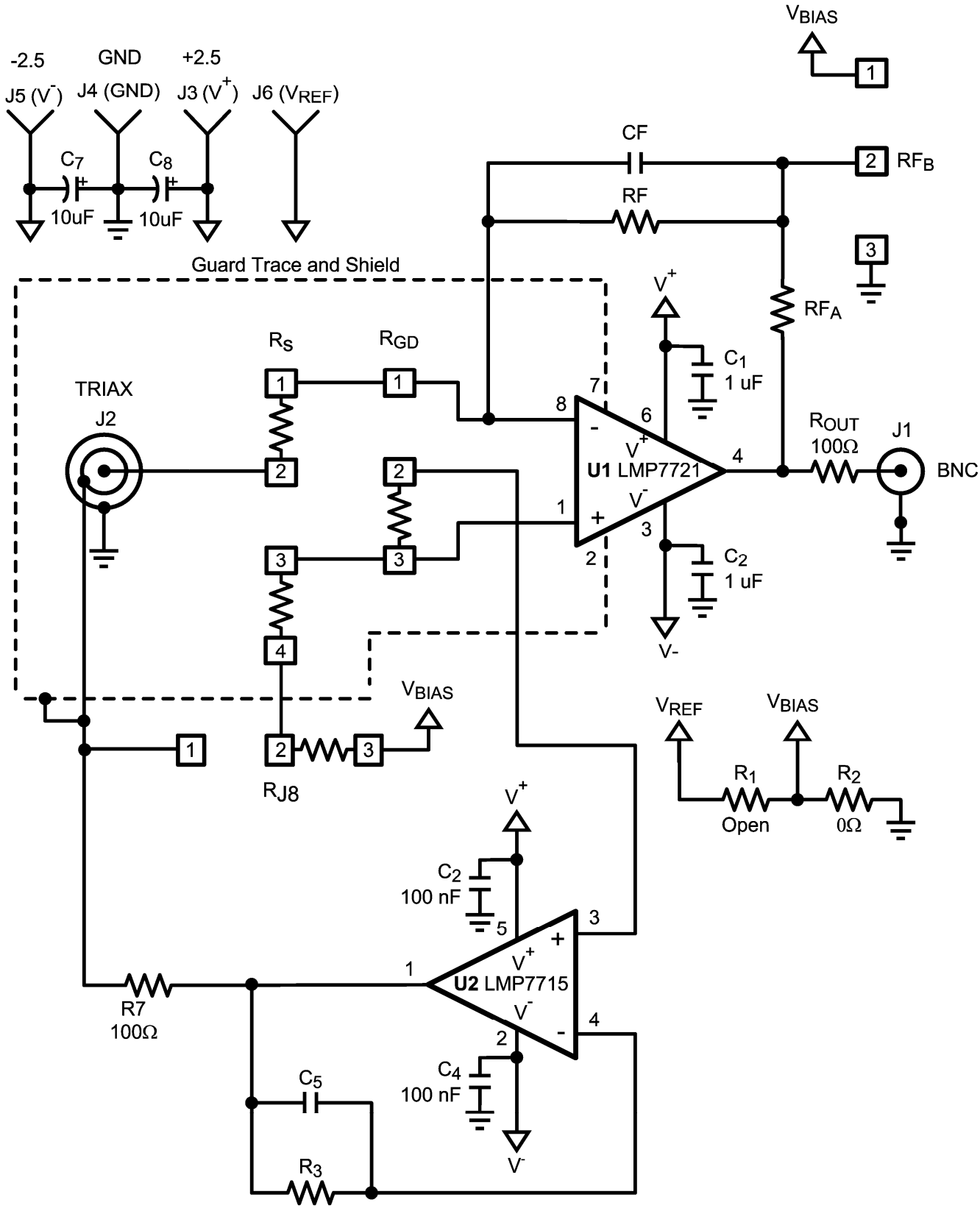

Figure 11. LMP7721 Transimpedance Configuration Schematic (GND referenced)

7.0 Bill of Materials

Designator	Value	Description	Part Number	Comment
C1, C2, C4, C6	1uF	Ceramic, X5R, 25V, 10%, 0805	MuRata GRM216R61E105KA12D	
C5	1000pF	Ceramic, X7R, 50V, 5%, 0805	Kemet C0805C102J5RACTU	
C7, C8	10uF	Tantalum, 25V, 20%, 6032-28	Vishay-Sprague 293D106X0025C2TE3	
CF	DNS	Ceramic, C0G/NP0, 50V, 5%, 0603	AVX 06035A220JAT2A	
J1	Triax or BNC	Triax BNC, Right Angle, 3 Lug, Trompeter 70 series or optional BNC	Trompeter-Emerson CBJR70A (Triax) or Amphenol 112404 (BNC)	For reference only. Connector identical to J2 provided with kit but not mounted.
J2	BNC	Connector, TH, BNC,	Amphenol 112404	
J3, J4, J5, J6	Banana, 4mm	Jack, Banana, Bare, Panel Mount	Emerson 108-0740-001	
R1, R2, R3	10.0k	1%, 0.125W, 0805	Vishay-Dale CRCW080510K0FKEA	
R4	100	5%, 0.25W, 1206	Vishay-Dale CRCW1206100RJNEA	
RF	0	5%, 0.25W, 1206	Vishay-Dale CRCW12060000Z0EA	
RFa	0	0.1%, 0.125W, 0805	Vishay-Dale CRCW08050000Z0EA	
RFb	Open	0.1%, 0.125W, 0805	Vishay-Dale CRCW08050000Z0EA	Not Stuffed
Rgd	10K	5%, 0.125W, 0603	Vishay-Dale CRCW060310K0FKEA	
RJ8	0	5%, 0.125W, 0805	Vishay-Dale CRCW08050000Z0EA	
RS, RS’	0	0.1%, 0.125W, 0805	Vishay-Dale CRCW08050000Z0EA	
ROUT	100	1%, 0.125W, 0805	Vishay-Dale CRCW0805100RFKEA	
Bottom Shield	Shield	Shield, RF, 0.5" x 1.0" x 0.25", SMT	FotoFab 0.5 X 1.0 X 0.25	Optional. Not Provided.
Top Shield	Shield	Shield, RF, 0.75 x 0.75 x 0.25, SMT	FotoFab 0.75 X 0.75 X 0.25	Optional. Not Provided.
U1	LMP7721MA	Precison 3fA Op Amp	National Semiconductor LMP7721MA	
U2	LMP7715MF	Precision CMOS Input Op Amp	National Semiconductor LMP7715MF	

The Bill of Materials reflects the “Buffer” configuration as shipped.

J1 connector is supplied as a BNC connector and is included in the kit, but is NOT stuffed on the board.

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