

AN-1660 LM2735Y 6-Pin WSON Demo Board

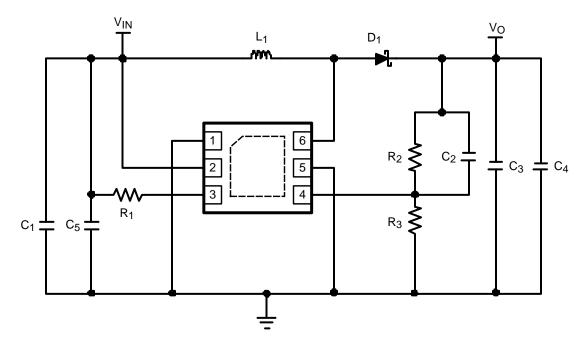
1 Introduction

This demo board converts 3V to 5.5V input to 12V output for up to 500mA load current using the LM2735Y 520kHz DC-DC switching converter. This is a 2-layer board using the bottom layer as a Ground plane.

A bill of materials describes the parts used on this demo board. A schematic and layout have also been included, along with measured performance characteristics. The above restrictions for the input voltage are valid only for the demo board as shipped with the demo board schematic shown in Figure 1.

2 Operating Conditions

- V_{IN} = 3V to 5.5V
- V_o = 12V
- I_o = 500mA





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3 Pin Description for 6-Pin WSON

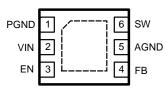


Figure 2. Pin-Out

Table 1. Pin Description

Pin	Name	Function		
1	PGND	Power ground pin. Place PGND and output capacitor GND close together.		
2	VIN	Supply voltage for power stage, and Input supply voltage.		
3	EN	Shutdown control input. Logic high enables operation. Do not allow this pin to float or be greater than VIN + 0.3V.		
4	FB	Feedback pin. Connect FB to external resistor divider to set output voltage.		
5	AGND	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to pin 5		
6	SW	Output switch. Connect to the inductor, output diode.		
DAP	GND	Signal & Power ground. Connect to pin 1 & pin 5 on top layer. Place 4-6 via's from DAP to bottom layer GND plane.		

4 Bill of Materials

Table 2. Bill of Materials

Part ID	Part Value	Manufacturer	Part Number
U1	2.1A Boost Regulator	Texas Instruments	LM2735
C1 Input Cap	22µF, 6.3V, X5R	TDK	C2012X5R0J226M
C5 Input Cap	No Load		
C3 Output Cap	10µF, 25V, X5R	TDK	C3216X5R1E106M
C4 Output Cap	No Load		
C2 Comp Cap	330pF	TDK	C1608X5R1H331K
D1, Catch Diode	0.4V _f Schottky 1A, 20V _R	ST	STPS120M
L1	22µH 2.3A	Coilcraft	DO3316P-223
R3	10.2kΩ, 1%	Vishay	CRCW06031022F
R2	86.6kΩ, 1%	Vishay	CRCW06038662F
R1	100kΩ, 1%	Vishay	CRCW06031003F



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5 LM2735Y η vs Load Current, V_o = 12V

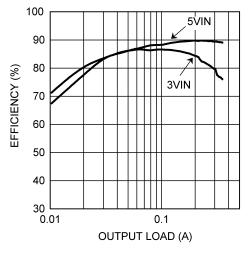


Figure 3. LM2735Y η vs Load Current, V_{o} = 12V



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PCB Layout

6 PCB Layout

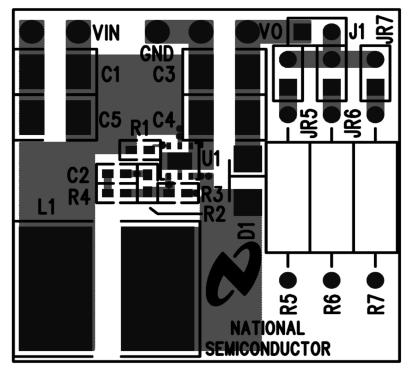


Figure 4. Top Layer

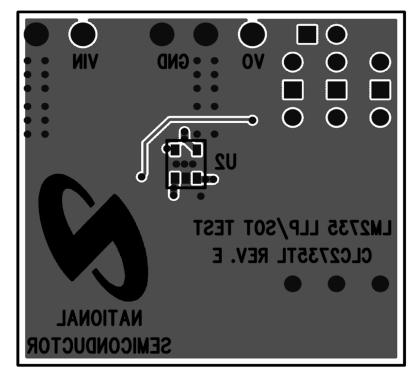


Figure 5. Bottom Layer

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