PMP9360 Test Results

Power Management Solutions

1. Block Diagram

2. Startup/Sequencing

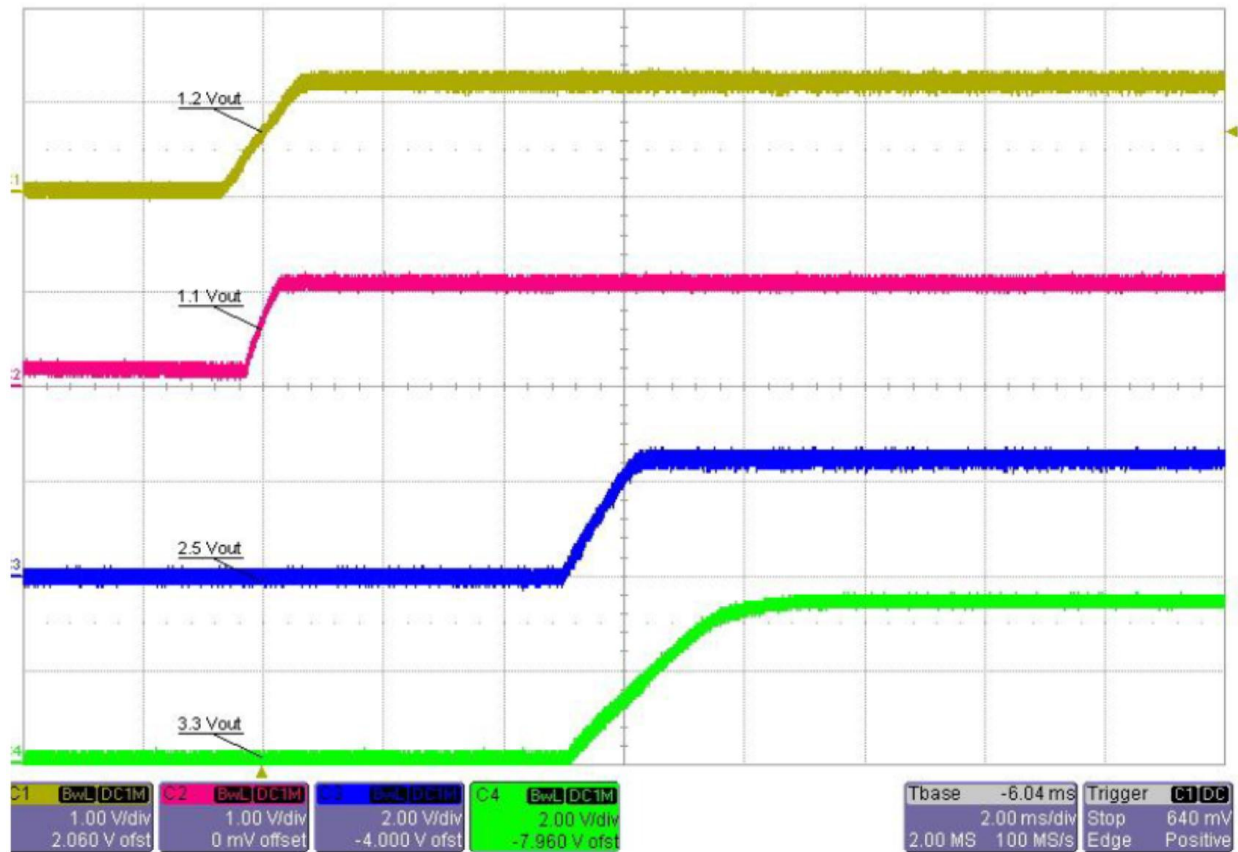The startup waveform is shown in Figure 1 and Figure 1.1. The input voltage is 12V, with no load at the output.

Ch1 => Output voltage 1.2V order #1
Ch2 => Output voltage 1.1V order #1
Ch3 => Output voltage 2.5V order #2
Ch4 => Output voltage 3.3V order #2
2ms/div
Full Bandwidth
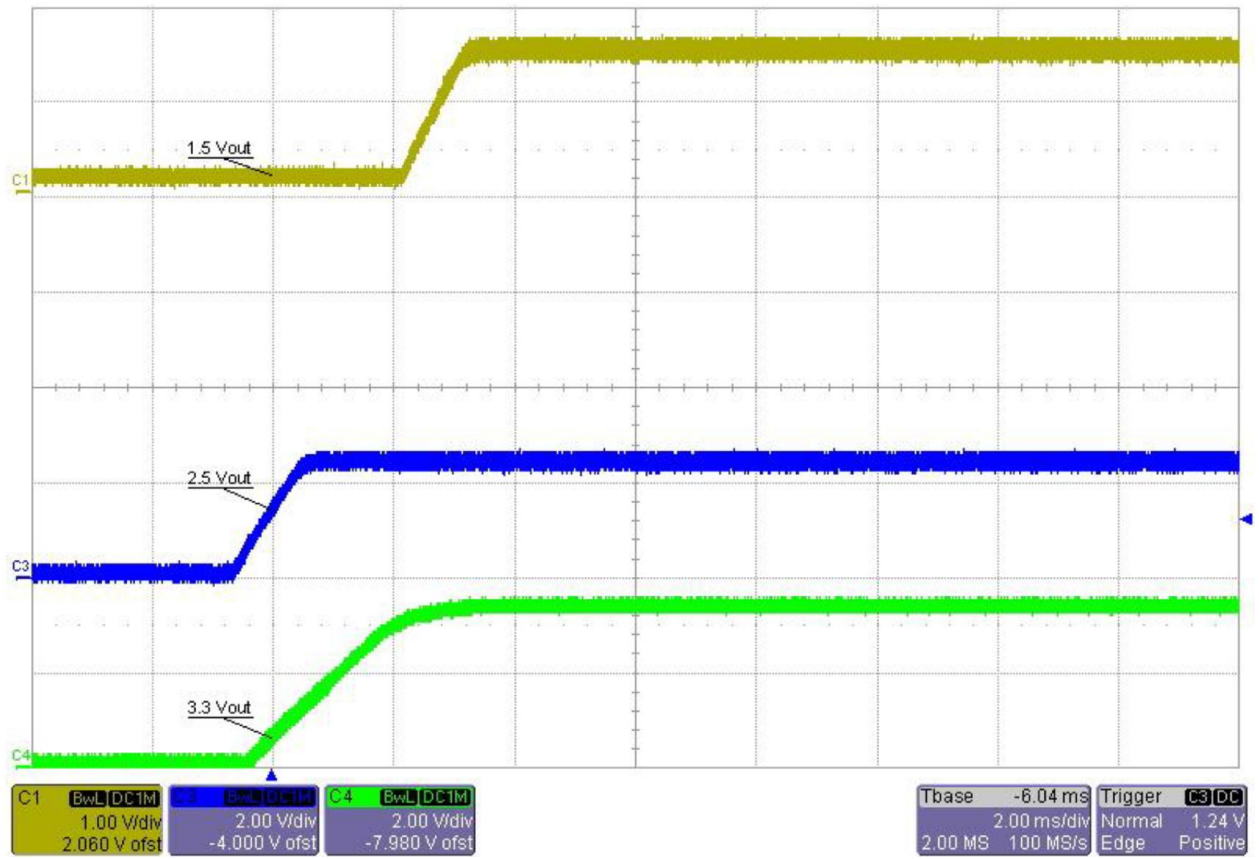
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Figure 1.1
Ch1 => Output voltage 1.5V order #3
Ch3 => Output voltage 2.5V order #2
Ch4 => Output voltage 3.3V order #2
2ms/div
Full Bandwidth

A selection of startup waveforms is shown in Figure 1.2 to demonstrate LDO startup. The input voltage is 12V, with no load at the output.
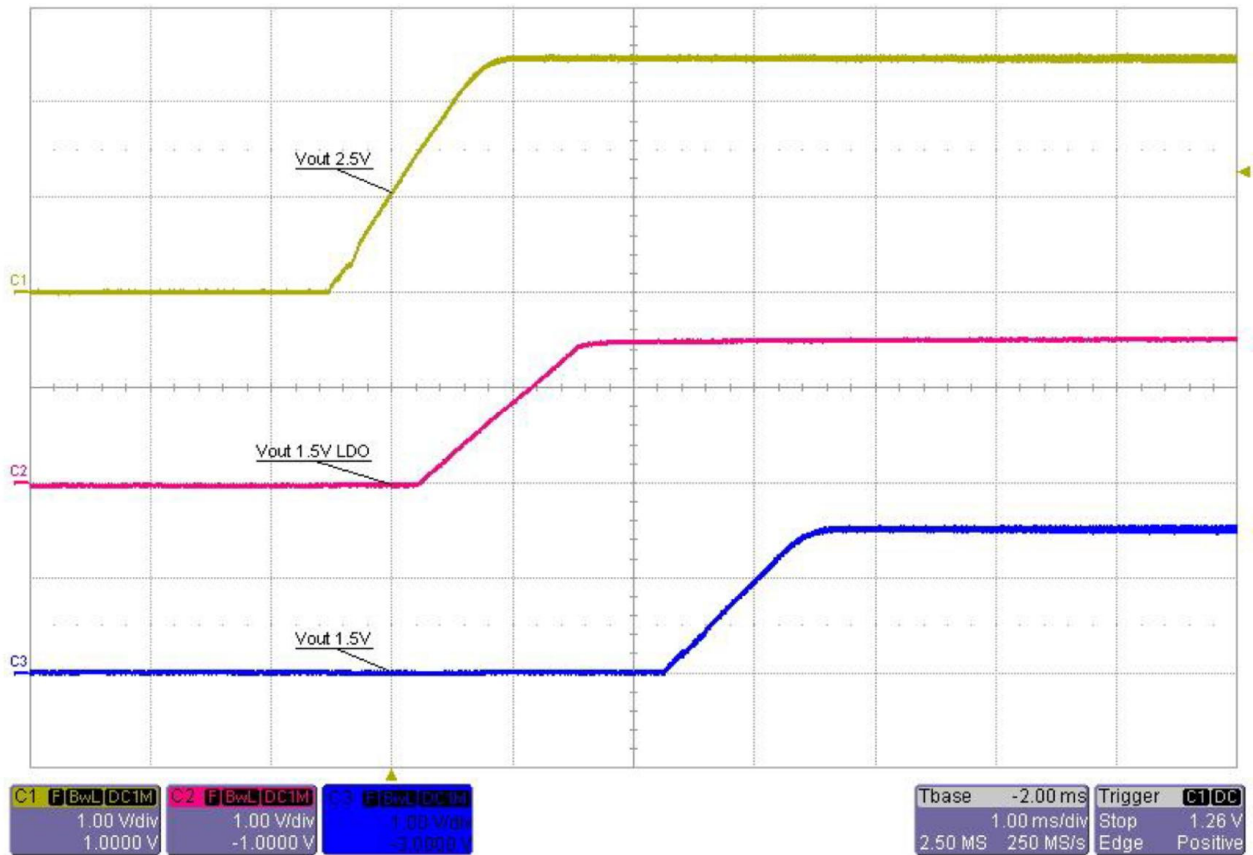

Figure 1.2

Ch1 => Output voltage 2.5V order #2
Ch2 => LDO Output voltage 1.5V order #2 + LDO delay
Ch2 => Output Voltage 1.5V order #3
2.5ms/div
Full Bandwidth

3. Synchronization

The switching nodes of the buck stages are shown in Figure 2 and Figure 2.1. The input voltage is 12V, with no load at the output.
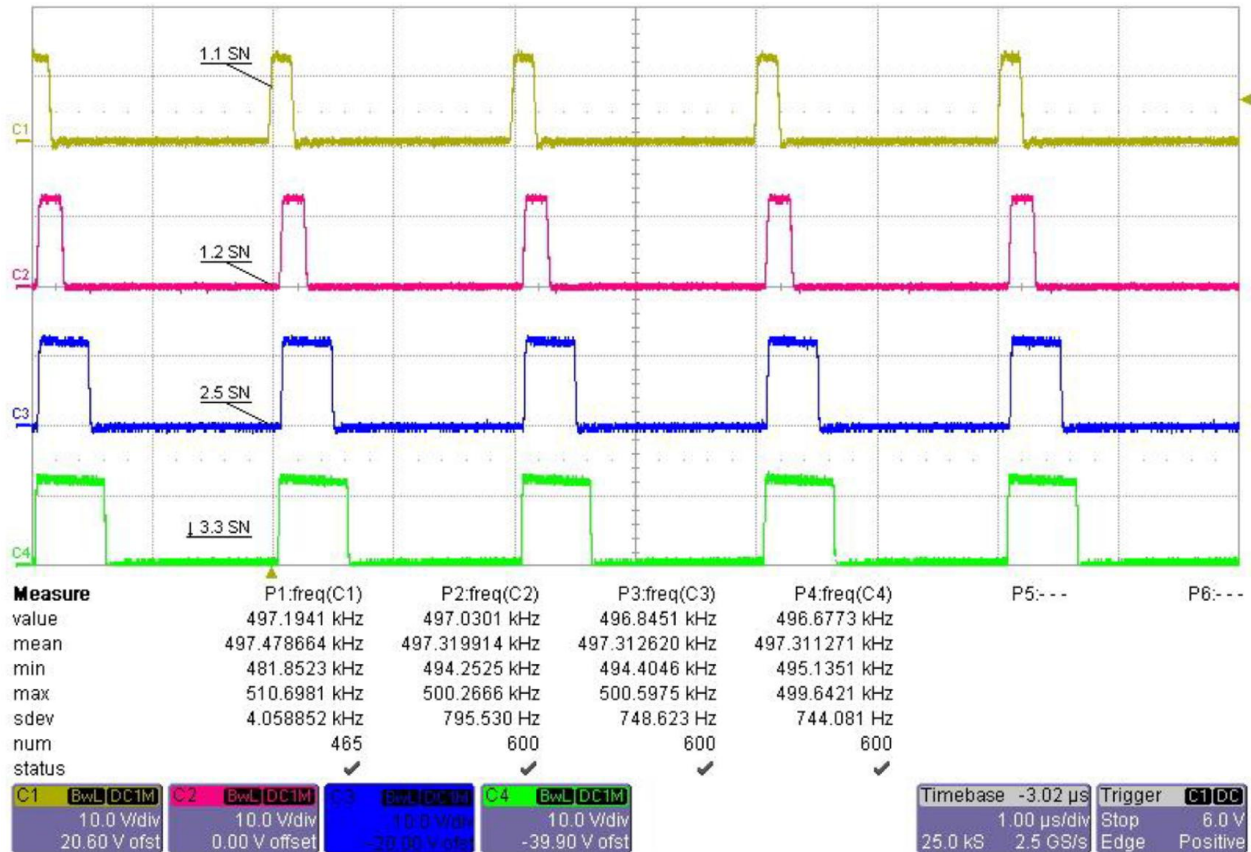

Measure	P1:freq(C1)	P2:freq(C2)	P3:freq(C3)	P4:freq(C4)	P5:- - -	P6:- - -
value	497.1941 kHz	497.0301 kHz	496.8451 kHz	496.6773 kHz		
mean	497.478664 kHz	497.319914 kHz	497.312620 kHz	497.311271 kHz		
min	481.8523 kHz	494.2525 kHz	494.4046 kHz	495.1351 kHz		
max	510.6981 kHz	500.2666 kHz	500.5975 kHz	499.6421 kHz		
sdev	4.058852 kHz	795.530 Hz	748.623 Hz	744.081 Hz		
num	465	600	600	600		
status	✔	✔	✔	✔		

Figure 2

Ch1 => Switching node for 1.1 Vout
Ch2 => Switching node for 1.2 Vout
Ch3 => Switching node for 2.5 Vout
Ch4 => Switching node for 3.3 Vout
Common frequency: 500 kHz
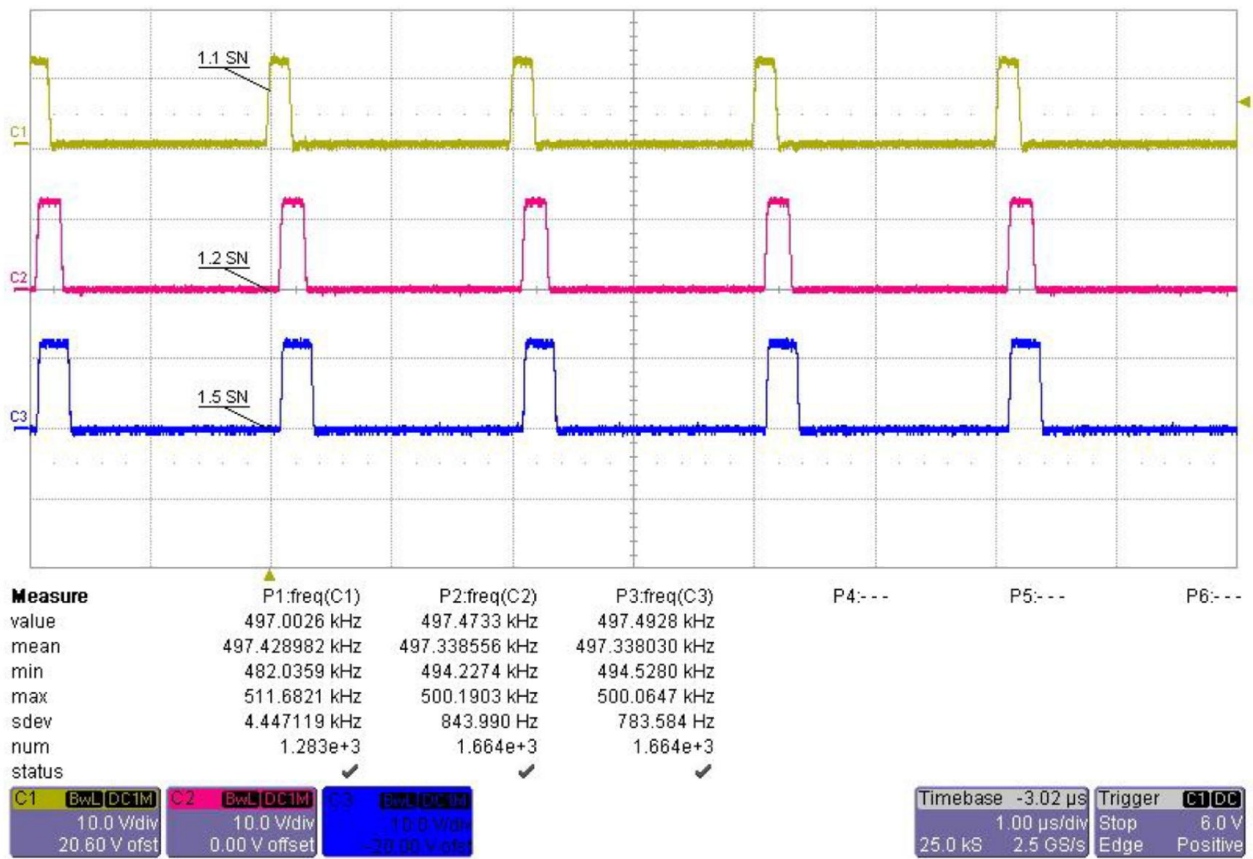*1µs/div*

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Figure 2.1

Ch1 => Switching node for 1.1 Vout
Ch2 => Switching node for 1.2 Vout
Ch3 => Switching node for 1.5 Vout
Common frequency: 500 kHz
1µs/div
Full Bandwidth

4. DDR Tracking
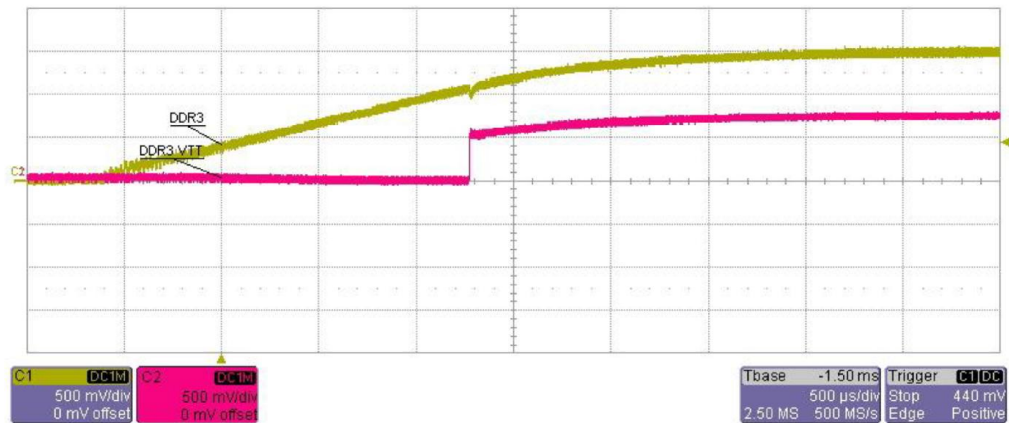
DDR tracking is shown in the Figures 5 and 6.

Figure 5

Ch1 => DDR3 1.5V output voltage from buck stage
Ch2 => DDR3 0.75V termination voltage from TPS51200
500μs/div
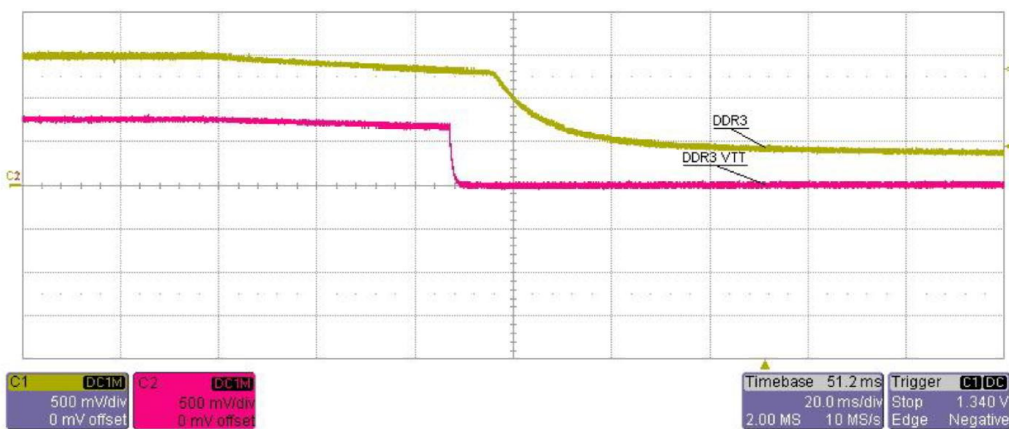*Full Bandwidth*

Figure 6

Ch1 => DDR3 1.5V output voltage from buck stage
Ch2 => DDR3 0.75V termination voltage from TPS51200
20ms/div
Full Bandwidth

5. Efficiency

The respective efficiencies of the buck stages providing 3.3V, 2.5V, 1.2V, 1.1V, and 1.5V are shown in Figures 7, 8, 9, 10, and 11 below. The input voltage is 12V.
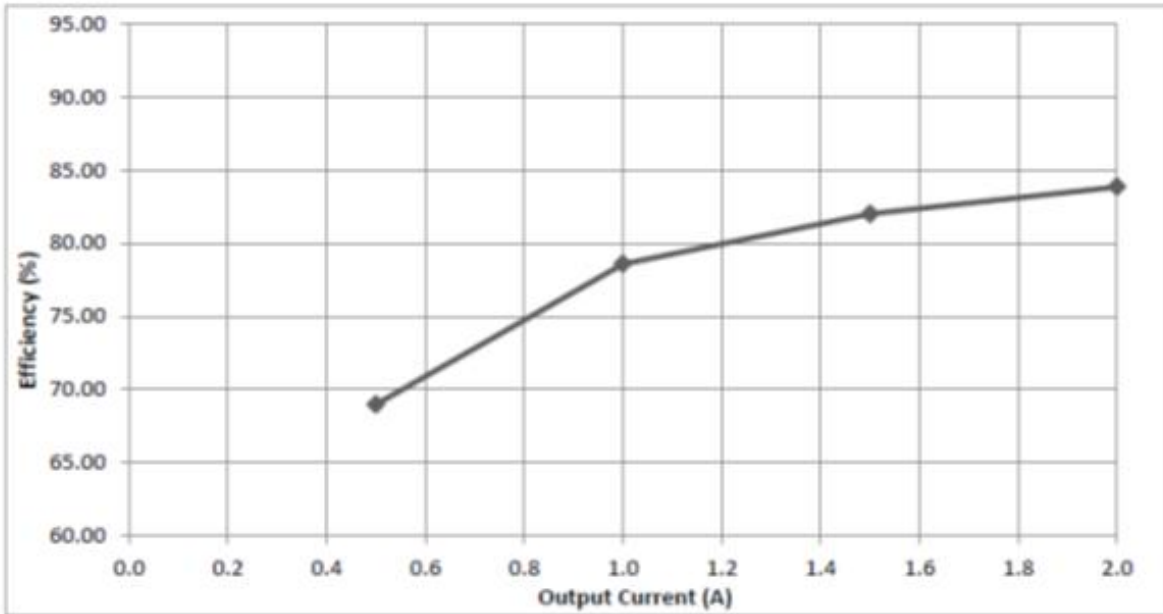

Figure 7:   3.3V Output

VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
12.00	0.20	3.31	0.5	2.400	1.655	68.96
12.00	0.35	3.3	1.0	4.200	3.300	78.57
12.00	0.50	3.28	1.5	6.000	4.920	82.00
12.00	0.65	3.27	2.0	7.800	6.540	83.85

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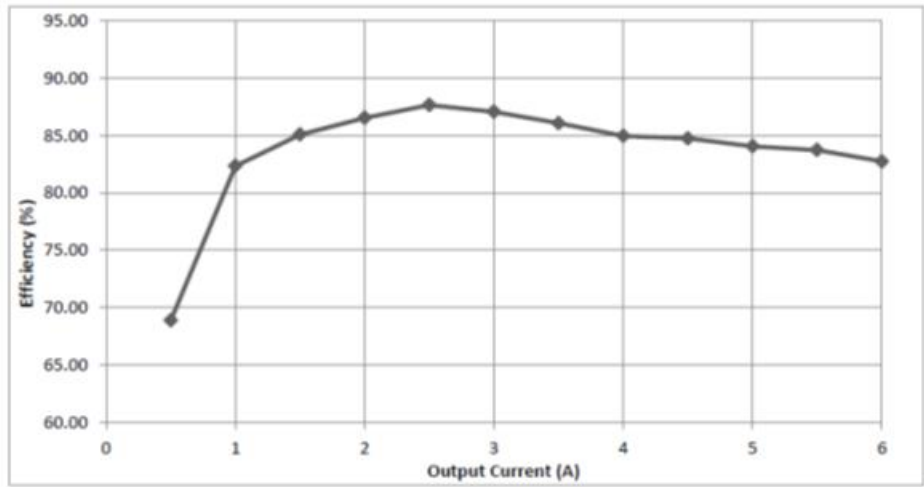
Figure 8:   2.5V Output

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Pin (W)	Pout (W)	Eff (%)
12.00	0.15	2.48	0.5	1.800	1.240	68.89
12.00	0.25	2.47	1.0	3.000	2.470	82.33
12.00	0.36	2.45	1.5	4.320	3.675	85.07
12.00	0.47	2.44	2.0	5.640	4.880	86.52
12.00	0.58	2.44	2.5	6.960	6.100	87.64
12.00	0.70	2.42	3.0	8.340	7.260	87.05
12.00	0.81	2.39	3.5	9.720	8.365	86.06
12.00	0.93	2.37	4.0	11.160	9.480	84.95
12.00	1.04	2.35	4.5	12.480	10.575	84.74
12.00	1.16	2.34	5.0	13.920	11.700	84.05
12.00	1.27	2.32	5.5	15.240	12.760	83.73
12.00	1.39	2.30	6.0	16.680	13.800	82.73
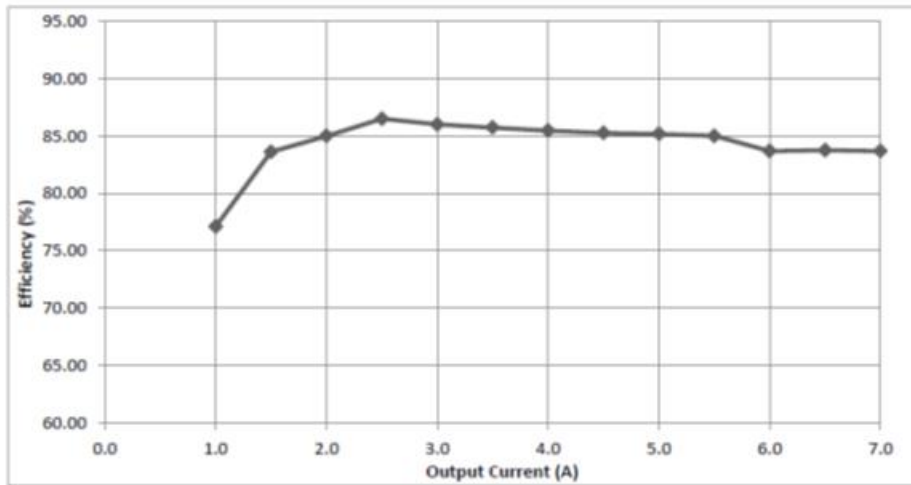
Figure 9:   1.2V Output

VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
11.99	0.13	1.20	1.0	1.559	1.202	77.12
11.98	0.18	1.20	1.5	2.156	1.803	83.61
11.98	0.24	1.20	2.0	2.875	2.404	84.99
11.98	0.29	1.20	2.5	3.474	3.005	86.49
11.98	0.35	1.20	3.0	4.193	3.606	86.00
11.97	0.41	1.20	3.5	4.908	4.207	85.72
11.97	0.47	1.20	4.0	5.626	4.808	85.46
11.97	0.53	1.20	4.5	6.344	5.409	85.26
11.96	0.59	1.20	5.0	7.056	6.010	85.17
11.96	0.65	1.20	5.5	7.774	6.608	85.00
11.96	0.72	1.20	6.0	8.611	7.206	83.68
11.95	0.78	1.20	6.5	9.321	7.807	83.75
11.96	0.84	1.20	7.0	10.046	8.407	83.68
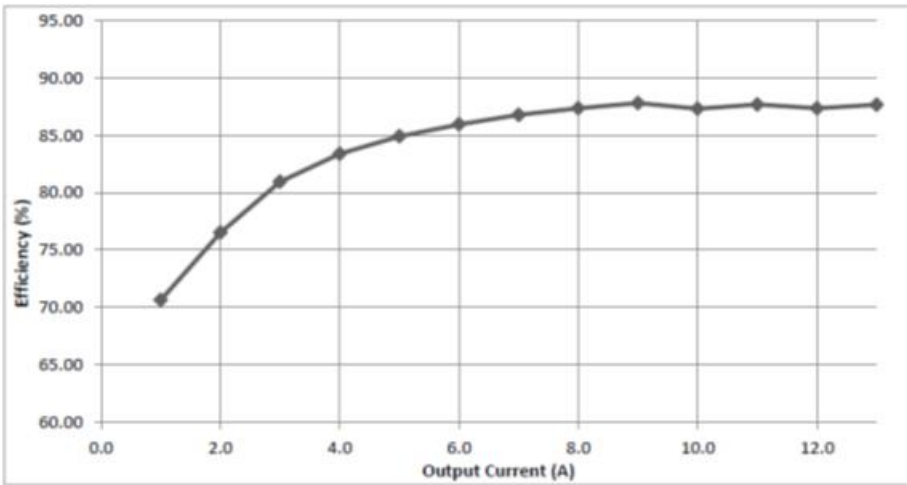
Figure 10: 1.1V Output

VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
12.01	0.13	1.10	1.0	1.561	1.103	70.65
12.00	0.24	1.10	2.0	2.880	2.204	76.51
12.00	0.34	1.10	3.0	4.080	3.303	80.96
12.00	0.44	1.10	4.0	5.280	4.403	83.39
12.00	0.54	1.10	5.0	6.480	5.502	84.91
12.00	0.64	1.10	6.0	7.680	6.601	85.95
11.99	0.74	1.10	7.0	8.873	7.700	86.78
11.99	0.84	1.10	8.0	10.072	8.798	87.35
11.99	0.94	1.10	9.0	11.271	9.896	87.80
11.99	1.05	1.10	10.0	12.590	10.992	87.31
11.99	1.15	1.10	11.0	13.789	12.089	87.67
11.98	1.26	1.10	12.0	15.095	13.186	87.35
11.98	1.36	1.10	13.0	16.293	14.282	87.66
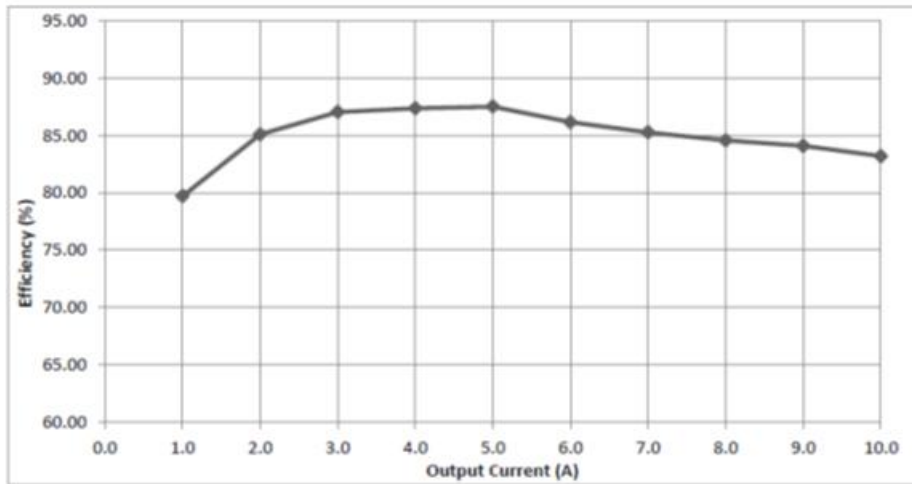
Figure 11:   1.5V Output

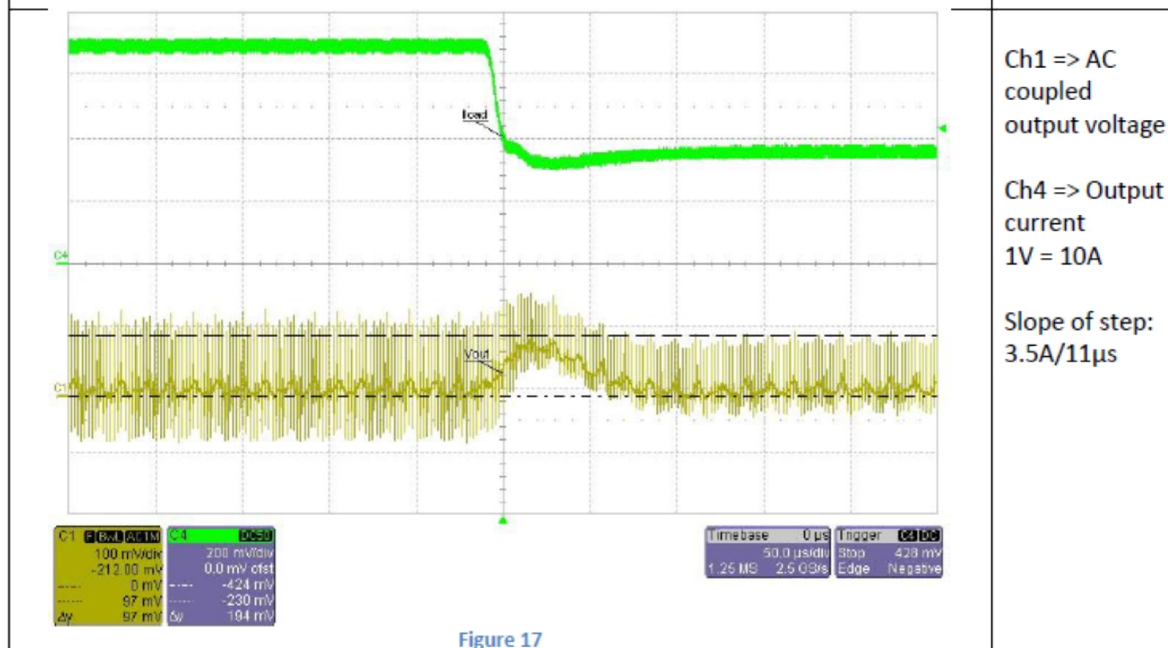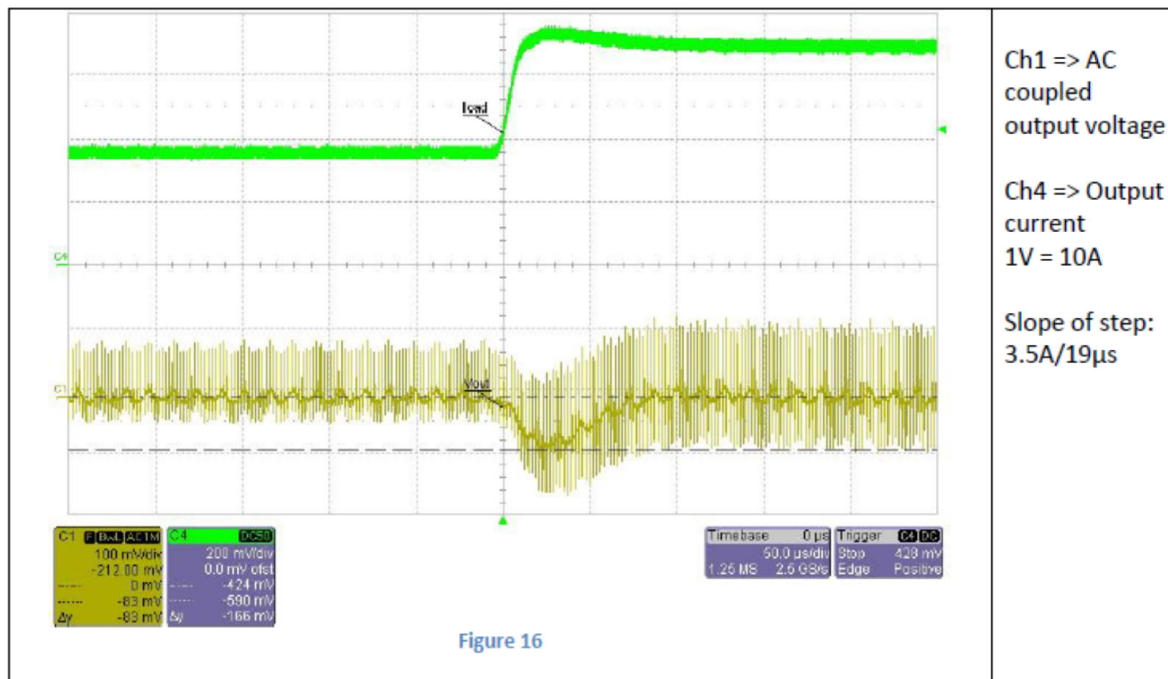| VIN (V)	IIN (A)	VOUT (V)	IOUT (A)	PIN (W)	POUT (W)	Eff (%)
11.99	0.16	1.53	1.0	1.918	1.529	79.70
11.98	0.30	1.53	2.0	3.594	3.058	85.09
11.97	0.44	1.53	3.0	5.267	4.584	87.04
11.96	0.59	1.53	4.0	6.997	6.112	87.36
11.96	0.73	1.53	5.0	8.731	7.640	87.51
11.95	0.89	1.53	6.0	10.636	9.162	86.15
11.94	1.05	1.53	7.0	12.537	10.689	85.26
11.94	1.21	1.53	8.0	14.447	12.216	84.56
11.93	1.37	1.53	9.0	16.344	13.743	84.09
11.92	1.54	1.53	10.0	18.357	15.270	83.18

6. Load Step

The load regulation of the LMZ31503 3.3V output is shown in Figures 12 and 13 below. The input voltage is 12V. The load step increases from 1A to 2A.
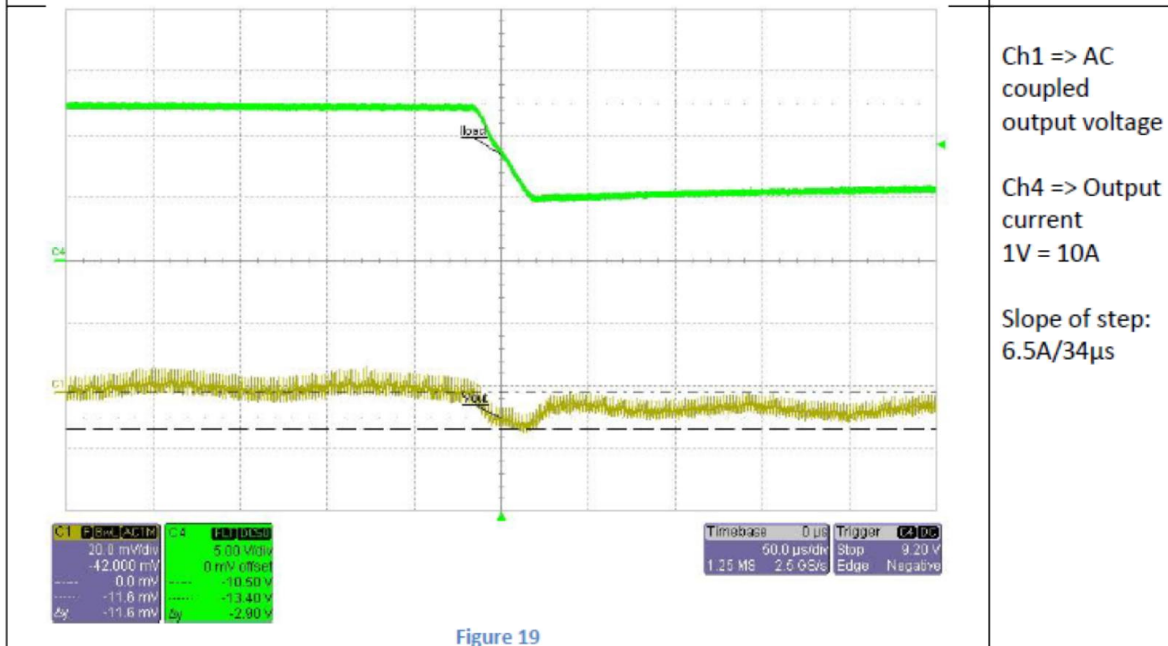

Ch1 => AC coupled output voltage

Ch4 => Output current 1V = 10A

Slope of step: 1A/16.5µs

Figure 12

Ch1 => AC coupled output voltage

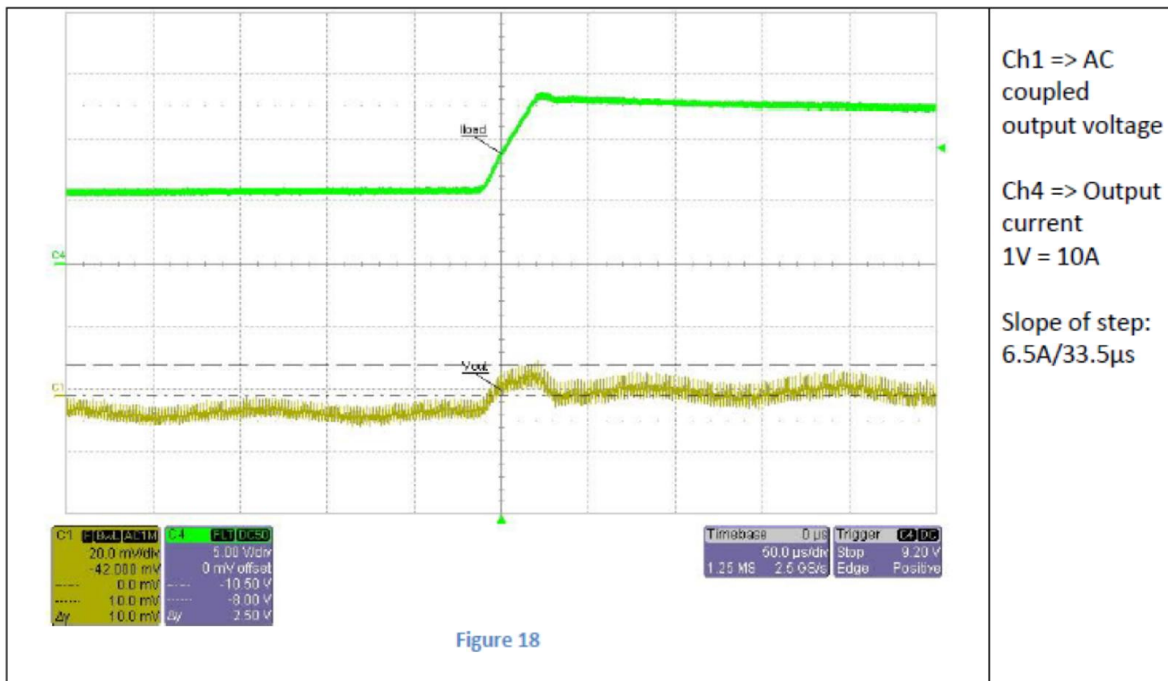Ch4 => Output current 1V = 10A

Slope of step: 1A/20µs
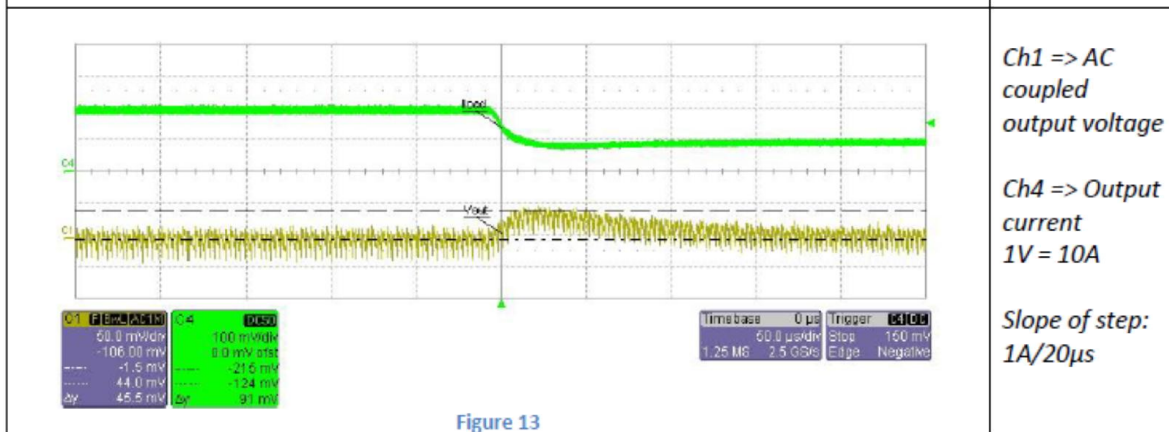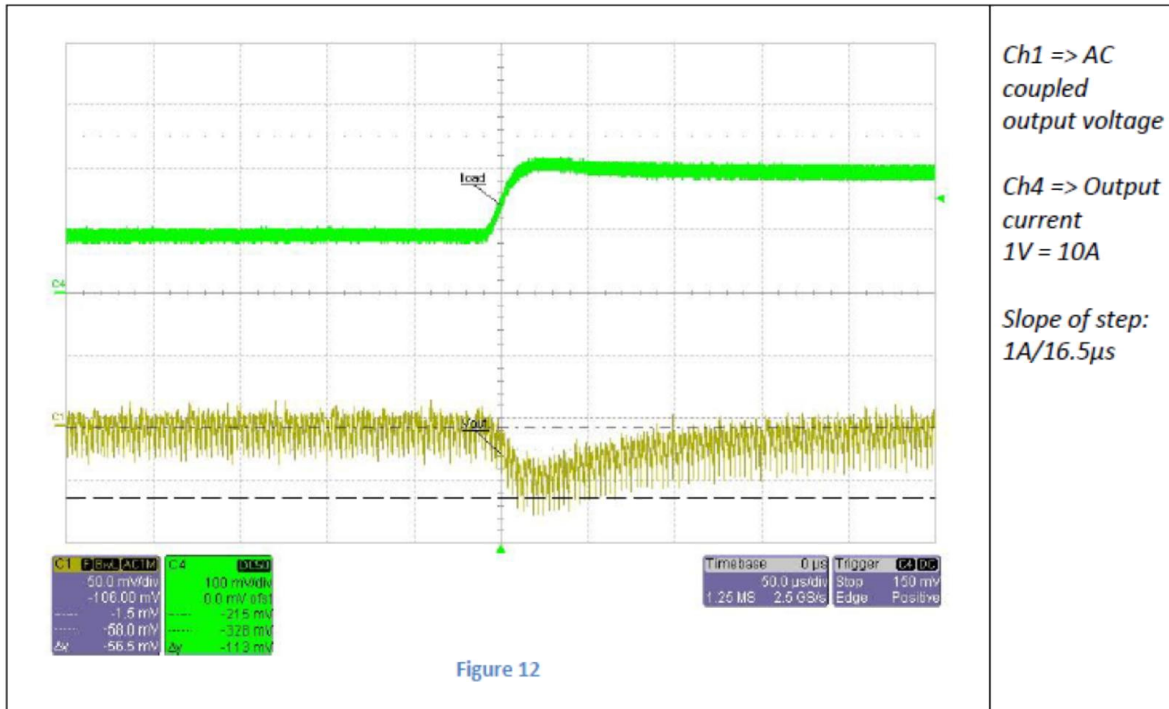
Figure 13

The load regulation of the LMZ31710 2.5V output is shown in Figures 14 and 15 below. The input voltage is 12V. The load step increases from 3A to 6A.

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step: 3A/22µs

Figure 14

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A
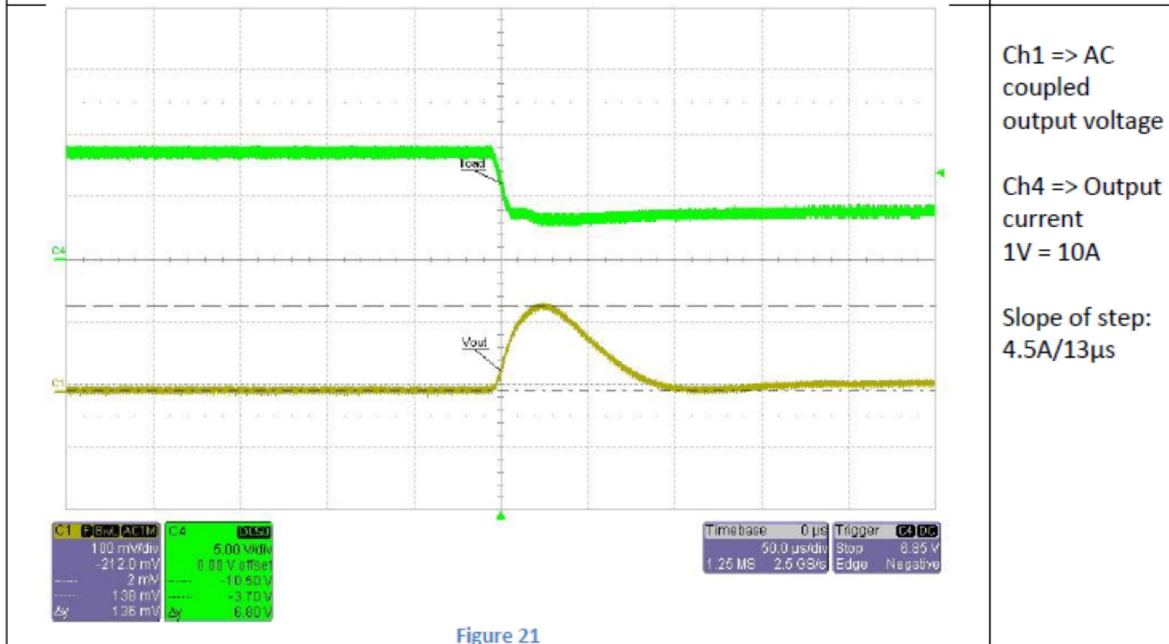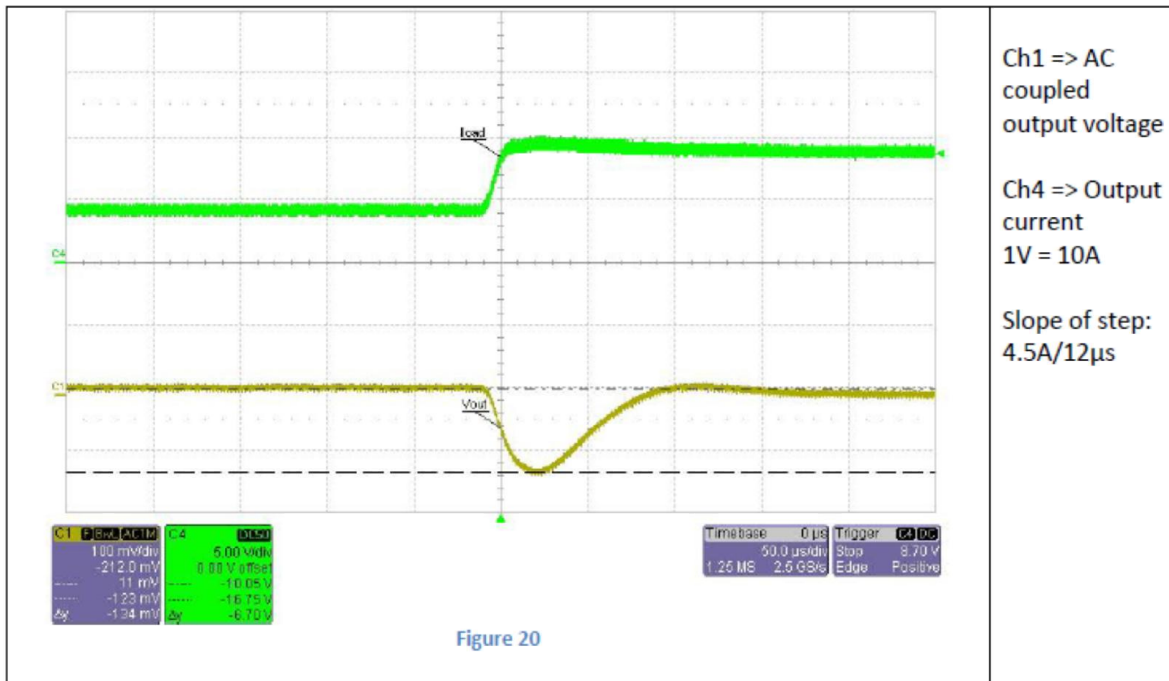
Slope of step: 3A/18µs
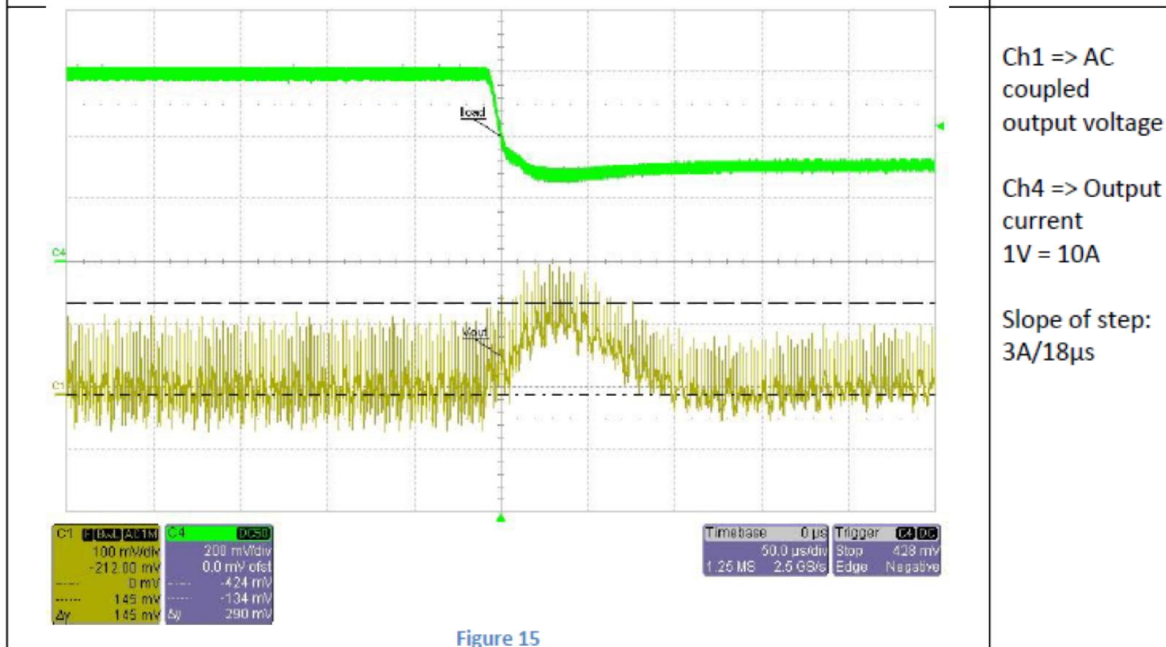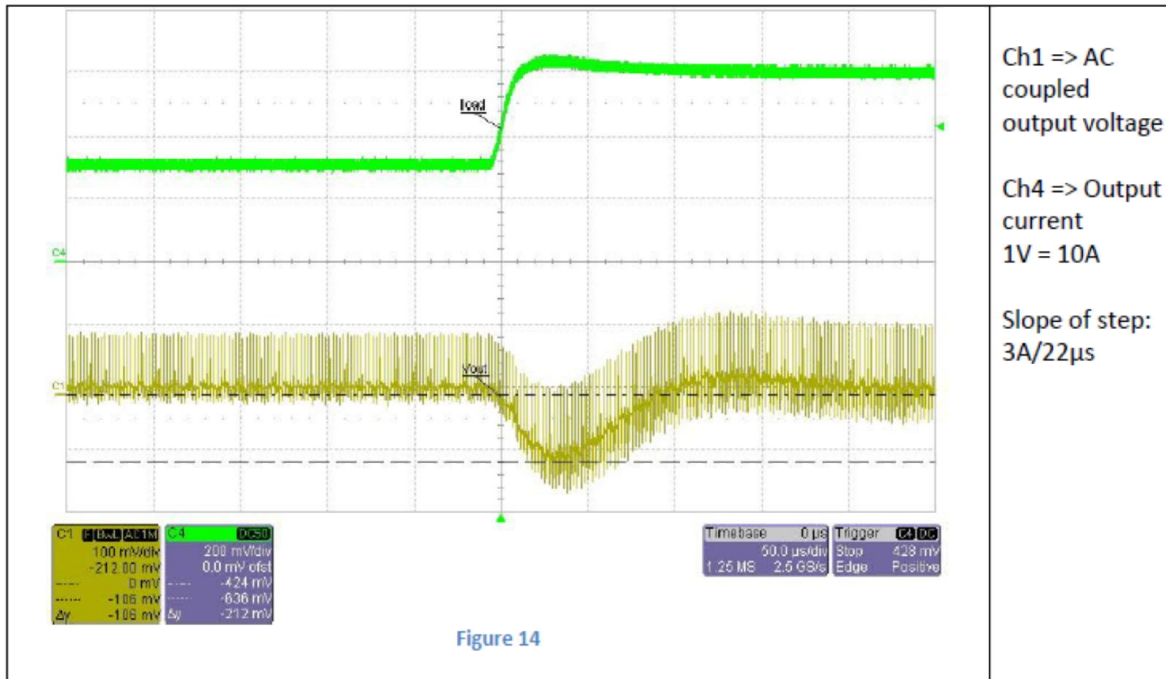
Figure 15

The load regulation of the LMZ31710 1.2V output is shown in the Figures 16 and 17 below. The input voltage is 12V. The load step increases from 3.5A to 7A.
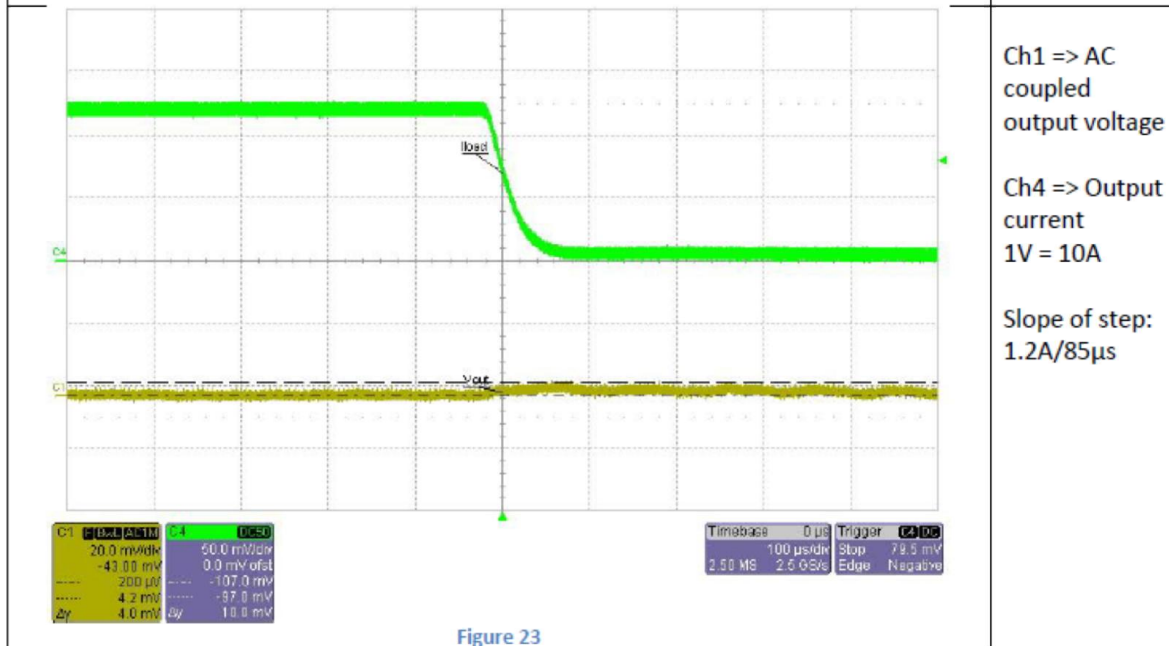

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step:
3.5A/19µs

Figure 16

Ch1 => AC coupled output voltage

Ch4 => Output current
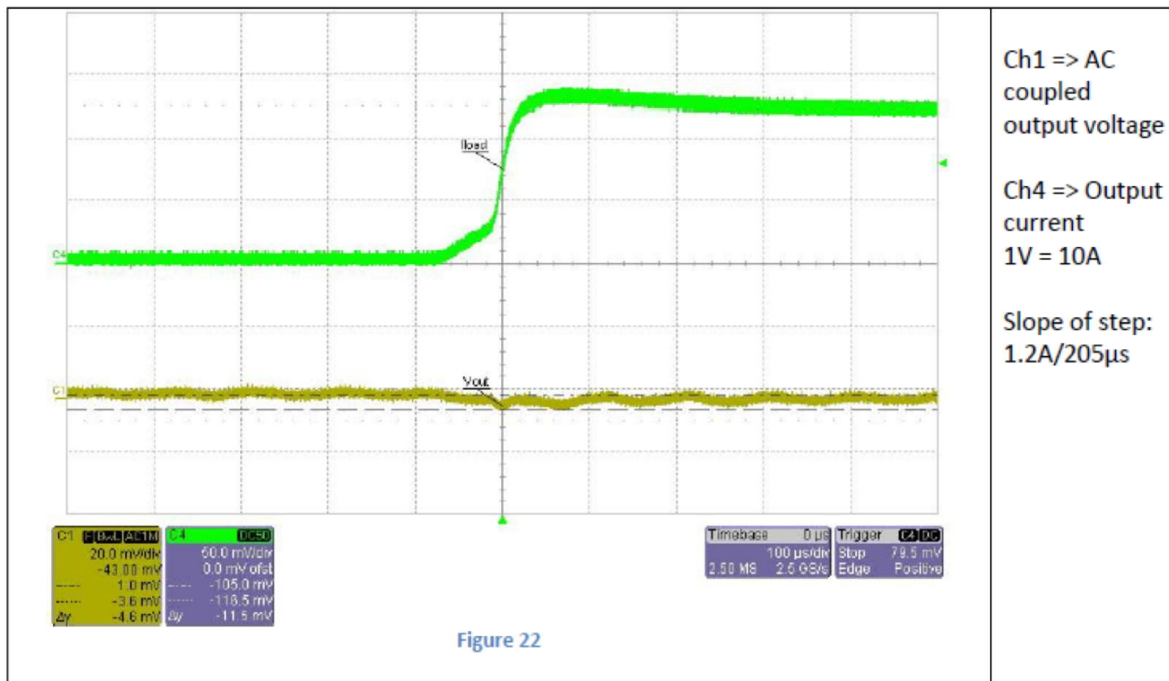1V = 10A

Slope of step:
3.5A/11µs

Figure 17

The load regulation of the LMZ31520 1.1V output is shown in the Figures 18 and 19 below. The input voltage is 12V. The load step increases from 6.5A to 13A.

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step:
6.5A/33.5µs

Figure 18

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step:
6.5A/34µs

Figure 19

The load regulation of the LMZ31710 1.5V output is shown in the Figures 20 and 21 below. The input voltage is 12V. The load step increases from 4.5A to 9A.

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step: 4.5A/12μs

Figure 20

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step: 4.5A/13μs

Figure 21

The load regulation of the 1.5V LDO output is shown in the Figures 22 and 23 below. The input voltage is 12V. The load step increases from 0A to 1.2A.

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step:
1.2A/205µs

Figure 22

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step:
1.2A/85µs

Figure 23

7. Frequency Response

Figure 24 shows the loop response of the LMZ31503 3.3V output with 1A load and 12V input.
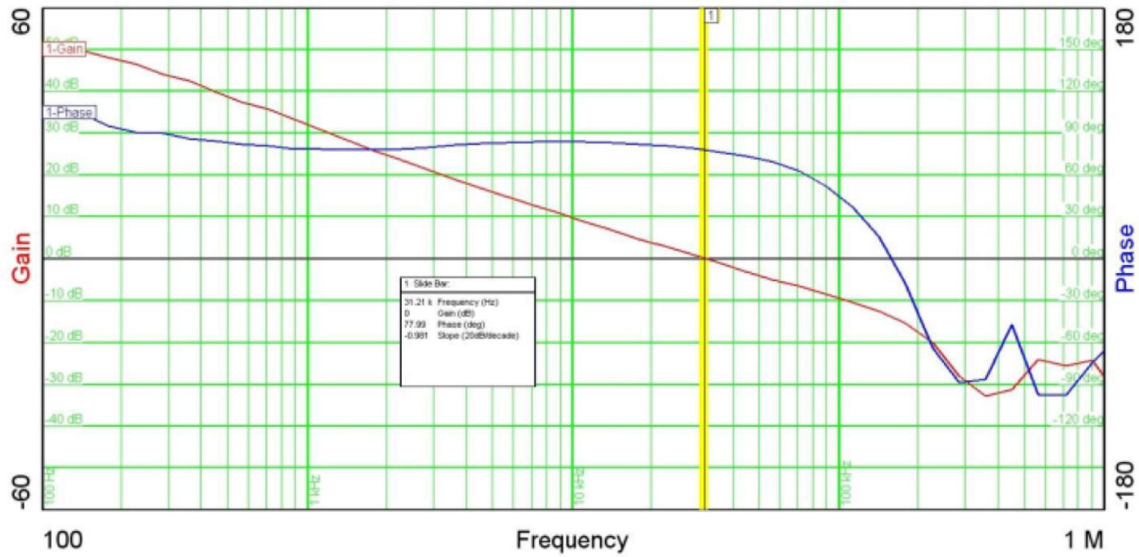
Figure 24

Table 1 summarizes the results from Figure 24.

Bandwidth (kHz)	31.21
Phase Margin	77.99°
Slope (20dB/Decade)	-0.981

Table 1

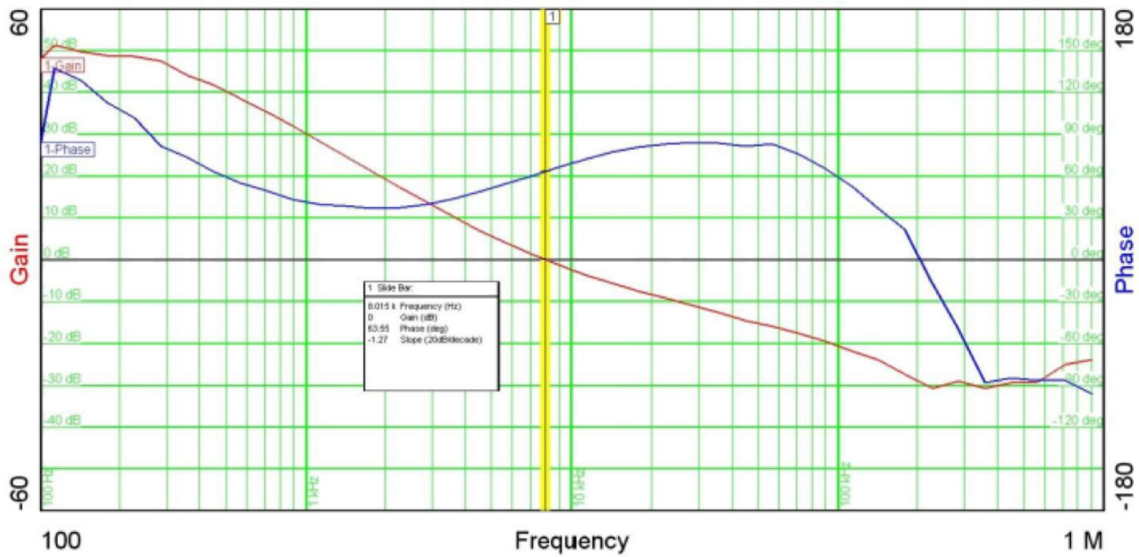Figure 25 shows the loop response of the LMZ31710 2.5V output with 3A load and 12V input.
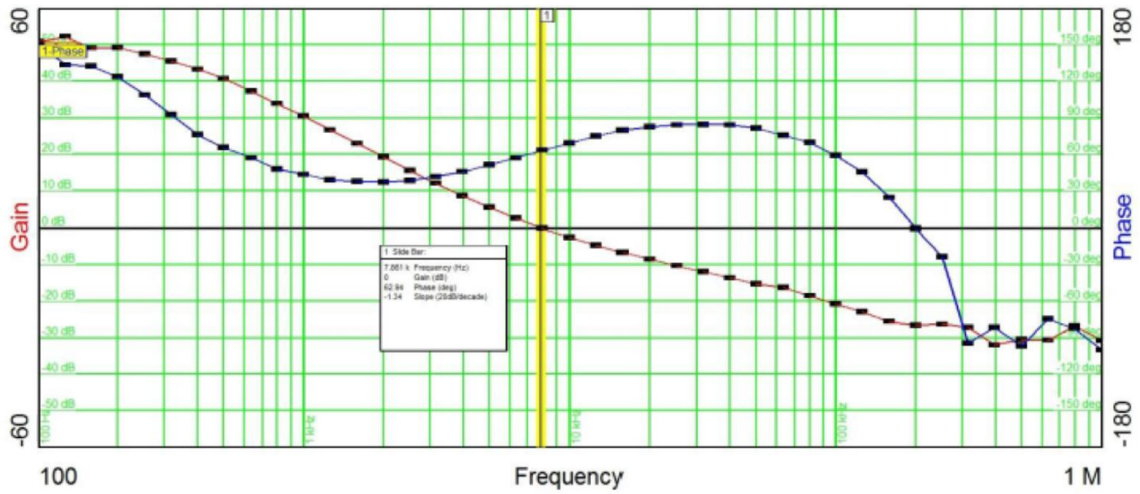
Figure 25

Table 2 summarizes the results from Figure 25.

Bandwidth (kHz)	7.861
Phase Margin	62.94°
Slope (20dB/Decade)	-1.34

Table 2

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Figure 26 shows the loop response of the LMZ31710 1.2V output with 3.5A load and 12V input.

Figure 26

Table 3 summarizes the results from Figure 26.

Bandwidth (kHz)	8.015
Phase Margin	63.55°
Slope (20dB/Decade)	-1.27

Table 3

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Figure 27 shows the loop response of the LMZ31520 1.1V output with 2A load and 12V input.
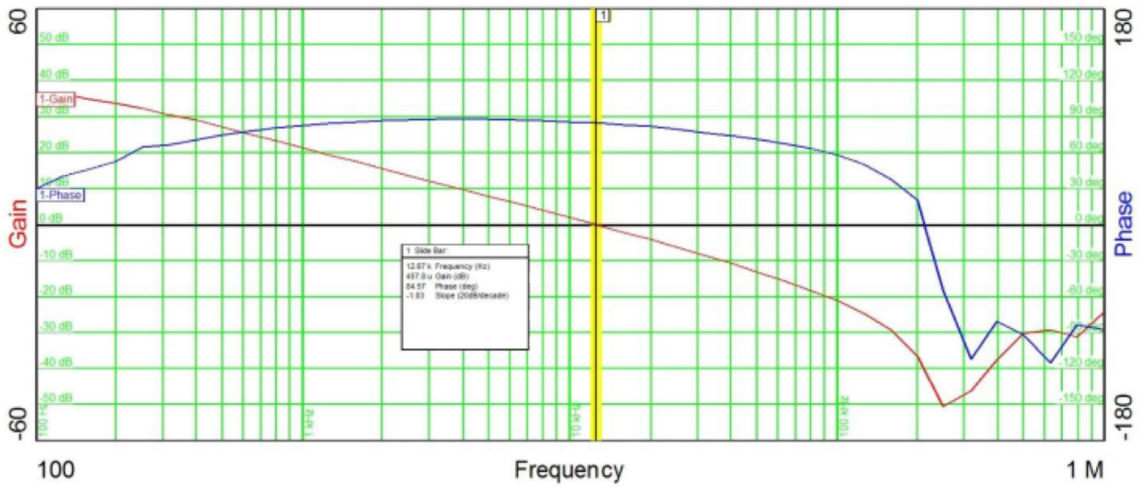
Figure 27

Table 4 summarizes the results from Figure 26.

Bandwidth (kHz)	12.67
Phase Margin	84.57°
Slope (20dB/Decade)	-1.03

Table 4

Figure 28 shows the loop response of the LMZ31710 1.5V output with 5A load and 12V input.
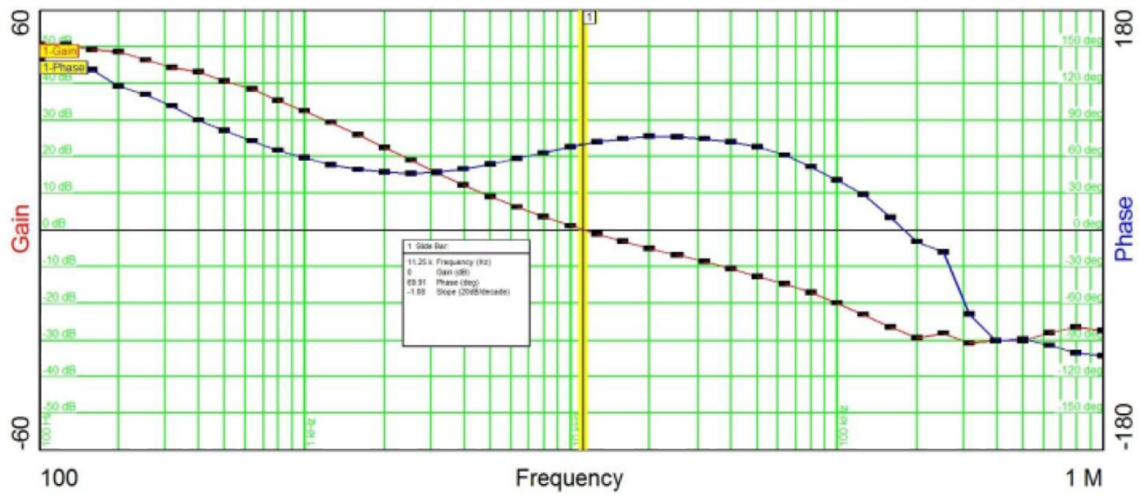

Figure 28

Table 5 summarizes the results from Figure 26.

Bandwidth (kHz)	11.25
Phase Margin	69.9°
Slope (20dB/Decade)	-1.08

Table 5

8. Miscellaneous

In order to synchronize the different buck stages, a square wave clock signal is required with a duty cycle between 20% and 80%. The LMZ31520 is used as the master clock but its duty cycle is only 9.2%. The following schematic and figure show the circuit used in order to provide a clock signal with 50% duty cycle.
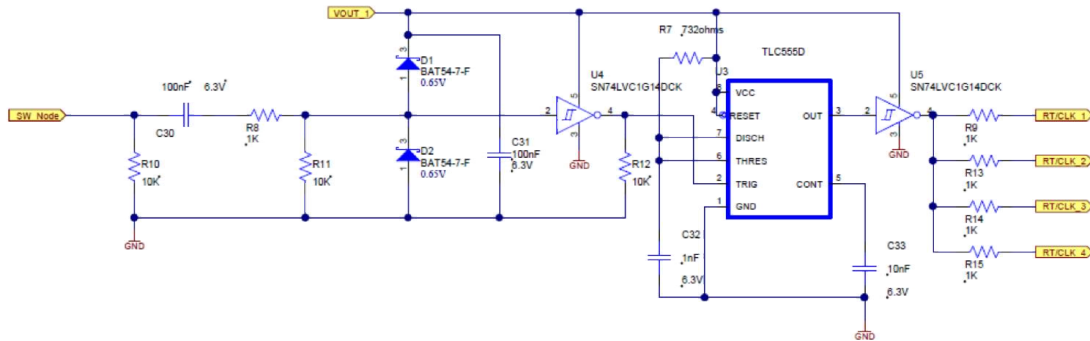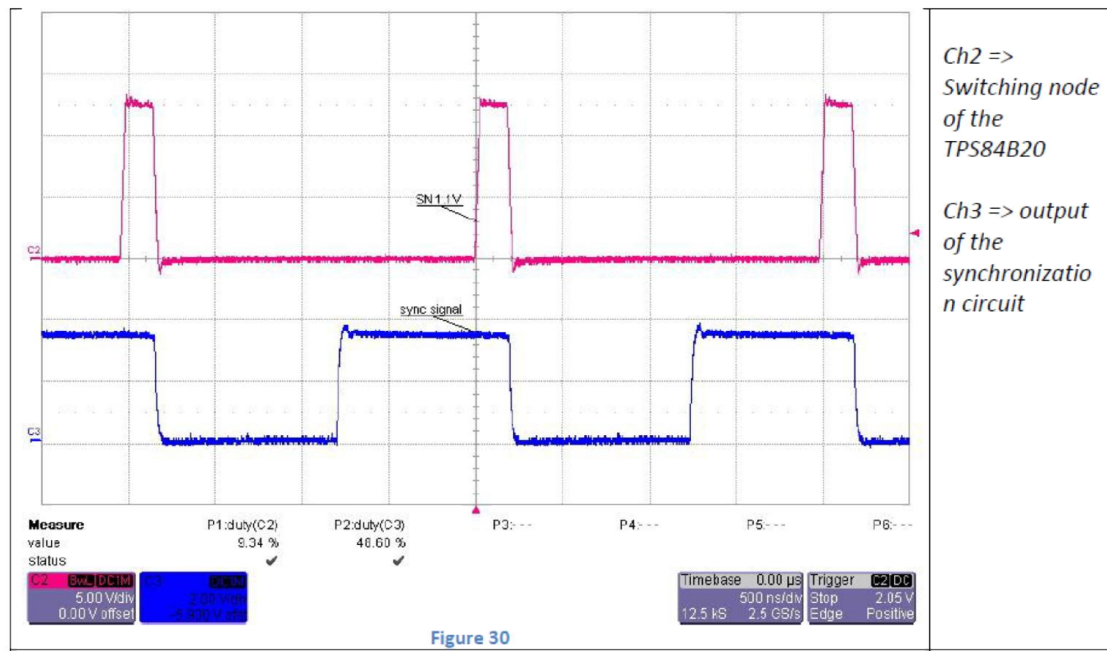

Figure 29:

Synchronization circuit

Ch2 =>
Switching node
of the
TPS84B20

Ch3 => output
of the
synchronizatio
n circuit

Figure 30

Ch2 => Measured duty cycle of the switching node: 9.3%
Ch3 => Measured duty cycle of the synchronization signal: 48.6%

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