With input voltage range and current capability as specified in Table 1, the family of PSR flyback DC/DC converters from TI provides flexibility, scalability, and optimized solution size for a range of applications. Using an 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch, these converters enable isolated DC/DC solutions with high density and low component count.

Table 1. PSR Flyback DC/DC Converter Family

<table>
<thead>
<tr>
<th>PSR FLYBACK CONVERTER</th>
<th>INPUT VOLTAGE RANGE</th>
<th>PEAK SWITCH CURRENT (TYP)</th>
<th>MAXIMUM LOAD CURRENT, V&lt;sub&gt;OUT&lt;/sub&gt; = 12 V, N&lt;sub&gt;PS&lt;/sub&gt; = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5181-Q1</td>
<td>4.5 V to 65 V</td>
<td>0.75 A</td>
<td>90 mA 180 mA 225 mA</td>
</tr>
<tr>
<td>LM5180-Q1</td>
<td>4.5 V to 65 V</td>
<td>1.5 A</td>
<td>180 mA 360 mA 450 mA</td>
</tr>
<tr>
<td>LM25180-Q1</td>
<td>4.5 V to 42 V</td>
<td>1.5 A</td>
<td>180 mA 360 mA 450 mA</td>
</tr>
<tr>
<td>LM25183-Q1</td>
<td>4.5 V to 42 V</td>
<td>2.5 A</td>
<td>300 mA 600 mA 750 mA</td>
</tr>
<tr>
<td>LM25184-Q1</td>
<td>4.5 V to 42 V</td>
<td>4.1 A</td>
<td>500 mA 1 A 1.25 A</td>
</tr>
</tbody>
</table>

The LM5180EVM-DUAL evaluation module (EVM) is a flyback DC/DC converter that employs primary-side regulation (PSR) based on sampling of the primary winding voltage of the transformer to achieve high conversion efficiency in a small footprint. It operates over a wide input voltage range of 10 V to 65 V and delivers dual isolated outputs of 15 V and −7.7 V at 200-mA rated load current. Operating without an optocoupler or transformer auxiliary winding, the converter provides an output voltage with better than ±2% load regulation. The flyback transformer has a turns ratio of 1 : 1 : 0.52 (PRI : SEC1 : SEC2) and provides 1500 VRMS primary-to-secondary isolation.

The EVM design uses the LM5180-Q1 PSR flyback converter with wide input voltage (wide V<sub>IN</sub>) range. An integrated 100-V, 1.5-A power MOSFET provides ample margin for line transients and switch (SW) node voltage spikes related to transformer parasitic leakage inductance. Load regulation errors related to transformer secondary winding resistance are avoided by virtue of the quasi-resonant boundary conduction mode (BCM) control scheme.

Additional features include current-mode control with internal compensation, hiccup-mode fault protection, low input quiescent current, programmable soft-start, and optional output voltage temperature compensation. UVLO protects the converter at low input voltage conditions, and the EN/UVLO pin supports adjustable input UVLO with user-defined hysteresis for application specific power-up and power-down requirements.

The LM5180 and LM5180-Q1 are available in a 8-pin WSON package with 4-mm × 4-mm footprint and 0.8-mm pin pitch to enable isolated DC/DC solutions with high density and low component count. Wettable flank pins provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs in high-reliability industrial and automotive applications. See the LM5180 and LM5180-Q1 device data sheets for more information.

Use the LM5180-Q1 with WEBENCH® Power Designer to create a custom regulator design. Furthermore, the user can download the LM5180 Quickstart Calculator to optimize component selection and examine predicted efficiency performance across line and load ranges.
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12 Output 1 Load Transient, 50 mA to 200 mA at 100mA/µs, I_{OUT2} = –200 mA, V_{IN} = 24 V .......... 12
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Trademarks
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1 High Density EVM Description

The **LM5180EVM-DUAL** EVM is designed to use a regulated or non-regulated high-voltage input rail ranging from 10 V to 65 V to produce a tightly-regulated, isolated output voltages of 15 V and –7.7 V at load currents up to 200 mA. This wide $V_{IN}$ range isolated DC/DC solution offers outsized voltage rating and operating margin to withstand supply rail voltage transients.

The power-train passive components selected for this EVM, including flyback transformer, flyback rectifying diodes, and ceramic input and output capacitors, are available from multiple component vendors. Transformers with functional or basic grade isolation are available with isolation voltages of 1.5 kV and greater.

1.1 Typical Applications
- Automotive HEV/EV powertrain systems
- Sub-AM band automotive body electronics
- Traction inverters: IGBT and SiC gate drivers
- Isolated field transmitters and field actuators
- Building automation HVAC systems
- Isolated bias power rails

1.2 Features and Electrical Performance
- Tightly-regulated, isolated output voltages of 15 V and –7.7 V with better than ±2% load regulation from 1% to 100% load
- Wide input voltage operating range of 10 V to 65 V
- Full load current of 200 mA, both outputs
- Maximum switching frequency of 350 kHz remains below the AM band for automotive applications
- High efficiency across wide load current range
  - Full load efficiency of 88% and 87.5% at $V_{IN} = 24$ V and 48 V, respectively
  - 88.5% efficiency at half-rated load, $V_{IN} = 24$ V
- 1.4-mA and 1.1-mA no-load supply current at $V_{IN} = 24$ V and 48 V, respectively
- Ultra-low conducted and radiated EMI signatures
  - Optimized for CISPR 25 class 5 requirements
  - Soft switching avoids diode reverse recovery
  - Input π-stage EMI filter with damping from electrolytic capacitor ESR
- Boundary conduction mode (BCM) control architecture provides fast line and load transient response
  - Peak current-mode control
  - Quasi-resonant switching for reduced power loss
  - Internal loop compensation
- Integrated 100-V flyback power MOSFET
  - Provides large headroom for input voltage transients
- Cycle-by-cycle overcurrent protection (OCP)
- Monotonic prebias output voltage start-up
- User-adjustable soft-start time set to 8 ms by 47-nF capacitor connected between SS/BIAS and GND
  - Option for external bias using transformer auxiliary winding connected to SS/BIAS
- Resistor-programmable input voltage UVLO with customizable hysteresis for applications with wide turn-on and turn-off voltage difference
  - Input UVLO set to turn on and off at $V_{IN}$ of 9 V and 7 V, respectively
- Low transformer primary-to-secondary (interwinding) capacitance to accommodate high $dv/dt$ secondary-side common-mode swings
- Fully assembled, tested, and proven PCB layout with 55-mm × 38-mm total footprint
## EVM Performance Characteristics

### Table 2. Electrical Performance Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage range, (V_{\text{IN}})</td>
<td>Operating</td>
<td>10</td>
<td>48</td>
<td>65</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage turnon, (V_{\text{IN(ON)}})</td>
<td>Adjusted using EN/UVLO divider resistors</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage turnoff, (V_{\text{IN(OFF)}})</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage hysteresis, (V_{\text{IN(HYS)}})</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input current, no load, (I_{\text{IN(NL)}})</td>
<td>(I_{\text{OUT1}} = I_{\text{OUT2}} = 0 \text{ mA}) (V_{\text{IN}} = 24 \text{ V}) (1.4)</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 48 \text{ V}) (1.1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 65 \text{ V}) (1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input current, disabled, (I_{\text{IN(OFF)}})</td>
<td>(V_{\text{EN}} = 0 \text{ V}) (V_{\text{IN}} = 24 \text{ V}) (10)</td>
<td>(\mu\text{A})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage, (V_{\text{OUT1}})</td>
<td>(I_{\text{OUT1/2}} = 5 \text{ mA to 200 mA})</td>
<td>14.7</td>
<td>15.0</td>
<td>15.3</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage, (V_{\text{OUT2}})</td>
<td></td>
<td>-7.5</td>
<td>-7.7</td>
<td>-7.9</td>
<td>V</td>
</tr>
<tr>
<td>Output current, (I_{\text{OUT1}})</td>
<td>(I_{\text{OUT2}}) (2) (V_{\text{IN}} = 12 \text{ V})</td>
<td>0</td>
<td>180</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 24 \text{ V})</td>
<td>0</td>
<td>220</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 48 \text{ V})</td>
<td>0</td>
<td>300</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 70 \text{ V})</td>
<td>0</td>
<td>350</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage regulation, (\Delta V_{\text{OUT}})</td>
<td>Load regulation, (V_{\text{IN}} = 24 \text{ V}) (I_{\text{OUT}} = 5 \text{ mA to 200 mA})</td>
<td>1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Line regulation, (I_{\text{OUT}} = 100 \text{ mA}) (V_{\text{IN}} = 10 \text{ V to 65 V})</td>
<td>1%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage ripple, (V_{\text{OUT(AC)}})</td>
<td>(V_{\text{IN}} = 24 \text{ V}, I_{\text{OUT1}} = I_{\text{OUT2}} = 200 \text{ mA})</td>
<td>100</td>
<td></td>
<td></td>
<td>mVrms</td>
</tr>
<tr>
<td>Output overcurrent protection, (I_{\text{OCP}})</td>
<td>(V_{\text{IN}} = 24 \text{ V})</td>
<td>250</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Soft-start time, (t_{\text{SS}})</td>
<td>(C_{\text{SS}} = 47 \text{ nF})</td>
<td>8</td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td><strong>SYSTEM CHARACTERISTICS</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching frequency, (F_{\text{SW(nom)}})</td>
<td>(V_{\text{IN}} = 24 \text{ V}, I_{\text{OUT1}} = I_{\text{OUT2}} = 100 \text{ mA})</td>
<td>350</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Half-load efficiency, (\eta_{\text{HALF}}) (1)</td>
<td>(I_{\text{OUT1}} = I_{\text{OUT2}} = 100 \text{ mA}) (V_{\text{IN}} = 12 \text{ V})</td>
<td>88.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 24 \text{ V})</td>
<td>88.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 48 \text{ V})</td>
<td>86%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 65 \text{ V})</td>
<td>85%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full load efficiency, (\eta_{\text{FULL}})</td>
<td>(I_{\text{OUT1}} = I_{\text{OUT2}} = 200 \text{ mA}) (V_{\text{IN}} = 24 \text{ V})</td>
<td>88%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 48 \text{ V})</td>
<td>87.5%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{\text{IN}} = 65 \text{ V})</td>
<td>87%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isolation rating(3)</td>
<td>Functional insulation</td>
<td>1500</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>LM5180 junction temperature, (T_{j})</td>
<td></td>
<td>-40</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) The default output voltages of this EVM are 15 V and –7.7 V. Efficiency and other performance metrics can change based on operating input voltage, load currents, externally-connected output capacitance(s), and other parameters.

(2) The output power delivered by the LM5180-Q1 PSR flyback converter increases with input voltage.

(3) The selected transformer provides functional isolation.
3 Application Circuit Diagram

Figure 1 shows the schematic of an LM5180-based flyback converter (EMI filter stage not shown). Soft start (SS), temperature compensation (TC), and UVLO (EN/UVLO) components are shown that are configurable as required by the specific application. The transformer turns ratio is 1 : 1: 0.52 and the primary-referred magnetizing inductance is 30 µH.

Figure 1. LM5180 PSR Flyback Dual-Output Schematic

4 EVM Photo

Figure 2. Dual-Output EVM Photo, 55 mm × 38 mm
5 Test Setup and Procedure

5.1 Test Setup

Table 3. EVM Connections

<table>
<thead>
<tr>
<th>LABEL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN+</td>
<td>Positive input voltage power and sense connection</td>
</tr>
<tr>
<td>VIN−</td>
<td>Negative input voltage power and sense connection</td>
</tr>
<tr>
<td>VOUT1</td>
<td>Output #1 power and sense connection</td>
</tr>
<tr>
<td>VOUT2</td>
<td>Output #2 power and sense connection</td>
</tr>
<tr>
<td>S-GND</td>
<td>Output return and sense connection</td>
</tr>
<tr>
<td>EN</td>
<td>ENABLE input – tie to GND to disable converter</td>
</tr>
<tr>
<td>SS/BIAS</td>
<td>External BIAS input</td>
</tr>
<tr>
<td>SW</td>
<td>SW node connection</td>
</tr>
</tbody>
</table>

Referencing the EVM connections described in Table 3, the recommended test setup to evaluate the LM5180EVM-DUAL is shown in Figure 3. Working at an ESD-protected workstation, make sure that any wrist straps, boot straps, or mats are connected and referencing the user to earth ground before power is applied to the EVM.

Refer to the LM5180 and LM5180-Q1 data sheets, LM5180 Quickstart Calculator, and WEBENCH® Power Designer for additional guidance pertaining to component selection and converter operation.
5.2 Test Equipment

**Voltage Source:** The input voltage source $V_{IN}$ must be a 0–65-V variable DC source.

**Multimeters:**
- **Voltmeter 1:** Input voltage at VIN+ to VIN–. Set voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 2:** Output voltage at VOUT1 to SGND. Set voltmeter to an input impedance of 100 MΩ.
- **Voltmeter 3:** Output voltage at VOUT2 to SGND. Set voltmeter to an input impedance of 100 MΩ.
- **Ammeter 1:** Input current. Set ammeter to 1-second aperture time.
- **Ammeter 2:** Load current, output #1. Set ammeter to 1-second aperture time.
- **Ammeter 3:** Load current, output #2. Set ammeter to 1-second aperture time.

**Electronic Loads:** The loads must be electronic constant-resistance (CR) or constant-current (CC) mode load capable of 0 Adc to 300 mAdc up to 15 V. For a no-load input current measurement, disconnect the electronic load as it may draw a small residual current.

**Oscilloscope:** With the scope set to 20-MHz bandwidth and AC coupling, measure the output voltage ripple directly across an output capacitor with a short ground lead normally provided with the scope probe. Place the oscilloscope probe tip on the positive terminal of the output capacitor, holding the ground barrel of the probe through the ground lead to the negative terminal of the capacitor. TI does not recommend using a long-leaded ground connection because this may induce additional noise given a large ground loop. To measure other waveforms, adjust the oscilloscope as needed.

**Safety:** Always use caution when touching any circuits that may be live or energized.

5.3 Recommended Test Setup

5.3.1 Input Connections

- Prior to connecting the DC input source, set the current limit of the input supply to 100 mA maximum. Ensure the input source is initially set to 0 V and connected to the VIN+ and VIN– connection points as shown in Figure 3. An additional input bulk capacitor is recommended to provide damping if long input lines are used.
- Connect voltmeter 3 at VIN+ and VIN– connection points to measure the input voltage.
- Connect ammeter 3 to measure the input current and set to at least 1-second aperture time.

5.3.2 Output Connections

- Connect electronic loads to VOUT1, VOUT2, and SGND connections as shown in Figure 3. Set the load to constant-resistance mode or constant-current mode at 0 A before applying input voltage.
- Connect voltmeters 1 and 2 at VOUT1, VOUT2, and SGND connection points to measure the output voltages.
- Connect ammeters 1 and 2 to measure the output currents.

5.4 Test Procedure

5.4.1 Line and Load Regulation, Efficiency

- Set up the EVM as described above.
- Set load to constant resistance or constant current mode and to sink 10 mA.
- Increase input source from 0 V to 24 V; use voltmeter 3 to measure the input voltage.
- Increase the current limit of the input supply to 500 mA.
- Using voltmeters to measure the respective output voltages, vary both loads from 10 mA to 200 mA DC; $V_{OUT1}$ and $V_{OUT2}$ must remain within the load regulation specification.
- Set the load currents to 100 mA (50% rated load) and vary the input source voltage from 10 V to 65 V; $V_{OUT1}$ and $V_{OUT2}$ must remain within the line regulation specification.
- Decrease loads to 10 mA. Decrease input source voltage to 0 V.
6 Test Data and Performance Curves

Figure 4 through Figure 16 present typical performance curves for the LM5180EVM-DUAL. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements.

6.1 Efficiency and Regulation

Figure 4. Conversion Efficiency (Linear Scale), Outputs Loaded Symmetrically

Figure 5. Conversion Efficiency (Log Scale), Outputs Loaded Symmetrically
Figure 6. Load Regulation (Linear Scale), Sum of $V_{OUT1}$ and $V_{OUT2}$ Measured, Outputs Loaded Symmetrically

Figure 7. Load Regulation (Log Scale), Sum of $V_{OUT1}$ and $V_{OUT2}$ Measured, Outputs Loaded Symmetrically
6.2 Operating Waveforms

6.2.1 Switching

Figure 8. SW Node Voltage, \( I_{\text{OUT1}} = -I_{\text{OUT2}} = 200 \text{ mA}, V_{\text{IN}} = 24 \text{ V} \)

Figure 9. SW Node Voltage, \( I_{\text{OUT1}} = -I_{\text{OUT2}} = 200 \text{ mA}, V_{\text{IN}} = 48 \text{ V} \)
Figure 10. Flyback Diode Voltages, $I_{OUT1} = -I_{OUT2} = 200$ mA, $V_{IN} = 24$ V

Figure 11. Flyback Diode Voltages, $I_{OUT1} = -I_{OUT2} = 200$ mA, $V_{IN} = 48$ V
6.2.2 Load Transient Response

Figure 12. Output 1 Load Transient, 50 mA to 200 mA at 100 mA/µs, $I_{OUT2} = -200$ mA, $V_{IN} = 24$ V

Figure 13. Output 2 Load Transient, 50 mA to 200 mA at 100 mA/µs, $I_{OUT1} = 200$ mA, $V_{IN} = 24$ V
6.2.3 Start-Up, Enable, and Short Circuit Recovery

(1) The internal soft-start timer is applicable here as the SS cap was not installed during these startup tests.

Figure 14. Start-Up, $V_{IN} = 24$ V, $I_{OUT1} = -I_{OUT2} = 200$ mA Resistive

Figure 15. Enable On, $V_{IN} = 24$ V, $I_{OUT1} = -I_{OUT2} = 200$ mA Resistive
Figure 16. Short Circuit Recovery, $V_{IN} = 24$ V, $I_{OUT1} = -I_{OUT2} = 200$ mA Resistive
7 EVM Documentation

7.1 Schematic

Figure 17. EVM Schematic
## 7.2 Bill of Materials

<table>
<thead>
<tr>
<th>COUNT</th>
<th>REF DES</th>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>MFR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1</td>
<td>Capacitor, Ceramic, 22 pF, 250 V, X7R, 0603</td>
<td>Std</td>
<td>Std</td>
</tr>
<tr>
<td>2</td>
<td>C2, C3</td>
<td>Capacitor, Ceramic, 10 µF, 25 V, X7R, 1206</td>
<td>GRM32ER6J107ME20</td>
<td>Murata</td>
</tr>
<tr>
<td>1</td>
<td>C6</td>
<td>Aluminum Electrolytic, 10 µF, 100 V, ±20%</td>
<td>865060845002</td>
<td>Würth Elektronik</td>
</tr>
<tr>
<td>1</td>
<td>C6</td>
<td>Aluminum Electrolytic, 33 µF, 100 V, ±20%, AEC-Q200 grade 2</td>
<td>EEE-FK2A330P</td>
<td>Panasonic</td>
</tr>
<tr>
<td>2</td>
<td>C7, C8</td>
<td>Capacitor, Ceramic, 4.7 µF, 100 V, X7S, 1210</td>
<td>C3225X7S475M200AB</td>
<td>TDK</td>
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<td>CMD4448</td>
<td>Central Semi</td>
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<td>Coilcraft</td>
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<td>LM5180QNGURQ1</td>
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<td>Test point for EN, SW, SS/BIAS, GND</td>
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7.3 PCB Layout

Figure 18 through Figure 21 show the design of the LM5180 2-layer PCB with 1-oz copper thickness. The EVM is a two-sided design with post connections for VIN+, VIN–, VOUT1+, VOUT2+, and SGND.

Figure 18. Top Copper (Top View)

Figure 19. Bottom Copper (Top View)
7.4 Assembly Drawings

Figure 20. Top Assembly

Figure 21. Bottom Assembly
7.4.1 PCB Layout Tips

Figure 22. Layout Design Tips for a Dual-output PSR Flyback Converter
8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support
For development support, see the following:

• For TI's reference design library, visit TI Designs
• For TI's WEBENCH Design Environments, visit the WEBENCH® Design Center
• LM5180 PSR Flyback Converter Quickstart Calculator and PSPICE simulation model

8.2 Documentation Support

8.2.1 Related Documentation
For related documentation, see the following:

• LM5180EVM-S05 EVM User’s Guide (SNVU592)
• LM25184EVM-S12 EVM User’s Guide (SNVU680)
• IC Package Features Lead to Higher Reliability in Demanding Automotive and Communications Equipment Systems (SNVA804)
• PSR Flyback Transformer Design for mHEV Applications (SNVA805)
• How an Auxless PSR Flyback Converter can Increase PLC Reliability and Density (SLYT779)
• Why Use PSR-Flyback Isolated Converters in Dual-Battery mHEV Systems (SLYT791)
• TI Designs:
  – Isolated IGBT Gate-Drive Power Supply Reference Design With Integrated Switch PSR Flyback Controller
  – Compact, Efficient, 24-V Input Auxiliary Power Supply Reference Design for Servo Drives
  – Reference Design for Power-Isolated Ultra-Compact Analog Output Module
  – HEV/EV Traction Inverter Power Stage with 3 Types of IGBT/SiC Bias-Supply Solutions Reference Design
  – 4.5-V to 65-V Input, Compact Bias Supply With Power Stage Reference Design for IGBT/SiC Gate Drivers
  – Channel-to-Channel Isolated Analog Input Module Reference Design
  – SiC/IGBT Isolated Gate Driver Reference Design With Thermal Diode and Sensing FET
  – >95% Efficiency, 1-kW Analog Control AC/DC Reference Design for 5G Telecom Rectifier
  – 3.5-W Automotive Dual-output PSR Flyback Regulator Reference Design
• TI Technical Articles:
  – Flyback Converters: Two Outputs are Better Than One
  – Common Challenges When Choosing the Auxiliary Power Supply for Your Server PSU
  – Maximizing PoE PD Efficiency on a Budget
• White Papers:
  – Valuing Wide \( V_{\text{in}} \) Low EMI Synchronous Buck Circuits for Cost-driven, Demanding Applications (SLYY104)
  – An Overview of Conducted EMI Specifications for Power Supplies (SLYY136)
  – An Overview of Radiated EMI Specifications for Power Supplies (SLYY142)
• Under the Hood of Flyback SMPS Designs (SLUP261)
• Flyback Transformer Design Considerations for Efficiency and EMI (SLUP338)
8.2.1.1 PCB Layout Resources

- AN-1149 Layout Guidelines for Switching Power Supplies (SNVA021)
- AN-1229 Simple Switcher PCB Layout Guidelines (SNVA054)
- Constructing Your Power Supply – Layout Considerations (SLUP230)
- Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x (SNVA721)
- TI Technical Articles:
  - High-Density PCB Layout of DC-DC Converters

8.2.1.2 Thermal Design Resources

- AN-2020 Thermal Design by Insight, Not Hindsight (SNVA419)
- AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages (SNVA183)
- Semiconductor and IC Package Thermal Metrics (SPRA953)
- Thermal Design Made Simple with LM43603 and LM43602 (SNVA719)
- PowerPAD Thermally Enhanced Package (SLMA002)
- PowerPAD Made Easy (SLMA004)
- Using New Thermal Metrics (SBVA025)
## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<table>
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<tr>
<th>Changes from A Revision (April 2019) to B Revision</th>
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<tr>
<td>• Added family of PSR flyback converters in <em>Table 1</em></td>
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<tr>
<td>• Updated <em>Section 1.1</em></td>
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<tr>
<td>• Added PCB layout tips in <em>Section 7.4</em></td>
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<tr>
<td>• Updated list of collateral in <em>Section 8</em></td>
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<tr>
<th>Changes from Original (October 2018) to A Revision</th>
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<tr>
<td>• Changed soft-start time, $t_{SS}$ from &quot;4 ms&quot; to &quot;8 ms&quot;</td>
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<td>• Changed part number for T1 (Würth Electronik) from &quot;TBD&quot; to &quot;750317595&quot;</td>
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