User's Guide
SNVU675–May 2019

Power Supply Design for Renesas R-Car M3 Using LP87565-Q1 and LP8732-Q1

This document details the design considerations of a power solution for the Renesas R-Car M3x SoC (system-on-chip) power rails using the LP87565-Q1 and LP8732-Q1 power management ICs. Additional TLV733P-Q1 LDOs are used for the peripheral rails. This power solution assumes an input voltage of 5 V (+/-5%). If the system input voltage is higher, for example a car battery, a buck converter as a pre-regulator should be used to generate a supply voltage of 5 V.

The LP87565-Q1 has four buck converters configured to work as dual 2-phase converters. LP8732-Q1 has two 2 A buck converters and two 300 mA LDOs. These devices are OTP programmable, meaning default register values are set in TI production line to desired values and it is also possible to control registers through I^2C after power-up. Contact TI sales for samples with specific OTP settings. I^2C configurable samples are available with part numbers LP875650RNFTQ1 and LP873200RHDRQ1. See the *LP8756x-Q1 Configuration Guide* and *LP8733-Q1 and LP8732-Q1 Configuration Guide* for details how to use these I^2C configurable devices.

This power solution is an example how R-Car M3x required rails can be powered with TI PMICs. Sequencing is handled through programmable startup/shutdown delays of the PMICs and GPIOs and it only requires a single Enable signal from the system to initiate the sequencing. This power solution is possible to customize and optimize based on the actual use case regarding SoC variant, current requirements, used peripherals, and so forth.

This solution supports DVFS for core rail through I^2C bus and also DDR backup feature (I^2C configurable).

1 Design Parameters

Table 1 shows the power rails, load requirements, and startup/shutdown sequencing requirements and Section 7 shows typical measurement data.

Table 1. Design Parameters

VOLTAGE (V)	RAIL NAME	MAX LOAD (mA)	SOURCE	STARTUP DELAY (ms)	SHUTDOWN DELAY (ms)
1.82	DDR0_1.8V	300	#1 LP8732 LDO0	5	15
	DDR1_1.8V	300	#1 LP8732 LDO1	5	15
1.1	VDDQVA_DDR0	2000	#1 LP8732 Buck0	11	9
	VDDQVA_DDR1	2000	#1 LP8732 Buck1	11	9
1.8	VDDQ18	500	#2 LP8732 Buck0	10	10
	VDDIO_1V8	30	#1 TLV733P-Q1	2	18
	VDDQVA_SD1	35	#2 TLV733P-Q1	12	8
	VDDQVA_SD2	35	#3 TLV733P-Q1	12	8
	VDDQVA_SD3	35	#4 TLV733P-Q1	12	8
3.3	VDDQVA_SD0	35	#2 LP8732 LDO0	12	8
	VDDQ33	1200	#2 LP8732 Buck1	9	11
	VDDIO_3V3	30	#5 TLV733P-Q1	2	18
0.9	VDD_DVFS	8000	LP87565 Buck0+1	8	12
0.82	VDD	8000	LP87565 Buck2+3	6	14
2.5	VDDQ25_ETH	40	#2 LP8732 LDO1	10	10
-	nRESET (PGOOD)	-	PGOOD / GPIO	22	0

2 Power Solution

Figure 1 shows an example block diagram of LP87565x-Q1, 2 pcs LP8732x-Q1, and 5 pcs TLV733P-Q1 devices powering the R-Car M3-W power rails.

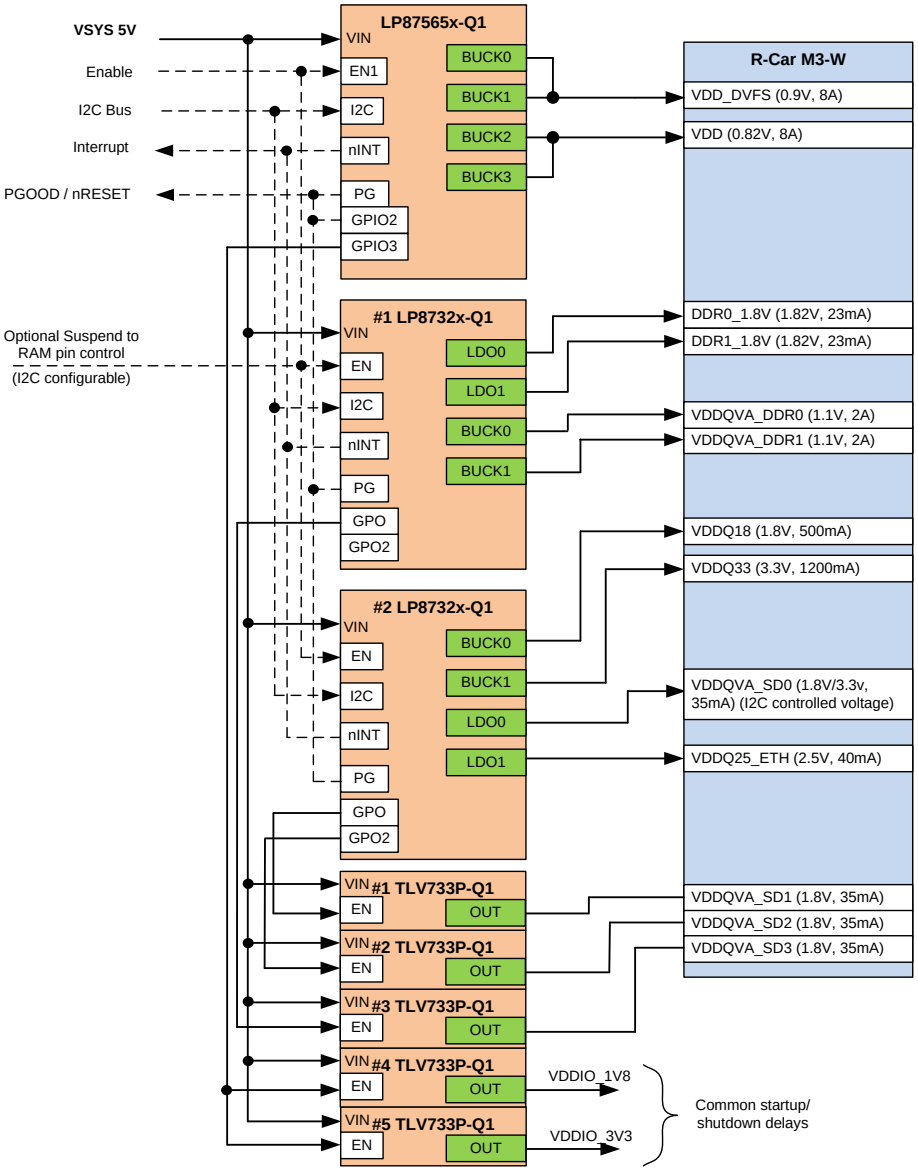

Figure 1. R-Car M3W Power Solution Block Diagram

Main features:

- After the devices are powered, the microcontroller can set the EN pin high to initiate the startup sequence.
- Startup delays are controlled internally in the LP87565-Q1 and LP8732-Q1 logic and TLV733P-Q1s are controlled with PMIC GPIOs.
- I^2C can be used to read status registers and reset interrupts.
- All PMIC devices have dedicated I^2C slave address so they can share the same I^2C bus. Note: If you are using generic I^2C configurable PMICs, the LP873200RHDRQ1 would have to be used with pin-to-pin compatible LP873300RHDRQ1 to achieve unique slave ID.
- PGOOD signals act as nRESET signal for the SoC and LP87565-Q1 GPIO2 keeps the signal low at startup for predefined time.

- Voltage control (1.8 V / 3.3 V) VDDQVA_SD0 rail done through I²C bus
- DDR backup functionality through I²C control. Core rail (VDD_DVFS) DVFS support through I²C

3 Sequencing

3.1 Startup

Figure 2 shows an example startup timing of the power rails and corresponding signals.

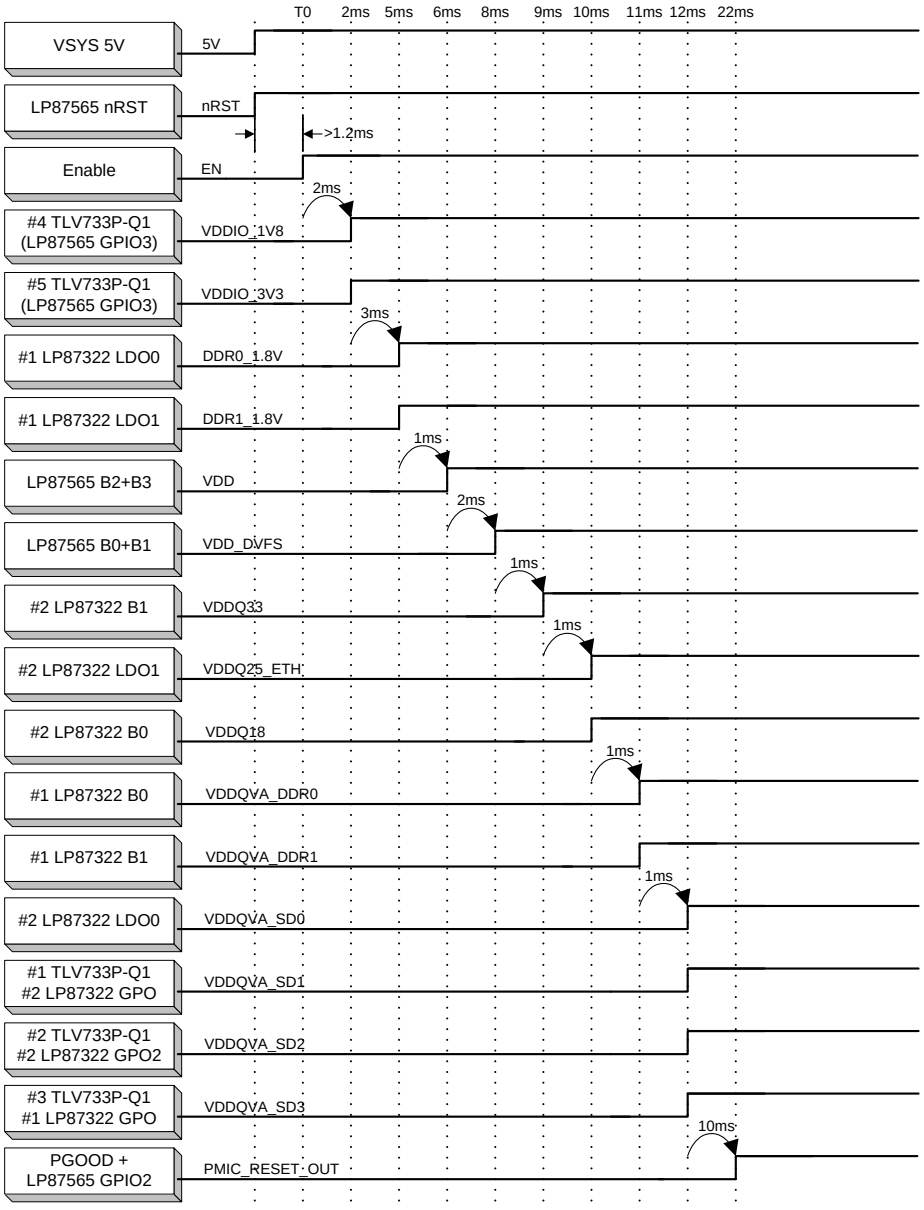

Figure 2. R-Car M3-W Power Startup Timing Diagram

3.2 Shutdown

Figure 3 shows an example of shutdown timing of the power rails and corresponding signals.

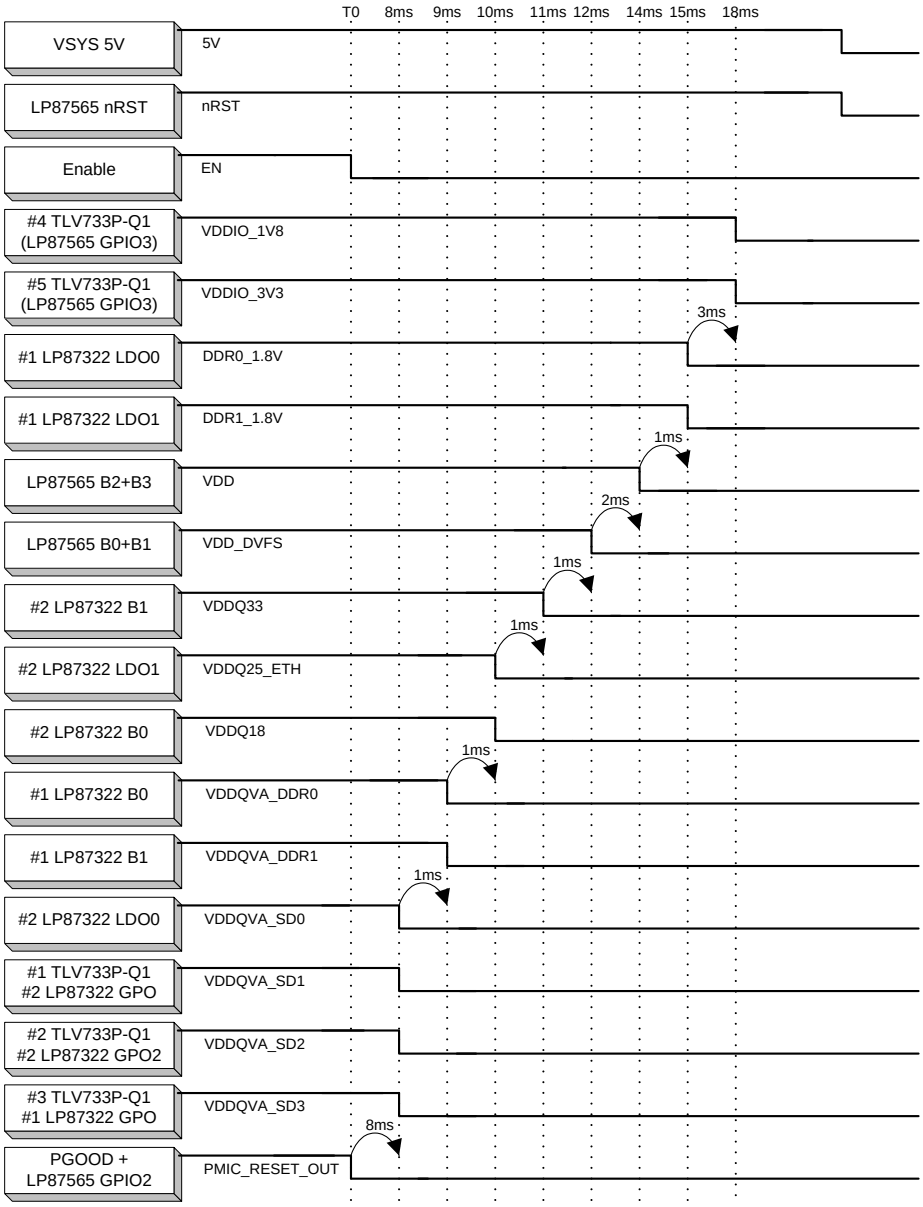

Figure 3. Shutdown Timing Diagram

4 Schematic

Figure 4 through Figure 8 show the R-Car M3-W power tree schematic with critical components. Snubbers are needed for LP87565-Q1 when input voltage of the system is >4 V, otherwise they are optional.

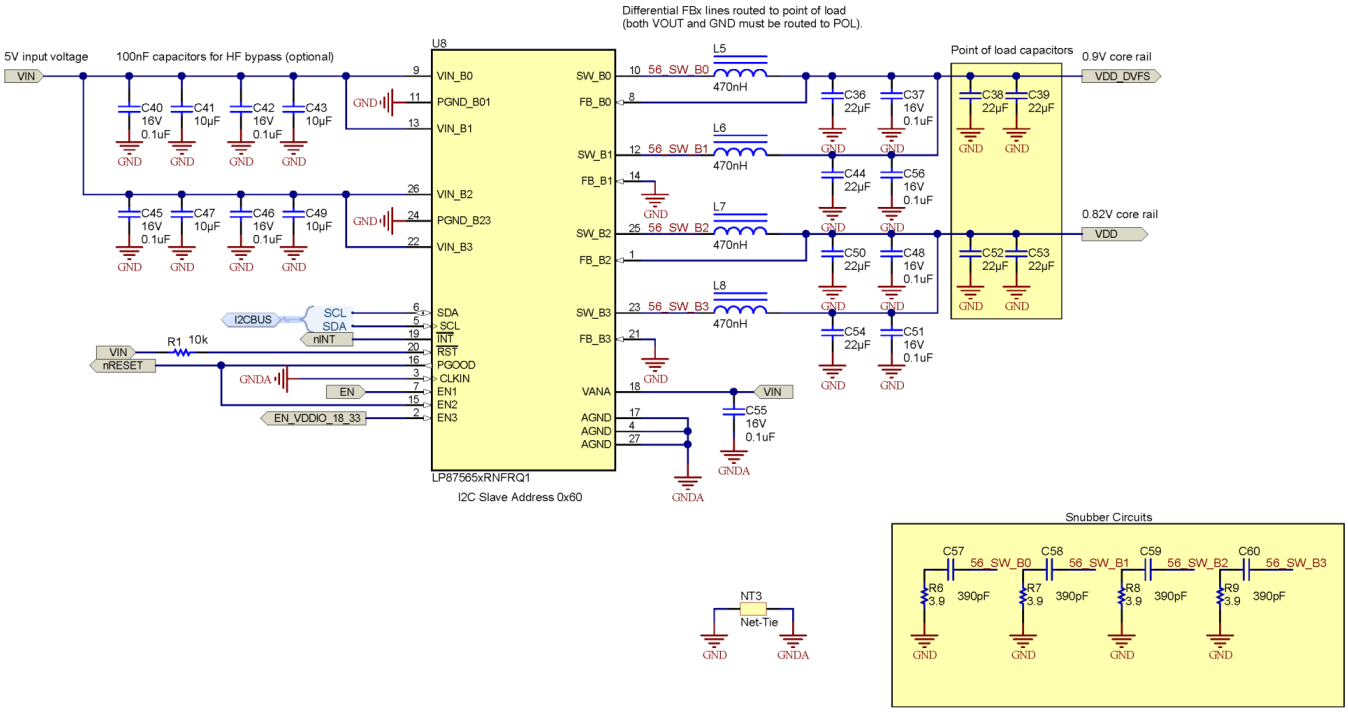

Figure 4. LP87565x Schematic

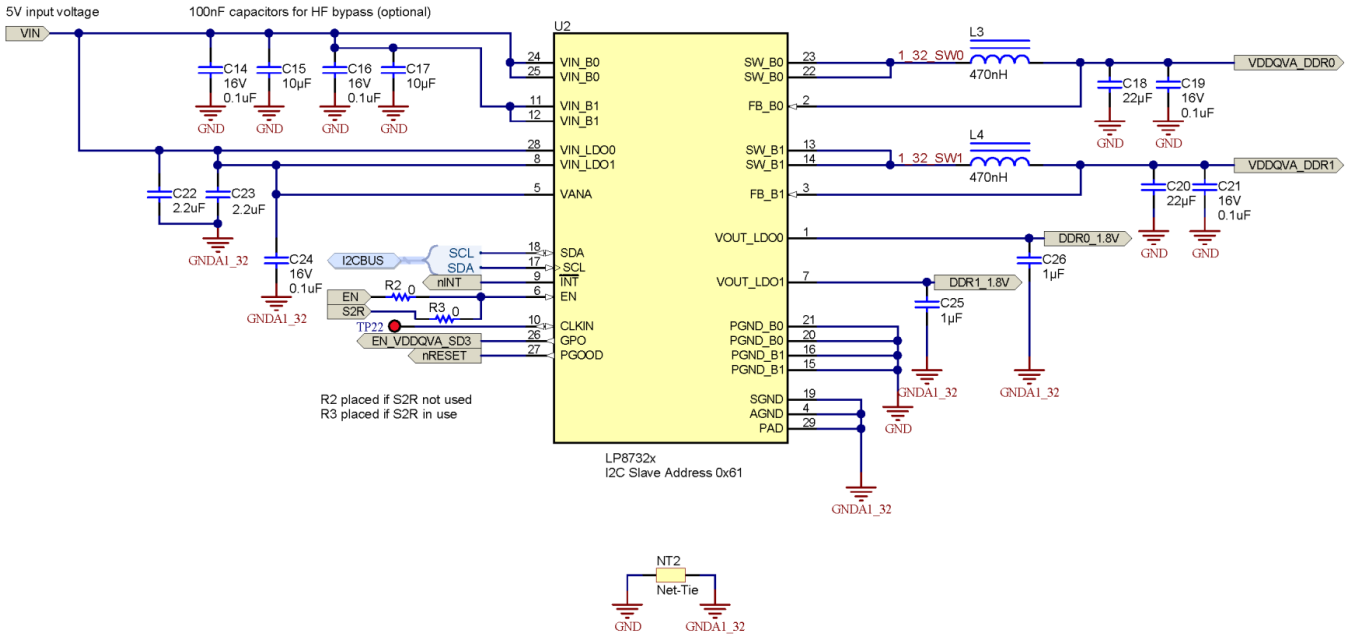

Figure 5. LP8732x-1 Schematic

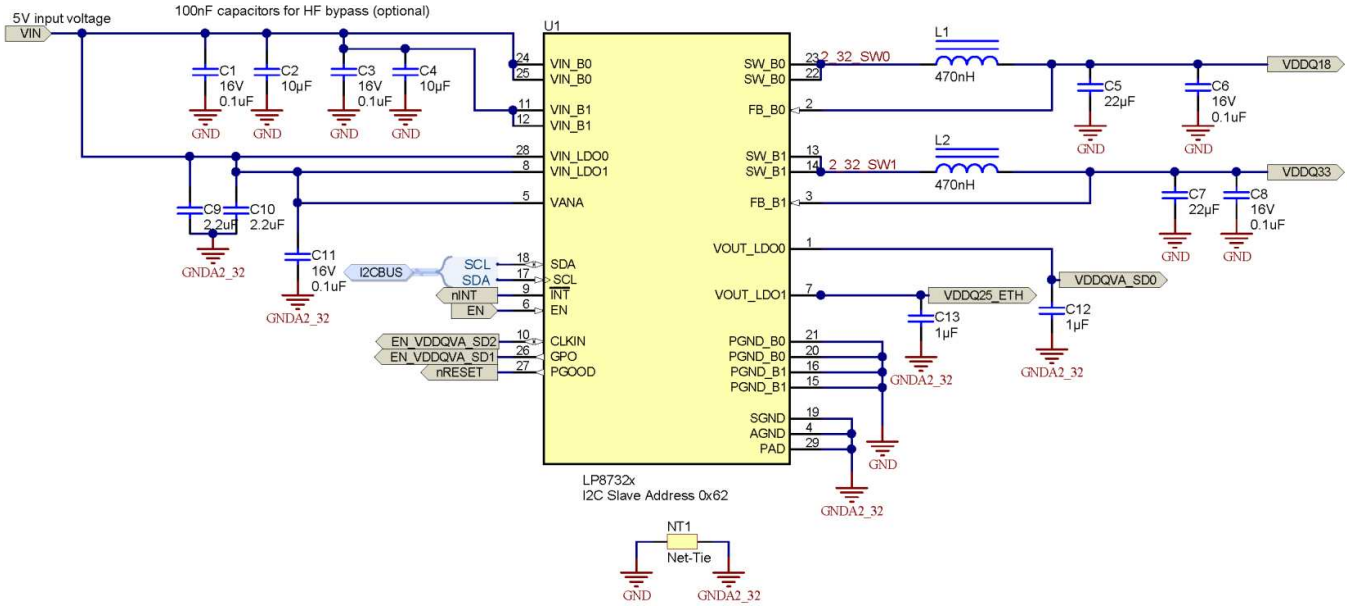

Figure 6. LP8732x-2 Schematic

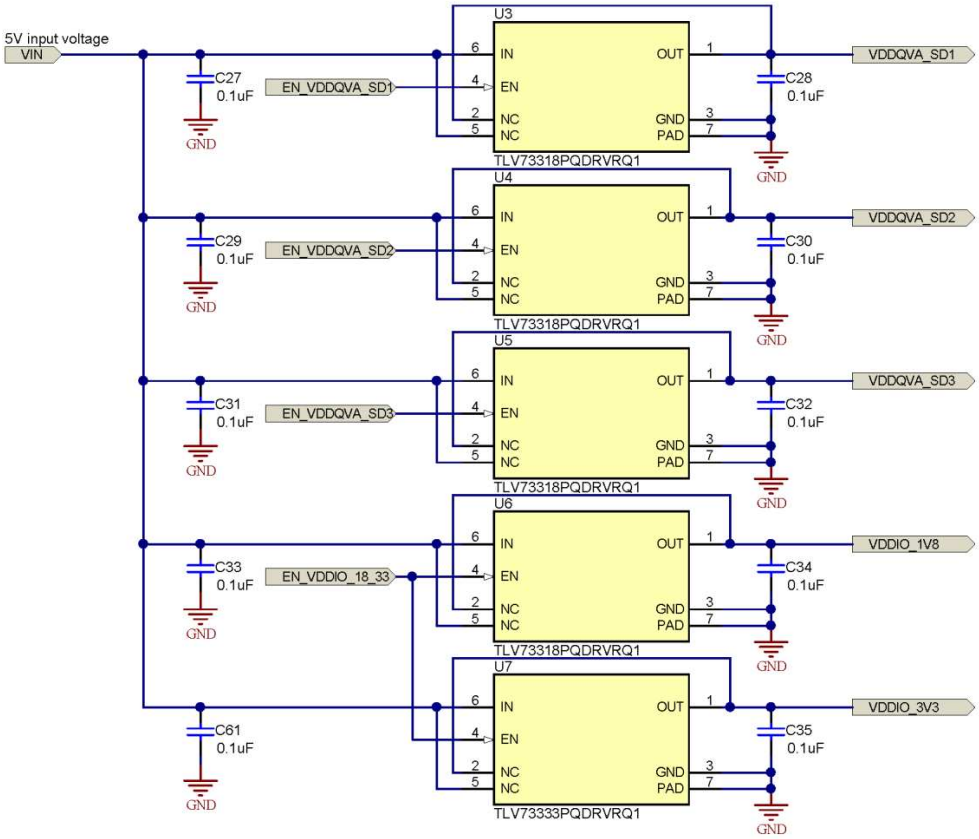

Figure 7. TLV733P-Q1LDO Schematic

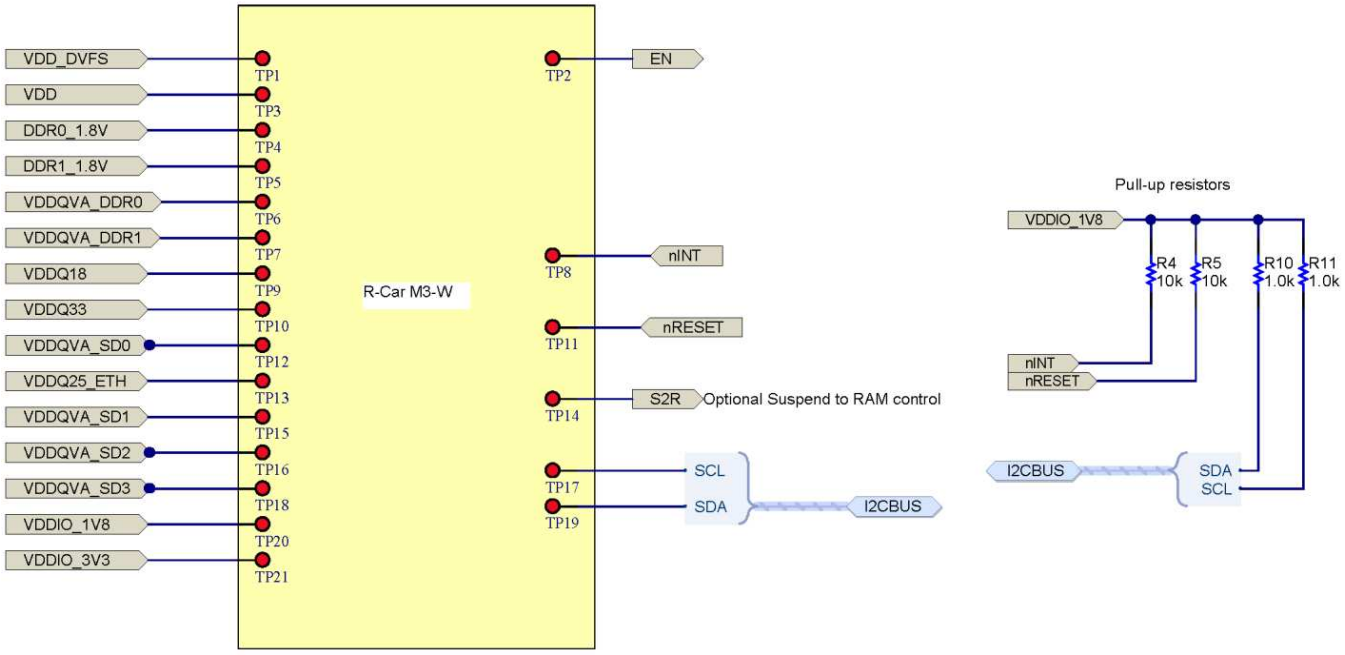

Figure 8. Connections to R-Car M3-W

5 Software Drivers

This solution supports DVFS for core rail through I^2C bus and also DDR backup feature (I^2C configurable).

Linux drivers for the LP875x and LP873x are available in public git repository. These can be used to help integrate the LP875x / LP873x control to system software:

LP8756x

- https://github.com/torvalds/linux/blob/master/drivers/mfd/lp87565.c
- https://github.com/torvalds/linux/blob/master/drivers/regulator/lp87565-regulator.c
- https://github.com/torvalds/linux/blob/master/drivers/gpio/gpio-lp87565.c

LP873x

- https://github.com/torvalds/linux/blob/master/drivers/mfd/lp873x.c
- https://github.com/torvalds/linux/blob/master/drivers/regulator/lp873x-regulator.c
- https://github.com/torvalds/linux/blob/master/drivers/gpio/gpio-lp873x.c

Note: Every header file is in the “include” folder starting from the root directory. So once in “include folder”, you can navigate to the relevant header file. For example, here is the LP87565.h file: https://github.com/torvalds/linux/blob/master/include/linux/mfd/lp87565.h.

6 Recommended External Components

Table 2 shows the recommended external components to use in this solution with the LP87565-Q1, LP8732-Q1, and TLV-733P-Q1s. It also shows the total solution size, including the PMIC device and the external components.

Table 2. Bill of Materials

COUNT	VENDOR	PART NUMBER	SYSTEM COMPONENT	W (mm)	L (mm)	H (mm)	UNIT AREA (1)	TOTAL BOARD AREA (1)
1	TI	LP87565x-Q1	Configurable 4-phase PMIC	4.00	4.50	0.90	27.50	27.50
4	Murata	DFE252012PD-R47M	LP87565x Inductor 0.47 µH, Imax 4.0 A, Rdc typ 21mΩ	2.50	2.00	1.20	10.50	42.00
4	Murata	GCM21BR71A106KE22	LP87565x SMPS Input Capacitor 10 µF, 10 V, 10%	2.00	1.25	1.25	6.75	27.00
4	Murata	GCM31CR71A226KE02	LP87565x SMPS Output Capacitor 22 µF, 10 V, 10%	3.20	1.60	1.80	10.92	43.68
13	Murata	GRT31CC80J476KE13	Point of load Capacitor 47 µF, 6.3 V, 10%.	3.20	1.60	1.60	10.92	141.96
1	Murata	GCM155R71C104KA55D	LP87565x Input Capacitor 0.1 µF, 16 V, 10%	1.00	0.50	0.50	3.00	3.00
4	TDK	CGA2B2C0G1H391J050BA	LP87565x Snubber capacitor, 390 pF	1.00	0.50	0.50	3.00	12.00
4	Vishay-Dale	CRCW04023R90JNED	LP87565x Snubber resistor, 3R9	1.00	0.50	0.50	3.00	12.00
2	TI	LP8732x-Q1	Configurable PMIC with 2 Bucks and 2 LDOs	5.00	5.00	0.90	36.00	72.00
4	Murata	DFE252012PD-R47M	LP87322x Inductor 0.47 µH, Imax 4.0 A, Rdc typ 21mΩ	2.50	2.00	1.20	10.50	42.00
4	Murata	GCM21BR71A106KE22	LP87322x SMPS Input Capacitor 10 µF, 10 V, 10%	2.00	1.25	1.25	6.75	27.00
4	Murata	GCM31CR71A226KE02	LP87322x SMPS Output Capacitor 22 µF, 10 V, 10%	3.20	1.60	1.60	10.92	43.68
4	Murata	GCM188R70J225KE22	LP87322x LDO Input Capacitor 2.2 µF, 6.3 V, 10%	1.60	0.80	0.90	4.68	18.72
4	Murata	GCM188R71C105KA64	LP87322x LDO Output Capacitor 1.0 µF, 16 V, 10%	1.60	0.80	0.90	4.68	18.72
1	Murata	GCM155R71C104KA55D	LP87322x Input Capacitor 0.1 µF, 16 V, 10%	1.00	0.50	0.50	3.00	3.00
4	TI	TLV733P-Q1	TLV733P-Q1 Low Dropout Regulator	2.00	2.00	0.80	9.00	45.00
4	Murata	GCM155R71C104KA55D	TLV733P-Q1 Input Capacitor 0.1 µF, 16 V, 10%	1.00	0.50	0.50	3.00	15.00
4	Murata	GCM155R71C104KA55D	TLV733P-Q1 Output Capacitor 0.1 µF, 16 V, 10%	1.00	0.50	0.50	3.00	15.00
							TOTAL	609.26 mm^2
							Routing area calculated with 0.3 routing factor	261.11 mm^2
							Total area	870.37 mm^2

(1) Assuming 1 mm keep-out around each component, and multiplying by component count

7 Measurements

Test data can be found in the Application Curves section of the *LP8756x-Q1 16A Buck Converter With Integrated Switches Data Sheet* and the *LP8732xx-Q1 Dual High-Current Buck Converter and Dual Linear Regulator Data Sheet*.

Additional bench test data for efficiency in specific conditions for this power tree can be seen in this section.

Measurements were taken on the LP87565Q1EVM and LP8732Q1EVM with default components.

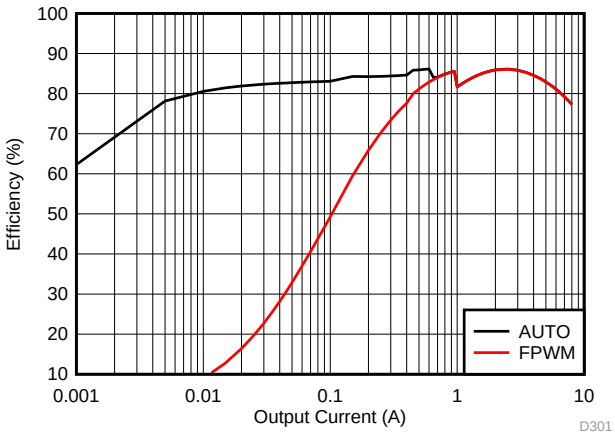

Figure 9. LP87565-Q1 Efficiency with Vin = 5 V, 25°C, Vout = 0.85 V

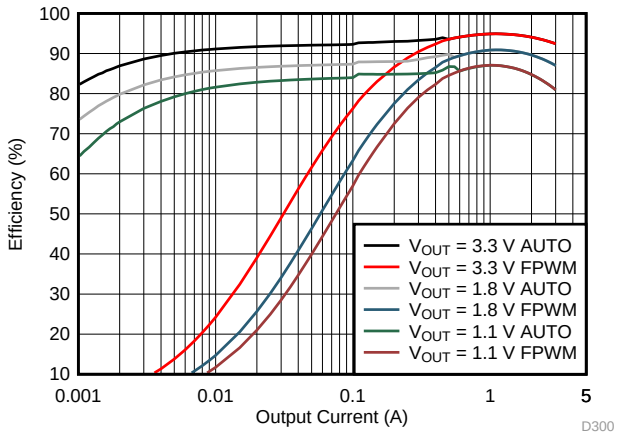

Figure 10. LP8732-Q1 Efficiency with Vin = 5 V, 25°C

8 Conclusion

With this presented solution with the LP87565-Q1 and LP8732-Q1 PMICs, it is possible to meet power requirements for R-Car M3 application processor while maintaining good efficiency. Sequencing is handled in PMICs and only one EN signal is needed from the controller. Solution is compact due to minimum number of external components. I^2C control allows DVFS for core rail and DDR Backup features.

9 References

See these references for additional information:

1. Texas Instruments, *LP8756x-Q1 16A Buck Converter With Integrated Switches Data Sheet* (SNVSB22)
2. Texas Instruments, *LP8732xx-Q1 Dual High-Current Buck Converter and Dual Linear Regulator Data Sheet* (SNVSB63)
3. Texas Instruments, *LP8756x-Q1 Configuration Guide* (SNVU590)
4. Texas Instruments, *LP8733-Q1 and LP8732-Q1 Configuration Guide* (SNVU582)

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