Power Supply Design for xWR Radar Using LP87702K-Q1

This document details the design considerations of a power solution for the AWR and IWR radar applications using LP87702K-Q1 power management integrated circuit. Supported radar devices include automotive AWR1443, AWR1642, AWR1843, and AWR6843 sensors as well as industrial IWR1443, IWR1642, IWR1843, and IWR6843 sensors. The main benefit of this design is that it does not require LDOs, which improves the overall efficiency of the system; hence, the lack of LDOs improves the thermal performance while meeting the xWR noise performance with a low cost LC filter. This power solution assumes an input voltage from 3 to 36 V which is converted to 3.3 V with LM61460-Q1.

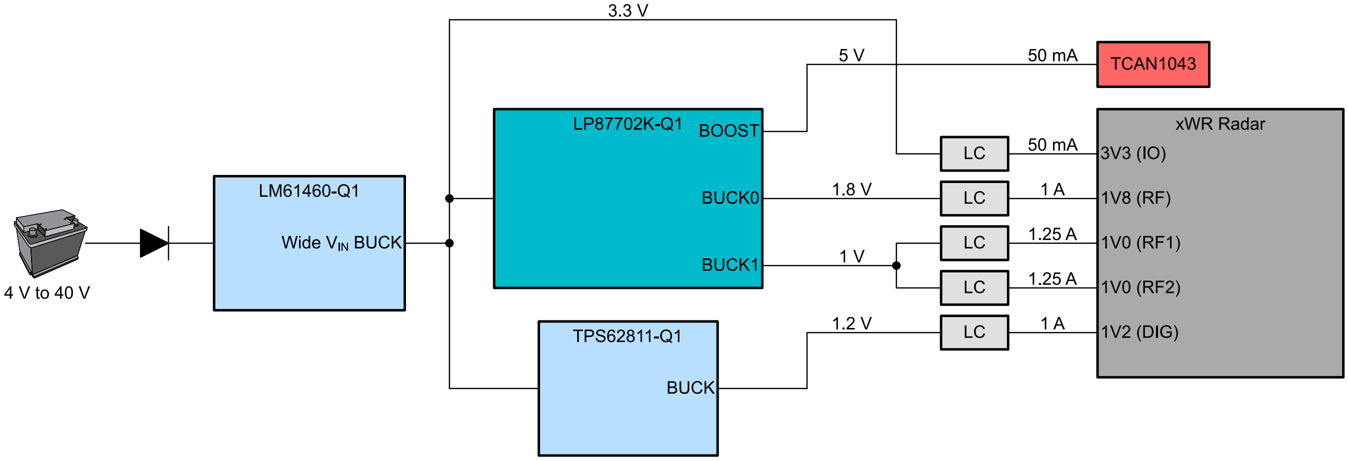

Figure 1. High Level Block Diagram

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1 Introduction

The LP87702K-Q1 has two individual buck converters and one boost converter. The LP87702K-Q1 is OTP programmable, meaning default register values are set in the TI production line to the desired values and it is also possible to control the registers through the I^2C after power-up. See the *LP877020-Q1 Configuration Guide* for details on how to use and configure LP87702K-Q1 through the I^2C. The main OTP settings for power rails are listed in Table 1.

Table 1. Main OTP Settings for Power Rails

Group	Description	Bit Name	LP87702K-Q1
Device Identification	OTP configuration	OTP_ID	23h
	Revision for OTP_ID	OTP_REV	0
BUCK0	Output voltage	BUCK0_VSET	1.8 V
	Enable, EN-pin or I^2C register	BUCK0_EN_PIN_CTRL, BUCK0_EN	EN1
	Force PWM	BUCK0_FPWM	Yes
	Peak current limit	BUCK0_ILIM	4 A
	Maximum load current	N/A	3 A
BUCK1	Output voltage	BUCK1_VSET	1.01 V
	Enable, EN-pin or I^2C register	BUCK1_EN_PIN_CTRL, BUCK1_EN	EN1
	Force PWM	BUCK1_FPWM	Yes
	Peak current limit	BUCK1_ILIM	4.5 A
	Maximum load current	N/A	3.5 A
BOOST	Mode, boost, or bypass	N/A	Boost
	Output voltage	BOOST_VSET	5 V
	Enable, EN-pin, or I^2C register	BOOST_EN_PIN_CTRL, BOOST_EN	EN1
	Peak current limit	BOOST_ILIM	1.4 A
	Maximum load current	N/A	0.6 A
VANA	VANA over-voltage threshold	N/A	4.3 V rising

The full list of register bits loaded from the OTP memory are shown in *LP87702-Q1 Technical Reference Manual*.

2 xWR Power Supply Requirements

The power supply design challenges for TI radar processors are described below, and the TI radar processors are addressed in this design.

1. 1.0 V/1.3 V RF and 1.8 V RF rails have very tight ripple specifications in (µV range) and it is very challenging to meet such a low ripple specifications for switching regulators.
2. Traditionally, LDO's are used on RF rails, but LDO solution suffers from poor thermal performance and it increases cost.

3. A low cost LC filter is used between switching regulators and AWR supply rails to filter the ripple. An LC filter should be carefully selected as a large inductance will cause load transient settling or ringing issues and also an increased voltage drop across them. A smaller inductance won't provide enough filtering performance.
4. All the power rails should be within ±5 % (except 1.2 V with -5% and +10% requirement) of nominal voltage level and increased ringing will result in violation of specification.
5. All the ringing should ideally settle very quickly (before ADC start-time) to avoid spurs related to power supply settling noise.
6. Higher regulator switching frequency helps to reduce the LC filter size and also increases regulator bandwidth to minimize the undershoot or overshoot during the load transient. All TI radar PMICs supplying the RF rails use 4 MHz or higher switching frequency.
7. LC filter is placed outside the switching regulator regulation loop. L (ferrite bead) is placed close to the regulator output and C of this LC filter includes the decoupling capacitors of the AWR supply pins.
8. The PCB size is very limited and hence it is necessary to have a very small power management solution size in case of USRR, SRR, and some MRR applications.
9. Increased board temperature will affect the AWR RF performance and hence it is necessary to reduce the effect of the board temperature rise due to the PMIC and regulators heating. Also some of the radar applications have plastic housing and thermal management becomes very critical.
10. System level safety requirements for radar sensors are increasing and hence it is necessary to have PMICs which meet system level safety goals (ASIL-B or ASIL-C at PMIC level).

2.1 Recommended Supply Voltage Requirements

Table 2 provides the recommended supply voltage range specifications for different AWR1843 supply rails. The external supply voltage on this pin should be 1.3 V in case the application uses an internal LDO on a 1.0 V or 1.3 V RF rail. If an internal LDO is not used or bypassed, then an external supply voltage on this pin should be 1.0 V. Often an internal LDO is not used as it increases the AWR internal power dissipation. A special power supply sequencing is not needed, but all the input supply rails should be settled before releasing the reset/power good signal to the AWR device. The CAN PHY may need to be controlled by both the PMIC and AWR to avoid a glitch in case the AWR IO enables the CAN PHY when the 3.3 V AWR rail is ramping but the 1.8 V rail is not active.

Table 2. AWR1843 Recommended Operating Supply

Input	Description	Minimum (V)	Nominal (V)	Maximum (V)
VDDIN	1.2 V digital power supply	1.14	1.2	1.32
VIN_SRAM	1.2 V power rail for internal SRAM	1.14	1.2	1.32
VNWA	1.2 V power rail for SRAM array back bias	1.14	1.2	1.32
VIOIN	I/O supply (3.3 V of 1.8 V). All CMOS I/Os would operate on this supply.	3.15	3.3	3.45
		1.71	1.8	1.89
VIOIN_18	1.8 V supply for CMOS I/O	1.71	1.8	1.9
VIN_18CLK	1.8 V supply for clock module	1.71	1.8	1.9
VIOIN_18IFF	1.8 V supply for LVDS port	1.71	1.8	1.9
VIN_13RF1 VIN_13RF2	1.3 V analog and RF supply. VIN_13RF1 and VIN_13RF2 could be shorted on the board.	1.23	1.3	1.36
VIN_13RF1 (1 V Internal LDO bypass mode) VIN_13RF2 (1 V Internal LDO bypass mode)		0.95	1.0	1.05
VIN18BB	1.8 V analog baseband power supply	1.71	1.8	1.9
VIN_18VCO	1.8 V RF VCO supply	1.71	1.8	1.9

2.2 Input Supply Current Requirements

Table 3 provides the peak supply current specifications and Table 4 provides the average power numbers. The typical supply currents and the average power depends on the application software and chirp configuration.

Table 3. AWR1843 Peak Current Specification

Supply name	Description	Maximum (mA)
VDDIN, VIN_SRAM, VNWA	Total current drawn by all nodes driven by 1.2 V rail.	1000
VIN_13RF1, VIN_13RF2	Total current drawn by all nodes driven by 1.3 V or 1.0 V rail (2 TX, 4 RX simultaneously).(1)	2000
VIOIN_18, VIN_18CLK, VIOIN_18DIFF, VIN_18BB, VIN_18VCO	Total current drawn by all nodes driven by 1.8 V rail.	850
VIOIN	Total current drawn by all nodes driven by 3.3 V rail.	50

(1) 3 Transmitters can be simultaneously deployed only in AWR1243P and AWR1843 devices with 1V/ LDO bypass and PA LDO disable mode. In this mode 1 V supply needs to be fed on the VOUT PA pin. In this case the peak 1 V supply current goes up to 2500 mA.

Table 4. AWR Average Power Consumption

<table>
<tr><th colspan="3">Condition</th><th>Description</th><th>Typical (W)</th></tr>
<tr><td rowspan="4">1.0 V internal LDO bypass mode</td><td rowspan="2">25 % duty cycle</td><td>1TX, 4RX</td><td rowspan="2">Use Case: Low power mode, 3.2 MSps complex transceiver, 25 ms frame time, 128 chirps, 128 samples/chirp, 8 µs interchirp time (25 % duty cycle), and DSP active.</td><td>1.3</td></tr>
<tr><td>2TX, 4RX</td><td>1.38</td></tr>
<tr><td rowspan="2">50 % duty cycle</td><td>1TX, 4RX</td><td rowspan="2">Use Case: Low power mode, 3.2 MSps complex transceiver, 25 ms frame time, 256 chirps, 128 samples/chirp, 8 µs interchirp time (50 % duty cycle), and DSP active.</td><td>1.77</td></tr>
<tr><td>2TX, 4RX</td><td>1.92</td></tr>
<tr><td rowspan="4">1.3 V internal LDO enabled mode</td><td rowspan="2">25 % duty cycle</td><td>1TX, 4RX</td><td rowspan="2">Use Case: Low power mode, 3.2 MSps complex transceiver, 25 ms frame time, 128 chirps, 128 samples/chirp, 8 µs interchirp time (25 % duty cycle), and DSP active.</td><td>1.4</td></tr>
<tr><td>2TX, 4RX</td><td>1.48</td></tr>
<tr><td rowspan="2">50 % duty cycle</td><td>1TX, 4RX</td><td rowspan="2">Use Case: Low power mode, 3.2 MSps complex transceiver, 25 ms frame time, 256 chirps, 128 samples/chirp, 8 µs interchirp time (50 % duty cycle), and DSP active.</td><td>1.94</td></tr>
<tr><td>2TX, 4RX</td><td>2.14</td></tr>
</table>

2.3 Input Supply Ripple Requirements

1.0 V RF and 1.8 V RF rails have very tight ripple specifications as ripple noise on these two rails affect the RF performance. Ripple on 3.3 V and 1.2 V rails do not directly affect the RF performance, but system level noise coupling could affect the RF performance; hence, it is necessary to minimize the ripple on these rails as well. Switching regulators have a fundamental ripple noise at switching frequency and this needs to be reduced. Table 5 provides the AWR device ripple noise specification. This ripple specification assumes a -105 dBc target spur level. If a higher spur can be tolerated based on the system requirements, then the ripple specifications can be relaxed. There is a dB-to-dB correlation between supply ripple and spur level. For example, a 1 dB increase in supply ripple will result in 1 dB increase in spur level.

Table 5. AWR1843 Ripple Specification

Frequency (kHz)	RF Rail		VCO/IF Rail
	1.0 V (Internal LDO bypass) (µV_{RMS})	1.3 V (µV_{RMS})	1.8 V (µV_{RMS})
137.5	7	648	83
275	5	76	21
550	3	22	11
1100	2	4	6
2200	11	82	13
4200	13	93	19
6600	22	117	29

3 Power Solution

Figure 2 shows an example block diagram of LP87702K-Q1, wide V_{IN} buck converter LM61460-Q1, TPS62811-Q1, and AWR or IWR radar IC device. The block diagram also includes a TCAN1043 CAN transceiver with CAN-FD.

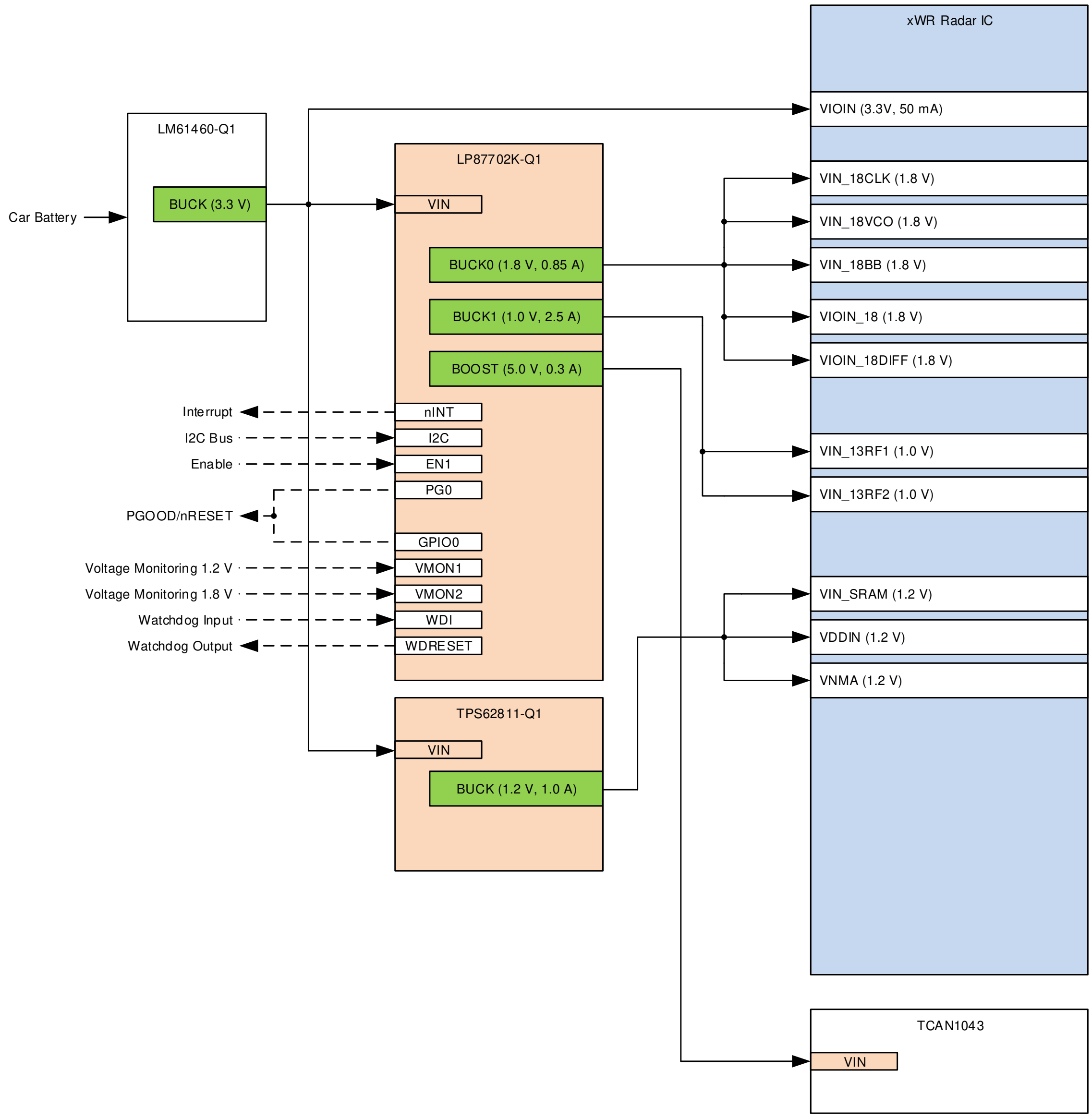

Figure 2. xWR Radar Input Power Tree Block Diagram

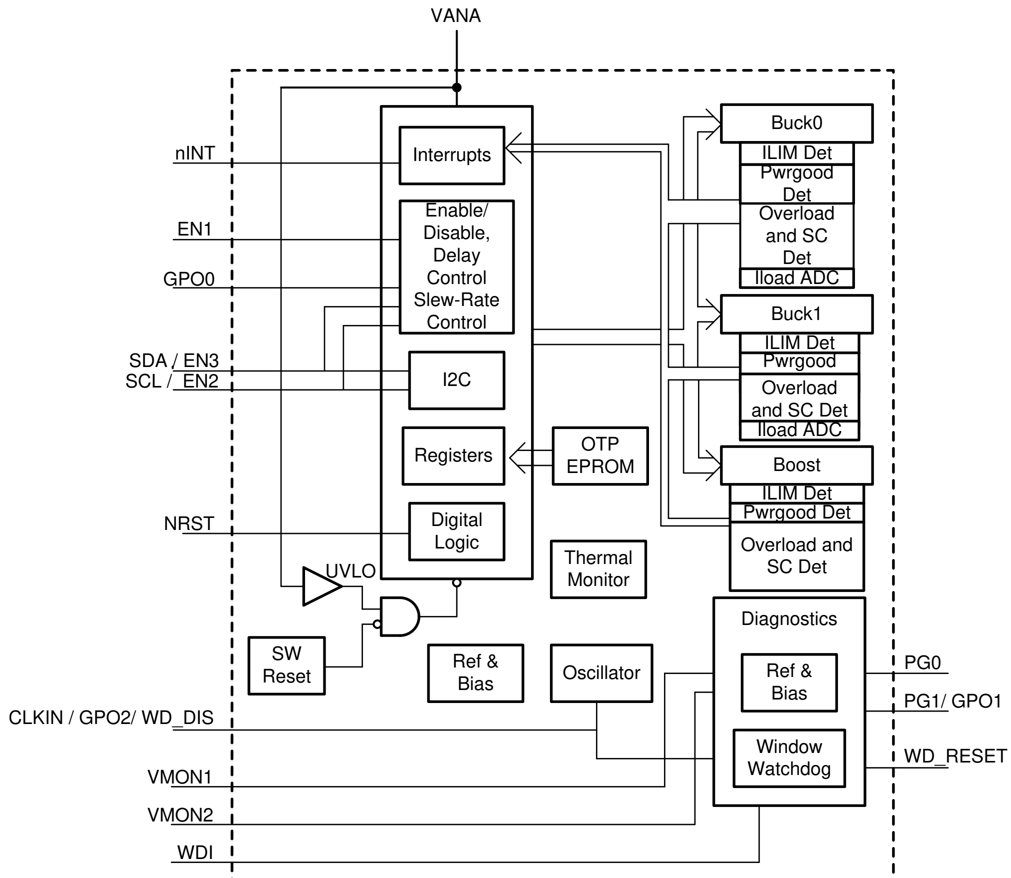

Figure 3. LP87702x-Q1 Block Diagram

Figure 3 shows the functional block diagram of LP87702-Q1.

This radar sensor reference design is intended to connect directly to the vehicle battery and therefore the wide V_{IN} controller is required. The following voltages required for the design are:

- 3.3 V for AWR1843 I/O—the LM61460-Q1 wide V_{IN} buck converter covers a wide range of input voltages and can be used with a car battery (12 V typical) for example. LM61460-Q1 generates the 3.3 V rail and the device is also used as pre-regulator supply for other low voltage DC-DC converters. The preregulator switching frequency is set with an external resistor to be at 2.1 MHz. The 3.3 V output for radar is filtered with second LC filter even though the rail does not affect RF performance. However, there is a possibility of noise coupling at system level which could affect the RF performance and therefore a ferrite bead or a small inductor is used between the switching regulator output and radar supply rails.
- 1.2 V for AWR1843 digital and SRAM—the TPS62811-Q1 generates this supply from 3.3 V input. The switching frequency for TPS62811-Q1 is controlled with COMP/FSET pin and the switching frequency is set to 2.25 MHz. Similarly as with 3.3 V rail, 1.2 V rail does not have an immediate effect on RF performance but the noise coupling could affect performance. A second LC filter is used to improve this performance.
- 1.8 V for AWR1843 analog, RF, VCO, and CMOS—the LP87702K-Q1 BUCK0 generates this supply from 3.3 V input. The output is filtered with second LC filter stage.
- 1 V for AWR1843 analog and RF—the LP87702K-Q1 BUCK1 generates this supply from 3.3 V input.
- 5 V for CAN-FD PHY—the LP87702K-Q1 BOOST converter generates this supply from 3.3 V input.

3.1 1.0 V and 1.8 V RF Rail LC Filters

The 1.0 V and 1.8 V regulators are switching at 4 MHz in forced PWM mode and the output is filtered with 470 nH inductor and 2 x 22 µF output capacitors to get good noise performance and stability. Shielded inductor with low DCR is recommended.

For the second stage filter, a 100 nH inductor such as NLCV32T-R10M-EFRD could be used. A ferrite bead could also be used to save cost and space and in this design MPZ2012S101A ferrites are used instead of inductors. The capacitance of the second LC filter includes the decoupling capacitors of the radar supply pins. Additional filter capacitor could help to improve the filtering performance and TI recommends to add a placeholder for at least one additional 22 µF capacitor after the ferrite bead to improve the noise filtering and load transient performance. Based on the performance evaluation on customer boards, if this capacitor is not needed, then it can be removed. The amount of ripple noise and load transient noise that can be tolerated depends on the application and use case. Figure 9 shows the ripple performance of LP87702k-Q1 against the AWR ripple specification with MPZ2012S101A ferrite.

Placing the LC filter (ferrite bead and one 22 µF filter capacitor after the ferrite bead) close to the regulator helps to filter the noise close to the source and this could potentially reduce the noise in the area close to the radar device on the PCB. If the LC filter is placed close to radar IC, switching regulator noise is spread in to the PCB and hence has a higher chance of coupling.

On 1.0-V rail, LC filter is split into two paths (RF1_1 and RF1_2) to decouple them from each other for improved noise performance and also reduce IR drop across the second stage inductor.

4 Measurements

Test data can be found in the Application Curves section 8.2.4 of the *LP87702-Q1 Dual Buck Converter and 5-V Boost With Diagnostic Functions* datasheet for the LP87702K-Q1. Similar data for the preregulator can be found in the section 9.2.3 Application Curves of *LM61460-Q1 Automotive 3-V to 36-V, 6-A, Low EMI Synchronous Step-Down Converter* datasheet.

Additional bench test data for LP87702K-Q1 efficiency in specific conditions for this power tree can be seen in this section. Figure 4, Figure 5, and Figure 6 show the efficiency measurement results for the LP87702K-Q1.

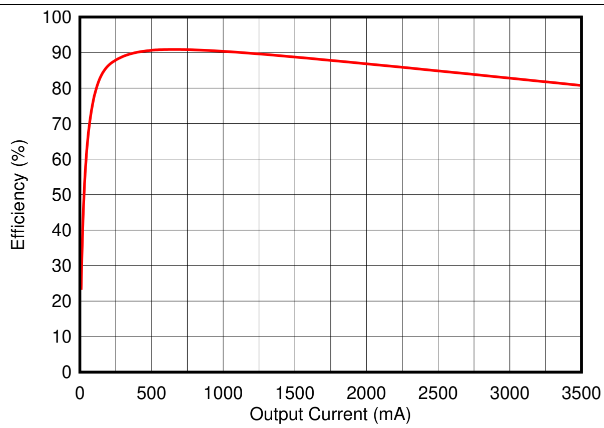

Figure 4. LP87702K-Q1 Buck Efficiency with V_{OUT} = 1.8 V, V_{IN} = 3.3 V, 25°C

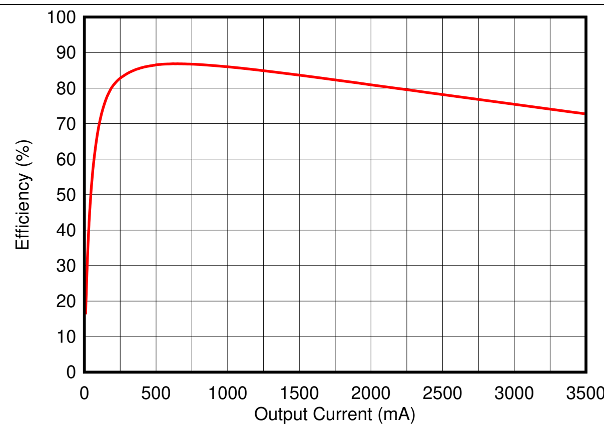

Figure 5. LP87702K-Q1 Buck Efficiency with V_{OUT} = 1.0 V, V_{IN} = 3.3 V, 25°C

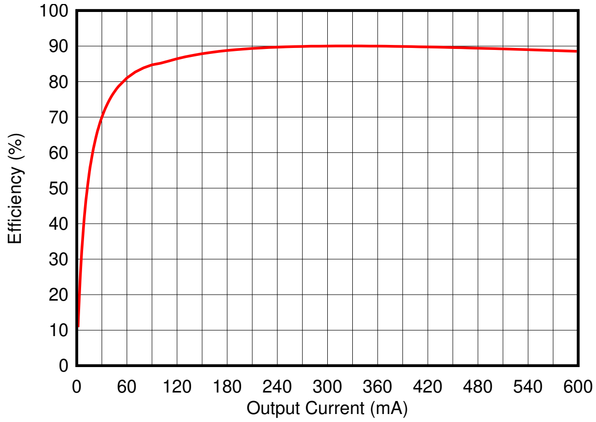

Figure 6. LP87702K-Q1 Boost Efficiency with V_{OUT} = 5.0 V, V_{IN} = 3.3 V, 25°C

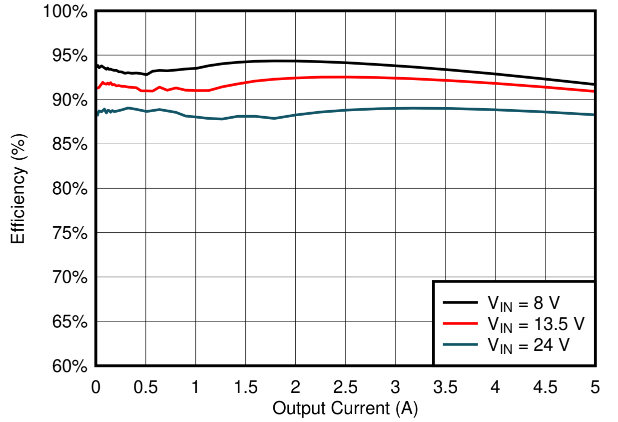

Figure 7. LM61460-Q1 Efficiency with V_{OUT} = 3.3 V, f_{sw} = 2.1 MHz, 25°C

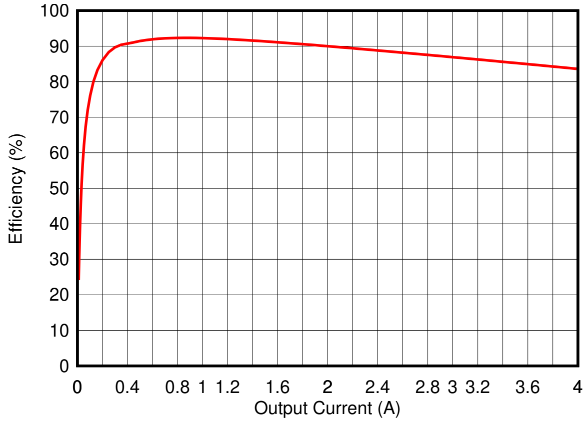

Figure 8. TPS62811-Q1 Efficiency with V_{OUT} = 1.2 V, V_{IN} = 3.3 V, f_{sw} = 2.25 MHz, 25°C

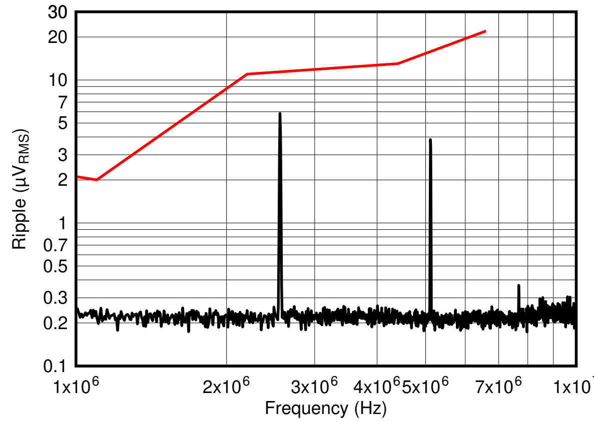

Figure 9. LP87702K-Q1 1 V Ripple Performance Against AWR Ripple Specification with MPZ2012S101A Ferrite

5 Schematic

Figure 10 shows the xWR radar power tree schematics with critical components. Notice the capacitors C31 and C36 are not populated but it is recommended to provision an area for third capacitor to improve noise performance if necessary.

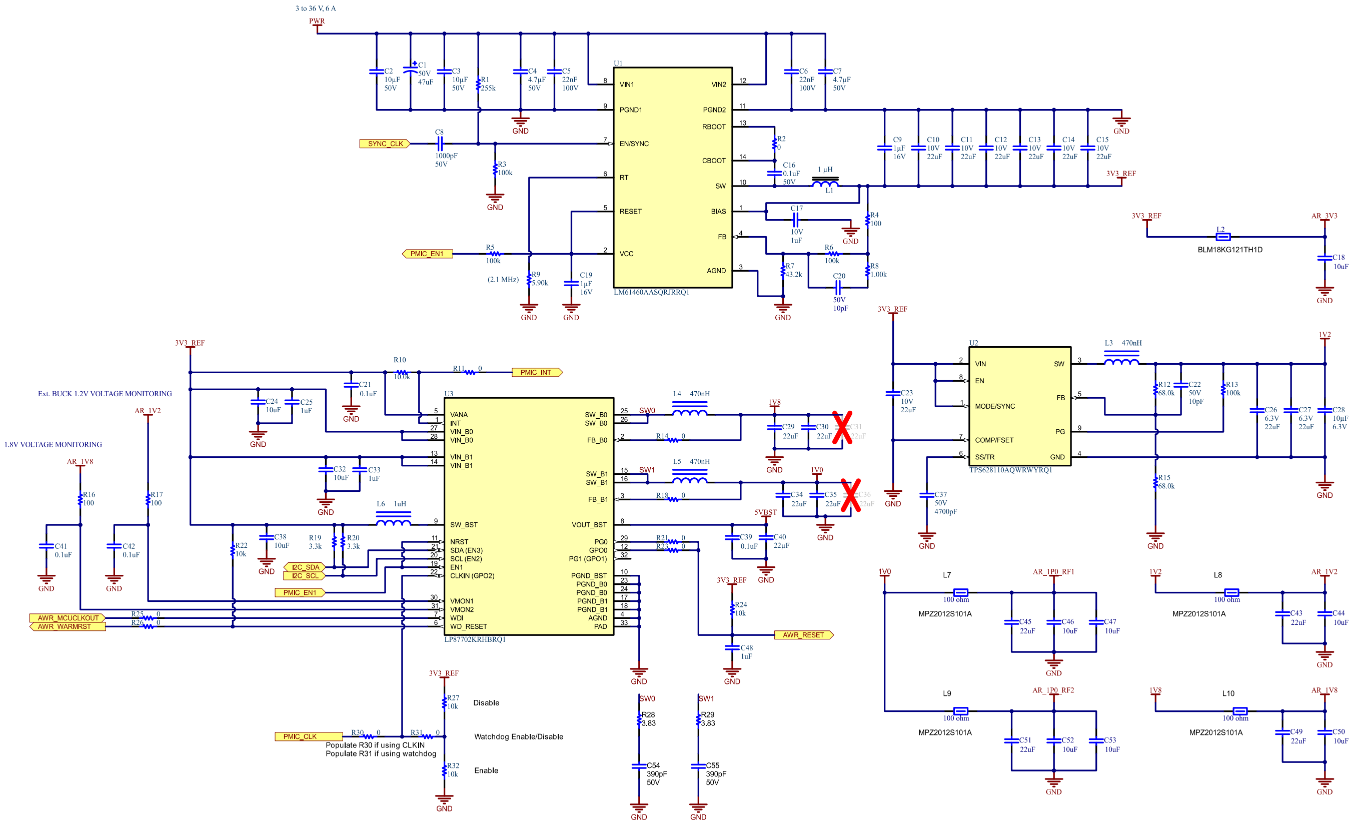

Figure 10. Schematic of the Power Tree

6 Bill of Materials

Table 6 shows the used components in this reference design with LP87702K-Q1, TPS62811-Q1, and LM61460-Q1 power tree.

Table 6. Bill of Materials

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
1	C1	1	47 µF	EEE-FK1H470XP	Panasonic	CAP, AL, 47 uF, 50 V, ± 20%, 0.68 Ω, AEC-Q200 Grade 2, SMD	SMT Radial D8
2	C2, C3	2	10 µF	CGA5L1X7R1H106K160AC	TDK	CAP, CERM, 10 µF, 50 V,± 10%, X7R, AEC-Q200 Grade 1, 1206	1206
3	C4, C7	2	4.7 µF	CGA5L3X7R1H475K160AE	TDK	CAP, CERM, 4.7 µF, 50 V,± 10%, X7R, AEC-Q200 Grade 1, 1206	1206
4	C5, C6	2	0.022 µF	CGA3E2X7R2A223K080AA	TDK	CAP, CERM, 0.022 uF, 100 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	0603
5	C8	1	1000 pF	GCM1885C1H102JA16D	MuRata	CAP, CERM, 1000 pF, 50 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	0603
6	C9, C19, C25, C33, C48	5	1 µF	GCM188R71C105KA64D	MuRata	CAP, CERM, 1 uF, 16 V, ± 10%, X7R, AEC-Q200 Grade 1, 0603	0603
7	C10, C11, C12, C13, C14, C15, C23	7	22 µF	GCM31CR71A226KE02	MuRata	CAP, CERM, 22 uF, 10 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206	1206
8	C16	1	0.1 µF	GCM155R71H104KE02D	MuRata	CAP, CERM, 0.1 uF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	0402
9	C17	1	1 µF	GCM155C71A105KE38D	MuRata	CAP, CERM, 1 uF, 10 V, ± 10%, X7S, AEC-Q200 Grade 1, 0402	0402
10	C18, C44, C46, C47, C50, C52, C53	7	10 µF	GCM21BR71A106KE22L	MuRata	CAP, CERM, 10 uF, 10 V, ± 10%, X7R, 0805	0805
11	C20	1	10 pF	06035A100JAT2A	AVX	CAP, CERM, 10 pF, 50 V, ± 5%, C0G/NP0, 0603	0603
12	C21	1	0.1 µF	GCM155R71C104KA55D	MuRata	CAP, CERM, 0.1 uF, 16 V, ± 10%, X7R, 0402	0402
13	C22	1	10 pF	GCM1555C1H100JA16D	MuRata	CAP, CERM, 10 pF, 50 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402
14	C24, C32, C38	3	10 µF	CL21B106KOQNNNE	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 16 V, ± 10%, X7R, 0805	0805
15	C26, C27	2	22 µF	GCM21BD70J226ME36L	MuRata	CAP, CERM, 22 uF, 6.3 V, ± 20%, X7T, AEC-Q200 Grade 1, 0805	0805
16	C28	1	10 µF	GCM21BR70J106KE22L	MuRata	CAP, CERM, 10 uF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 0805	0805

Table 6. Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
17	C29, C30, C34, C35	4	22 µF	GCM31CR70J226KE23L	MuRata	CAP, CERM, 22 uF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206	1206
18	C37	1	4700 pF	GCM155R71H472KA37D	MuRata	CAP, CERM, 4700 pF, 50 V, ± 10%, X7R, AEC-Q200 Grade 1, 0402	0402
19	C39, C41, C42	3	0.1 µF	0402YC104KAT2A	AVX	CAP, CERM, 0.1 uF, 16 V, ± 10%, X7R, 0402	0402
20	C40	1	22 µF	GRT21BR61E226ME13L	MuRata	CAP, CERM, 22 µF, 25 V,± 20%, X5R, AEC-Q200 Grade 3, 0805	0805
21	C43, C45, C49, C51	4	22 µF	CGA5L1X7R0J226M160AC	TDK	CAP, CERM, 22 uF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206	1206
22	C54, C55	2	390 pF	CGA2B2C0G1H391J050BA	TDK	CAP, CERM, 390 pF, 50 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402
23	L1	1		XEL5030-102MEB	Coilcraft	Inductor, Shielded, Composite, 1.0H, 16.9 A, 0.0084 Ω, AEC-Q200 Grade 1	SMT_5MM28_5MM48
24	L2	1	120 Ω	BLM18KG121TH1D	MuRata	Ferrite Bead, 120 Ω at 100 MHz, 1.9 A, 0603	0603
25	L3, L4, L5	3	470 nH	DFE252012PD-R47M	MuRata Toko	Inductor, Shielded, 470 nH, 4.7 A, 0.021 Ω, SMD	1008
26	L6	1	1 µH	DFE252012PD-1R0M	MuRata Toko	Inductor, Shielded, 1 uH, 3.8 A, 0.035 Ω, AEC-Q200 Grade 1, SMD	1008
27	L7, L8, L9, L10	4	100 Ω	MPZ2012S101A	TDK	Ferrite Bead, 100 Ω at 100 MHz, 4 A, 0805	0805
28	R1	1	255 kΩ	CRCW0603255KFKEA	Vishay-Dale	RES, 255 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603
29	R2, R11, R14, R18, R21, R23, R25, R26, R30, R31	10	0 Ω	CRCW04020000Z0ED	Vishay-Dale	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
30	R3, R5, R6, R13	4	100 kΩ	CRCW0402100KFKED	Vishay-Dale	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
31	R4, R16, R17	3	100 Ω	CRCW0402100RFKED	Vishay-Dale	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
32	R7	1	43.2 kΩ	CRCW040243K2FKED	Vishay-Dale	RES, 43.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
33	R8	1	1.00 kΩ	CRCW04021K00FKED	Vishay-Dale	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
34	R9	1	5.90 kΩ	CRCW04025K90FKED	Vishay-Dale	RES, 5.90 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402

Table 6. Bill of Materials (continued)

Item #	Designator	Quantity	Value	Part Number	Manufacturer	Description	Package Reference
35	R10	1	10.0 kΩ	CRCW040210K0FKED	Vishay-Dale	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
36	R12, R15	2	68.0 kΩ	RC0603FR-0768KL	Yageo	RES, 68.0 k, 1%, 0.1 W, 0603	0603
37	R19, R20	2	3.3 kΩ	CRCW04023K30JNED	Vishay-Dale	RES, 3.3 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
38	R22, R24, R27, R32	4	10 kΩ	CRCW040210K0JNED	Vishay-Dale	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
39	R28, R29	2	3.83 Ω	CRCW04023R83FKED	Vishay-Dale	RES, 3.83, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402
40	U1	1		LM61460AASQRJRRQ1	Texas Instruments	Automotive 6-A Low Noise Synchronous Buck Regulators, RJR0014A (VQFN-HR-14)	RJR0014A
41	U2	1		TPS628110AQWRWYRQ1	Texas Instruments	Automotive Low Input Voltage, Adjustable-Frequency Step-down Converter, RWY0009A (VQFN-HR-9)	RWY0009A
42	U3	1		LP87702DRHBRQ1	Texas Instruments	Boost and Dual Buck Regulators With Diagnostic Functions, RHB0032N (VQFN-32)	RHB0032N
43	C31, C36	0	22 µF	GCM31CR70J226KE23L	MuRata	CAP, CERM, 22 uF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206	1206

7 Conclusion

With this presented solution with the LP87702K-Q1, TPS62811-Q1, and LM61460-Q1 devices, it is possible to meet the power requirements for xWR radar applications while maintaining good efficiency. Solution is compact due to minimum number of external components which also results in low cost. This reference design also includes SafeTI™ components that comply with applicable ISO 26262 requirements.

In addition, LP8770 FMEDA and Functional Safety Manual available to support ASIL compliant system designs. These documents can be requested from the LP87702-Q1 product page.

8 References

See these references for additional information:

1. Texas Instruments, AWR1843 Radar Board Powered by TPS65313-Q1 Wide VIN Safety PMIC and TPS65653-Q1.
2. Texas Instruments, *LP87702-Q1 Dual Buck Converter and 5-V Boost With Diagnostic Functions* datasheet.
3. Texas Instruments, *LP87702-Q1 Technical Reference Manual*.
4. Texas Instruments, *TPS6281x-Q1 2.75-V to 6-V Adjustable-Frequency Step-Down Converter* datasheet.
5. Texas Instruments, *LM61460-Q1 Automotive 3-V to 36-V, 6-A, Low EMI Synchronous Step-Down Converter* datasheet.

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