This user’s guide describes the TLV803EA29DPW-EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

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1 Introduction

The TLV803EA29DPW-EVM is an evaluation module (EVM) for the TLV803E voltage supervisor also called a Reset IC. The TLV803EA29DPW-EVM can be used with any TLV803ExxxDPW devices variants. The TLV803E has a supply voltage range of 1.7 V to 6 V, and offers connections for all device input and output pins. Test points are provided to give the user access to extra connections if needed for oscilloscope or multimeter measurements.

Figure 1. TLV803EA29DPW-EVM Board Top
1.1 Related Documentation

TLV803E / TLV809E Datasheet

1.2 TLV803E Applications

- Applications using DSPs, microcontrollers, or microprocessors
- Wireless communication systems
- Portable/battery-powered equipment
- Setup boxes and TVs
- Building automation
- Notebook/desktop computers, servers
2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TLV803EA29DPW-EVM schematic, bill of materials (BOM), and layout.

2.1 TLV803EA29DPW-EVM Schematic

Figure 3. TLV803EA29DPW-EVM Schematic
# 2.2 TLV803EA29DPW-EVM Bill of Materials

## Table 1. EVM BOM

<table>
<thead>
<tr>
<th>DESIGNATOR</th>
<th>QTY</th>
<th>VALUE</th>
<th>DESCRIPTION</th>
<th>PACKAGE REFERENCE</th>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPCB</td>
<td>1</td>
<td></td>
<td>Printed Circuit Board</td>
<td>LP042</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>1</td>
<td>0.1uF</td>
<td>CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603</td>
<td>0603</td>
<td>C0603C104K8RACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>FID1, FID2, FID3</td>
<td>3</td>
<td></td>
<td>Fiducial mark. There is nothing to buy or mount.</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>H1, H2, H3, H4</td>
<td>4</td>
<td></td>
<td>Bumpon, Hemisphere, 0.44 X 0.20, Clear</td>
<td>Transparent Bumpon</td>
<td>SJ-5303 (CLEAR)</td>
<td>3M</td>
</tr>
<tr>
<td>J1, J2, J3, J4, J5</td>
<td>5</td>
<td></td>
<td>Header, 100mil, 2x1, TH</td>
<td>Header, 2x1, 100mil, TH</td>
<td>800-10-002-10-001000</td>
<td>Mill-Max</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>10.0k</td>
<td>RES, 10.0 k, 1%, 0.1 W, 0603</td>
<td>0603</td>
<td>RC0603FR-0710KL</td>
<td>Yageo</td>
</tr>
<tr>
<td>SH-J1</td>
<td>1</td>
<td></td>
<td>Shunt, 100mil, Tin plated, Black</td>
<td>Shunt Connector Black Open Top, 2x1</td>
<td>SNT-100-BK-T-H</td>
<td>Samtec</td>
</tr>
<tr>
<td>TP1, TP2, TP3, TP4</td>
<td>4</td>
<td></td>
<td>Test Point, Miniature, SMT</td>
<td>Test Point, Miniature, SMT</td>
<td>5019</td>
<td>Keystone</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td></td>
<td>Low Power 250-nA IQ and Small Size Supply Voltage Supervisor</td>
<td>X2SON</td>
<td>TLV803EA29DPWR</td>
<td>Texas Instruments</td>
</tr>
</tbody>
</table>
2.3 Layout and Component Placement

Figure 4 shows the top assembly of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 5 and Figure 6 show the top and bottom layouts, Figure 7 and Figure 8 show the top and bottom layers, and Figure 9 shows the top solder mask of the EVM.
3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each EVM has an input power supply connection, and output RESET pin, and a ground pin.

3.1 EVM Test Points

Table 2 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

<table>
<thead>
<tr>
<th>TEST POINT NUMBER</th>
<th>TEST POINT SILKSCREEN LABEL</th>
<th>FUNCTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP1</td>
<td>V$_{DD}$</td>
<td>Connection to V$_{DD}$ pin</td>
<td>Allows user to monitor the V$<em>{DD}$ pin. The V$</em>{DD}$ pin connects to the input power supply.</td>
</tr>
<tr>
<td>TP2</td>
<td>RESET</td>
<td>Connection to RESET pin</td>
<td>Allows user to monitor the RESET pin. This pin changes logic state depending on the voltage on V$_{DD}$.</td>
</tr>
<tr>
<td>TP3</td>
<td>MR</td>
<td>Connection to MR pin</td>
<td>Allows user to connect to the manual reset pin to force a reset condition.</td>
</tr>
<tr>
<td>TP4</td>
<td>GND</td>
<td>Connection to GND pin</td>
<td>Allows user to connect to the GND pin.</td>
</tr>
</tbody>
</table>

3.2 EVM Jumpers

Table 3 lists the jumpers on the TLV803EA29DPW-EVM. As ordered, the EVM will have 5 jumpers populated.

<table>
<thead>
<tr>
<th>JUMPER</th>
<th>DEFAULT CONNECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>Shorted</td>
<td>Both pins on J1 are connected together. Connect one of the pins to the positive (V$_{DD}$) terminal of the power supply.</td>
</tr>
<tr>
<td>J2</td>
<td>Shorted</td>
<td>Both pins on J2 are connected together. Use either pin on jumper J3 to monitor the RESET output pin.</td>
</tr>
<tr>
<td>J3</td>
<td>Shorted</td>
<td>Both pins on J3 are connected together. Use either pin on jumper J4 as the ground connection.</td>
</tr>
<tr>
<td>J4</td>
<td>Shorted</td>
<td>Both pins on J4 are connected together. Use either pin on jumper J5 as the ground connection.</td>
</tr>
<tr>
<td>J5</td>
<td>Closed</td>
<td>Connect a shunt jumper to jumper J5 to use R1 as the pull-up resistor on the RESET output pin.</td>
</tr>
</tbody>
</table>
4 EVM Setup and Operation

This section describes the functionality and operation of the TLV803EA29DPW-EVM. The user must read the TLV803E / TLV809E Datasheet for electrical characteristics of the device.

4.1 Input Power (V_{DD})

The V_{DD} supply is connected through the J1 header on board. Both pins of jumper J1 are connected together so power can be applied to either pin. Supply voltage is dependent on what the user wants to monitor, but the range is 0.7 V to 6 V. Table 4 details the nominal supply and typical threshold voltage.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>NOMINAL SUPPLY VOLTAGE (V)</th>
<th>TYPICAL THRESHOLD VOLTAGE (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV803EA29DPWR</td>
<td>3.3</td>
<td>2.9 (+/- 2% MAX)</td>
</tr>
</tbody>
</table>

4.2 Monitoring Voltage on V_{DD}

The TLV803E device monitors voltage via the V_{DD} pin. The EVM provides jumper J1 and test point TP1 for connecting the power supply input to the V_{DD} pin. If the voltage on this pin drops below V_{IT}, RESET is asserted low. The V_{DD} pin is connected internally to a comparator through an internal resistor divider at the positive input and the negative input is connected to an internal reference. The internal resistor divider is set to provide the input voltage threshold to cause a reset, V_{IT}, that corresponds to the chosen device variant. Please see the Device Comparison Table in the TLV803E / TLV809E Datasheet for more information on the different device variants.

Upon startup, the TLV803E requires V_{DD} to be above V_{POR} before the RESET output is in the correct logic state. Figure 10 shows the propagation time delay high-to-low (t_{PDHL}) when a voltage fault occurs by V_{DD} falling below V_{IT}, to the time RESET transitions active low. Figure 12 shows the reset time delay when the fault condition is removed by V_{DD} rising above V_{IT}, to the time RESET transitions inactive high. The TLV803E has built-in glitch immunity so falling voltage transients on V_{DD} are ignored if the falling pulse duration is less than the glitch immunity timing (t_{GI}). The glitch immunity specification depends on the amplitude of the voltage transient and the operating conditions. Please see the Glitch Immunity specification in the Timing Requirements section of the TLV803E / TLV809E Datasheet for more detailed information.

![Figure 10. TLV803EA29DPW-EVM Propagation Delay Time High-to-Low (t_{PDHL})](image1)

![Figure 11. TLV803EA29DPW-EVM Reset Delay Time (t_{D})](image2)
4.3 Reset Output (RESET)

The TLV803EA29DPW-EVM comes populated with TLV803EA29DPWR device variant which has open-drain, active-low output topology for the RESET pin. The other device variants provide different output topologies and/or different voltage threshold options and can be used on this EVM. Note: if using a TLV809E device variant with push-pull output topology, the pull-up resistor must be disconnected by leaving jumper J5 open. The EVM provides a jumper J2 and a test point TP2 connected directly to the RESET pin for monitoring and/or interfacing to other devices. The reset signal will be asserted low when the voltage on the \( V_{DD} \) pin falls below \( V_{IT-} \). When the voltage on \( V_{DD} \) rises higher than the hysteresis voltage above the threshold voltage \( (V_{HYS} + V_{IT-}) \) or also labeled \( V_{IT+} \), the RESET pin is pulled high to the inactive state indicating no fault condition. As Figure 13 shows, when returning from a fault condition, that is when \( V_{DD} \) rises above \( V_{IT+} \), \( V_{DD} \) must be above \( V_{IT+} \) for longer than the reset delay \( (t_D) \) otherwise RESET will not transition back to logic high inactive state. This is to prevent a premature signaling of no fault condition if \( V_{DD} \) briefly comes out of undervoltage condition before faulting again.

![Figure 12: TLV803EA29DPW-EVM Return From Fault Glitch Immunity](image)

**Figure 12. TLV803EA29DPW-EVM Return From Fault Glitch Immunity**

4.4 Manual Reset (MR)

The manual reset (MR) pin is a digital input that forces a reset if the input signal is less than 0.4 V and is inactive when above 0.8 x \( V_{DD} \). The MR pin has an internal 100 kΩ pull-up resistor connected to \( V_{DD} \) and can be directly connected to an MCU GPIO, external switch, or left floating if not being used. The device remains in reset condition as long as MR is logic low. The \( \text{RESET} \) output returns from reset condition after MR remains logic high for the reset time delay \( (t_D) \).

**Revision History**

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>June 2020</td>
<td>*</td>
<td>Initial Release</td>
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