ABSTRACT

The Texas Instruments LMQ66430-2EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMQ66430-Q1 wide-input voltage buck converter. The LMQ66430-Q1 is an easy-to-use synchronous step-down voltage converter capable of driving up to 3 A of load current from an input voltage of up to 36 V. The LMQ66430-2EVM features an output voltage of 3.3 V and a switching frequency of 2.2 MHz. By default this EVM is populated with the LMQ66430MC3RXBRQ1. This EVM is capable of supporting the entire LMQ664x0-Q1 family of devices by exchanging the default IC with other variants in the family including the non-automotive grade devices. See the data sheet for additional features, detailed descriptions, and available options.

<table>
<thead>
<tr>
<th>Table 1-1. Device and Package Configurations</th>
</tr>
</thead>
<tbody>
<tr>
<td>EVM</td>
</tr>
<tr>
<td>LMQ66430-2EVM</td>
</tr>
</tbody>
</table>

Figure 1-1. LMQ66430-2EVM Board

**CAUTION**

Caution Hot surface.
Contact may cause burns.
Do not touch.
Table of Contents

1 Setup........................................................................................................................................................................................4
  1.1 Test Points........................................................................................................................................................................4
  1.2 Jumpers............................................................................................................................................................................5
2 Operation................................................................................................................................................................................5
  2.1 Quick Start........................................................................................................................................................................5
3 Schematic.............................................................................................................................................................................6
4 Board Layout........................................................................................................................................................................7
5 Bill of Materials..................................................................................................................................................................10
6 Test Results........................................................................................................................................................................11
  6.1 LMQ66430-2EVM Test Results........................................................................................................................................11

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1 Setup

This section describes the test points and connectors on the EVM and how to properly connect, set up, and use the LMQ66430-Q1 EVM.

1.1 Test Points

The test points on the board can be used to connect to the input of a power supply and output load for the EVM. See Figure 1-1 for typical test setup. The functions of the test point connections are:

- **Vin_EMI** — Input supply to EVM including an EMI filter. Connect to a suitable input supply. Connect at this point for EMI tests.
- **GND_EMI** — Ground connection for the input supply
- **Vin** — Input supply to the IC. Can be connected to a digital multimeter to measure the input voltage after EMI filter.
- **VOUT** — Output voltage test point of EVM. Can be connected to a desired load.
- **GND** — Ground test points
- **PG** — This test point is connected to the PGOOD pin from the IC. Can be tied to an external supply through a pullup resistor or left open.
- **SYNC** — In a MODE/SYNC trim part, this test point is connected to the SYNC pin of the IC. This test point can also be connected to an external clock to synchronize the IC. Make sure the RT resistor is not installed when applying a synchronous clock input. If RMOD is installed, JMODE/SYNC jumper must not short pin 2 to either adjacent pins while applying a synchronous clock input. For evaluating RT trim parts, see the JMODE/SYNC jumper description in Section 1.2.
- **Vcc** — This test point is connected to the Vcc pin of the IC.
- **AGND** — This test point represents the analog ground test point and is connected to the ground plane.

![Figure 1-1. EVM Board Connections](image)

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1.2 Jumpers

See Figure 1-2 for jumper locations.

- **JMODE/SYNC** — Use this jumper to select the mode of operation in a MODE/SYNC trim part. Connecting a jumper between pin 1 and 2 sets the IC operation to PFM (pulse frequency modulation) mode for a higher efficiency at light load. A jumper between pin 2 and pin 3 causes the IC to operate in FPWM (forced pulse width modulation) mode. By default, the jumper is connected between pin 1 and 2. Pin 1 is indicated by the dot on the PCB. When evaluating RT trim parts this jumper can be used to set the switching frequency as long as RMOD is populated and RT is not populated. With RMOD populated, connecting a jumper between pin 1 and 2 sets the switching frequency to 2.2 MHz while connecting the jumper between pin 2 and 3 sets the switching frequency to 1 MHz. If the RT resistor is used to set the switching frequency then RMOD should be depopulated, effectively removing the JMODE/SYNC jumper.

- **JEN** — This jumper allows the ENABLE input to be connected to VIN or GND. Connecting a jumper between pin 1 and 2 shorts the ENABLE input to VIN, enabling the part. Connecting a jumper between pin 2 and 3 shorts the ENABLE input to GND, disabling the part. By default, this jumper is left open because there is a pullup resistor RENT to VIN to enable the IC.

- **JGOOD** — Use this jumper to select how the PGOOD pin is connected. A jumper between pin 1 and 2 uses Vcc as the pullup voltage for PGOOD. In this configuration, the PGOOD pin is pulled up to Vcc through RPG when the output voltage is within regulation. Connecting a jumper between pin 2 and 3 uses VOUT as the pullup voltage for PGOOD. By default, this jumper is not populated.

![Figure 1-2. Jumper Locations](image)

2 Operation

2.1 Quick Start

1. Connect the voltage supply between the Vin_EMI and GND_EMI supply connections.
2. Connect the load between the VOUT and GND test points.
3. Set the supply voltage at an appropriate level between 3.5 V to 36 V. Set the current limit of the supply to an appropriate level.
4. Turn on the power supply. With the default configuration, the EVM powers up and provides $V_{OUT} = 3.3$ V.
5. Monitor the output voltage. The maximum load current is rated at 3 A with the LMQ66430-Q1 device.
3 Schematic

VIN = 3.6V – 36V

Figure 3-1. LMQ66430-2EVM Schematic
4 Board Layout

Figure 4-1. Top View of EVM

Figure 4-2. EVM Top Copper Layer
Figure 4-3. Mid-Layer One

Figure 4-4. Mid-Layer Two
Figure 4-5. EVM Bottom Copper Layer
<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part number</th>
<th>QTY</th>
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<td>CBULK</td>
<td>47-µF 50-V Aluminum Electrolytic Capacitors Radial, Can - SMD 1500 hours at 125°C</td>
<td>Vishay BC Components</td>
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<td>Inductor, Shielded, 3.3 µH, 5 A, 0.0286 Ω, SMD</td>
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<td>RK73Z1ETTP</td>
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<td>SNT-100-BK-G</td>
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<tr>
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<td>Terminal, Turret, TH, Double</td>
<td>Keystone</td>
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<td>4</td>
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<tr>
<td>U1</td>
<td>3-V to 36-V, 3-A Synchronous Buck Converter Optimized for Ultra Low EMI and Light Load Efficiency</td>
<td>Texas Instruments</td>
<td>LMQ66430MC3RXBRQ1</td>
<td>1</td>
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</tbody>
</table>
6 Test Results
6.1 LMQ66430-2EVM Test Results

The LMQ66430-2EVM variant is used for all figures below.

6.1.1 Efficiency and Load Regulation

![Graph showing efficiency and load regulation](image)

**Figure 6-1.** 3.3 V\text{OUT}, AUTO Mode Efficiency

![Graph showing 3.3 V\text{OUT}, 2.2 MHz Load Regulation](image)

**Figure 6-2.** 3.3 V\text{OUT}, 2.2 MHz Load Regulation

![Graph showing 3.3 V\text{OUT}, FPWM Mode Efficiency](image)

**Figure 6-3.** 3.3 V\text{OUT}, FPWM Mode Efficiency

![Graph showing Input Current vs Load Current for 3.3 V\text{OUT}](image)

**Figure 6-4.** Input Current vs Load Current for 3.3 V\text{OUT}

6.1.2 Load Transients

![Graph showing Load Transient 12 V\text{IN}, 3.3 V\text{OUT}, I\text{OUT} = 0 A to 2 A, Slew Rate = 1 A/\mu s, FPWM](image)

**Figure 6-5.** Load Transient 12 V\text{IN}, 3.3 V\text{OUT}, I\text{OUT} = 0 A to 2 A, Slew Rate = 1 A/\mu s, FPWM

![Graph showing Load Transient 12 V\text{IN}, 3.3 V\text{OUT}, I\text{OUT} = 0.5 A to 1.5 A, Slew Rate = 1 A/\mu s](image)

**Figure 6-6.** Load Transient 12 V\text{IN}, 3.3 V\text{OUT}, I\text{OUT} = 0.5 A to 1.5 A, Slew Rate = 1 A/\mu s
6.1.3 Output Ripple and Thermal Picture

![Output Ripple at 12 V_IN, 3.3 V_OUT, No Load](image1)

![Thermal Capture, 12 V_IN, 3.3 V_OUT, 2 A Load, 2.2 MHz, θ_JA= 40°C/W](image2)
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