EVM User's Guide: TPS389387EVM TPS389387EVM Joint Evaluation Module

Texas Instruments

Description

The TPS389387EVM demonstrates the functionality of the TPS38700S-Q1 sequencer and TPS389006 voltage monitoring device. If needed, then connectors and pins are provided to give the user access for oscilloscope or multi-meter measurements.

The EVM comes pre-populated with two devices: a TPS389006 I2C programmable 6 channel supervisor and a TPS38700S-Q1 I2C programmable 6 channel sequencer. The EVM is intended to be operated with an up to 12 rail programmable virtual power tree generated from MSP430 launchpad dev board. This EVM must be used with the MSP430 MCU variant, MSP430FR2355.

Get Started

- 1. Order the TPS3839387EVM.
- 2. Order additional components
 - a. MSP430 MCU variant, MSP430FR2355 (MSP-EXP430FR2355).
 - b. USB-TO-GPIO2 connector (USB-TO-GPIO2).
- 3. Download Code Composer Studio[™] integrated development environment (IDE).



TPS389387EVM Board Top

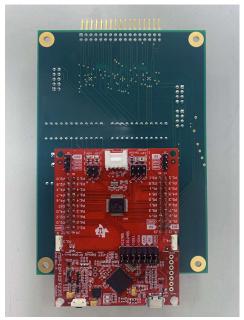
- Download the Fusion Digital Power Designer Platform GUI originally designed for the TPS38700Q1EVM.
- Download the zip file containing the .C code referenced in TPS389387EVM Evaluation Instructions.
- 6. Download the comprehensive reference design files.
- See the latest Design & development pages for MSP430[™].

Features

- TPS3839387EVM is a USB-powered EVM, but has additional provision for external power.
- There is a connector available to interface with different power tree types.

Applications

- Wired networking
- Data center & enterprise computing
- Motor drives
- Factory automation & control
- Grid infrastructure
- Advanced driver assistance system (ADAS)



TPS389387EVM Board Bottom with MSP430

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1 Evaluation Module Overview

1.1 Introduction

This User's Guide describes how to use the TPS389387EVM joint evaluation module (EVM) for engineering demonstration and evaluation of the combined monitor and sequencer devices of TPS389006 Multichannel Voltage Supervisor and the TPS38700S-Q1 Sequencer. This User's Guide contains the EVM schematic, bill of materials (BOM), assembly drawing, top and bottom board layouts, and setup instructions.

Additional functionality of the TPS38700S-Q1 sequencer can be tested through the TPS38700-Q1 GUI. To use this EVM, the MSP-EXP430FR2355 MSP430 launchpad and USB-TO-GPIO2 connector is required.

1.2 Kit Contents

The package includes:

- The USS evaluation module (EVM) with both TPS38700S-Q1 and TPS389006 devices pre-populated.
- The graphical user interface (GUI) to control the configurable parameters of the sequencer IC, TPS38700S-Q1.
- A zip file contained editable code that controls the TPS389387EVM. This is run through Code Composer Studio IDE (CCS), and can be downloaded here.

Not included:

- MSP430, a microcontroller development kit for rapid prototyping. The variant, MSP430FR2355, can be ordered on ti.com through the product page (MSP-EXP430FR2355).
- USB-TO-GPIO2 connector for I2C communication between the GUI and devices. The USB-TO-GPIO2 can be ordered on ti.com through the product page (USB-TO-GPIO2).

1.3 Specification

This sequencer and voltage monitoring device is intended for use in any application with multiple rails that require a specific configuration or series of triggers. TPS38700S-Q1 has a maximum of six enables that can be independently configured or triggered in any sequence through the use of I2C.

In this EVM, the TPS38700S-Q1 is used in tandem with TPS389006. The TPS389006-Q1 uses its sequence logging feature to monitor and assign timestamps/log for the power rails turning on and off. Through the SYNC pin, TPS38700S-Q1 is able to detect the status of the voltage monitoring channels of the TPS389006, and can use this information to verify proper sequencing. This means the sequencer will know the state of all monitor channels and can 'wait' until the channel status changes before sending out another signal, ensuring further sequencing accuracy.

This EVM connects a single TPS38700S-Q1 to a TPS389006. However, in other applications, the TPS389006 SYNC feature allows for communication across multiple devices. If more than 6 rails require monitoring, multiple TPS389006 ICs could be connected and sequenced (ie. if 18 Rails need sequencing, 3 TPS389006 ICs can be used).

1.4 Device Information

The TPS389006 IC variant on this EVM is configured for six integrated multichannel window inputs to monitor six distinct input voltage rails. The device also includes internal glitch immunity and noise filters to eliminate false resets resulting from erroneous signals. The TPS389006 device does not require any external resistors for setting overvoltage and undervoltage reset thresholds which optimizes and improves the reliability for safety systems.

TPS389006 has full I2C functionality which gives flexibility in selecting thresholds, reset delays, glitch filters, and pin functionality. This device offers CRC error checking, sequence logging during turn ON or turn OFF, and a built-in ADC for voltage readouts to provide redundant error checking. In addition to these features, TPS389006 offers a sync feature for rail tagging. Rail tagging works across multiple instances of TPS389006 devices. If users need a different TPS389006 variant, the currently attached device must be removed from the board. The EVM board is designed to support all variants of TPS389006.

The TPS38700S-Q1 IC variant on this EVM is a programmable 6 channel sequencer. The device offers the option of battery backup power and the ability to communicate faults via I2C. The NIRQ pin serves as an interrupt flag to alert the system to possible faults, and the NRST pin asserts logic high under reset condition.

1.5 Sync Function

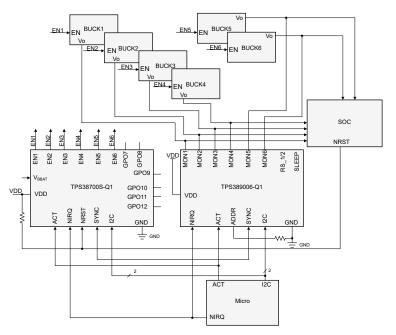


Figure 1-1. Typical Sync Configuration

The TPS389006 is equipped with a SYNC pin as shown in Figure 1-1. It also has a sequence logging feature to monitor and assign timestamps/log for the power rails turning on and off. It can perform sequence logging on a single device or across multiple devices on a board. When either the ACT or SLEEP pin transitions from low to high or high to low, the sequence logging function becomes active until the expiry of the sequence timeout (SEQ_TOUT). During the sequence timeout, the UV faults can be masked (Automask - AMSK) to allow the power rails to rise without triggering a fault. The TPS389006 is designed to assert active low output signals (NIRQ) when the monitored voltage is outside the safe window.

In this EVM, when ACT is driven high, the first EN signal in the power up sequence is turned on by TPS38700S-Q1. Then, the MON1 voltage rises and triggers TPS389006 to send the first SYNC signal which causes TPS38700S-Q1 to turn on the second EN voltage. This process repeats until all Enable voltages turn on. Note that the TPS389006 defaults to using UV thresholds for sending the SYNC pulse when sequencing up. When ACT is driven low, the first EN signal in the power down sequence is immediately driven low. When the corresponding MON voltage drops below the threshold, TPS389006 sends a SYNC pulse. The SYNC pulse causes TPS38700S-Q1 to turn off the second EN signal. This process also repeats until all voltages have been turned off. By default, SYNC voltage thresholds for TPS389006 are based on the OFF voltage. The voltage thresholds can be changed to UV voltage thresholds for both sequencing up and down. Note that the TPS389006 defaults to using OFF voltage threshold (MONx<140mV) for sending the SYNC pulse when sequencing down.

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2 Hardware

2.1 Setup

This section describes all the parts of the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent power supply connection, but all grounds are interconnected on the board.

2.2 Connectors, Headers, and LEDs

 Table 2-1 defines the location and function of all connectors, headers, jumpers and LEDs on the EVM. Use

 Figure 6-1 or the labeled diagram for further reference of pin numbers.

Location	Pins/Silkscreen Label	Function/Description		
J1/J2/J3/J4		Connector to MSP430.		
J16		Pins 1-4: Connects I2C to MSP430. Pins 5-8; Connects MSP430 to sequencer & monitor enables.		
J17		Pins 1-2: Connects interrupts to MSP430. Pins 3-4: Connects resets to MSP430. Pins 5-8: Adds pull-up resistors to I2C. Not necessary if USB-to-I2C connector is used (J19).		

Table 2-1. Connectors, Headers, LEDs of TPS389387EVM

Table 2-1. Connectors, Headers, LEDs of TPS389387EVM (continued)						
Location	Pins/Silkscreen Label	Function/Description				
	Pin 1	Allows user to monitor TPS389006 Power Rail 12.				
	Pin 2	Allows user to monitor TPS38700S-Q1 Enable 12.				
	Pin 3	Allows user to monitor TPS389006 Power Rail 11.				
	Pin 4	Allows user to monitor TPS38700S-Q1 Enable 11.				
	Pin 5	Allows user to monitor TPS389006 Power Rail 10.				
	Pin 6	Allows user to monitor TPS38700S-Q1 Enable 10.				
	Pin 7	Allows user to monitor TPS389006 Power Rail 9.				
	Pin 8	Allows user to monitor TPS38700S-Q1 Enable 9.				
	Pin 9	Allows user to monitor TPS389006 Power Rail 8.				
	Pin 10	Allows user to monitor TPS38700S-Q1 Enable 8.				
	Pin 11	Allows user to monitor TPS389006 Power Rail 7.				
	Pin 12	Allows user to monitor TPS38700S-Q1 Enable 7.				
	Pin 13	Allows user to monitor TPS389006 Power Rail 6.				
	Pin 14	Allows user to monitor TPS38700S-Q1 Enable 6.				
	Pin 15	Allows user to monitor TPS389006 Power Rail 5.				
	Pin 16	Allows user to monitor TPS38700S-Q1 Enable 5.				
J18	Pin 17	Allows user to monitor TPS389006 Power Rail 4.				
JIO	Pin 18	Allows user to monitor TPS38700S-Q1 Enable 4.				
	Pin 19	Allows user to monitor TPS389006 Power Rail 3.				
	Pin 20	Allows user to monitor TPS38700S-Q1 Enable 3.				
	Pin 21	Allows user to monitor TPS389006 Power Rail 2.				
	Pin 22	Allows user to monitor TPS38700S-Q1 Enable 2.				
	Pin 23	Allows user to monitor TPS389006 Power Rail 1.				
	Pin 24	Allows user to monitor TPS38700S-Q1 Enable 1.				
	Pin 25	I2C SCL.				
	Pin 26	TPS38700S-Q1 Sequencer Enable.				
	Pin 27	I2C SDA.				
	Pin 28	nIRQ or Interrupt.				
	Pin 29	TPS38900 Monitor Enable.				
	Pin 30	TPS38700S-Q1 Reset.				
	Pin 31	Ground.				
	Pin 32	Ground.				
	Pin 33	Ground.				
	Pin 34	Ground.				
J19		Header for USB-TO-GPIO2 connector; Used for TPS38700-Q1 GUI and I2C communication.				
J20		Selection between external power connector & MSP430 Power.				
J21		External Power Connector.				

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		LEDs of TPS389387EVM (continued)
Location	Pins/Silkscreen Label	Function/Description
	PWR1	Switch for TPS389006 Power Rail 1.
	PWR2	Switch for TPS389006 Power Rail 2.
	PWR3	Switch for TPS389006 Power Rail 3.
	PWR4	Switch for TPS389006 Power Rail 4.
	PWR5	Switch for TPS389006 Power Rail 5.
SW1	PWR6	Switch for TPS389006 Power Rail 6.
5001	PWR7	Switch for TPS389006 Power Rail 7.
	PWR8	Switch for TPS389006 Power Rail 8.
	PWR9	Switch for TPS389006 Power Rail 9.
	PWR10	Switch for TPS389006 Power Rail 10.
	PWR11	Switch for TPS389006 Power Rail 11.
	PWR12	Switch for TPS389006 Power Rail 12.
	EN1	Switch for TPS38700S-Q1 Enable 1.
	EN2	Switch for TPS38700S-Q1 Enable 2.
	EN3	Switch for TPS38700S-Q1 Enable 3.
	EN4	Switch for TPS38700S-Q1 Enable 4.
	EN5	Switch for TPS38700S-Q1 Enable 5.
SW2	EN6	Switch for TPS38700S-Q1 Enable 6.
3002	EN7	Switch for TPS38700S-Q1 Enable 7.
	EN8	Switch for TPS38700S-Q1 Enable 8.
	EN9	Switch for TPS38700S-Q1 Enable 9.
	EN10	Switch for TPS38700S-Q1 Enable 10.
	EN11	Switch for TPS38700S-Q1 Enable 11.
	EN12	Switch for TPS38700S-Q1 Enable 12.
D1		LED 1; Turns on for nirQ/Interrupt.
D2		LED 2; Turns on for Enable 1.
D3		LED 3; Turns on for Enable 2.
D4		LED 4; Turns on for Enable 3.

2.3 EVM Jumpers

Table 2-2 lists the jumpers on the TPS389387EVM. The EVM has five jumpers installed.

Table 2-2. Jumper Configuration					
Jumper	Pins/Silkscreen Label	Jumper Configuration			
J16	SCL	Open			
J16	DA	Open			
J16	MON_EN	Shunted			
J16	SEQ_EN	Shunted			
J17	nIRQ	Shunted			
J17	RST	Shunted			
J17	I2C Pullup	Open			
J20	1-2	If Shunted, then external power supply is 5 V.			
J20	2-3	If Shunted, then external power supply is 6 V.			

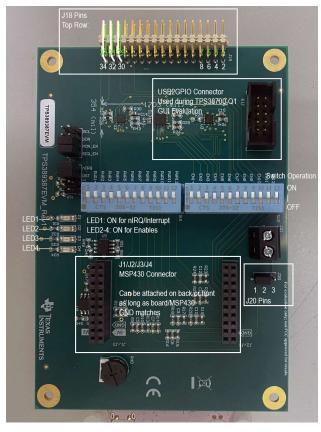


Figure 2-1. Labeled TPS389387EVM Pins and Connector Locations

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3 Software

3.1 Software Description

This section describes the software functionality and operation of this EVM. Refer to the TPS389006 and TPS38700S-Q1 data sheet for details on the electrical characteristics of the respective devices.

The EVM comes pre-populated with a TPS389006 I2C programmable 6 channel supervisor and a TPS38700S-Q1 I2C programmable 6 channel sequencer, and a 12 rail programmable virtual power tree generated from the MSP430 launchpad dev board. This EVM is capable of different configurations to fully evaluate the functionality and interactions between the TPS389006 and TPS38700S-Q1 device variants. With the current devices, the EVM can monitor and sequence up to 6 channels.

The default configuration of the EVM Jumpers is referenced in Table 2-2.Consult the Device Threshold Table in the TPS389006-Q1 data sheet to verify proper voltage monitored values.

To test the functionality of TPS389387EVM, go to TPS389387EVM Evaluation Instructions.

To communicate with the TPS38700S-Q1 and TPS389387EVM, including reading and writing to the registers, as well as clearing interrupts, follow TPS38700-Q1 GUI instructions.

Software Usage Guide

This table lists actions that the EVM user may wish to perform and the corresponding software interfaces. **Table 3-1. Software Usage Guide**

Action	User interface
Change the voltage level for voltage outputs 1-6	MSP430 .C code in Code Composer Studio
Change the threshold voltages of the TPS389006 device	Fusion Digital Power Designer I2C GUI
Change the power up and power down sequence of the TPS38700S-Q1 device	Fusion Digital Power Designer I2C GUI
Change MSP430 generated output power rails to respond to enable inputs	MSP430 .C code in Code Composer Studio
Clear TPS389006 or TPS38700S-Q1 fault interrupts	Fusion Digital Power Designer I2C GUI



4 TPS389387EVM Evaluation Instructions

Equipment Needed

Hardware Equipment Needed for TPS389387EVM Evaluation:

- TPS389387EVM
- MSP430 LaunchPad[™], MSP-EXP430FR2355
- MSP430 connector/power cable (USB to micro-USB)
- Multi-channel oscilloscope to review evaluation waveforms
- Jumper cables for additional evaluation

Software Needed for TPS389387EVM Evaluation:

- A zip file contained editable code that controls the TPS389387EVM. This can be downloaded here.
- Code Composer Studio IDE (CCS), CCS v8.0 or higher. Code Composer Studio Desktop is a professional integrated development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio is comprised of a suite of tools used to develop and debug embedded applications. Code Composer Studio includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. Learn more about CCS and download at Code Composer Studio.

Hardware Setup

Follow the steps below for the hardware setup:

- Attach the MSP430 to the pins at the bottom side of the TPS389387EVM. The orientation is detailed in TPS389387EVM Board Bottom with MSP430. Make sure that the GND pins match the corresponding board connector.
- 2. Connect the power cable to the MSP430 and USB port of the computer.
- 3. Make sure all jumpers are connected as per the guidelines in Table 2-2.

Software Setup

- 1. Download Code Composer Studio IDE (CCS) to edit the code for this EVM.
 - a. There is a cloud composer available, but this is not necessary.
 - b. CCS can ask if additional components are needed. Please select the MSP430 option before proceeding to download.
- 2. Download the code required to evaluate the EVM.
- 3. Launch CCS and import the code into the workspace. Refer to the CCS Getting Started instructions on ti.com for additional help.
 - a. When CCS has been launched, select a workspace directory. This defines the location of your project on your operating system.

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b. Use Project>Import Existing CCS Eclipse Project. Go to the desired demo project directory that contains main.c. This is illustrated in Figure 4-1.

Name	Date modified
power_tree_sim	8/5/2022 4:04 PM

<		
power_tree_sim		
	Select Folder	Cancel

Figure 4-1. Selecting the Project Directory in CCS

- c. Click OK.
- d. CCS recognizes the project and allows the user to import. Check to make sure the CCS has found the project, by looking for a checkmark to the left of the project name. This is shown in Figure 4-2.

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Discovered projects:		
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	Refre	esh
Automatically import referenced projects found in same search-directory		
Copy projects into workspace		
Open <u>Resource Explorer</u> to browse a wide selection of example projects		
⑦ Finish	Cance	el

Figure 4-2. Recognizing the Project in CCS

e. If CCS does not show a checkmark, then this means that your workspace already has a project by that name. Resolve this by renaming or deleting that project.



f. At this point, the code is fully uploaded to CCS. The workspace looks like Figure 4-1.

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Figure 4-3. CCS Workspace with Code Uploaded

- 4. Edit the code to confirm correct operation.
 - a. To change the output voltages for virtual power tree, edit line 8. This line reads as follows:

const float outputVoltages[] = {1600,1600,1600,1600,1600,1600,3000,2500,2500,2500,2500,2500};

Each of the values within the brackets correspond to the Vout for the TPS389006's power monitor rails. These values are all in millivolts.

b. To change whether each virtual power rail requires an enable signal from the sequencer to start up, edit line 13. This line reads as follows:

const int requiresEN = 0;

If the value after the "=" is a 0, then an enable signal from the sequencer is not required. If this value is set to 1, then an enable signal from the sequencer is required to start up.



5. Run the code by selecting *Run> Start Debugging* in the CCS workspace. See Figure 4-4 for more information.

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Figure 4-4. Run Code in CCS

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- 6. Once the code is run, confirm correct operation.
 - a. Check output voltages by measuring waveforms resultant from connections between pins in the header (J18) and oscilloscope. For more clarity on the pin locations, look at the schematic or Figure 2-1.
 - b. Determine correct operation of Enables and Interrupts by examining the LEDs on the EVM. See LED functionality in Table 2-1.
 - c. By pressing and holding button S1 on the MSP430 launchpad, the sequencer powers down the voltage rails in sequence. Releasing the button causes the power rails to power up in sequence. The power up and power down sequence can be checked by connecting an oscilloscope to the enable outputs of header J18.
 - d. Figure 4-5 shows correct operation of the first three enable signals in the power up sequence and the corresponding sync pulses from the TPS389006.

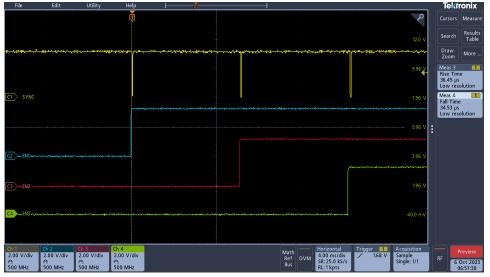


Figure 4-5. Power Sequence Up with Sync



e. Figure 4-6 shows correct operation of the first three enable signals in the power down sequence and the corresponding sync pulses from the TPS389006.

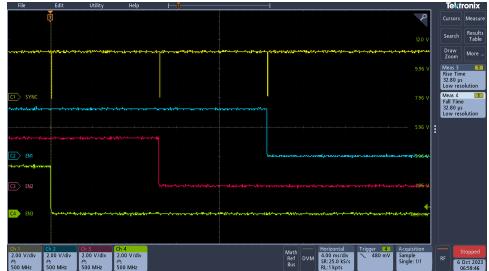


Figure 4-6. Power Sequence Down with Sync

f. Figure 4-7 shows where to place the oscilloscope probe on the EVM to view the sync signal. Place the probe on the terminal of R30 closest to device U2.

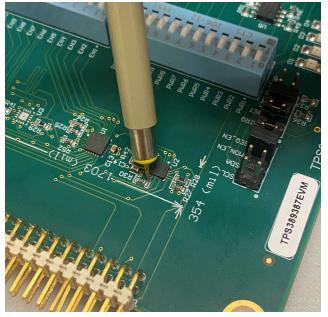


Figure 4-7. Sync Signal Probe

- 7. The dipswitches can also be used to manually test the functionality of the device interrupts and enables.
 - a. LED1 (D1) turns on in the case of an interrupt. This can be tested by using the dipswitches that control the TPS389006 power rail (SW1). When these dipswitches are flipped to the off position, the respective rail is manually turned off, resulting in an interrupt and turning on LED1.
 - b. LED2 (D2) turns on when Enable 1 is activated. This can be tested using the dipswitches that control the TPS38700S-Q1 Enables (SW2). When these dipswitches are flipped to the off position, the respective EN is manually turned off, resulting in LED2 to turn off.
 - c. LED3 (D3) and LED4 (D4) turn on when Enable 2 and Enable 3 are activated, respectively. This can be verified in the same way as LED2.



5 TPS38700-Q1 GUI instructions

Equipment Needed:

- TPS389387EVM
- USB-TO-GPIO2 connector
- MSP430 LaunchPad™, MSP-EXP430FR2355
- MSP430 connector/power cable (USB to micro-USB)
- Multi-channel oscilloscope to review evaluation waveforms
- Jumper cables for additional evaluation

5.1 GUI Installation

Follow the steps below for GUI installation:

- 1. Install the GUI.
 - a. Download the Fusion Digital Power Designer Platform GUI for TPS38700Q1EVM.
 - b. Open the downloaded file.
 - c. In the Welcome Wizard window, click Next.

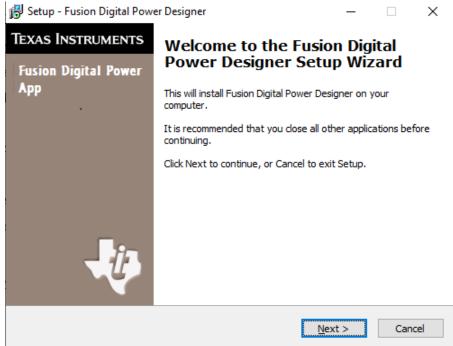


Figure 5-1. Welcome Setup Window

d. Accept the license agreement and then click Next.

滑 Setup - Fusion Digital Power Designer		_		×
License Agreement Please read the following important informatio	n before continuing.			Ì
Please read the following License Agreement. agreement before continuing with the installat		erms of thi	s	
Important - Please read the fol carefully. This is a legally binding this license agreement, you will be and agree to the terms of this li- click "I have read and agree" un to accept and agree to the terms of behalf of yourself and your comp enter into and to be bound by the agreement on behalf of yourself and	agreement. Aft e asked whether icense agreeme less: (1) you are of this license ag oany; and (2) yo terms of this lega	eryoure youacc nt.Do authoriz reement uintend ally bind	ead ept not zed on l to	
 I accept the agreement I do not accept the agreement 				
	< Back Nex	t >	Cano	el

Figure 5-2. Setup License Agreement Window

e. The default destination folder works best. Click Next.

🔀 Setup - Fusion Digital Power Designer	_		×
Select Destination Location Where should Fusion Digital Power Designer be installed?			Ð
Setup will install Fusion Digital Power Designer into the follo	wing fo	lder.	
To continue, click Next. If you would like to select a different folder,	click Br	owse.	
rogram Files (x86)\Texas Instruments\Fusion Digital Power Designer	E	Browse	
At least 72.6 MB of free disk space is required.			
< Back Next	t >	Ca	incel

Figure 5-3. Setup Destination Window

f. Click Next for the Select Start Menu Folder option.

🔀 Setup - Fusion Digital Power Designer	_		×
Select Start Menu Folder Where should Setup place the program's shortcuts?			ð
Setup will create the program's shortcuts in the following s	Start Me	nu folder.	
To continue, click Next. If you would like to select a different folder	, click Bi	rowse.	
Texas Instruments\Fusion Digital Power Designer	E	Browse	
Don't create a Start Menu folder			
< Back Ne	xt >	Ca	ncel

Figure 5-4. Setup Window - Start Menu Selection

g. There is no need to install additional options for this EVM. Click Next.

🗊 Setup - Fusion Digital Power Designer		_		×
Select Additional Tasks Which additional tasks should be performed?			0	
Select the additional tasks you would like Set Power Designer, then click Next.	up to perform wh	ile installing Fu	sion Digit	al
Additional icons:				
Create a desktop icon				
Create a Quick Launch icon				
Other desktop shortcuts				
SMBus I2C SAA Debug Tool				
UCD9xxx Device GUI				
Additional Tasks:				
Add application directory to your system	PATH			
[< Back	Next >	Can	ncel

Figure 5-5. Setup Window - Additional Tasks



h. Click Install to install the Fusion software.

😽 Setup - Fusion Digital Power Designer 🦳 —		×
Ready to Install Setup is now ready to begin installing Fusion Digital Power Designer on your computer.		
Click Install to continue with the installation, or click Back if you want to review change any settings.	or	
Destination location: C:\Program Files (x86)\Texas Instruments\Fusion Digital Power Designer		^
<	>	<u> </u>
< Back Install	Ca	ancel

Figure 5-6. Setup Installation Window

i. Click on Finish to complete the installation setup and launch the software.

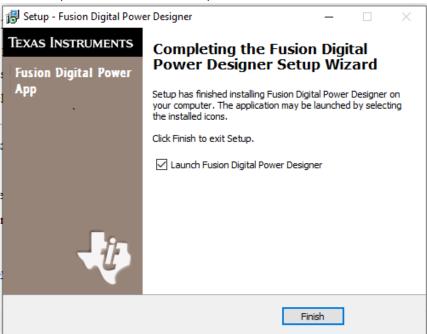


Figure 5-7. Installation Complete Window



5.2 Quick Start for TPS38700-Q1 GUI

Follow the steps below precisely to quickly evaluate the TPS38700S-Q1 on the TPS389387EVM. In this quick start, Enable 1 and Enable 2 signals after the ACT pin is triggered are detailed.

- 1. Install the GUI based on Section 5.1. Skip this section if the TPS38700Q1EVM GUI is already installed.
- Attach the MSP430 to the pins at the bottom side of the TPS389387EVM. The orientation is detailed in TPS389387EVM Board Bottom with MSP430. Make sure that the GND pins match the corresponding board connector.
- 3. Connect the MSP430 power cable to the MSP430 and USB port of the computer.
- 4. Make sure all jumpers are connected as per the guidelines in Table 2-2.
- 5. Connect TI's USB-TO-GPIO2 connector to J19 of the EVM and to the USB port of the computer.
- 6. Once the TI's USB-TO-GPIO2 connector is connected to the EVM and the computer, launch the evaluation software Fusion Digital Power Designer.
- 7. Click on I2C GUI in the bottom right.

TE	EXAS	Ins	TRU	MEN	rs	
Fusion Di Version 7.4.3	-		<u> </u>	nər,		
No Devices Fo	devices were	e found. Plea:	se check tha	t the serial cabl	e end of your USB adapter	r is attached to your device and
Scanning Mode:	DeviceI	DAndCode	AndICDe	viceID		
USB Adapter Fire	nware Vers	ion: 1.0.1	1			
Bus Speed:	Packet E	rror Checki	ng:		ALERT Pullup:	2.2 kΩ 🗸
○ 100 kHz	Enable	ed		•) Serial	CLOCK Pullup:	2.2 kΩ 🗸
400 kHz	🔿 Disab	led			DATA Pullup:	2.2 kΩ 🗸
Signals SMBALERT#:	ACK: High	(Refresh	1		
Control Lines:	#1	#2	#3	#4	#5	
(dick to set)	O High	O High	O High	O High	O High	Refresh All
	Low	Low	• Low	Low	Low Offline Mode Exit Pro	ogram 12C GUI

Figure 5-8. Fusion Welcome Window



8. Click on Change Scan Mode to select TPS38700x and then click OK.

🜵 Texas Instruments - Fusion Digital Power De	signer		_ D 🔀
File Tools			
Q Skip scanning for all Change Scan Mode St	tart Polling Polling Interval 1000 ms		
# Address △ Device			
Timestamp Message			
Copy Log Clear Log			Indude poling activities
Fusion Digital Power Designer v7.6.6.Beta No Adap	pter	Not Saved	😽 TEXAS INSTRUMENTS fusion digital power

Figure 5-9. Fusion Scan Window

le Tools	1			
Skip scanning	he is a stre	Polling Polling Interval 1000 ms		_ = ×
Hudit		skip TPS638x0/63831 TPS696xx	TP538700x XP553830 TP5542A50	TPS54xC2x
	1d 0x01 TPS38700x	✓ 18d 0x12 TPS38700x ✓	34d 0x22 TPS38700x S0d 0x32 TPS38700x	✓ 66d 0x42 TPS38700x
	2d 0x02 TPS38700x	✓ 19d 0x13 TPS38700x ✓	35d 0x23 TPS38700x S1d 0x33 TPS38700x	G7d 0x43 TPS38700x
	3d 0x03 TPS38700x	✓ 20d 0x14 TPS38700x ✓	36d 0x24 TPS38700x 52d 0x34 TPS38700x	✓ 68d 0x44 TPS38700x
	4d 0x04 TPS38700x	✓ 21d 0x15 TPS38700x ✓	37d 0x25 TPS38700x S3d 0x35 TPS38700x	✓ 69d 0x45 TPS38700x
	5d 0x05 TPS38700x	✓ 22d 0x16 TPS38700x ✓	38d 0x26 TPS38700x 54d 0x36 TPS38700x	✓ 70d 0x46 TPS38700x
	6d 0x06 TPS38700x	✓ 23d 0x17 TPS38700x ✓	39d 0x27 TPS38700x S5d 0x37 TPS38700x	✓ 71d 0x47 TPS38700x
	7d 0x07 TPS38700x	✓ 24d 0x18 TPS38700x ✓	40d 0x28 TFS38700x S6d 0x38 TFS38700x	✓ 72d 0x48 TPS38700x
1	8d 0x08 TPS38700x	✓ 25d 0x19 TPS38700x ✓	41d 0x29 TPS38700x S7d 0x39 TPS38700x	✓ 73d 0x49 TPS38700x
	9d 0x09 TPS38700x	✓ 26d 0x1A TPS38700x ✓	42d 0x2A TPS38700x S8d 0x3A TPS38700x	✓ 74d 0x4A TPS38700x
nestamp	10d 0x0A TPS38700x	✓ 27d 0x1B TPS38700x ✓	43d 0x28 TPS38700x 59d 0x38 TPS38700x	✓ 75d 0x4B TPS38700x
in the stand p	11d 0x08 TPS38700x	✓ 28d 0x1C TPS38700x ✓	44d 0x2C TPS38700x	✓ 76d 0x4C TPS38700x
	13d 0x0D TPS38700x	✓ 29d 0x1D TPS38700x	45d 0x2D TPS38700x	✓ 77d 0x4D TPS38700x
	14d 0x0E TPS38700x	✓ 30d 0x1E TPS38700x ✓	46d 0x2E TPS38700x C 62d 0x3E TPS38700x	✓ 78d 0x4E TPS38700x
	15d 0x0F TPS38700x	✓ 31d 0x1F TPS38700x	47d 0x2F TPS38700x	✓ 79d 0x4F TPS38700x
	16d 0x10 TPS38700x	✓ 32d 0x20 TPS38700x ✓	48d 0x30 TPS38700x < 64d 0x40 TPS38700x	✓ 80d 0x50 TPS38700x
	17d 0x11 TPS38700x	✓ 33d 0x21 TPS38700x ✓	49d 0x31 TPS38700x	✓ 81d 0x51 TPS38700x
			ОК	
Copy Log	ClearLog			Include poling activities

Figure 5-10. Fusion Scan Selection Window

9. Scan for the TPS38700-Q1 by clicking on Scan for TPS38700x on top left of the window.

🜵 Texas	Instrument	s - Fusion Digital P	ower Designer				
File To	ols						
Q, Scan f	or TPS38700x	Change Scan Mod	le 🕨 🕨 Start Polling	Polling Interval	1000 ms		
#	Address	△ Device					
Log							
Log							
Timestar		Messag					
13:09:13				ock: 2.2 kΩ; Data: 2.2 kΩ): ACK		
13:09:13			Mode (PEC): ACK				
13:09:13	3.365	SetBuss	Speed (Speed400KHz)): ACK			

Figure 5-11. Fusion Scan Window - Scanning for TPS38700Q1EVM 10. Once the EVM is discovered, select *Click to Configure* (text in blue).

🏘 Texas Instruments - Fusion	Digital Power Designer	- (•		💶 🖻 ≚
File Tools					
Q Scan for TPS38700x Change	Scan Mode -> Start Polling Polling Interval	1000 ms			
# Address △	Device				
1 3Ch (60d)	TPS38700C			Click to Configure	
Log					
Timestamp	Message				^
13:20:10.132	Scanning USB Adapter #1 at address 121d (TPS387	-			
13:20:10.196	I2CRead (Address 121d, Cmd 0x01): NACK <empty< td=""><td></td><td></td><td></td><td></td></empty<>				
13:20:10.252	Scanning USB Adapter #1 at address 122d (TPS387	10x) for devices			
13:20:10.303	I2CRead (Address 122d, Cmd 0x01): NACK <empty< td=""><td>></td><td></td><td></td><td></td></empty<>	>			
13:20:10.356	Scanning USB Adapter #1 at address 123d (TPS387	I0x) for devices			
13:20:10.411	I2CRead (Address 123d, Cmd 0x01): NACK <empty< td=""><td>></td><td></td><td></td><td></td></empty<>	>			
13:20:10.471	Scanning USB Adapter #1 at address 124d (TPS387	0x) for devices			
13:20:10.524	I2CRead (Address 124d, Cmd 0x01): NACK <empty< td=""><td>></td><td></td><td></td><td></td></empty<>	>			
13:20:10.580	Scanning USB Adapter #1 at address 125d (TPS387	00x) for devices			
13:20:10.633	I2CRead (Address 125d, Cmd 0x01): NACK <empty< td=""><td>></td><td></td><td></td><td></td></empty<>	>			
13:20:10.694	Scanning USB Adapter #1 at address 126d (TPS387	0x) for devices			
13:20:10.753	I2CRead (Address 126d, Cmd 0x01): NACK <empty< td=""><td>></td><td></td><td></td><td></td></empty<>	>			
13:20:10.801	Found 1 device.				 (ii)
Copy Log Clear Log					Include polling activities
Fusion Digital Power Designer v7	4.2.2.Alpha USB Adapter v1.0.11 [PEC: 400 kHz]		Not Saved	ta Texas Inst	RUMENTS fusion digital power

Figure 5-12. Fusion Scan Window - Scan for TPS38700Q1EVM Completed



🐶 Texas

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11. Select Refresh All to update the GUI to the preprogrammed device configuration.

	((A 8							
Config System Config	Sequence Config	Watchdog Config	Alarms (RTC) C	onfig					atus Registers - Inter	rupt			V	1 5	Status
Fime Config ———]]	IN	T_SRC (10h)	GIR	I	NT SRC2 (11h)	OLR		EN_ST
250 🗸								7	F_INTERR	OLR	7	F_VENDOR	OLR		
Time slot between sequ	uencing points = T	TIME[7:0] * SSTEP	+ T_min, where T	_min = 125 μs				6	EM_PD	(CLB)	6	F_SDA	CLR		EN1
	TIME[7:0]	Min (-6%)	Typical	Max (+6%)				5	WDT	OIR	5	RT_CRC	OLR		
Power-up / Sleep-exit	t 2 🗘	587.5	625.0 💭	662.5 μs	3			4	PEC	(GLB)	4	BIST	OLR		EN2
Power-down / Sleep-e	entry 2 🔅	587.5	625.0	662.5 µs	:			3	RTC	018	3	LDO	OLR		
									C C2	OLR	2	TSD	OLR		-
								2	F_EN						
Pins mapping									F_EN F_OSC		1	ECC DED	000		ENG
If Pin not mapped (Nor			-					1	F_OSC	013	1	ECC_DED	OLC.		EN3
	e of the time slot[1:	15], pin will be up	Power-up/Sleep-	exit sequence), or do					F_OSC			ECC_DED			EN3
If Pin not mapped (Nor If Pin is mapped to one	e of the time slot[1:	15], pin will be up	Power-up/Sleep-	exit sequence), or do				1	F_OSC	OLR OLR	1	ECC_DED	OLC.		EN4
If Pin not mapped (Nor If Pin is mapped to one	e of the time slot[1:	15], pin will be up s first up (or down	Power-up/Sleep-	exit sequence), or do	own (Power-do		·	1 0 Sta	F_OSC F_NRSTIRQ	OLR OLR	1	ECC_DED	018 018		EN4
If Pin not mapped (Nor If Pin is mapped to one sequence) within the t	e of the time slot[1: ime slot where 1st i	15], pin will be up s first up (or down	Power-up/Sleep- I, and 15th is last	exit sequence), or do up (or down).	own (Power-do	leep-entry	·	1 0 Sta	F_OSC F_NRSTIRQ atus Register - Contr	OLR OLR	1	ECC_DED PBSP	018 018		EN4 EN5
If Pin not mapped (Nor If Pin is mapped to one sequence) within the t Pins 13 (CLK320E)	e of the time slot[1: ime slot where 1st i Power U 4th	15], pin will be up s first up (or down Up P V 4th	Power-up/Sleep- i, and 15th is last	exit sequence), or do up (or down).	e Exit	ileep-entry Sileep En	ntry	1 0 Sta	F_OSC F_NRSTIRQ atus Register - Contr TL_STAT (13h)	OLR OLR	1	ECC_DED PBSP AST_RST (1Ah)	018 018		EN4
If Pin not mapped (Nor If Pin is mapped to one sequence) within the tr Pins 13 (CLK32OE) 19 (EN1)	e of the time slot[1: ime slot where 1st i Power t 4th 1st	15], pin will be up is first up (or down Jp P V 4th Sth	Power-up/Sleep- i, and 15th is last ower Down	exit sequence), or do up (or down). Sleep None None	exit	Sleep En	atry	1 0 Sta 7	F_OSC F_NRSTIRQ htus Register - Contr L_STAT (13h) ST_WD_EN	OLR OLR	1 0	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST NPWR_BTN	018 018)	EN4 EN5 EN6
If Pin not mapped (Nor If Pin is mapped to one sequence) within the t Pins 13 (CLK320E)	e of the time slot[1: ime slot where 1st i Power U 4th	15], pin will be up s first up (or down Up P V 4th	Power-up/Sleep- i, and 15th is last	exit sequence), or do up (or down).	Exit	ileep-entry Sileep En	ntry	1 0 5ta 7 6 5 4	F_OSC F_NRSTIRQ tus Register - Contro L_STAT (13h) ST_WD_EN ST_WBAT ST_NBAT ST_NIRQ ST_NIRST	OLR OLR	1 0 7 6 5 4	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD	018 018		EN4 EN5 EN6
If Pin not mapped (Nor If Pin is mapped to one sequence) within the tr Pins 13 (CLK32OE) 19 (EN1)	e of the time slot[1: ime slot where 1st i Power t 4th 1st	15], pin will be up is first up (or down Jp P V 4th Sth	Power-up/Sleep- i, and 15th is last ower Down	exit sequence), or do up (or down). Sleep None None	exit	Sleep En	atry	1 0 Sta 7 6 5 4 3	F_OSC F_NRSTIRQ tus Register - Contro T_STAT (13h) ST_WD_EN ST_WD_EN ST_VBBAT ST_JHIRQ ST_JHIRQ ST_JHIRST ST_ACTSLP	OLR OLR	1 0 7 6 5 4 3	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST NPWR_BTN NPWR_BTN NEM_PD ACTSHDN	018 018]	EN4 EN5
If Pin not mapped (Nor If Pin is mapped to one sequence) within the the Pins 13 (CLK32OE) 19 (EN1) 20 (EN2)	e of the time slot[1: ime slot where 1st i Power t 4th 1st 1st	15], pin will be up is first up (or down s first up (or down yp P y 4th y 5th y 1st y 4th	Power-up/Sleep- i, and 15th is last ower Down	exit sequence), or do up (or down). Sleep None Ist	Exit V	Sleep En ne ne	r itry V V V	1 0 5 7 6 5 4 3 2	F_OSC F_NRSTIRQ atus Register - Contr T_STAT (13h) ST_WD_EN ST_VBBAT ST_NURQ ST_JIRST ST_ATSLP AT_ACTSHDN	01	1 0 7 6 5 4 3 2	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST NFWR_BTN NEM_PD ACTSHDN WDT_SHDN			EN4 EN5 EN6 EN7
If Pin not mapped (Nor If Pin is mapped to one sequence) within the tr Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3) 22 (EN4)	e of the time slot[1: ime slot where 1st i Power t 4th 1st 1st 2nd 2nd	15), pin will be up is first up (or down Jp P P V 4th V 5th V 1st V 4th V 4th	Power-up/Sleep- i, and 15th is last ower Down	exit sequence), or do up (or down). Sleep None Ist 3rd None	Exit	Sleep En ne ne d	xtry V V V V	1 0 5 7 6 5 4 3 2	F_OSC F_NRSTIRQ tus Register - Contro T_STAT (13h) ST_WD_EN ST_WD_EN ST_VBBAT ST_JHIRQ ST_JHIRQ ST_JHIRST ST_ACTSLP	01	1 0 7 6 5 4 3	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST NFWR_BTN NEM_PD ACTSHDN WDT_SHDN			EN4 EN5 EN6 EN7
If Pin not mapped (Nor If Pin is mapped to one sequence) within the tr Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3)	e of the time slot[1: ime slot where 1st i Power t 4th 1st 1st 2nd	15], pin will be up is first up (or down s first up (or down yp P y 4th y 5th y 1st y 4th	Power-up/Sleep- i, and 15th is last ower Down	exit sequence), or do up (or down). Sleep None None 1st 3rd	Exit V	sleep entry sleep En ne d	xtry V V V V V	1 0 5 7 6 5 4 3 2	F_OSC F_NRSTIRQ atus Register - Contr T_STAT (13h) ST_WD_EN ST_VBBAT ST_NURQ ST_JIRST ST_ATSLP AT_ACTSHDN	01	1 0 7 6 5 4 3 2	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST NPWR_BTN NPWR_BTN NFM_BTN WDT_SHDN 0 00b: Normal ACT/SHD			EN4 EN5 EN6

Figure 5-13. TPS38700 GUI Window - Sequence Config Tab



5.3 GUI

This section shows the graphical user interface (GUI) to use to interact with the EVM. This was originally designed for the TPS38700-Q1, but all GUI functionality is applicable for the TPS38700S-Q1. Refer to the TPS38700-Q1 Multichannel I2C Programmable Voltage Sequencer data sheet for details on the register description of the device.

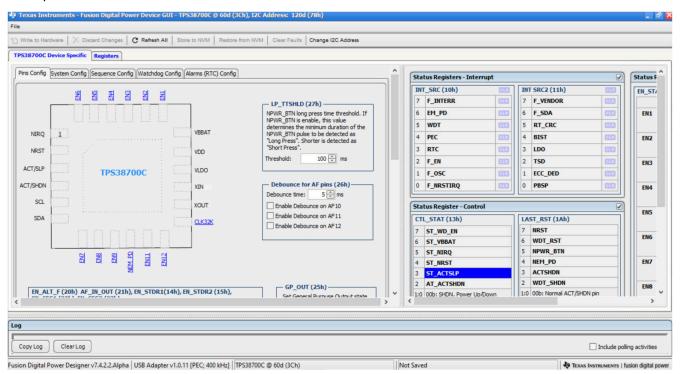


Figure 5-14. Main GUI Screen

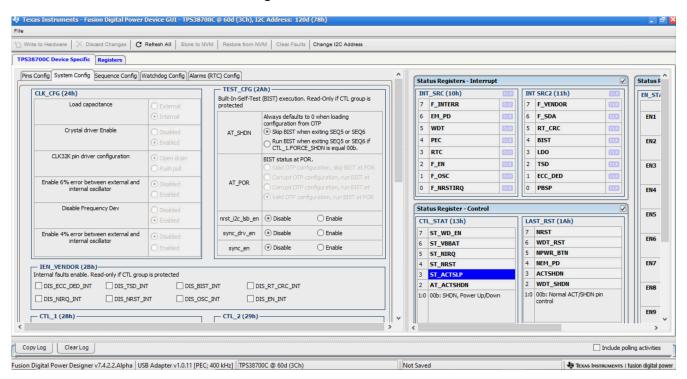


Figure 5-15. System Config

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TPS38700-Q1 GUI instructions

Config System Config	g Sequence Confi	ig Watchdog Confi	g Alarms (RTC) C	onfig				^ G	tatus Registers	Interrunt				Statu
Time Config									NT SRC (10h)	our		NT 5RC2 (11h)		EN_S
250 🗸									7 F_INTERR	OLR		F_VENDOR	GLR	
Time slot between sec	quencing points =	TIME[7:0] * SSTER	+ T_min, where T	Γ_min = 125 μs				6	5 EM_PD	OLR	e	F_SDA	OLR	EN
	TIME[7:	:0] Min (-6%)	Typical	Max (+6%)					5 WDT	OLD	5	RT_CRC	GLR	
Power-up / Sleep-ex	dt 2	587.5	625.0 💭	662.5	μs			4	4 PEC	GLR	4	BIST	OLR	EN
Power-down / Sleep	entry 2	\$ 587.5	625.0 💭	662.5	μs			3	3 RTC	GLR	3	B LDO	OLR	
									2 F_EN	OLE	2	2 TSD	OLR	EN
Pins mapping If Pin not mapped (No	one), pin maintain p	previous state, unle	ss entering BACKU	JP or FAILSAFE st	ate, in these tw	o states, pin is	pulled Low.		1 F_05C	OLR		ECC_DED		EN
	ne of the time slot[[1:15], pin will be up	Power-up/Sleep-	exit sequence), or					1 F_OSC 0 F_NRSTIRQ	(OLR	-111-	ECC_DED	810 810	EN:
If Pin not mapped (No If Pin is mapped to on	ne of the time slot[[1:15], pin will be up st is first up (or dow	Power-up/Sleep-	exit sequence), or up (or down).			try		1 F_OSC 0 F_NRSTIRQ tatus Register -	(OLR		ECC_DED PBSP		
If Pin not mapped (No If Pin is mapped to on sequence) within the Pins	ne of the time slot[time slot where 1s Power	[1:15], pin will be up st is first up (or down r Up	Power-up/Sleep- n), and 15th is last	exit sequence), or up (or down).	eep Exit	down/Sleep-en	try Entry	S	F_OSC F_NRSTIRQ tatus Register - TL_STAT (13h)	(OLR		AST_RST (1Ah)	810 810	EN4
If Pin not mapped (No If Pin is mapped to on sequence) within the Pins 13 (CLK320E)	e of the time slot[time slot where 1s Power 4th	1:15], pin will be up st is first up (or down r Up	o (Power-up/Sleep-in), and 15th is last Power Down	exit sequence), or : up (or down).	eep Exit	down/Sleep-en Sleep None	Entry		- - 1 F_05C > F_NRSTIRQ tatus Register - - TL_STAT (13h) - ' ST_WD_EN	(OLR		AST_RST (1Ah)	810 810	EN4
If Pin not mapped (No If Pin is mapped to on sequence) within the Pins 13 (CLK320E) 19 (EN1)	Power 4th 1st	1:15], pin will be up t is first up (or down r Up v 4th v 5th	o (Power-up/Sleep n), and 15th is last Power Down	exit sequence), oi : up (or down).	r down (Power- eep Exit	down/Sleep-en Sleep None None	Entry	SI C	- F_05C > F_NRSTIRQ tatus Register - - TL_STAT (13h) - ST_WD_EN - ST_VBBAT -	(OLR		AST_RST (1Ah) WDT_RST	810 810	EN4
If Pin not mapped (No If Pin is mapped to on sequence) within the Pins 13 (CLK320E)	e of the time slot[time slot where 1s Power 4th	1:15], pin will be up st is first up (or down r Up	o (Power-up/Sleep-in), and 15th is last Power Down	exit sequence), or : up (or down).	r down (Power- eep Exit	down/Sleep-en Sleep None	Entry	SI 6 5 4	F_OSC F_OSC F_NRSTIRQ TL_STAT (13h) / ST_WD_EN is ST_VBBAT is ST_NIRQ	(OLR	L 7 6 5 4	ECC_DED PBSP AST_RST (1Ah) INRST WDT_RST NPWR_BTN NEM_PD	810 810	EN4
If Pin not mapped (No If Pin is mapped to on sequence) within the Pins 13 (CLK320E) 19 (EN1)	Power 4th 1st	1:15], pin will be up t is first up (or down r Up v 4th v 5th	Power-up/Sleep- n), and 15th is last Power Down	exit sequence), oi : up (or down).	r down (Power- eep Exit	down/Sleep-en Sleep None None	Entry	SI 6 5 4 3	F_OSC F_OSC F_NRSTIRQ tatus Register - TL_STAT (13h) ST_WD_EN ST_WBAT ST_NRST ST_NRST ST_NRST ST_ACTSLP	Control	1 0 7 6 5 4 3	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST INPWR_BTN NEM_PD ACTSHDN	810 810	EN4 EN3
If Pin not mapped (No If Pin is mapped to on sequence) within the Pins 13 (CLK320E) 19 (EN1) 20 (EN2)	e of the time slot[Power 4th 1st 1st	1:15], pin will be up st is first up (or down r Up V 4th V 5th V 1st	o (Power-up/Sleep-in), and 15th is last Power Down	exit sequence), or : up (or down).	r down (Power- eep Exit	down/Sleep-en Sleep None None 3rd	Entry	SI 7 6 5 8 7 7 6 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	F_OSC F_OSC F_NRSTIRQ TL_STAT (13h) / ST_WD_EN is ST_VBBAT is ST_NIRQ	Control	L 7 6 5 4 3 2	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST INPWR_BTN NEM_PD ACTSHDN		EN4 EN3
If Pin not mapped (No If Pin is mapped to on sequence) within the Pins 13 (CLK320E) 19 (EN1) 20 (EN2) 21 (EN3)	e of the time slot f time slot where 1s Power 4th 1st 2nd	1:15], pin will be up st is first up (or down r Up V 4th V 5th V 1st V 1st	b (Power-up/Sleep- n), and 15th is last Power Down n v t v n v t v	exit sequence), or : up (or down). Site None Ist 3rd	r down (Power- eep Exit v v	down/Sleep-en Sleep None None 3rd 2nd	Entry V	SI 7 6 5 8 7 7 6 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8	F_OSC F_OSC F_NRSTIRQ tatus Register - TTL_STAT (13h) ST_WD_EN ST_WBAT ST_NRST ST_NRST ST_ACTSLP AT_ACTSHD	Control	L 7 6 5 4 3 2	ECC_DED PBSP AST_RST (1Ah) NRST WDT_RST NPWR_BTN NEM_PD ACTSHON WDT_SHON		EN4 EN5 EN6

Figure 5-16. Sequence Config

WDT (80h:83h) MODE On expires, first interrupt, then reset, then power-down according the Power-Down Mode On expires, first interrupt, then reset, then power-down according the Power-Down Mode On expires, then reset, then power-down according the Power-Down Mode On expires, then reset, then power-down according the Power-Down Mode Automatic disable in sleep mode Automatic disable in sleep mode	Status Registers - Interrupt INT SRC (10h) INT SRC2 (11h) INT SRC (10h) 7 F_UNTERR 000 7 F_UNT SRC2 (10h) 000 6 EH_PD 000 5 RT_CRC 000 5 WDT 000 5 RT_CRC 000	Status EN_ST
Disabled On expires, first interrupt, then reset, then power-down according the Power-Down Mode On expires, then reset, then power-down according the Power-Down Mode On expires, power-down according the WDT_CFG.PDMD	7 F_INTERR 000 7 F_VENDOR 000 6 EM_PD 000 6 F_SDA 000	
Oisabled automatically in sleep mode Enabled in sleep mode Delay from POR (or from value written to WDT_CFG.WDTEN) to first open window Delay of 1 WDT period	4 PEC GE 3 RTC GE 2 F_EN GE 1 F_OSC GE 0 F_NRSTIRQ GE Status Register - Control GE	EN2 EN3 EN4
WDT period 2 Power-Down Mode for WDT force power-down • • Normal ACT/SHDN pin control • • Force power-down sequence, then resume normal ACT/SHDN pin control immediately • • Force power-down sequence, then resume normal ACT/SHDN pin control after 1 sec delay • • Force power-down sequence, then resume normal ACT/SHDN pin control when ACT/SHDN is Low, or when RTC alarm occurs as • Force power-down sequence, then resume normal ACT/SHDN pin control when ACT/SHDN is Low, or when RTC alarm occurs as • Force power-down in CT_2, RTC_T, and RTC_A Key to reset WDT 0 😇	CTL_STAT (13h) LAST_RST (1Ah) 7 ST_WD_EN 7 6 ST_VBBAT 6 5 ST_NIRQ 6 4 ST_NRST 3 3 ST_ACTSLP 3 2 AT_ACTSHON 2 1:0 00b: SHDN, Power Up/Down 1:0	EN5 EN6 EN7 EN8 EN9

Figure 5-17. Watchdog Config



TPS38700-Q1 GUI instructions

Ø Texas Instruments - Fusion Digital Power Device GUI - TP538700C @ 60d (3Ch), I2C Address: 120d (78h) File		_ 2 2
Withe to Hardware X Discard Changes C Refresh All Store to NVM Restore from NVM Clear Faults Change I2C Address		
TP538700C Device Specific Registers		
Pins Config System Config Sequence Config Watchdog Config Alarms (RTC) Config	Status Registers - Interrupt	Status F
Alarm	INT_SRC (10h) 018 INT SRC2 (11h) 018	EN ST
Disable Alarm	7 F_INTERR 018 7 F_VENDOR 018	
CTL_2.RTC_WAKE and CTL_2.RTC_PU are clear; RTC_A[31:0] are set to 0xFFFFFFFF.	6 EM_PD 018 6 F_SDA 018	EN1
Alarm to assert NIRQ for interrupt based wake CTL_2.RTC_WAKE and CTL_2.RTC_PU are dear; RTC_A[31:0] are set to value different than 0xFFFFFFFFF. When RTC_T[31:0] is	5 WDT 000 5 RT_CRC 000	
equal RTC_A[31:0], PSEQ interrupts MCU; MCU asserts either ACT/SLP or ACT/SHDN	4 PEC 013 4 BIST 010	EN2
Autonomous wake from sleep. PSEQ ransitions from SLEEP -> ACTIVE CTL_2.RTC_WAKE is set. When RTC_T[31:0] is equal RTC_A[31:0], an interrupt is asserted, INT_SRC.RTC status bit and	3 RTC 013 3 LDO 019	Line
CTL_1.FORCE_ACT bit are set. As a result of interrupt, the processor wakes, determines cause of interrupt, deasserts ACT/SLP,	2 F EN 013 2 TSD 013	EN3
and dars CTL_1.FORCE_ACT O Autonomous wake from shutdown. PSEQ transitions from SHDN2 ->ACTIVE	1 F OSC 003 1 ECC DED 003	EN3
Requires a software shutdown and ACT/SHDN remains asserted. Processor set CTL_2.PU, then set CTL_1.SHDN to 11b. The		
PSEQ is forced into shutdown mode until RTC_T[31:0] is equal RTC_A[31:0], or ACT/SHDN de-asserted and re-asserted by the system.	0 F_NRSTIRQ 013 0 PBSP 013	EN4
RTC_T [70h:73h] RTC_A [74h:77h]	Status Register - Control	
Value at POR = 0x00000000. Value at POR = 0xFFFFFFF	CTL_STAT (13h) LAST_RST (1Ah)	EN5
Total seconds 241 💭 0x000000F1 sec Total seconds 4,294,967,295 💭 0xFFFFFFF sec	7 ST WD EN 7 NRST	
0 ♥ days 0 ♥ h 4 ♥ min 1 ♥ sec 49,710 ♥ days 6 ♥ h 28 ♥ min 15 ♥ sec	6 ST_VBBAT 6 WDT_RST	EN6
	5 ST_NIRQ 5 NPWR_BTN	
Read Write	4 ST_NRST 4 NEM_PD	EN7
	3 ST_ACTSLP 3 ACTSHDN	
	2 AT_ACTSHDN 2 WDT_SHDN	EN8
	1:0 00b: SHDN, Power Up/Down 1:0 00b: Normal ACT/SHDN pin control	
		EN9
		V
< >	> <	>
CopyLog	Indude poli	ing activities
usion Diaital Power Designer v7.4.2.2.Alpha USB Adapter v1.0.11 (PEC: 400 kHz1 TPS38700C @ 60d (3Ch)	Not Saved	usion digital power

Figure 5-18. Alarms Config

le												
Write to Hardwa	are 🛛 🗙 Discard Changes 📔	C Refresh All St	ore to NVM Resto	re from NVM	Clear Fau	ults Change	e I2C Addres	5				
P538700C Dev	vice Specific Registers											
<u>1 2 3 </u>										Clear	Status	Refresh All Write All
Code 👻	Register Name	= Group =	Value (Hex)				В	it Fields				Poll =
				0	0	0	0	0	0	0	0	
							c	LOSE				
)x81	WDT_CLOSE	WDT	0x00	7	<i>6</i>	5	4	3	2	1	<i>o</i> 0	Refresh Write
				U	U	U	0	U	U	U	U	
							WOT	LOPEN				
0x82	WDT_OPEN	WDT	0x00	7	6	5	4	3	2	1	0	Refresh Write
							WD	п_кеу				
0x83	WDT_KEY		0x00	7	6	5	4	3	2	1	0	Refresh Write
				0	0	0	0	0	0	0	0	
				RSVD	WRK	SEQS	SBQP	SEQC	WDT	RTC	CTL	
0xF0	PROT0	PROT	0x00	7	6 0	5	.≁ []	3	2	1	0	Refresh Write
)xF1	PROT1	PROT	0x00	RSVD	WRK 6	seqs	SEQP 4	seqc	wот 2	RTC	CTL .	Refresh Write
JXF1	PROTI	PROT	0,00	7	Ô	0	Ū	3	í d	1	0	
												``
11												
Copy Log	Clear Log											Include polling activitie

Figure 5-19. Registers



6 Hardware Design Files

6.1 Schematic

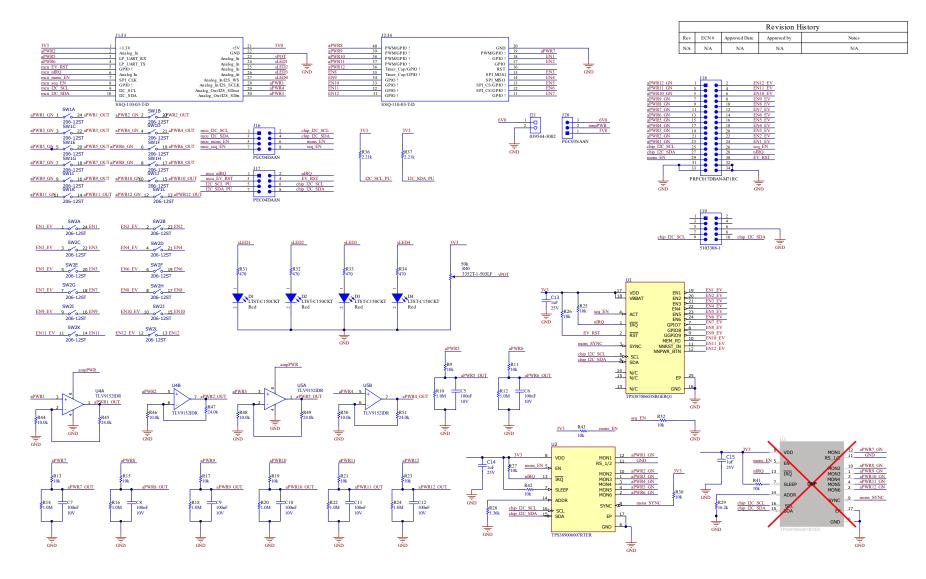


Figure 6-1. TPS389387EVM Schematic



6.2 PCB Layout

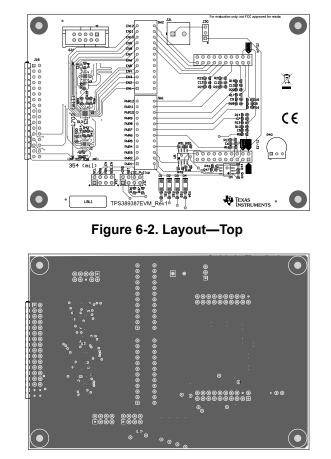
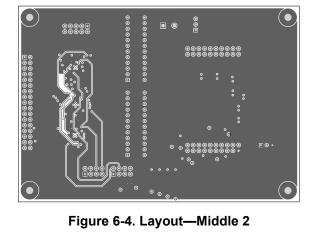


Figure 6-3. Layout—Middle 1





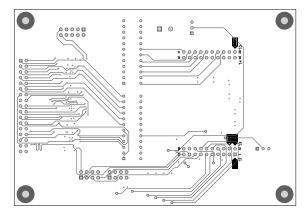


Figure 6-5. Layout-Bottom



6.3 Bill of Materials

Table 6-1. Bill of Materials

. .			of Materials				
Designator	Qty	Description	Comment	Footprint	LibRef		
C5, C6, C7, C8, C9, C10, C11, C12	8	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603	C0603X104K8RACTU	0603	CMP-0006981-4		
C13, C14, C15	3	1 μF ±10% 25 V Ceramic Capacitor X5R 0603 (1608 Metric)	GRM188R61E105KAA DD	FP- GRM188R61E105KA ADD_0603-MFG	CMP-0094239-1		
D1, D2, D3, D4	4	LED, Red, SMD	LTST-C150CKT	LTST-C150CKT_Red	CMP-0003043-3		
J1/J3	1	Receptacle, 2.54mm, 10x2, Tin, TH	SSQ-110-03-T-D	BoosterPack_40pin_J 1J3	CMP-0003837-4		
J2/J4	1	Receptacle, 2.54mm, 10x2, Tin, TH	SSQ-110-03-T-D	BoosterPack_40pin_J 2J4	CMP-0078266-4		
J16, J17	2	Header, 100mil, 4x2, Tin, TH	PEC04DAAN	CONN_PEC04DAAN	CMP-0054542-2		
J18	1	Header, 100mil, 17x2, Gold, R/A, TH	TSW-117-08-G-D-RA	Sullins_PRxC017DBA N-M71RC	CMP-0054606-1		
J19	1	Header (shrouded), 100mil, 5x2, Gold, TH	5103308-1	CONN_5103308-1	CMP-0054834-2		
J20	1	Header, 100mil, 3x1, Tin, TH	PEC03SAAN	CONN_PEC03SAAN	CMP-0002338-1		
J21	1	Terminal Block, 5.08mm, 2x1, TH	039544-3002	Molex_039544-3002	CMP-0055345-1		
R9, R11, R13, R15, R17, R19, R21, R23, R25, R26, R27, R30, R41, R42, R43, R52	16	RES, 10 k, 5%, 0.1 W, 0603	RC1608J103CS	0603	CMP-0025945-3		
R10, R12, R14, R16, R18, R20, R22, R24	8	RES, 1.0 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031M00JNEA	0603	CMP-0025736-4		
R28	1	RES, 5.36 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06035K36FKEA	0603	CMP-0022511-4		
R29	1	RES, 16.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060316K2FKEA	0603	CMP-0022079-4		
R31, R32, R33, R34	4	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603470RJNEA	0603	CMP-0025813-4		
R36, R37	2	RES, 2.21 k, 0.1%, 0.1 W, 0603	RT0603BRD072K21L	0603	CMP-0024063-3		
R40	1	Trimming Potentiometer, 50K, 0.5W, TH	3352T-1-503LF	Bourns_3352T	CMP-0001777-2		
R44, R46, R48, R50	4	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0FKEA	0603	CMP-0021998-4		
R45, R47, R49, R51	4	RES, 24.0 k, 1%, 0.1 W, 0603	RC0603FR-0724KL	0603	CMP-0022945-5		
SW1, SW2	2	Dip Switch SPST 12 Position Through Hole Slide (Standard) Actuator 50 mA 24VDC	206-12ST	FP-206-12ST_DIP24- MFG	CMP-0086642-1		

Table 6-1. Bill of Materials (continued)							
Designator	Qty	Description	Comment	Footprint	LibRef		
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9	9	Shunt, 2.54mm, Gold, Black	60900213421	Shunt, 2.54mm, Black			
U1	1	ASIL-A Multichannel I2C Programmable Voltage Sequencer	TPS38700603SRGER Q1	VQFN24			
U2	1	SIL-3 Multichannel Overvoltage and Undervoltage I2C Programmable Voltage Supervisor and Monitor	TPS389006007RTER	WQFN16			
U4, U5	2	General Purpose Amplifier 2 Circuit Rail-to-Rail 8-SOIC	TLV9152IDR	D0008A-MFG	CMP-0091916-1		

7 Additional Information

Warning - External Connections: All external connections to the hardware must stay within the recommended operating conditions and intended usage for all hardware/components connected in the system.

7.1 Related Documentation

TPS38700S-Q1 data sheet: TPS38700S-Q1 Multichannel I2C Programmable Voltage Sequencer

TPS389006 data sheet: TPS389006 Multichannel I2C Programmable Voltage Supervisor and Monitor

MSP-EXP430FR2355: MSP430FR2355 LaunchPad™ development kit

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8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

С	hanges from Revision * (October 2023) to Revision A (February 2024)	Page
•	Added the TPS3839387EVM zip file link containing the .C code	1

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User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

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3.1.1 Notice applicable to EVMs not FCC-Approved:

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3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

- 3.3 Japan
 - 3.3.1 Notice for EVMs delivered in Japan: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に 輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 Notice for Users of EVMs Considered "Radio Frequency Products" in Japan: EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧くださ い。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html
- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 EVM Use Restrictions and Warnings:

- 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
- 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
- 4.3 Safety-Related Warnings and Restrictions:
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and inability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
- 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
- 5. Accuracy of Information: To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
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