TMS470R1x F05 Flash Reference Guide

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Texas Instruments

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Post Office Box 655303 Dallas, Texas 75265

REVISION HISTORY

REVISION	DATE	NOTES
B	9/05	Updates: Page 6, information on number of wait states and maximum device speed added. Page 17, information on device endian configuration removed. Page 18, bit 5 of FMREGOPT (data path test write enable) defined. Page 19, information on pipeline mode when operating above the maximum frequency for standard read mode added. Page 19, note title corrected. Page 21, information on minimum delay added. Page 21, typo corrected in the name of FMBAC2 register bits 7:4. Page 22, typo corrected (active changed to standby). Page 22, information on minimum delay added. Page 22, WAIT[7:4] and WAIT[3:0] bit values changed to indicate four digits. Page 24, PSLEEP[14:0] reset value indicated as device-specific. Page 24, information on minimum delay added. Page 25, PSTDBY[10:0] reset value indicated as device-specific. Page 25, information on minimum delay added. Page 28, added section 5.3 Page 29, added section 5.4

Contents

MCU F05 Flash Module

The flash electrically erasable programmable read-only memory (flash EEPROM, or flash) module is a type of nonvolatile memory which has fast read access times but slower write and erase times. Flash EEPROM performs erasing by sector, rather than word at a time as in regular EEPROM.

Topic **Page**

1 Overview

The MCU F05 flash module is generally used to provide permanent program/ data storage or factory calibration data; and can be programmed and electrically erased many times to allow for faster code development.

Flash EEPROM differs from standard EERPOM in that all bits in a flash sector are erased in bulk, whereas standard EEPROM is erased a word at a time.

1.1 Features

- ❏ Supports multiple flash banks for program and data storage.
- ❏ Contains up to 8 banks of up to 16 Megabits each
- ❏ Enables simultaneous read access on a bank while performing a write or erase operation on any one of the remaining banks.
- ❏ Supports erase and program suspend, which allows software to fetch data from the flash bank currently being erased or programmed.
- ❏ Supports automating flash erase and programming through integrated state machine
- ❏ Allows up to 32 sectors per flash bank
- ❏ Provides optional set of four 32-bit protection keys.
- ❏ Provides built-in power mode control logic.

1.2 Definition of Terms

Terms used in this document have the following meanings:

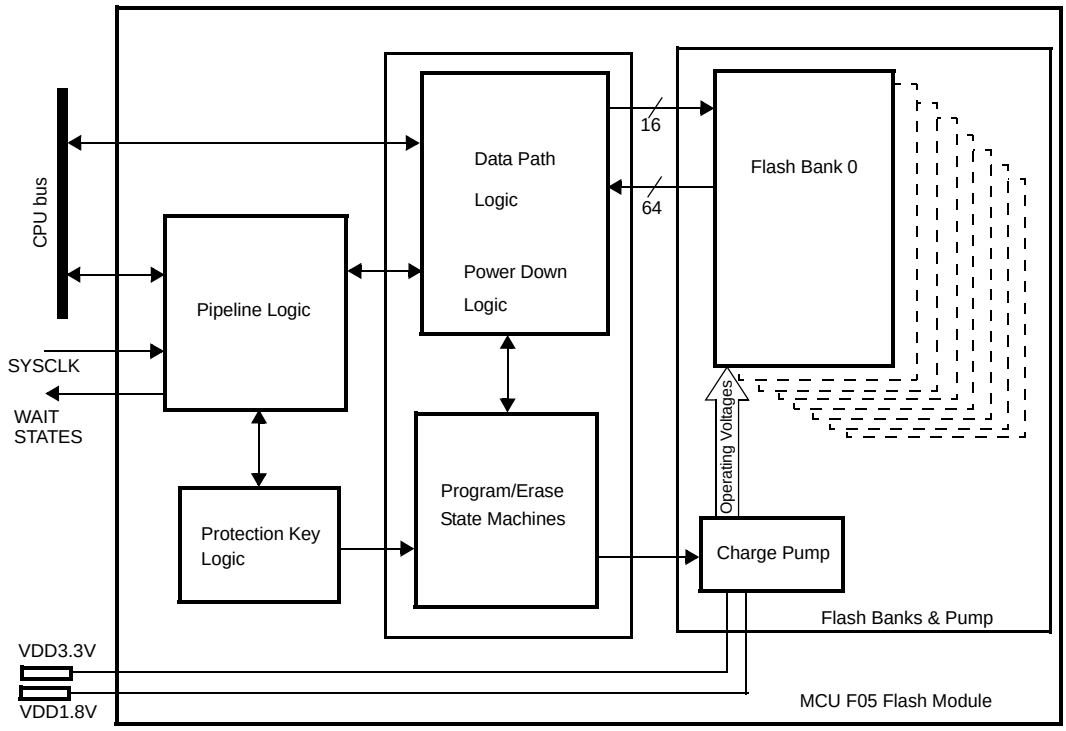
- ❏ BAGP (bank active grace period): Time (in SYSCLK cycles) from the most recent flash access of a particular bank until that bank enters fallback power mode. This reduces power consumption by the flash: however, it can also increase access time.
- ❏ Charge pump: Voltage generators and associated control (logic, oscillator, and bandgap, for example).
- ❏ CSM (command state machine): One of the three state machines present in the flash module.
- ❏ Fallback power mode: The power mode (active, standby or sleep, depending on which mode is selected) into which a bank or the charge pump falls back each time the active grace period expires.

- ❏ Flash bank: A group of flash sectors which share input/output buffers, data paths, sense amplifiers, and control logic.
- ❏ Flash module: Flash banks, charge pump, power and mode control logic, data path, wait logic, and write/erase state machines.
- ❏ MCU F05 flash module: Flash module and CPU interface which includes pipeline logic and protection logic.
- ❏ OTP (one-time programmable): A program-only-once flash sector (cannot be erased)
- ❏ PAGP (pump active grace period): Time (in SYSCLK cycles) from when the last of the banks have entered fallback power mode until the pump enters a fallback power mode. This can reduce power consumption by the flash; however, it can also increase access time.
- ❏ Pipeline mode: The mode in which flash is read 64 bits at a time, giving faster apparent access times.
- ❏ Sector: A contiguous region of flash memory which must be erased simultaneously due to physical construction constraints.
- ❏ Standard read mode: The mode assumed when the pipeline mode is not enabled and flash is read no more than 32 bits at a time.

2 Functional Block Diagram

The MCU F05 flash module consists of several major functional elements as shown in Figure 1.

Figure 1. F05 Flash Module Functional Block Diagram



Up to eight banks of flash can be present in a single flash module. The present design supports up to 32 sectors per bank.

State machines in the flash module perform program, erase, and verify operations. The state machines permit the use of simpler program/erase/ verify software algorithms.

A single charge pump can supply all required voltages for up to eight flash banks. The MCU F05 flash module requires 1.8V and 3.3V power supplies for normal operation. Program and erase operations do not require any additional power supply.

The pipeline logic speeds up the apparent read access time of the flash module.

Programming the power-down logic correctly can produce significant power savings. The power-down registers control the power mode for each bank individually as well as for the charge pump.

The entire module is protected from unauthorized erasures or writes when the optional four 32-bit protection key words are used.

3 Operation

The following sections discuss various issues related to reset, reading, erasing, programming, power mode, protection, and wait state generation.

3.1 Reset State

The reset state exhibits the following properties:

1) Wait states are set to 15
2) Pipeline mode default is device specific
3) The OTP sector is turned off
4) All levels of protection are enabled
5) Power modes are set to *Active* (no power savings)

Your boot code must initialize the wait states and the desired pipeline mode to achieve the best possible system performance.

3.2 Flash Read Modes

In addition to *standard read mode*, the flash module also has *pipeline mode*, which affects the technique used to fetch the next memory word. Using this mode correctly increases clock speeds and CPU throughput.

3.2.1 Standard Read Mode

Standard read mode is defined as the mode in effect when pipeline mode is inactive. The number of wait states should be set to zero in the flash control register FMBAC2.7:0. The maximum speed of the device in standard read mode is device specific. It is typically 24MHz.

3.2.2 Pipeline Mode

In *pipeline mode*, two words are read in parallel from the flash core. Storing these two words in pipeline data buffers increases the bandwidth of the data coming out of the flash core, which provides effectively zero wait states on as many accesses as possible.

In pipeline mode, the flash data is always latched into the pipeline buffer first, then read from the pipeline buffer to the CPU. Pipeline mode removes the flash memory access time from the critical timing path, which allows the clock frequency to be higher.

Pipeline mode is enabled by setting the ENPIPE bit within the flash control register FMREGOPT.0. The number of wait states should be set to one in pipeline mode. The pipeline mode default is device specific.

3.3 Flash Commands

The MCU F05 flash module should be programmed, erased and verified only by using the F05 Flash API Library Functions. These functions are written, compiled and validated by Texas Instruments. The information provided in this document is intended to help explain how these functions work. It is not intended to provide sufficient detail for implementing programming or erasing functions.

The flash module contains a Command State Machine (CSM) to perform program, erase, and validate operations. The CSM supports the commands shown in Table 1. At the end of a system reset, the CSM is in Idle mode. The completion of any command also returns the CSM to Idle mode.

Table 1. Flash Command Summary

Command Operand	Description	Write Cycles Required
0x0010	Program	2
0x0020	Erase Sector	2
0x0040	Clear Status Register	1
0x0080	Suspend (program or erase)	1
0x0200	Resume Programming	1
0x0400	Resume Erasing	1
0x0800	Program OTP	2
0x1000	Validate Sector	2

Command writes (as well as OTP reads) can be performed only when pipeline mode is off. This is necessary to prevent data stored in the pipeline buffers from becoming inconsistent with the data stored in memory. For this reason, entering configuration mode disables pipeline mode.

The program, erase, and validate sector commands require two write cycles, whereas the remaining commands require only one write cycle.

After a program, erase, or validate sector command has been written to the flash module, the module waits indefinitely for the second write cycle to latch the address and/or data; therefore, the valid data write cycle must have valid data, whether it immediately follows the command or not.

The control port can be used to read or write registers, or bank reads can be performed between the command and the data for the program or erase command.

The BUSY status bit becomes active upon receipt of any command except for the clear status command.

After an erase or program command has been issued, the operation cannot be aborted except by resetting the flash module. The operation can, however, be allowed to complete or be suspended. A suspended operation, likewise, can only be aborted by resetting the flash module.

3.3.1 CPU Operations Required for Executing Commands

Before the MCU F05 flash module can execute a command, the host CPU must do the following:

1) Set the bit GLBCTRL4 of the GLBCTRL register (in the System module) to enable writing to the flash registers
2) Select the desired bank to be programmed by writing BANK[2:0] of FMMAC2
3) Select one or more bits in FMBSEA or FMBSEB to disable Level 1 protection for the particular sector to be erased/written
4) Write the correct four 32-bit FMPKEY words (if applicable)
5) Clear the READOTP bit in the FMREGOPT register
6) Write an operand, as shown in Table 1, to any location in flash memory which initiates the operation

For operations that apply to specific address locations (program, erase, and validate) the host must also:

7) Write the desired data half-word to the appropriate address in the selected flash bank

After these operations have been completed in sequence, the command is performed. These flash commands are described in the following sections in more detail.

3.3.2 Program Sector Command

If not already set up, the host must follow the procedure outlined in Section 3.3.1 above. Writing the program operand, as shown in Table 1, to any location in flash memory initiates the program operation. This must be followed by writing the desired data half-word to the appropriate address in the selected flash bank.

Note: Program Data to the Flash Module in Half-Words

All data programmed into the MCU F05 flash module must be done one half-word (16 bits) at a time.

The flash module checks the sector protection status and, if allowed, proceeds to program and verify the data. Once the command is received, the busy flag is held active.

While the busy flag is active, the flash module responds only to the suspend command. If an attempt is made to read a bank being programmed, invalid data is returned. Reads may be performed correctly on other banks. If the program operation is suspended and the suspended bank is read, then only data other than the address that was being programmed should be assumed valid.

If the program operation is suspended, the busy flag becomes inactive within 2.0μs of receiving the suspend command.

During the program operation, 3.3V V_{DD} must remain within the appropriate range; otherwise, the error flag 3VSTAT is set in the status register FMMSTAT.3.

When the program command is complete, the user should parse the Status register to verify that the command was successful. Upon completion, the flash module resets the CSM state to Idle mode; therefore, the program command must be reissued before another half-word is written to flash memory.

3.3.3 Erase Sector Command

If it is not already set up, the host must follow the procedure outlined in Section 3.3.1. Writing the erase operand, as shown in Table 1, to any location in flash memory, initiates the erase operation. This is followed by writing any data to the selected sector address (an address anywhere within the sector to be erased), in the flash memory.

The flash module checks the sector enable status and, if allowed, proceeds to erase and verify the data. Once the command is received, the busy flag is held active.

While the busy flag is active, the flash module responds only to the suspend command. If an attempt is made to read a bank being erased, invalid data is returned. Reads can be performed on other banks. If the erase operation is suspended and the suspended bank is read, then the entire sector's data is assumed invalid. Read data from other sectors and banks is invalid due to the partial erasure of this sector.

If the erase operation is suspended, the busy flag becomes inactive within 2.0μs of receiving the suspend command.

Upon completion of the erase command, the user should parse the Status register to verify that the command was successful.

During the erase operation, 3.3V V_{DD} must remain within the appropriate range; otherwise, the error flag 3VSTAT is set in the status register FMMSTAT.3.

When the erase operation is complete, the flash module resets the CSM state to Idle mode; therefore, the erase command must be reissued before another sector can be erased.

3.3.4 Suspend/Resume Commands

The suspend command allows erase or program operations, whichever is active, to be suspended so other operations can be performed on the affected bank. It is also possible to suspend a program operation so that a sector in a different bank can be erased, or suspend an erase operation so that information may be programmed in a different bank. The suspend command is acted upon only if the BUSY bit of FMMSTAT is high and the flash module is performing an erase or program operation. Issuing a suspend command when BUSY is low has no effect on the flash module.

Note: Flash Module Ignores All But Suspend Command When BUSY Bit is High

If a command other than suspend is issued while the BUSY bit is high, it is ignored.

It is possible to suspend an operation at certain points in the operation of the state machine so that the operation actually finishes and the suspend flags are never set. Issuing a resume command when suspend is not active has no effect on the flash module.

Only one operation can be active at a time. Also, a program operation cannot be initiated while a previous program operation is suspended, and an erase operation cannot be initiated while a previous erase operation is suspended. The flash module ignores any command that violates these conditions.

3.3.5 Clear Status Command

The Status register allows the user to determine whether an erase/program operation is successfully completed, in progress, suspended, or failed.

If not already set up, the host must follow the procedure outlined in Section 3.3.1. Writing the clear status operand, as shown in Table 1, to any location in flash memory, executes the clear status operation.

If the BUSY bit is low, this operation clears the following status bits: SLOCK (sector locked), CSTAT (command status), 3VSTAT (3.3V V_{DD} status), INVDAT (invalid program data) in the FMMSTAT register.

3.3.6 Program OTP Command

The flash module may have one or more OTP sectors, up to one OTP sector per flash bank. A minimum of one is required for production and test purposes. Each OTP sector contains 2K bytes. The bits can be programmed via the program OTP command. Once the command is issued, the bank identifier, address within the OTP sector, and the data must be specified.

The program OTP flow is the same as the program half-word flow. It can be suspended and resumed.

3.3.7 Validate Sector Command

A validate sector command has been provided to enable the host to determine if a sector contains depleted bits. A depleted bit may occur only in the unlikely event that an erase operation has been started, but not completed. The following conditions could leave depleted bits in a sector:

- ❑ An erase is in progress when power is removed
- ❑ An erase suspend is active when power is removed
- ❑ A flash module reset interrupts an erase operation
- ❑ A flash module reset occurs while an erase suspend is active

After a flash module reset, including power up, the host should perform a validation check on sectors which may have been corrupted to check that no sectors contain depleted bits. It is not required to check sectors which are not programmed in the field, as they cannot have depleted bits. It is, however, possible for depleted bits in one sector to cause bits in another sector to read incorrectly; therefore, it is vital that depleted bits be corrected.

Note: There Is No Suspend for the Validate Sector Command

The *validate sector* command cannot be suspended.

3.4 Data Security

Data security against either accidental or deliberate access by unauthorized agents is built into the flash module in two levels of data security: Level 1 security allows each sector to be individually protected from any access other than read; level 2 security protects the entire module from non-read access using four optional 32-bit protection keys.

3.4.1 Sector Enable

Sector enable (registers BSEA and BSEB) is a means of preventing data from being modified within a sector. Since the flash module may store permanent and/or semi-permanent program code and/or data this capability is provided. A sector is protected if data within that sector is prevented from being modified (the sector-enable bit for that sector is cleared). Currently the MCU F05 flash module supports a maximum of 32 sectors per bank.

Flash memory can be programmed or erased only if the specified sector is enabled. If the sector is protected, then the state machine of the flash module halts and sets the status bit SLOCK in FMMSTAT.0.

At power up, all of the sector-enable bits are initialized so that the flash memory location cannot be modified. Sector enable is a feature used only by the flash module when erasing or programming flash memory.

When an erase or program operation resumes from a suspended state, the sector-enable bit is checked again as though it were a new erase or program command.

3.4.2 Four-Word Protection Keys

If this option is present, the CPU reads the four stored protection keys out of the flash bank one at a time and into a register in the flash module. After the CPU loads each key from the bank to the control logic, the CPU must load an identical user key into the FMPKEY control register. The CPU must load and match all four keys before any program or erase command can be sent to the flash module.

To enable the module for programming, the CPU must load each stored key value from the bank to the control logic by performing a normal read access to one of the four protection key addresses in the flash module. The CPU must then load the matching user key value into the FMPKEY register while in configuration mode. This process is repeated until all four keys are loaded and matched. The control logic monitors which keys have been matched, so the CPU can not gain write access until it loads and matches all four keys at least once without any intervening mismatch.

If the CPU writes a mismatching key at any time (that is, if the user key does not match the key that was most recently loaded from the bank to the control logic), then all key match states are cleared and the CPU must *reload and rematch all four keys again* to gain write access to the module. This feature can be used to disable write access after programming is completed.

After the CPU has successfully loaded and matched all four keys, flash write access is enabled and the PROTL2DIS flag (FMBBUSY.15) is set until either a device reset occurs or until the CPU writes a mismatching key to the FMPKEY register.

To store the key values, the CPU programs the key data into the bank by performing normal program and erase operations on these four protection key addresses. The key values are stored in the bank as ordinary data, so the CPU must provide the correct keys before it can perform any program or erasure of the key values.

When a new device is delivered to the customer, the keys will be all ones, so keys of all ones should be used to enable flash writes for the first time. Once the keys are changed in the flash bank, the CPU must deliberately write a mismatching key value to FMPKEY in order to disable further programming until the new key values have been loaded and matched. In other words, the flash module remains enabled for the remainder of this programming session even though the keys have been modified in flash.

The difference between flash protection key read accesses and other reads is that the key data does not propagate to the CPU data bus *until the correct keys are written* and the user has taken all required steps to gain programming access. This is intended to prevent unauthorized discovery of the stored keys by reading them out via the CPU: only a user who already knows the keys can gain access to them.

The availability of this protection feature and the location of the four protection keys depend on the specific device being used (as specified in the specific TMS470R1x device data sheet). If this feature is not available, then the four protection key addresses in the module are available for normal memory access.

3.5 Automatic Power-down of Flash Banks

The flash module provides a mechanism to automatically power down flash banks after they have not been accessed for some user programmable time. Special timers automatically sequence the power up and power down of each bank independently of each other. The charge pump module has its own independent power up/down timers.

3.5.1 Active Grace Period

Active grace period (AGP) is a feature which the host can use to optimize the flash module power consumption/access time trade-off. Faster access times are associated with higher power modes of operation. At one extreme, the power control logic could attempt to reduce power consumption by putting the banks and charge pump into a low-power mode immediately at the end of every flash access; however, if accesses are a few cycles apart, this can actually increase power consumption over if the flash had remained powered, because the banks and charge pump consume more power during flash startup and access.

Active grace periods (supported for each bank independently in addition to the charge pump module) allow the banks and/or charge pump to be maintained in active mode for a specified period following an access. This is done in anticipation of another read within the AGP time, to allow the subsequent read to have a faster access and spend less time dissipating power than if the bank went into one of the low power modes immediately. On the other hand, if the next access does not occur within the AGP time, the power control logic can automatically put the bank and/or charge pump into a low-power mode to reduce power consumption during long periods of inactivity.

AGP is realized by a set of host-programmable counters which keep the flash bank or charge pump in active mode until the counter expires, at which time the bank or charge pump reverts to its fallback power mode. See register descriptions for FMBAC1, FMBAC2, FMMAC1, FMMAC2, and FMPAGP.

The bank and/or charge pump are kept active in anticipation of another read. Assuming AGP is being utilized, the bank AGP counter is set, keeping the bank active, while an access is in progress. The counter begins counting when no more accesses are in progress. If the AGP timers have not timed out and another access occurs then there is a substantial performance gain compared to the access when the bank is not active (either the bank is in standby or Sleep mode). If the AGP counter times out, the bank or charge pump is put into a host programmable fallback power mode. The host can program the fallback power mode to be standby or sleep mode to reduce power consumption, or program it to be active mode to keep the bank active regardless of counter settings (default).

The charge pump AGP counter remains in its initialized state when any one of the banks is active, including the AGP counter of the bank. The charge pump AGP counter begins counting when all banks have become inactive.

The bank and charge pump active grace period counters count at SYSCLK frequency.

3.5.2 Power Mode Control

The primary contributors to flash module power consumption are the flash banks, and the charge pump. This section deals with how the flash wrapper handles the control of the different power modes of the flash banks and charge pump.

A couple of the components of the module power reduction have been discussed. These are the bank fallback power bits in the FMBAC1 register, the charge pump fallback power bits in the FMMAC2 register, and the BAGP and PAGP operation. The fallback power control bits contain the bank and charge pump modes, which become active upon time-out of the AGP counters described in Section 3.5.2. Any access to a flash bank causes the bank and charge pump to go into active mode, regardless of their current state. Also, any erase, program, or validate sector command causes the charge pump to become active.

If the charge pump is in sleep mode when the flash access begins, the power mode control logic automatically sequences the charge pump to standby mode, then to active mode. Also, if any bank is active or in standby mode, the charge pump is active, independent of the charge pump fallback power mode.

The host can override the power control functions of the flash module by setting all of the AGP counters to zero. In this case, the power mode control logic still sequences the pump through standby mode automatically if needed, and it activates the pump automatically if any bank is put into any power mode other than sleep mode.

3.6 Wait States

The number of wait states can vary depending on the type of read access performed. The different types of read accesses are defined below:

- *Initial Access* - First address read after initialization of the flash. Typically after reset.
- *Sequential Access* - Instruction accesses the very next flash address from the previous instruction’s flash address.
- *Random Access* - Instruction accesses a non-sequential flash address from the previous instruction’s address.

Wait states are added to a read access when either the flash bank or charge pump are not active, or when the flash bank can not have data valid at the frequency demanded by the host. The flash module generates an internal

ready signal for each bank based on the values in the wait state registers which depend on the status of the bank, the charge pump, and the data rate.

The bank has three wait state generators and the pump has two wait state counters. Both the bank and the charge pump have standby and sleep counters which are initialized when a transition is made from non-active mode to active mode. The bank also has a wait state counter to allow for a faster clock than the flash data rate. All wait state generators are clocked by the flash system clock.

The outputs of the charge pump counters and bank counters are combined. The resulting signal generates the wait states and ready signal of each bank when an access is in progress.

3.7 VDD3V Out of Range Check

The VDD3V out of range status bit informs the host if there was a low supply during an erase or program operation. A comparator in the charge pump module sets the 3VSTAT bit if the 3.3V supply is less than 2.4V for more than three SYSCLK cycles; otherwise it is cleared.

4 Control Registers

This section covers the MCU F05 flash module control register memory map and a basic description of each register and its bits.

4.1 Memory Map

The MCU F05 flash module uses several registers to control the various modes of operation, numbers of wait states, and bank selection. All user flash registers are shown in Table 2 and Table 3. The addresses shown are relative offsets from the base address, which depends upon the device being used. See the specific TMS470R1x device data sheet for the register base address.

Table 2. 32-bit Flash Memory Registers

Offset Address	Register	31 - 24	23 - 16	15	14 - 8	7	6	5	4	3	2	1	0
0x1C00	FMRE-GOPT	Reserved								RD MRGN1	RD MRGN0	READ OTP	ENPIPE
0x1C08	FMBBUSY	Reserved		PROTL 2 DIS	Reserved	BUSY[7:0]							
0x1C0C	FMPKEY	PKEY[31:0]											

Table 3. 16-bit Flash Memory Registers

Offset Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000	FMBAC1	BAGP								BSTDBY						BNKPWR	
0x0004	FMBAC2	OTP PROT DIS	BSLEEP							WAIT				WAIT			
0x0008	FMBSEA	BSEA															
0x000C	FMBSEB	BSEB															
0x0010	FMBRDY	Reserved										BANK RDY	Reserved				
0x2814	FMPRDY	Reserved						PUMP RDY	Reserved								
0x3C00	FMMAC1	PROTL 1 DIS	PSLEEP														
0x3C04	FMMAC2	PSTDBY											PMPPWR	BANK			
0x3C08	FMPAGP	PAGP															
0x3C0C	FMMSTAT	Reserved I							BUSY	ERS	PGM	INV DAT	CSTAT	3V STAT	ESUSP	PSUSP	SLOCK

4.2 Register Access

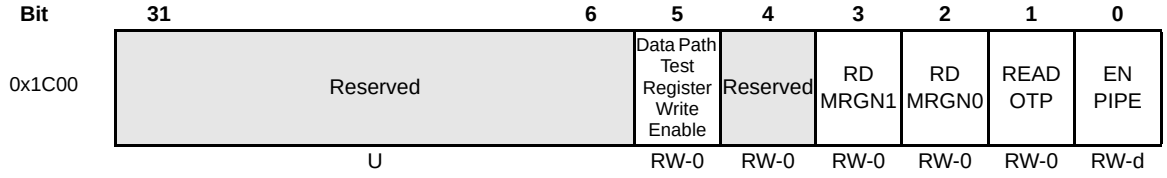
The flash module control registers can only be read and/or written by the CPU while it is in system configuration mode. Configuration mode is enabled by setting the GLBCTRL.4 bit (in the System module).

The first three registers shown in Table 2, FMREGOPT, FMBBUSY, and FMPKEY, are all word access only, whereas the remaining registers shown in Table 3 are half-word. On TMS470 devices these registers are in the lower

half-word. Half-word registers can be read and written as word access or half-word access. In word access the upper half-word is indeterminate on read and is ignored on write.

4.3 Option Control Register (FMREGOPT)

FMREGOPT is a word-access only register. It supports OTP sector access, margin testing, and pipeline mode. There is only one FMREGOPT register for the entire MCU F05 flash module.



RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset, -d: Device specific value

Bits 31:6 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 5 **Data Path Test Register Write Enable.**

Bit 4 **Reserved**

This bit is reserved for TI's use. **Do not set this bit** as it will cause the user OTP sector to be disabled even when otherwise enabled by READOTP.

Bit 3 **RDMRGN1.** Read Margin 1.

When set, enables Read Margin 1 mode (RDMRGN1 is overridden by RDMRGN0).

Bit 2 **RDMRGN0.** Read Margin 0.

When set, enables Read Margin 0 mode (RDMRGN0 mode overrides RDMRGN1 mode).

Bit 1 **READOTP.** Read OTP Sector.

When set, this bit enables reading from the OTP sector. The starting address of the OTP sector is located at the relative flash module address 0x0000 in the first bank of the flash module. Clear this bit should after the OTP sector is read to ensure that flash programming functions normally.

Bit 0 **ENPIPE.** Enable Pipe Mode.

Pipeline mode is active when ENPIPE is set, configuration mode is disabled, and the MCU F05 flash module is not in halt mode. Pipeline mode is overridden in configuration mode and in halt mode. The default value of ENPIPE is device specific. See the device-specific datasheet for the reset state of ENPIPE. Pipeline mode must be enabled before the device is configured to operate above the maximum frequency for standard read mode (typically 24MHz). This is regardless of the number of wait states.

Note: Command Writes and OTP Reads Performed Only in Standard Read Mode

Command writes and OTP reads can be performed only if pipeline mode is off. This is necessary to prevent data stored in the pipeline buffers from becoming inconsistent with the data stored in memory. Pipeline mode is disabled in configuration mode.

4.4 Bank Busy Register (FMBBUSY)

FMBBUSY is a word-access read-only register. It supports checking the busy status of all banks in parallel. The MCU F05 flash module has only one FMBBUSY register.

Bit	31 - 16	15	14 - 8	7	6	5	4	3	2	1	0
0x1C08	Reserved	PROTL2DIS	Reserved	BUSY[7:0]							
	U	R-0	U	R-0							

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bits 31:16 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 15 **PROTL2DIS.** Protection Key Level 2 Disabled Flag.

This bit is read-only and when set, it indicates that all four protection keys have been written correctly. If any of the 128 protection key bits are incorrect then PROTL2DIS is zero. Writes to this bit have no effect.

Bits 14:8 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 7-0 **BUSY[7:0].** Bank Busy.

This read-only location allows the CPU to determine if any flash bank is busy performing an OTP read, a command operation, or in the process of being reset. It displays the states of the BUSY signals from each bank simultaneously. Each bit corresponds to one flash bank. These bits are read-only. Writes have no effect.

4.5 Protection Key Register (FMPKEY)

FMPKEY is a word-access only register. It controls access protection for the entire MCU F05 flash module. The MCU F05 flash module has only one FMPKEY register.

Bit	31	0
0x1C0C	PKEY[31:0]	
	RW-0	

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bits 31-0 **PKEY[31:0].** Protection Key.

These bits receive and store the four 32-bit protection keys from the CPU for the four 32-bit protection key feature. See Section 3.4.2, *Four-Word Protection Keys*.

4.6 Bank Access Control Register 1 (FMBAC1)

FMBAC1 is a half-word register. It controls bank standby mode wait state generation, bank fallback power mode, and bank active grace period (AGP) delay. Each bank in the flash module has one FMBAC1 register. The bank is selected via BANK[2:0] of the FMMAC2 register. As only one bank at a time can be selected by FMMAC2, only the register of the selected bank appears at this address.

Bit	15	8	7	2	1	0
0x0000	BAGP[7:0]		BSTDBY[5:0]		BNKPWR[1:0]	
	RW-00000000		RW-111111		RW-11	

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bits 15-8 **BAGP[7:0].** Bank Active Grace Period.

These bits contain the starting count value for the BAGP down counter. Any access to a given bank causes its BAGP counter to reload the BAGP value for that bank. After the last access to this flash bank, the down counter delays

from 0 to 255 SYSCLK cycles before putting the bank into one of the fallback power modes as determined by BNKPWR[1:0] in this register. See Section 3.5.2, *Power Mode Control* on page 15 for bank activation logic.

Bits 7-2 **BSTBY[5:0]. Bank Standby.**

These bits contain the starting count value for the bank standby down counter. While the bank is in standby mode, the power mode management logic holds the bank standby counter at this value. When the bank exits standby power mode, the down counter delays (counts down to zero) from 0 to 63 SYSCLK cycles before putting the bank into bank active mode. These bits should be programmed to provide a minimum delay of 100nS.

Bits 1-0 **BNKPWR[1:0].** Bank Power Mode.

These bits describe the fall back power mode which the flash bank enters after the bank active grace period counter has timed out. The default (11 binary) is to stay active.

00 = Sleep (Sense amplifiers and sense reference disabled)
01 = Standby (Sense amplifiers disabled, but sense reference enabled)
10 = Reserved
11 = Active (Both sense amplifiers and sense reference enabled)

4.7 Bank Access Control Register 2 (FMBAC2)

FMBAC2 is a half-word register. It controls wait state generation, bank sleep delay, and OTP sector protection. There is one FMBAC2 register for each bank in the flash module. The bank is selected via BANK[2:0] of the FMMAC2 register. As only one bank at a time can be selected by FMMAC2, only the register of the selected bank appears at this address.

Bit	15	14 … 8	7 … 4	3 … 0
0x0004	OTP PROT DIS	BSLEEP[6:0]	WAIT[7:4]	WAIT[3:0]
	RW-0	RW-1111111	RW-1111	RW-1111

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bit 15 **OTPPROTDIS.** OTP Sector Protection Disable.

When this bit is set, it enables programming of the OTP sector. This bit can be set only when PROTL1DIS = 1.

Bits 14-8 **BSLEEP[6:0].** Bank Sleep.

These bits contain the starting count value for the bank sleep down counter. While the bank is in sleep mode, the power mode management logic holds the bank sleep counter at this value. When the bank exits sleep power mode, the down counter delays from 0 to 127 SYSCLK cycles before putting the bank into standby mode. These bits should be programmed to provide a minimum delay of 1.9μS.

Bits 7-4 **WAIT[7:4].** Wait State Counter.

These bits contain the starting count value for the wait state down counter. The down counter delays from 0 to 15 SYSCLK cycles before indicating that data is available. For normal operation, these bits are set to 0000 for single cycle standard read mode, or to 0001 for pipeline mode. Wait bits 7:4 must match wait bits 3:0.

Bits 3-0 **WAIT[3:0].** Wait State Counter.

For normal operation, these bits are set to 0000 for single cycle standard read mode, or to 0001 for pipeline mode. Wait bits 3:0 must match wait bits 7:4.

4.8 Bank Sector Enable Registers (FMBSEA and FMBSEB)

FMBSEA and FMBSEB are half-word registers. Together they provide one enable bit per sector for up to 32 sectors per bank. Each bank in the flash module has one FMBSEA and one FMBSEB register. The bank is selected via the BANK[2:0] bits of the FMMAC2 register. As only one bank at a time can be selected by FMMAC2, only the register for the bank selected appears at this address.

Bits	15	0
0x0008	BSE[15:0]	
	RW-0x0000	

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bits 15-0 **BSE[15:0].** Bank Sector Enable.

When set, a bit enables the corresponding numbered sector for program or erase access. These bits can be set only when PROTL1DIS = 1.

Addr	15	0
0x000C	BSE[31:16]	
	RW-0x0000	

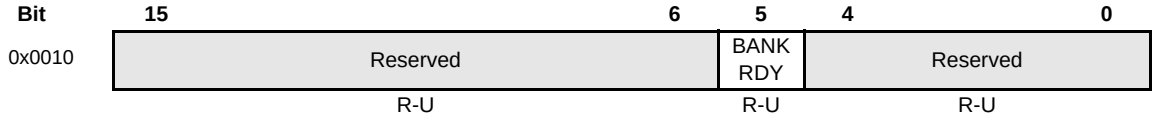
RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bits 15-0 **BSE[31:16].** Bank Sector Enable.

When set, a bit enables the corresponding numbered sector for program or erase access. These bits can be set only when PROTL1DIS = 1.

4.9 Bank Ready Register (FMBRDY)

FMBRDY is a half-word register. It allows the user to determine if the associated bank is ready for read access. FMBRDY is a local register; therefore, there is one for each flash bank present.



R: Read Only, -U: Undefined after reset

Bits 15-6 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 5 **BANKRDY.** Bank Ready.

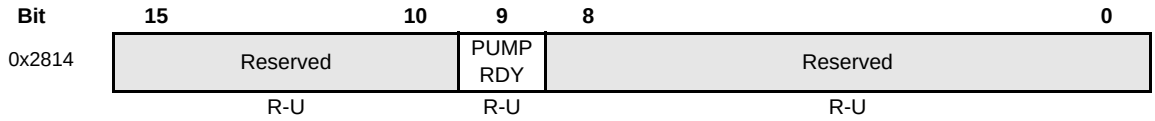
This is a read-only bit which allows software to determine if a bank is ready for access before the access is attempted.

Bits 4-0 **Reserved**

Read values are indeterminate. Writes have no effect.

4.10 Pump Ready Register (FMPRDY)

FMPRDY is a half-word register. It allows software to determine if the charge pump is ready for flash read access. FMPRDY is a global register; therefore, the MCU F05 flash module has only one FMPRDY register.



R: Read Only, -U: Undefined after reset

Bits 15-10 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 9 **PUMPRDY.** Pump Ready.

This is a read-only bit which allows software to determine if the charge pump is ready for flash access before the access is attempted.

Bits 8-0 **Reserved**

Read values are indeterminate. Writes have no effect.

4.11 Module Access Control Register 1 (FMMAC1)

FMMAC1 is a half-word register. It supports charge pump sleep wait state generation and Level 1 protection. FMMAC1 is a global register; therefore, the flash module has only one, regardless of the number of banks present.

Bit	15	14 ... 0
0x3C00	PROTL1DIS	PSLEEP[14:0]
	RW-0	RW-d

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset, -d: Device specific value

Bit 15 **PROTL1DIS.** Level 1 Protection Disable.

Setting this bit enables writing to the OTPROTDIS bits as well as to the Sector Enable registers, FMBSEA and FMBSEB, for all banks. Clearing this bit disables these accesses.

Bits 14-0 **PSLEEP[14:0].** Pump Sleep.

These bits contain the starting count value for the charge pump sleep down counter. While the charge pump is in sleep mode, the power mode management logic holds the charge pump sleep counter at this value. When the charge pump exits sleep power mode, the down counter delays from 0 to 32767 SYSCLK cycles before putting the charge pump into standby power mode (the flash module *can not* exit charge pump sleep mode directly to active mode). These bits should be programmed to provide a minimum delay of 2μS.

4.12 Module Access Control Register 2 (FMMAC2)

FMMAC2 is a half-word register. It supports control port operations, charge pump fallback power mode, and charge pump standby wait state generation. FMMAC2 is a global register; therefore, the flash module has only one, regardless of the number of banks present.

Bit	15	5	4	3	2	0
0x3C04	PSTDBY[10:0]		PMPPWR[1:0]		BANK[2:0]	
	RW-d		RW-11		RW-000	

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset, -d: Device specific value

Bits 15-5 **PSTDBY[10:0].** Pump Standby.

These bits contain the starting count value for the charge pump standby down counter. While the charge pump is in standby mode, the power mode management logic holds the charge pump standby counter at this value. When the charge pump exits standby power mode, the down counter delays from 0 to 2047 SYSCLK cycles before putting the charge pump into active mode. These bits should be programmed to provide a minimum delay of 1μS.

Bits 4-3 **PMPPWR[1:0].** Flash Pump Fallback Power Mode.

These bits select what power mode the charge pump enters after the pump active grace period (PAGP) counter has timed out.

00 = Sleep (all pump circuits disabled)
01 = Standby (only bandgap reference active)
10 = Reserved
11 = Active (all pump circuits active)

Bits 2-0 **BANK[2:0].** Bank Enable.

These bits select which bank is enabled for operations such as local register access, OTP sector access, and program/erase commands. BANK selects only one bank at a time from up to eight banks depending on the specific device being used. For example, a value of 000 binary selects Bank 0; 101 binary selects Bank 5.

4.13 Pump Active Grace Period Register (FMPAGP)

FMPAGP is a half-word register. It supports the pump active grace period delay value. FMPAGP is a global register; therefore, the flash module has only one, regardless of the number of banks present.

Bit	15		0
0x3C08	PAGP[15:0]		
	RW-0000000000000000		

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bits 15-0 **PAGP[15:0]. Pump Active Grace Period.**

This register contains the starting count value for the PAGP mode down counter. Any access to flash memory causes the counter to reload with the PAGP value. After the last access to flash memory, the down counter delays from 0 to 65535 SYSCLK cycles before entering one of the charge pump fallback power modes as determined by PMPPWR[1:0] in the FMMAC2 register. See Section 3.5.2, *Power Mode Control* on page 15 for charge pump activation logic.

4.14 Module Status Register (FMMSTAT)

FMMSTST is a half-word-access read only register. This register indicates whether an erase or program operation has been completed, suspended, failed, or is in progress. FMSTAT is a global register; therefore, the flash module has only one, regardless of the number of banks present.

Bit	15	10	9	8	7	6	5	4	3	2	1	0
0x3C0C	Reserved			BUSY	ERS	PGM	INVDAT	CSTAT	3VSTAT	ESUSP	PSUSP	SLOCK
	U		R-0	R-1->0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

RW: Read/Write in all modes, U: Undefined, *-0:* Value after reset

Bits 15-9 **Reserved**

Read values are indeterminate. Writes have no effect.

Bit 8 **BUSY.** Busy.

When set, this bit indicates that a program, erase, or suspend operation is being processed, or that the module is in the process of being reset. Initially after reset, BUSY is set, then it is cleared after the flash module is ready for access.

Bit 7 **ERS.** Erase Active.

When set, this bit indicates that the flash module is actively performing an erase operation. This bit is set when erasing starts and is cleared when erasing is complete. It is also cleared when the erase is suspended and set when the erase resumes.

Bit 6 **PGM.** Program Active.

When set, this bit indicates that the flash module is currently performing a program operation. This bit is set when programming starts and is cleared when programming is complete. It is also cleared when programming is suspended and set when programming is resumes.

Bit 5 **INVDAT.** Invalid Data.

When set, this bit indicates that the user attempted to program a “1” where a “0” was already present. This bit is cleared by the Clear Status command.

Bit 4 **CSTAT.** Command Status.

When set, this bit informs the host that the program, erase, or validate sector command failed. This bit is cleared by the Clear Status command.

Bit 3 **3VSTAT.** VDD3V Status.

When set, this bit indicates if the 3.3V power supply dipped below the lower limit allowable during a program or erase operation. This bit is cleared by the Clear Status command.

Bit 2 **ESUSP.** Erase Suspend.

When set, this bit indicates that the flash module has received and processed an erase suspend command. This bit remains set until the erase resume command has been issued.

Bit 1 **PSUSP.** Program Suspend.

When set, this bit indicates that the flash module has received and processed a program suspend command. This bit remains set until the program resume command has been issued.

Bit 0 **SLOCK.** Sector Lock Status.

When set, this bit indicates that the operation was halted because the target sector was locked for erasing and programming either by the sector protect bit or by write protection key logic. This bit is cleared by the Clear Status command.

5 Application Information

5.1 Powering Down Flash for Halt Mode

To completely power down all of the flash banks and the flash pumps, the code must be executing from RAM or some memory other than flash when the CPU is halted. The host must first set the fallback power bits to sleep mode. Then, before the host enables halt mode, it must execute from RAM long enough to let the active grace period for all banks and the charge pump expire. Also, the device must be in configuration mode.

Note: When Putting All Banks Into Sleep or Standby Mode, Ensure That There Are No Accesses to Non-Existing Memory

If all banks are in sleep or standby mode and an access to a non-existing bank is performed, the CPU will hang. This can be avoided by setting the memory decoder to enable only the amount of flash that is physically implemented on the chip.

5.2 Setting a Different Number of Wait States for Each Bank

Typically, the number of wait states is set to the same value for all banks - one when in pipeline mode and zero when not in pipeline mode. If for any reason the number of wait states will differ between banks, the bank with the higher number of wait states must be set before the bank with the lower number.

5.3 Mapping the Flash Memory

On devices which have programmable memory mapping, the flash memory must be mapped to address zero or to an address that is a multiple of the space decoded by the flash module. The flash module decodes a space eight times the size of the largest bank. No other memories can be mapped into this space.

For example, if a device has 768K bytes of flash and the largest bank is 256K bytes, this memory must start at address 0x00000000, or 0x00200000, or 0x00400000 etc. In this example, if the flash starts at 0x0000000, then RAM can not be mapped at an address below 0x00200000.

5.4 Initial Data Reads in Pipeline Mode

The initial data reads of flash memory in pipeline mode should not be from the first 16 bytes of flash memory. After reset the flash data pipeline address register points to address zero implying these 16 bytes are already in the pipeline, when they are not. If needed, flush the data pipeline by doing two dummy reads from non-sequential addresses such as 0x0010 and 0x0018 before reading any of the first 16 bytes of flash.