User's Guide

Hardware Design Guide for AM64x/AM243x Devices

Texas Instruments

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1 Introduction

The Hardware Design Guide for AM64x/AM243x family of Devices Application Report provides a starting point for the engineers designing with AM64x/AM243x processors. It provides an overview of the flow, design efforts and highlights important areas that must be addressed. Note that this document does not contain all the information needed to complete the system design. In many cases, it refers to the device-specific data manual or to various other user guides as sources for specific information.

The guide is organized in a sequential manner. It starts from decisions that must be made during the initial planning stages of the design, through the selection of key devices, electrical, and thermal requirements. For ensuring design success, issues discussed in each of the section should be resolved before moving to the next section.

Note

This guide may not cover every aspect of the system design.

Note

The AM64x/AM243x device has capabilities to help system designers address safety requirements.

This guide is focused on non-safety applications.

1.1 Before Getting Started

The AM64x/AM243x processors includes wide variety of capabilities, not all of which will be used in every design. Consequently, the requirements for different designs using the same device can vary widely depending on the target application. Designers must understand the requirements before determining the details of the design. In addition, the design may require additional circuitry to operate correctly in the target environment. For the selected device and determine the following, see latest device-specific collaterals on TI.com like the data sheet, Errata, TRM and EVM User's guides:

- What are the expected environmental conditions for the device operation, target boot mode, storage type and interfaces used
- How much processing will each of the cores in the selected device be performing
- What is the DDR memory type, speed and interface that will be used
- Peripherals attached to the processor

1.2 Device (Processor) Selection

Selection of device is the most important step during the system design process. For selecting the device variant, device density, features, package (ALV), and speed grade that is applicable, see the *Functional Block Diagram* and *Device Comparison* section in device-specific data sheet.

1.2.1 Availability of Tightly Coupled Memory (TCM)

Refer device-specific data sheet for the R5F Tightly Coupled Memory (TCM) information. Irrespective of the number of cores available, the TCM remains in the subsystem that can be used by the processor. For AM642x, one core from each subsystem(cluster) is available resulting in 256K.

Please note that lockstep is not supported on AM64x devices.

1.3 Technical documentation

A number of document relevant to the selected device are provided on the product folder page. Read through relevant documents before the start of design.

1.4 Design Documentation

Throughout this guide, TI recommends generating a design document periodically. Generating and storing this information provides you with the foundation for the documentation package, and this design document will be needed when seeking external review support.

2 System Block Diagram

A detailed System Block Diagram, covering all the functional blocks and required interfaces is key to a successful design.

2.1 Creating the System Block Diagram

The first step during the system design is to create a detailed System Block Diagram. The System Block Diagram includes all major functional blocks, associated devices, interfaces and illustrates the I/Os (ports) used for interconnecting the devices.

The following is a collection of resources to support the System Block Diagram creation process:

- The SK-AM64B (AM64B starter kit for AM64x Sitara processors), TMDS64EVM (AM64x evaluation module for Sitara processors) and any other available EVMs are a good source to start with the design.
- The TI.com links referred below provide Device Functional Block Diagrams, Device Data sheet, User Guide, Errata, application notes, design considerations, and other related information for various applications. Design and development section include EVM information, Design tools, simulation models and software. As part of support and training, links to commonly applicable E2E threads are available.
  - AM6411 Product Folder
  - AM6412 Product Folder
  - AM6421 Product Folder
  - AM6422 Product Folder
  - AM6441 Product Folder
  - AM6442 Product Folder
  - AM2431 Product Folder
  - AM2432 Product Folder
  - AM2434 Product Folder

2.2 Selecting the Boot Mode

The System Block Diagram should indicate the interface used for booting.

The AM64x/AM243x device contains multiple peripheral interfaces that support boot mode. Examples include: eMMC, MMC/SD, QSPI, OSPI, GPMC (NOR/NAND), Ethernet, USB (Target & Host), PCIe, xSPI, I2C, and UART. The AM64x/AM243x device supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, the ROM moves on to the backup mode.

The boot mode pins and the associated resistor configurations provide inputs on the boot mode setting to be used by the ROM code for boot. These pins are sampled at power-on-reset, and must be properly set up before releasing (deassertion) the reset.

Boot mode configurations can be categorized as below:

PLL Config: BOOTMODE [02:00] – Denotes system clock frequency (MCU_OSC0_XI/XO) to ROM code for PLL configuration

Primary Boot Mode: BOOTMODE [06:03] – Selects the configured boot (primary) mode after POR, i.e., (that is), the peripheral/memory to boot from.

Primary Boot Mode Config: BOOTMODE [09:07] – These pins provide optional configurations for primary boot and are used in conjunction with the boot mode selected.

Backup Boot Mode: BOOTMODE [12:10] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot fails.

Backup Boot Mode Config: BOOTMODE [13] – This pin provides optional configurations for the backup boot devices.

Reserved: BOOTMODE [15:14] – Reserved pins.

Key considerations for boot mode configuration:

- TI recommends including provision to configure boot modes used during development, such as UART boot or No-boot mode for JTAG debug.
- Boot pins have other functions after reset. Ensure the board design takes this into account when choosing pullup/pulldown resistors for the boot pins. If these pins are driven by another device, they must return to the proper boot configuration levels whenever the device is reset (indicated by the PORz_OUT pin) to enable it to boot properly.
- The functionality of some boot mode pins are reserved. These pins should not be left floating and must be terminated (pullup or pulldown). For details regarding termination of reserved boot mode pins, see the *Boot Mode Pins* section of the *Initialization* chapter of the device-specific TRM.

For details regarding boot modes, see the *Initialization* chapter of the device-specific TRM.

Note

It is the user responsibility to set the boot mode pins (via pullups or pulldowns, and optionally jumpers/switches) depending on the desired boot scenario.

2.3 Confirming Pin Multiplexing Compatibility

The processor contains a number of peripheral interfaces. To optimize size, pin count, package cost while maintaining maximum functionality, many of the device pads (pins) can multiplex up to eight signal functions. Thus, not all peripheral interface instances can be used simultaneously.

Texas Instruments has developed SysConfig-PinMux Tool that helps a system designer select the appropriate function using pin-multiplexing configuration too for their AM64x/AM243x based system design.

Note

The pinmux configuration generated using SysConfig-PinMux Tool for the design should be saved along with other design documentation.

3 Power Supply

After completing the device selection and system block diagram, next design process is to determine the power supply needs for the selected processor.

3.1 Power Supply Architecture

The power supply architecture that can be considered are listed below:

3.1.1 Integrated power architecture

Based on Multi-channel ICs (PMIC), refer *Powering the AM64x with the TPS65220 or TPS65219 PMIC*, *Using LP8733xx and TPS65218xx PMICs to Power AM64x and AM243x Sitara Processors* and *Powering the AM64xx with the LP8733xx PMIC* application notes.

3.1.2 Discrete power architecture

Based on DC-DC converters and LDOs, refer *TMDS64EVM (AM64x evaluation module for Sitara processors)* EVM schematic.

3.2 Power (Supply) Rails

For the full list of processor power supply rails and recommended operating range, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details about select power rails.

3.2.1 Core Supply

Core supply VDD_CORE can be operated at 0.75 V or 0.85 V. When VDD_CORE is operating at 0.75 V, VDD_CORE shall be ramped up prior to all 0.85 V supplies.

Core supplies VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, VDDA_0P85_USB0 and VDDR_CORE are specified to operate at 0.85 V only.

VDD_CORE and VDDR_CORE are expected to be powered by the same source so these ramp together when VDD_CORE is operating at 0.85 V.

VDD_MMC0 and VDD_DLL_MMC0 shall be connected to the same power source as VDD_CORE when MMC0 is not used. In this case, VDD_MMC0 and VDD_DLL_MMC0 shall be operated at a nominal voltage of 0.75 V or 0.85 V.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.2 Peripheral Power Supply

The processor includes dedicated peripheral supply pins for USB, MMC0, PLLs, ADC, SERDES and are operated at 1.8 V. An additional 3.3 V analog supply is required for USB.

Depending on the selected memory DDR PHY and DDR clock IO supply can be 1.1 V or 1.2 V.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 Internal LDOs for IO groups

The processor includes eight internal LDOs, with the output of each connected to a pin (CAP_VDDSx [x=0-5], CAP_VDDSHV_MMC1, CAP_VDDS_MCU) on the processor. A capacitor must be connected to each of these LDO output pins. For guidance on the capacitor selection and connection, see the *Power Supply* section in the *Signal Descriptions* chapter of the device-specific data sheet.

3.2.4 Dual-Voltage LVCMOS I/Os

The processor includes seven dual-voltage I/O domains (VDDSHVx [x=0-5] and VDDSHV_MCU), where each domain provides power to a fixed set of I/Os. Each I/O power domain can be configured for 3.3 V or 1.8 V, which determines a common operating voltage for the entire set of I/Os powered by the respective I/O power domain. All signals connected to these domains must operate from the same power source that is being used to power the respective VDDSHVx supply rail. The AM64x/AM243x I/O buffers are not fail-safe. The supply voltage for the VDDSHVx rail must be present before any voltage is applied to the associated I/Os.

I/O grouping information is summarized below:

VDDSHV0 – Voltage for the General I/O group

VDDSHV1 – Voltage for the PRG0 I/O group

VDDSHV2 – Voltage for the PRG1 I/O group

VDDSHV3 – Voltage for the GPMC I/O group

VDDSHV4 – Voltage for the Flash I/O group

VDDSHV5 – Voltage for the MMC1 I/O group

VDDSHV_MCU – Voltage for the MCU General I/O group

3.2.5 Dual-Voltage Switching SDIO I/Os

The processor includes one integrated SDIO LDO to support SD card I/O voltage switching. An output capacitor of 3.3-µF must be connected to the LDO output pin.

Only one MMCSD port (selectable through V1P8_SIGNAL_ENA bit) can be connected to the SDIO LDO in a given system.

For more details, refer the *Integrated Low-dropout Regulator (LDO)* section in the *Power* chapter of the device-specific TRM.

3.2.6 VPP (eFuse ROM programming supply)

VPP pin is left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply is only be sourced while programming the eFuse. The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be ramped up after the proper device power-up sequence.
- The VPP pin have high current transients and a local bulk capacitors are likely needed near the VPP pin to assist the LDO transient response.
- Select the power supply with quick discharge capability or use a discharge resistor. A Maximum current of 400 mA is required for programming.
- If an external power supply is used, the supply shall be applied after the processor supplies are stable.
- The VPP power supply must be disabled (left floating (HiZ) or grounded) when not programming the OTP registers.

For more information, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.3 Determining System Power Requirements

The maximum and minimum current requirements for each of these voltage rails are not available in the device-specific data sheet. These requirements are highly application-dependent and must be calculated for a specific use case.

3.4 Power Supply Filters

The processor contains multiple analog supply pins that provide power to sensitive analog circuitry such as VDDA_1V8_MCU, VDDA_PLLx [x=0-2], VDDA_1V8_SERDES, VDDA_1V8_USB0 and VDDA_ADC. These must be attached to filtered supply sources.

3.5 Power Supply Decoupling and Bulk Capacitors

To properly decouple the supply planes from system noise, decoupling and bulk capacitors are required. For adding bulk and decoupling capacitors, see the *TMDS64EVM (AM64x evaluation module for Sitara processors)*, *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)* and other EVM schematic.

For guidance on optimizing the selection and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis*.

3.6 Power Supply Sequencing

A detailed diagram of the power supply sequencing (Power-Up/Power-Down) for the processor can be found in the device-specific data sheet. All power supplies associated with the processor should allow for controlled sequencing using on-board logic when using discrete power solution or a PMIC based power supply.

3.7 Supply Diagnostics

The processor includes below voltage monitor pins:

- VMON_1V8_SOC, VMON_1V8_MCU and VMON_3V3_SOC, VMON_3V3_MCU: These pins can be connected directly to their respective 1.8 V and 3.3 V supplies. An internal resistor divider is implemented inside the processor for each of these pins. Consider adding a 0.1-µF filter capacitor to these pins.
- VMON_VSYS: Connect the system voltage (3.3 V or 5 V) through a voltage divider (0.45 V ±3%). Consider implementing a capacitor for noise filtering as described in the device-specific data sheet.

For more information see the *System Power Supply Monitor Design Guidelines* section in the *Applications, Implementation, and Layout* chapter of the device-specific data sheet

3.8 Power Supply Monitoring

Consider provisioning for external monitoring of supply rails and load currents.

For more information, see the *TMDS64EVM (AM64x evaluation module for Sitara processors)* and *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)* schematic.

Now that the power supply components have been selected, create a power supply rails and interconnection block diagram and power sequence diagram.

4 Clocking

The next design step is proper clocking, and providing appropriate clocks to all connected devices in the system. These clocks can be generated by pairing external crystals with an internal oscillator or they can be generated externally by a clock generator or oscillator. This section describes the clocks available in the processor and the requirements for these clocks.

4.1 System Clock Input

The processor clock inputs and recommended oscillator connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet. MCU_OSC0 clock is required for proper operation of the processor.

4.2 Unused Clock Inputs

Not Applicable.

4.3 Single-ended Clock Source

The MCU_OSC0 internal oscillator can be sourced from a crystal or an LVCMOS square-wave digital clock source. For more details, see the *Input Clocks / Oscillators* section in the *Specifications* chapter of the device-specific data sheet.

Note

Be sure to terminate the XO pin as per the data sheet recommendation when using an external clock.

4.4 Crystal selection

When selecting a crystal, the system designer must consider the temperature and aging characteristics based on the worst case environment and expected life expectancy of the system.

5 JTAG

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. Although JTAG is not required for operation, TI strongly recommends that a JTAG connection be included in the designs.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the device configuration.

As an emulation interface, the JTAG port can be used in various modes:

- Standard emulation: requires only five standard JTAG signals
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in this mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the device configuration.

For supported JTAG clocking rates, see the device-specific TRM.

5.1.2 System Implementation of JTAG / Emulation

The JTAG and Emulation pins on this processor are in same power domains. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 I/Os are powered by the VDDSHV_MCU domain. VDDSHV_MCU can be configured either 1.8 V or 3.3 V.

For most other system-level implementation details, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 JTAG Termination

For terminating the JTAG interface signal, refer the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

6 Device Configurations and Initialization

When the voltage rails and the required clocks are present and stable, the processor reset may be deasserted (released) to start the processor initialization.

6.1 Device Reset

The processor can be reset in several ways. The methods are described in detail in the device-specific data sheet and TRM.

The device includes three external reset input pins (MCU_PORz, MCU_RESETz, and RESETz_REQ) and three reset status output pins (MCU_RESETSTATz, PORz_OUT and RESETSTATz). Be sure to provide the terminations recommended in the device-specific data sheet.

For MCU_PORz, a 3.3V signal can be applied to this input, but the input thresholds are still a function of the IO supply voltage (VDDS_OSC).

Additional reset modes are available through internal registers and emulation.

Note that TI recommends implementing RESET logic using AND gate for on-board Media and Data Storage devices and other peripherals as applicable. One of the AND gate input shall be controlled by processor GPIO pin with provision to isolate. Other AND gate input shall be the Main Domain warm reset status output (RESETSTATz) Signal. Ensure the reset outputs are terminated as per the device recommendations.

The 3.3 V power source for the SD Card and SDIO_LDO needs to be routed through an external power switch that can be controlled. This controlled power switch is required to reset the SD Card since cycling power to the card is the only way to reset the card back to its default state.

For more information, refer the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)* and *TMDS64EVM (AM64x evaluation module for Sitara processors)* schematics.

6.2 Boot Modes

For more details about the processor boot mode options, see Section 2.2.

Boot modes and certain device configuration selections are latched at the rising edge of MCU_PORz. The configuration and boot mode inputs are multiplexed with GPIO pins or pins with other functions. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for their primary function. The PORZ_OUT pin indicates latching of boot mode configuration.

6.3 Watchdog Timer

Consider using external or internal watchdog timer based on the application requirement.

7 Peripherals

This section covers the device peripherals and modules, and is intended to be used in addition to the information provided in the device-specific data sheet, TRM, and relevant application reports. The three types of documents should be used as follows:

- Data Sheet: AC Timings, Used pin guidance
- TRM: Functional Description, Programming Guide, Register offsets
- Application Reports: System-level understanding and issues

7.1 Selecting Peripherals Across Functional Domains

The processor is partitioned into two functional domains, each containing specific processing cores and peripherals:

- MAIN domain
- Microcontroller (MCU) domain

For most use cases, peripherals from any of the domain can be used. All peripherals, regardless of their domain, are memory mapped, and the Arm® Cortex®-A53 cores can see and access all peripherals in the MCU domain.

7.2 Memory, Media and Data Storage Interfaces

DDR Subsystem supports only LPDDR4 and DDR4. Refer device-specific data sheet and TRM for data bus width (16-Bit), inline ECC support, speed (up-to 1600 MT/s) and Max addressable range (2GBytes (DDR4 or LPDDR4)) selection.

For more details, refer the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

Media and Data Storage interface support includes 2 x Secure Digital (SD) ((4b+8b) (8-bit eMMC, 4-bit SD/SDIO)) interface, 1 x General-Purpose Memory Controller (GPMC) and OSPI/QSPI.

For more details, refer the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.3 Ethernet Interface

The AM64x supports up to five (5) concurrent external Ethernet ports. Pinmuxing overlaps one of the CPSW and ICSSG external ports so this is an either/or port instance.

Before configuring the MDIO interface refer advisory *i2329 MDIO: MDIO interface corruption (CPSW and PRU-ICSS) (AM64x/AM243x Processor Silicon Revision 1.0, 2.0)*

7.3.1 Common Platform Ethernet Switch 3-port Gigabit Ethernet (CPSW3G)

AM64x/AM243x provides an Integrated Ethernet switch. An Integrated Ethernet switch supporting two external Ethernet ports RMII (10/100) or RGMII (10/100/1000) using CPSW3G subsystem. For configuring RMII interface, see the *CPSW0 RMII Interface* section of the device-specific TRM for the recommended configuration.

CPSW3G allows using mixed RMII/RGMII topology.

For more details on the Ethernet interface, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.3.2 Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU-ICSSG)

AM64x/AM243x provides two instances of PRU-ICSSG subsystems and supports UART0, eCAP0, PWM, IEP0 and IEP1 peripheral modules.

Each PRU_ICSSG contains 2 x Ethernet ports (MII (10/100) or RGMII (10/100/1000)). Refer the TRM for information on support for SGMII mode. PRU-ICSSG supports Profinet IRT, Profinet RT, EtherNet/IP, EtherCAT, Time-Sensitive Networking (TSN), and more industrial protocols.

For selecting the device with required PRU-ICSSG functionality refer What PRU_ICSSG functionality is on each AM64x device?

For more details, refer the *Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit (PRU_ICSSG)* section in the *Processors and Accelerators* chapter of the device-specific TRM.

7.4 Universal Serial Bus (USB) Subsystem

AM64x/AM243x processor provides 1 x USB 3.1 Dual-Role Device (DRD) Subsystem (USBSS). These Ports can be configurable as USB host (SuperSpeed Gen 1 (5 Gbps), High-speed (480 Mbps), Full-speed (12 Mbps), and Low-speed (1.5 Mbps)), USB device (High-speed (480 Mbps), and Full-speed (12 Mbps)), or USB Dual-Role device.

Follow USB VBUS Design Guidelines for scaling the VBUS voltage connected to the processor.

Refer the device-specific TRM for USB connection and On-The-Go feature support.

For more details, refer the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.5 Peripheral Component Interconnect Express (PCIe) Subsystem

One PCI-Express Gen2 controller (PCIE) Supports Gen2 and Single Lane operation.

For more details, refer the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

Note

No PCIe completion is generated as long as POWER_STATE_CHANGE_ACK is '0'. Configure POWER_STATE_CHANGE_ACK to '1' for generating PCIe completion.

Note

- The Serdes PHY (interface) of AM64x/AM243x is common for USB SuperSpeed and PCIe interface. Therefore, USB shall be limited to non-SuperSpeed modes when using the SerDes PHY for PCIe.
- The use of USB3 and PCIe is mutually exclusive on this device so these cannot be used at the same time.

7.6 General Connectivity

The processor provides multiple instances of I2C, UART, ADC (12-Bit), McSPI, FSI_RX, FSI_TX, EPWM, ECAP, EQEP, MCAN and GPIOs.

For I2C interface with open drain outputs, an external termination is recommended irrespective of peripheral usage.

The number of peripheral instances depends on the application and can be configured using the SysConfig-PinMux Tool.

For more details, refer the *Peripherals* chapter of the device-specific TRM.

7.7 Analog-to-Digital Converter (ADC)

The AM64x/AM243x provides single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels) with programmable data rate up to 4 MSPS.

Refer Errata for guidance on using SR2.0 devices on existing boards, and recommendations for new board designs.

For ADC termination (entire ADC or any of the ADC input not used) refer Pin Connectivity Requirements section in device-specific data sheet.

For more details, refer the *General Connectivity Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

7.7.1 Change Summary of AM64x SR2.0 ADC Errata

One of the two pins currently assigned to the MMC0 PHY IO supply (VDDS_MMC0) in the SR1.0 device is assigned as the ADC0_REFP pin in SR2.0. No compatibility issue is observed when installing a SR2.0 device on a PCB that was designed for the SR1.0 pin assignment since the ADC0_REFP operates at the same voltage as VDDS_MMC0. However, the ADC can have performance issues if trying to use the device when a SR2.0 device is installed on a PCB designed for SR1.0 devices since noise from the MMC0 PHY IO supply can couple directly into the ADC0_REFP pin.

SR1.0 device cannot be installed on a PCB designed for SR2.0 devices since this PCB has a dedicated ADC0_REFP source which gets shorted to VDDS_MMC0 when a SR1.0 device is installed.

One of the VSS pin is re-assigned to be ADC0_REFN. Currently ADC0_REFN is connected to VSS in the package. This change eliminates any direct coupling of package ground bounce into the ADC reference. This pin change does not have any impact on the PCB design since the SR1.0 VSS pin is already connected to the PCB VSS plane and we expect the new SR2.0 ADC0_REFN pin to also be connected to the PCB VSS power plane.

7.8 Terminations of Unused peripherals and I/Os

All power pins must be supplied with the voltages specified in Recommended Operating Conditions section, unless otherwise specified.

AM64x/AM243x has package balls that have specific connectivity requirements and package balls that can be unused.

For information on terminating the unused peripherals and I/Os, see the *Pin Connectivity Requirements* section of the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

8 I/O Buffers and Termination

An important step in the hardware design, before beginning schematic capture, is to confirm both DC and AC electrical compatibility between the processor and interfaced devices.

- The device-specific data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, run IBIS simulations using IBIS models provided for the processor to confirm signal integrity.
  - AM64x/AM243x IBIS Model

For more information on terminations, see the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

9 Power Consumption and Thermal Solutions

The Processor power consumption can vary depending on usage, implementation, topology, component selection, and process variation.

9.1 Power Consumption

For information on the device power consumption, see the *AM64x/AM243x Power Estimation Tool* application note.

9.2 Power Savings Modes

The device supports multiple power saving modes. For more details, see the *Device Power States* section in the *Device Configuration* chapter of the device-specific TRM.

9.3 Guidance on Thermal Solution

The *Thermal Design Guide for DSP and Arm Application Processors* application report provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

For more information, see AM64x/AM243x Thermal Model.

10 Schematics Recommendations

At this stage of the design, schematic capture can be started. To support in creating the schematics, see the below collection of information.

10.1 Selection of Component and Values

Be sure to use the passive component values recommended in the data sheet when ever applicable.

10.2 Schematics development

The Schematics can be drawn newly or reused. For an example during the schematics capture phase, see the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*, *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)* and *TMDS64EVM (AM64x evaluation module for Sitara processors)* schematics.

During schematic capture, follow *AM64x/AM243x Schematic Checklist* and Errata (*AM64x/AM243x Processor Silicon Revision*).

Note

When the EVM schematics is reused, ensure the functionality is reviewed and review change in net name before reuse.

When schematics is reused, the DNI setting are reset. Make sure the DNIs are reconfigured (populating DNIs could affect the functionality).

10.3 Reviewing the schematics

After completing the schematic capture, check the design against the *AM64x/AM243x Schematic Checklist*.

Plan an internal schematic review to review the schematics with reference to the schematic checklist and inspect other key areas of the schematic for errors, inaccuracies, missing net connections, and so forth.

10.4 Floor planning of the PCB

After schematic capture, TI recommends floor planning of the board to determine the interconnect distances between the various devices, board size and outline.

11 Layout and Routing Guidelines

After completing schematic capture and reviews, the next design step is the PCB layout. For information supporting the board layout, see the following section.

11.1 Escape Routing Guidelines

The *AM64x and AM243x BGA Escape Routing* application report provides a sample PCB escape routing for the AM64x/AM243x processor.

11.2 DDR Board Design and Layout Guidelines

The goal of the *AM64x/AM243x DDR Board Design and Layout Guidelines* application report is to make the DDR4, and LPDDR4 system implementation straight forward for all designers. Requirements have been captured as a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4, and LPDDR4 memories that follow the guidelines in this document.

DDR target impedance is 40-ohms (single-ended) and 80-ohms (differential) for the DDR traces.

For the propagation delay, the delay to be considered for DDR/LPDDR is the delay related to the traces on the board.

There is no need to include any package level propagation delay.

Refer design guide for DDR4 data rate, device bit width, device count and LPDDR4 SDRAM Count, Channel Width, Channels, Die, Ranks.

11.3 High-Speed Differential Signal Routing Guidance

The *High-Speed Interface Layout Guidelines* application report provides guidance for successful routing of the high-speed differential signals. This includes PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. TI supports only designs that follow the board design guidelines contained in the application report.

Note

Consider using the *SK-AM64B (AM64B starter kit for AM64x Sitara processors)* and *TMDS64EVM (AM64x evaluation module for Sitara processors)* layouts as reference.

12 References

- Texas Instruments: *AM64x Sitara™ Processors Data Sheet*
- Texas Instruments: *AM243x Sitara™ Microcontrollers Data Sheet*
- Texas Instruments: *AM64x/AM243x Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM64x/AM243x Silicon Errata*
- Texas Instruments: *SK-AM64B (AM64B starter kit for AM64x Sitara processors)*
- Texas Instruments: *TMDS64EVM (AM64x evaluation module for Sitara processors)*
- Texas Instruments: *TMDS64GPEVM (General-purpose evaluation module for Sitara processors)*
- Texas Instruments: *TMDS243EVM (AM243x evaluation module for Arm Cortex-R5F-based MCUs)*
- Texas Instruments: *TMDS243GPEVM (AM243x general-purpose evaluation module for Arm Cortex-R5F-based MCUs)*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors Application Report*
- Texas Instruments: *PRU-ICSS Feature Comparison*
- Texas Instruments: *Industrial Communication Protocols Supported on Sitara™ Processors and MCUs*
- Texas Instruments: *Powering the AM64x with the TPS65220 or TPS65219 PMIC*
- Texas Instruments: *Using LP8733xx and TPS65218xx PMICs to Power AM64x and AM243x Sitara Processors*
- Texas Instruments: *Powering the AM64xx with the LP8733xx PMIC*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *AM64x/AM243x Power Estimation Tool*
- Texas Instruments: *AM64x/AM243x Schematic Checklist*
- Texas Instruments: *AM64x and AM243x BGA Escape Routing*
- Texas Instruments: *AM64x/AM243x DDR Board Design and Layout Guidelines*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*

13 Terminology

CPSW3G – Common Platform Ethernet Switch 3-port Gigabit

E2E – Engineer to Engineer

ECAP – Enhanced Capture

ECC – Error-Correcting Code

eMMC – embedded Multi-Media Card

EMU – Emulation Control

EPWM – Enhanced Pulse-Width Modulator

EQEP – Enhanced Quadrature Encoder Pulse

FSI_RX – Fast Serial Interface Receiver

FSI_TX – Fast Serial Interface Transmitter

GPIO – General Purpose Input/Output

GPMC – General-Purpose Memory Controller

HS-RTDX – High Speed Real Time Data eXchange

I2C – Inter-Integrated Circuit Interface

IBIS – Input/Output Buffer Information Specification

IEP – Industrial Ethernet Peripheral

JTAG – Joint Test Action Group

LDO – Low Dropout

LVCMOS – Low voltage complementary metal oxide semiconductor

MCAN – Modular Controller Area Network

McSPI– Multichannel Serial Peripheral Interfaces

MII – Media Independent Interface

MMC – Multi-Media Card

OSPI – Octal Serial Peripheral Interface

PCB – Printed Circuit Board

PMIC – Power management integrated circuit

POR – Power-on Reset

PRU-ICSSG – Programmable Real-Time Unit and Industrial Communication Subsystem - Gigabit

PWM – Pulse-Width Modulator

QSPI – Quad Serial Peripheral Interface

RGMII – Reduced Gigabit Media Independent Interface

RMII – Reduced Media Independent Interface

SD – Secure Digital

SDIO – Secure Digital Input Output

SGMII – Serial Gigabit Media Independent Interface

SPI – Serial Peripheral Interface

TCK – JTAG Test Clock Input

TDI – JTAG Test Data Input

TDO – JTAG Test Data Output

TMS – JTAG Test Mode Select Input

TRM – Technical Reference Manual

TRSTn – JTAG Reset

UART – Universal Asynchronous Receiver/Transmitter

USB – Universal Serial Bus

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