OMAP5910 Dual-Core Processor PWL, PWT, and LED Reference Guide

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Preface

Read This First

About This Manual

The OMAP5910 Pseudonoise pulse-width light modulator (PWL), pulse-width tone (PWT), and light-emitting diode (LED) modules are described in this document.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the OMAP5910 device and related peripherals. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

OMAP5910 Dual-Core Processor MPU Subsystem Reference Guide (literature number SPRU671)

OMAP5910 Dual-Core Processor DSP Subsystem Reference Guide (literature number SPRU672)

OMAP5910 Dual-Core Processor Memory Interface Traffic Controller Reference Guide (literature number SPRU673)

OMAP5910 Dual-Core Processor System DMA Controller Reference Guide (literature number SPRU674)

OMAP5910 Dual-Core Processor LCD Controller Reference Guide (literature number SPRU675)

OMAP5910 Dual-Core Processor Universal Asynchronous Receiver/Transmitter (UART) Devices Reference Guide (literature number SPRU676)

OMAP5910 Dual-Core Processor Universal Serial Bus (USB) and Frame Adjustment Counter (FAC) Reference Guide (literature number SPRU677)

OMAP5910 Dual-Core Processor Clock Generation and System Reset Management Reference Guide (literature number SPRU678)

OMAP5910 Dual-Core Processor General-Purpose Input/Output (GPIO) Reference Guide (literature number SPRU679)

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OMAP5910 Dual-Core Processor Inter-Integrated Circuit (I2C) Controller Reference Guide (literature number SPRU681)

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OMAP5910 Dual-Core Processor Inter-Processor Communication Reference Guide (literature number SPRU683)

OMAP5910 Dual-Core Processor Camera Interface Reference Guide (literature number SPRU684)

OMAP5905 Dual-Core Processor Multichannel Serial Interface (MCSI) Reference Guide (literature number SPRU685)

OMAP5910 Dual-Core Processor Micro-Wire Interface Reference Guide (literature number SPRU686)

OMAP5910 Dual-Core Processor Real-Time Clock (RTC) Reference Guide (literature number SPRU687)

OMAP5910 Dual-Core Processor HDQ/1-Wire Interface Reference Guide (literature number SPRU688)

OMAP5910 Dual-Core Processor PWL, PWT, and LED Peripheral Reference Guide (literature number SPRU689)

OMAP5910 Dual-Core Processor Multichannel Buffered Serial Port (McBSP) Reference Guide (literature number SPRU708)

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PWL, PWT, and LED

The OMAP5910 Pseudonoise pulse-width light modulator (PWL), pulse-width tone (PWT), and light-emitting diode (LED) modules are described in this chapter. Figure 1 shows the location of these modules on the OMAP5910 Functional Overview.

Figure 1. OMAP5910 Functional Overview

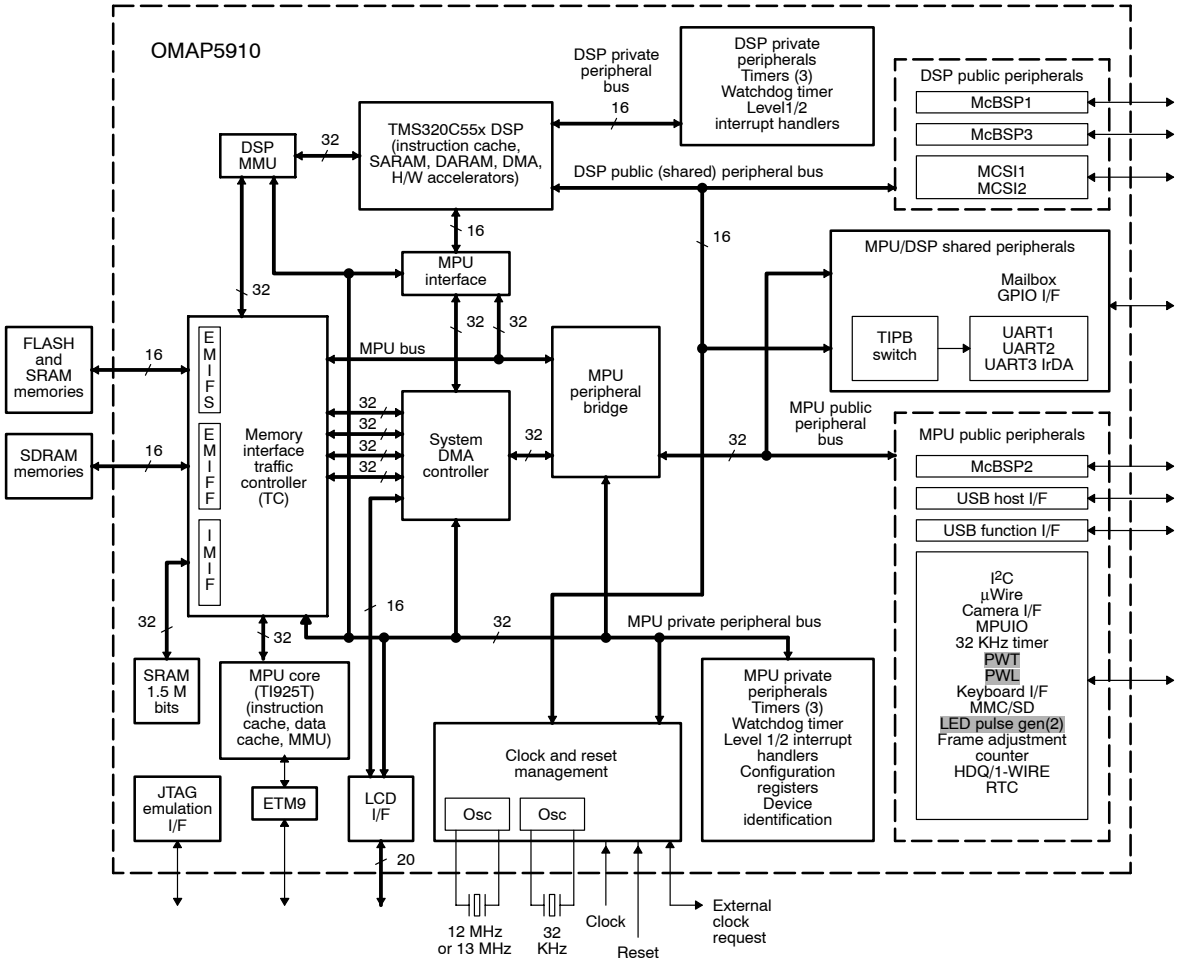


Figure 1 shows the PWL,PWT, and LED modules highlighted in the lower right corner as part of the MPU public peripherals.

1 Pseudonoise Pulse-Width Light Modulator Overview

This pulse-width light (PWL) module provides control of LCD backlighting and keypad voltage by employing a 4096-bit random sequence generator. This voltage-level control technique decreases the spectral power at the modulator's harmonic frequencies. The module uses a 32-kHz clock from the ultra−low power device (ULPD) module on the Clock and Reset Management module. For more information on the ULPD module see SPRU678.

1.1 PWL Functional Description

The PWL module is composed of a pseudorandom 8-bit data generator and a programmable threshold comparator (see Figure 2).

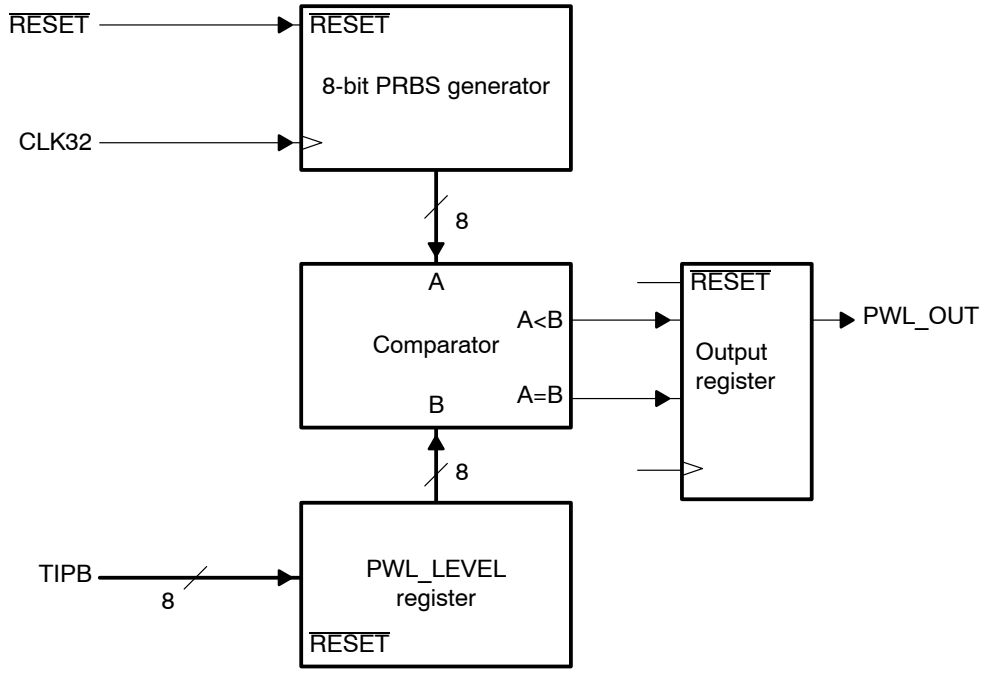
The pseudorandom 8-bit data generator is built using a linear−feedback shift register (LFSR). It generates a white normal-law random value between 1 and 255. The LFSR polynomial generator output is P(x) = x[7] + x[3] + x[2] + x[1].

The comparator generates:

- 0 if the random value is greater than or equal to the programmable threshold
- 1 if the random value is less than the programmable threshold

Assuming the random sequence is normal, it generates a sequence whose mean value is proportional to the comparator threshold.

Figure 2. PWL Block Diagram



1.2 PWL Level and Control Registers

Table 1 lists the PWL registers. Table 2 and Table 3 describe the individual registers.

Table 1. PWL Registers

Name	Description	R/W	Size	Address
PWL_LEVEL	PWL-level	R/W	8 bits	FFFB:5800
PWL_CTRL	PWL control	R/W	8 bits	FFFB:5804

Table 2. PWL Level Register (PWL_LEVEL) Field Descriptions

Bits	Field	Descriptions	Reset Value
7–0	PWL_LEVEL	Defines the mean value of the PWL output signal. 0 leads to a continuous 0 output. 255 to an almost continuous 1 output: 255/256 cycles in high level.	00h

Table 3. PWL Control Register (PWL_CTRL) Field Descriptions

Bits	Field	Descriptions	Reset Value
7–1	–	Reserved	
0	CLK_ENABLE	Internal clock is enabled when 1.	0

2 Pulse-Width Tone Module Overview

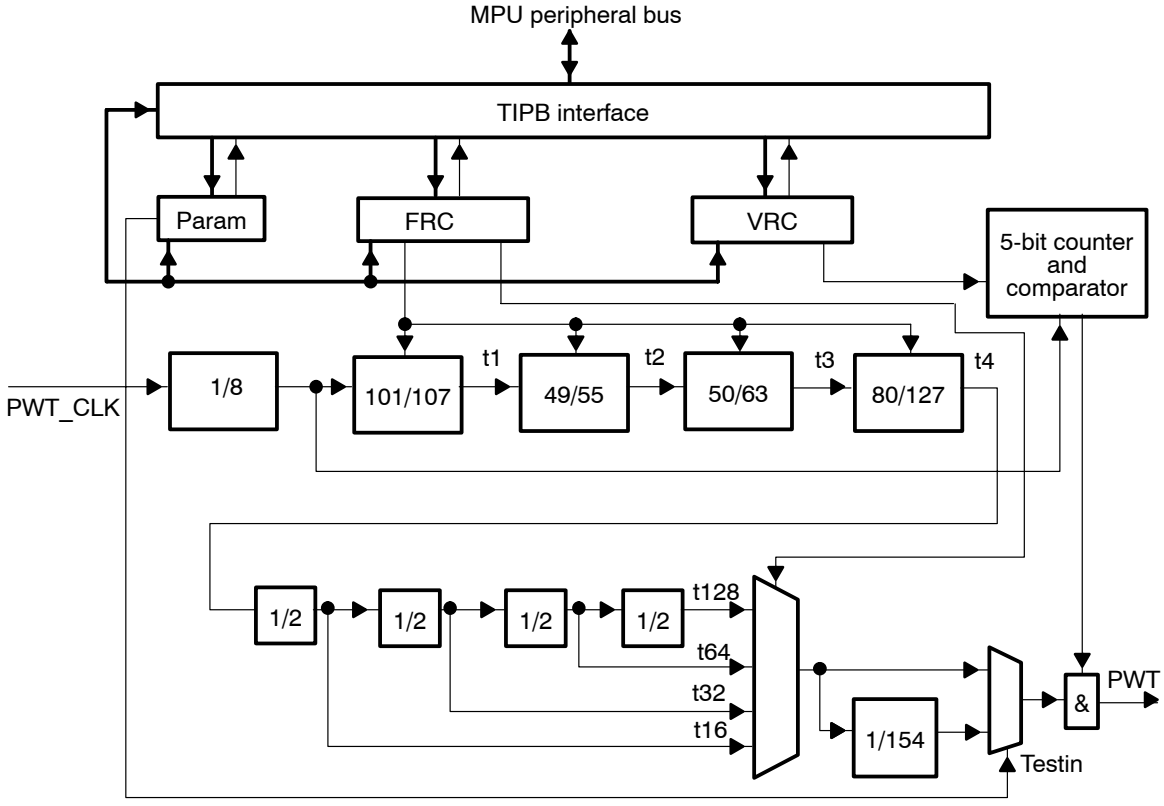
The pulse-width tone (PWT) module generates a modulated frequency signal for driving an external buzzer. The frequency is programmable with 12 half-tone frequencies per octave. The volume level is also programmable. All frequencies are generated from the PWT_CLK, which is a 12 or 13 MHz clock derived in the Clock and Reset Management module.

2.1 PWT Features

The PWT module has the following features (see Figure 3):

- ❑ Frequency control
- ❑ Octave selection
- ❑ Volume control
- ❑ Clock enable

Figure 3. PWT Block Diagram



Note: FRC = Frequency Control Register and VRC = Voltage Control Register

2.2 PWT Registers

Start address (hex): FFFB: 6000

Table 4 lists the PWT registers. Table 5 through Table 7 describe the individual registers.

Table 4. PWT Registers

Register	Description	R/W	Size	Address
FRC	PWT frequency control	R/W	8 bits	FFFB:6000
VRC	PWT volume control	R/W	8 bits	FFFB:6004
GCR	PWT general control	R/W	8 bits	FFFB:6008

Table 5. PWT Frequency Control Register (FRC) Field Descriptions

Bits	Field	Descriptions	R/W	Reset Value
7–6	Reserved			
5–2	FRQ	Frequency selection (12 frequencies: 0000–1011, 11xx illegal)	R/W	0000
1–0	OCT	Octave selection	R/W	00

Table 6. PWT Volume Control Register (VRC) Field Descriptions

Bits	Field	Descriptions	R/W	Reset Value
7	Reserved			
6–1	VOL	Volume selection	R/W	000000
0	ONOFF	Switch ON/OFF tone (on: 1, off: 0).	R/W	0

Table 7. PWT General Control Register (GCR) Field Descriptions

Bits	Field	Descriptions	R/W	Reset Value
7–2	Reserved			
1	TESTIN	Divider 1/154 switched ON/OFF (on: 0, off: 1).	R/W	0
0	CLK_EN	PWT clock enable (clock disabled: 0, clock enabled: 1).	R/W	0

2.3 PWT Programming

2.3.1 Buzzer Frequency

To obtain the required frequencies, the PWT clock is fed through a series of dividers. Four frequency dividers with the coefficients $^{101}/_{107}$, $^{49}/_{55}$, $^{50}/_{63}$, and $^{80}/_{127}$ are connected in series and can be enabled with the four frequency selection bits (FRQ) in the frequency control register (FRC). If a divider is not enabled, the clock passes through the divider without any change. The octave selection bits (OCT) in the FRC provide a range of four octaves (12, 14, 18, 116).

The clock is further divided by 154 to generate the required frequencies on the PWT output. Frequency examples generated from a 12 MHz PWT_CLK are shown in Table 8).

Table 8. Buzzer Frequencies (With 12 MHz PWT_CLK)

FRC FREQ OCT	Buzzer Frequency	FRC FREQ OCT	Buzzer Frequency
0000 00	4868 Hz	0000 10	1217 Hz
0001 00	4595 Hz	0001 10	1149 Hz
0010 00	4337 Hz	0010 10	1084 Hz
0011 00	4093 Hz	0011 10	1023 Hz
0100 00	3864 Hz	0100 10	966 Hz
0101 00	3647 Hz	0101 10	912 Hz
0110 00	3442 Hz	0110 10	860 Hz
0111 00	3249 Hz	0111 10	812 Hz
1000 00	3066 Hz	1000 10	767 Hz
1001 00	2894 Hz	1001 10	723 Hz
1010 00	2732 Hz	1010 10	683 Hz
1011 00	2579 Hz	1011 10	644 Hz
0000 01	2434 Hz	0000 11	608 Hz
0001 01	2297 Hz	0001 11	574 Hz
0010 01	2168 Hz	0010 11	541 Hz
0011 01	2046 Hz	0011 11	511 Hz
0100 01	1932 Hz	0100 11	483 Hz

Table 8. Buzzer Frequencies (With 12 MHz PWT_CLK) (Continued)

FRC FREQ OCT	Buzzer Frequency	FRC FREQ OCT	Buzzer Frequency
0101 01	1824 Hz	0101 11	456 Hz
0110 01	1721 Hz	0110 11	430 Hz
0111 01	1624 Hz	0111 11	406 Hz
1000 01	1533 Hz	1000 11	383 Hz
1001 01	1447 Hz	1001 11	361 Hz
1010 01	1366 Hz	1010 11	341 Hz
1011 01	1289 Hz	1011 11	322 Hz
		11XX XX	Not allowed

2.3.2 Buzzer Volume

The buzzer volume can be programmed (see Table 9) with the VOL bits (6 to 1) in the volume control register (VRC). The higher the 6 bit value, the louder the buzzer. For each period of the PWT output, the signal is held high for VOL+1 PWT_CLK periods. PWT is held low for the remainder of the period.

- ❏ VOL value: 0 =<y<64
- ❏ Output signal H pulse width = (y+1) x (PWT_CLK period)

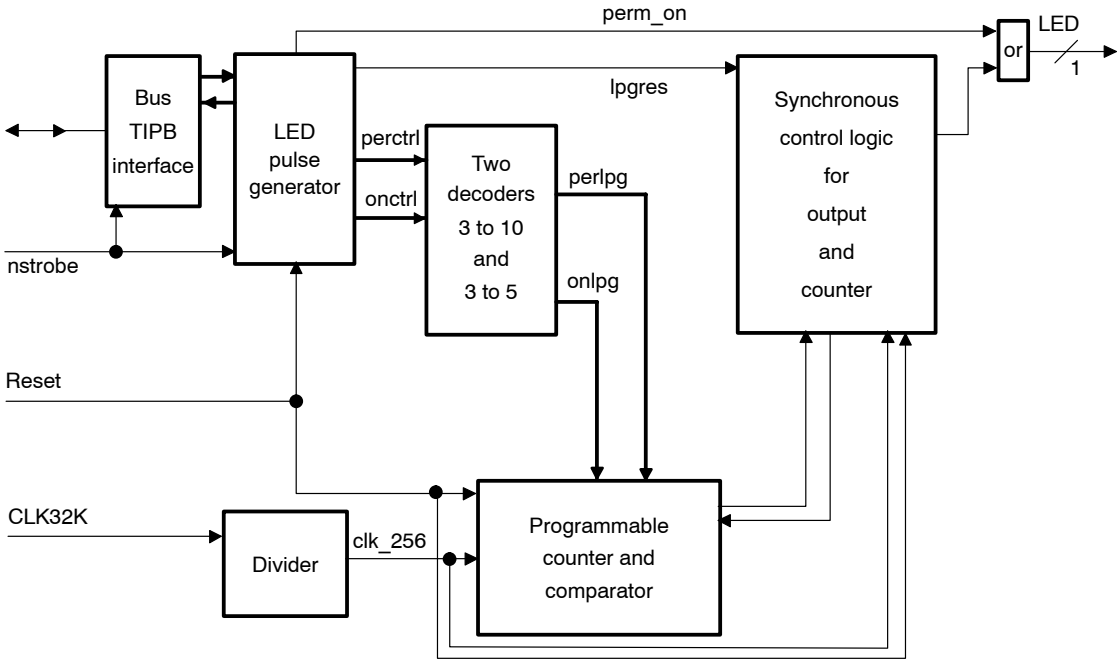
Table 9. Buzzer Volume

VRC Bits 6-1 ; 0	Buzzer/Loudspeaker
111111 1	Loud
000000 1	Quiet
xxxxx 0	Off

3 LED Pulse Generator

The LED pulse generator (LPG) module controls indicator LEDs (see Figure 4). The blinking period is programmable between 152 ms and 4s, and the LED can be switched on permanently. The OMAP5910 device has two LED modules. Each LED module drives a single output pin (LED1, LED2) on the OMAP5910 device which can be used to switch an LED driver.

Figure 4. LED Pulse Generator Block Diagram



3.1 Features

The LPG has the following programmable features:

- Blink period
- Pulse width
- Power management

3.2 LED Pulse Generator

LCR LPGRES (bit 6) = 0 resets the pulse generator and switches off the LED. It is possible to switch on the LED independently from the pulse generator circuit with LCR PERM_ON (bit 7) set to 1. A device reset causes a reset to the LPG and the output (LED) is held low.

3.3 LED Pulse Generator Power Management

The LPG input clock comes from the 32-kHz ULPD clock because it must work even when the OMAP5910 system is in deep sleep mode. The internal clock of the LPG runs at 256 Hz. For the lowest power, the power management register (PMR) CLK_EN (bit 0) should be set to 0 if the LPG is not used.

3.4 LED Pulse Generator Registers

The registers for the two LPGs are mapped in the OMAP5910 device at the following addresses:

- ❏ LPG1 address is FFFB:D000
- ❏ LPG2 address is FFFB:D800

Table 10 lists the LPG control and power management registers. Table 11 through Table 14 describe the register bits.

Table 10. LED Pulse Generator Control and Power Management Registers

Register	Description	Access	Size	Offset (hex)
LCR	LPG control	R/W	8 bits	0x00
PMR	Power management	R/W	8 bits	0x04

Table 11. LPG Control Register (LCR) Field Descriptions

Bits	Field	Description	R/W	Reset Value
7	PERM_ON	Set high to force permanent light on.	R/W	0
6	LPGRES	LPG counter reset, active low.	R/W	0
5–3	ONCTRL	Time LED is on.	R/W	000
2–0	PERCTRL	LED blink period.	R/W	000

The blinking period of the LED is programmable with LCR PERCTRL (bits 2–0). The various settings for the period are given in Table 12.

Table 12. LED Blinking Period Control (PERCTRL) Settings

PERCTRL	Period	Number of Clock Cyles (256 Hz)
000	125 ms	32
001	250 ms	64
010	500 ms	128
011	1 s	256
100	1.5 s	384
101	2 s	512
110	2.5 s	640
111	3 s	768

The on time (high pulse width) of the LED is programmable by LCR ONCTRL (bits 5–3).

Table 13. LED On Time (High Pulse Width)

ONCTRL	Time the LED is on	Number of Clock Cyles (256 Hz)
000	3.889 ms	1
001	7.789 ms	2
010	15.59 ms	4
011	31.39 ms	8
100	46.59 ms	12
101	62.59 ms	16
110	78.39 ms	20
111	93.59 ms	24

Table 14. Power Management Register (PMR) Field Descriptions

Bits	Field	Value	Description	R/W	Reset Value
7–1	Reserved				
0	CLK_EN		Functional clock enable:	R/W	0
		0	Clock disabled		
		1	Clock enabled		

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