TMS320TCI6484 DSP
Power/Sleep Controller (PSC)

User's Guide

Literature Number: SPRUFK1
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About This Manual

The TMS320TCI6484 device is single-core DSP platform architected primarily for the communications infrastructure market. This document covers the usage of the Power/Sleep Controller (PSC) in TMS320TCI6484 device.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320TCI6484 DSP. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

SPRS438 — *TMS320TCI6484 Communications Infrastructure Digital Signal Processor Data Manual.*

SPRU189 — *TMS320C6000 DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C6000 digital signal processors (DSPs).

SPRU198 — *TMS320C6000 Programmer's Guide.* Describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

SPRU301 — *TMS320C6000 Code Composer Studio Tutorial.* Introduces the Code Composer Studio™ integrated development environment and software tools.

SPRU321 — *Code Composer Studio Application Programming Interface Reference Guide.* Describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

SPRU871 — *TMS320C64x+ Megamodule Reference Guide.* Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRU190 — *TMS320C6000 DSP Peripherals Overview Reference Guide.* Provides a brief description of the peripherals available on the TMS320C6000 digital signal processors (DSPs).

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TMS320TCI6484 DSP Power/Sleep Controller (PSC)

1 Introduction/Feature Overview

The TMS320TCI6484 device is single-core DSP platform architected primarily for the communications infrastructure market. This document covers the usage of the Power/Sleep Controller (PSC) in TMS320TCI6484 device. The intent is not to keep this document as a user's guide, but to actually add this to the TMS320TCI6484 data manual, once it is available.

1.1 Purpose of the Peripheral

The purpose of the PSC is to reduce power when a module is not being utilized. In the TMS320TCI6484 system, the PSC is responsible for managing transitions of clock on/off and memory sleep on/off. The PSC provides the user with an interface to control several important power and clock operations. These operations are the focus of this document.

1.2 Features

The PSC includes the following features:

- Provides software interface to:
  - Control module memory sleep on/off.
  - Control module clock on/off.
  - Control CPU local resets.
- Supports emulation features: power, clock, and reset.

1.3 Terms and Abbreviations

3GPP — Third-Generation Partnership Project

CPU — Central Processing Unit of the C64x+ Core

DSP — Digital Signal Processor

GPSC — Global Power/Sleep Controller; manages the LPSCs.

LPSC — Local Power/Sleep Controller; one per module.

PSC — Power/Sleep Controller, including one GPSC and multiple LPSCs

RAC — Receive Accelerator, including GCCP cores, FEI, and BEI

RSA — Rake/Search Accelerator for accelerating CR functions

TCP — Turbo Coprocessor

VCP — Viterbi Coprocessor

WCDMA — Wideband Code Division Multiple Access

2 Power/Sleep Controller

2.1 Power and Reset Domains

The TCI6484 comprises several power domains to enable minimizing power dissipation for unused logic on the device. The GPSC is used to control sleep for memories within each power domain.

Additionally, clock gating to each of the logic blocks is managed by the LPSCs of each module. For modules with a dedicated clock or multiple clocks, the LPSC communicates with the PLL controller to enable and disable that module's clock(s) at the source. For modules that share a clock with other modules, the LPSC controls the clock gating.

Figure 1 shows the PSC components and the power and clock domains they control. Many modules reside in the *AlwaysOn* domain, that always has power and clocks provided. These consist primarily of the infrastructure components that are responsible for the clock and reset control (PLL Controller, PSC), the switch fabric that connects all of the modules, and small modules that do not need dynamic enable/disable because they do not consume a significant amount of power.

Figure 1. Power and Clock Domains

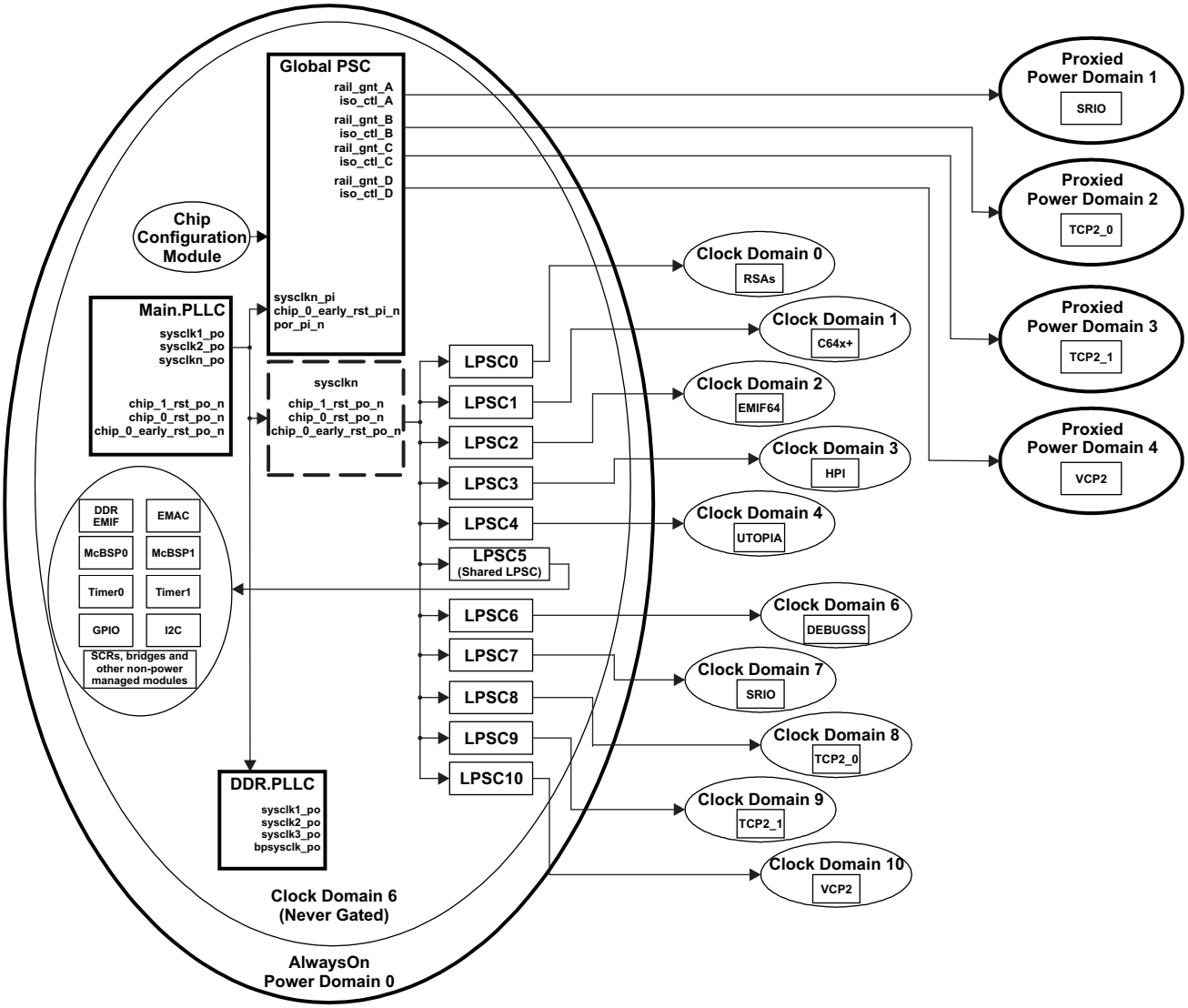


Table 1 summarizes the TCI6484 power domains.

Table 1. TCI6484 Power Domains

Domain	Block(s)	Note	Power Connection
AlwaysOn	Core, L1/L2 RAMs	L2 RAMs can sleep	Software power-down from the CPU
AlwaysOn	Most peripheral logic	Cannot be disabled	Always on
AlwaysOn	I/O: All 1.8-/3.3-V LVCMOS I/O, most peripherals	Cannot be disabled	Always on
A	RapidIO	RAMs can sleep	Software control
B	TCP2_0	RAMs can sleep	Software control
C	TCP2_1	RAMs can sleep	Software control
D	VCP2	RAMs can sleep	Software control

Table 2 summarizes the TMS320TCI6484 clock domains. These may also be referred to later in the document as modules.

Table 2. TCI6484 Clock Domains

LPSC Number	Module(s)	Notes
0	RSAs	Software control
1	CPU	Cannot be controlled; always on
2	EMIF64	Software control
3	HPI	Software control
4	UTOPIA	Software control
5	Shared LPSC for all modules other than those listed in this table.	Cannot be controlled; always on
6	DEBUGSS	Software control
7	SRIO	Software control
8	TCP2_0	Software control
9	TCP2_1	Software control
10	VCP2	Software control
No LPSC	Bootcfg, PSC, Main PLLCTL, Efuse, and DFT.	These modules do not use LPSC.

2.2 Power Domain and Module States Defined

The PSC module organizes modules into different power domains and into different modules (clock domains). Note that there is no relationship between a power domain and a module. These are completely separate entities and may be controlled separately.

2.2.1 Power Domain States

A power domain can only be in one of two states: **ON** or **OFF**, defined as follows:

- **ON:** Power to the power domain is on. Memories are awake.
- **OFF:** Power to the power domain is off. Memories are asleep (low-leakage standby mode).

In the TCI6484 device, the AlwaysOn power domain is always in the ON state, when the chip is powered on. The other power domains, however, can be in either the ON or OFF state; i.e., the memory for a specific module can remain powered down if it is not used.

2.2.2 Module States

A module can be in one of two states: **Enable** or **SwRstDisable**. As shown in Table 3, these two states correspond to combinations of module reset asserted or de-asserted and module clock on or off. Note that module reset is defined to completely reset a given module, such that all hardware is put back into its default state. For more information on module reset, see Curie Chip Architecture (XXXX-SYS-FS-001) Revision XXXX.

Table 3. Module States

Module State	Module Reset	Module Clock
Enable	De-asserted	ON
SwRstDisable	Asserted	OFF

The module states are defined as follows:

- **Enable:** A module in the Enable state has its module reset de-asserted and its clock on. This is the normal run-time state for a given module.
- **SwRstDisable:** A module in the SwResetDisable state has its module reset asserted and its clock OFF. This state is not expected to be initiated by software.

2.2.3 Local Reset

In addition to module reset described in the previous section, the C64x+ CPU can be reset using a special local reset. When local reset is asserted, the internal memories (L1P, L1D, and L2) for the core are still accessible. The local reset only resets the corresponding C64x+ core, not the rest of the chip. Local reset is intended to be used by the watchdog timers to reset the C64x+ core in the event of an error. The procedures for asserting and de-asserting local reset are as follows (Y denotes the module domain number):

- Set **MDCTL[Y].LRSTZ** to 0x0 to assert local reset.
- Set **MDCTL[Y].LRSTZ** to 0x1 to de-assert local reset. The 64x+ core immediately executes program instructions after reset is de-asserted. Note that the boot sequence does not re-occur unless there is a chip-level reset. Execution of code previously in L2 begins execution.

2.3 Executing State Transitions

This section describes how to execute state transitions for power domains and modules. Examples show how to enable only power domains, only modules, or a combination. Although you have complete control of the sequencing, for TI recommendations, see Section 2.3.4.

2.3.1 Power Domain State Transitions

This section describes the basic procedure for transitioning the state of a power domain which, in the case of the TCI6484 device is limited to the memories located in a particular domain. The majority of the modules on the chip are always in the ON state. The PSC handles all required internal operations to wake memories for the controlled power domains.

Note: As mentioned previously, in the TCI6484 device there are multiple power domains. The AlwaysOn power domain is always in the ON state when the chip is powered-on, and therefore it is not possible to transition this domain to the OFF state. Conversely, the other domains are in the OFF states when the chip is powered-on. Transitions from ON to OFF are never allowed.

The procedure for power domain state transitions follows (X denotes the power domain number, Y denotes the module domain number):

- Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. Wait for any previously initiated transitions to finish before initiating a new transition.

- Set **PDCTL[X].NEXT** for an ON (0x1) transition. Note: When **PTCMD.GO[X]** is set to 0x1 in the next step, the **PDCTL[X].NEXT** field of this power domain and the **MDCTL[Y].NEXT** field of the module in this power domain are evaluated. Therefore, you may set the **MDCTL[Y].NEXT** field for multiple modules before executing this step. Note that, if enabling other modules, ensure that if they are not in the AlwaysOn domain, the memories for that module are not asleep.
- Set **PTCMD.GO[X]** to 0x1 to initiate the state transition(s). The PSC awakens the memory for that particular domain.
- Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. The domain is safely in the new state only after **PTSTAT.GOSTAT[X]** is cleared to 0x0.

2.3.2 Module State Transitions

This section describes the procedure for transitioning the module state.

Note: In the TCI6484 device, the following procedure is directly applicable for all LPSC-controlled modules, except the C64x+ core domains. To transition the module state, you must be aware of several system considerations. Transitions from Enable to any other state are not allowed. Also, before transitioning a module to Enable, if the memories are not in the AlwaysOn power domain, they must be turned on before or in parallel with the transition. See Section 2.3.1.

The procedure for module state transitions follows (X denotes the power domain number, Y denotes the module domain number):

- Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. Wait for any previously initiated transitions to finish before initiating a new transition.
- Set **MDCTL[Y].NEXT** to Enable (0x3). Note that you may set transitions in multiple **MDCTL[Y].NEXT** fields in this step as long as the corresponding power domain is on.
- Set **PTCMD.GO[X]** to 0x1 to initiate the transition(s).
- Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. The module is safely in the new state only after **PTSTAT.GOSTAT[X]** clears to 0x0.

2.3.3 Concurrent Power Domain/Module State Transitions

This section describes the basic procedure for transitioning the state of a power domain and module domain for modules which are not in the AlwaysOn domain. You may do these separately as described in the sections above, if desired.

The procedure for concurrent power domain/module state transitions follows (X denotes the power domain number, Y denotes the module domain number):

- Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. Wait for any previously initiated transitions to finish before initiating a new transition.
- Set **PDCTL[X].NEXT** for an ON (0x1) transition.
- Set **MDCTL[Y].NEXT** to Enable (0x3). Note that you may set transitions in multiple **MDCTL.NEXT** fields in this step as long as the corresponding power domain is on.
- Set **PTCMD.GO[X]** 0x1 to initiate the state transition(s). The PSC awakens the memory for that particular domain, starts the module clock, then de-asserts the module reset.
- Wait for **PTSTAT.GOSTAT[X]** to clear to 0x0. The domain is safely in the new state only after **PTSTAT.GOSTAT[X]** is cleared to 0x0.

2.3.4 Recommendations for Power Domain/Module Sequencing

As noted in Section 2.2 and Section 2.3, a particular peripheral's power domain must be enabled before the module is enabled.

Unless there is a system level reason to perform both functions separate from each other, the recommendation is to use the sequence listed in Section 2.3.3 rather than individual sequencing. Even though a single write to the appropriate GO bit starts the power domain and module transition, it is still sequenced such that the memory is guaranteed to awaken before the module is enabled. Thus, there is no ill effect in performing these together.

It is important to know that when a power domain is enabled that all memories for that module are immediately moved from a low-leakage sleep state to an active awake state. This means that there will be a spike in power consumption for that particular time, in other words di/dt will be affected. To minimize the effect on di/dt of enabling power domains, it is recommended to power up modules one at a time. It is also recommended that all modules be initialized early in the application to avoid a large spike in di/dt during normal operation where the application may already be drawing a fair amount of current from the supply.

2.4 Emulation Support in the PSC

The PSC supports commands that allow emulation tools to have some control over the state of power domains and modules.

In particular, the PSC supports the following emulation commands:

- Power on and enable features:
  - **Force Power:** Allows emulation to force the power domain into and ON state.
  - **Force Active:** Allows emulation to force the power domain into and ON state and force the module into the Enable state.
- Reset features:
  - **Assert Reset:** Allows emulation to assert the module's local reset.
  - **Wait Reset:** Allows emulation to keep local reset asserted for an extended period of time after software initiates local reset de-assert.
  - **Block Reset:** Allows emulation to block software initiated local and module resets.

Local reset applies only to the C64x+ core domains; module reset applies to all other domains.

3 PSC Registers

This section includes the PSC memory map and bit registers.

3.1 Power and Sleep Controller (PSC) Register Map

This section includes the PSC memory map and bit registers. Table 4 provides the PSC register memory map.

Table 4. PSC Register Memory Map

Offset	Register	Description	See
0x0	PID	Peripheral Revision and Class Information	Section 3.2.1
0x014	VCNTLID	Voltage Control Identification Register	Section 3.2.2
0x120	PTCMD	Power Domain Transition Command Register	Section 3.2.3
0x128	PTSTAT	Power Domain Transition Status Register	Section 3.2.4
0x200	PDSTATx	Power Domain Status Register 0-5	Section 3.2.5
0x300	PDCTL0	Power Domain Control Register 0 (AlwaysOn)	Section 3.2.6
0x304	PDCTL1	Power Domain Control Register 1 (Serial RapidIO)	Section 3.2.6
0x308	PDCTL2	Power Domain Control Register 2 (TCP2_0)	Section 3.2.6
0x30C	PDCTL3	Power Domain Control Register 3 (TCP2_1)	Section 3.2.6
0x310	PDCTL4	Power Domain Control Register 4 (VCP2)	Section 3.2.6
0x800	MDSTAT0	Module Status Register 0 (C64x+ Core RSAs)	Section 3.2.7
0x804	MDSTAT1	Module Status Register 1 (C64x+ Core)	Section 3.2.7
0x808	MDSTAT2	Module Status Register 2 (EMIF64)	Section 3.2.7
0x80C	MDSTAT3	Module Status Register 3 (HPI)	Section 3.2.7
0x810	MDSTAT4	Module Status Register 4 (UTOPIA)	Section 3.2.7
0x814	MDSTAT5	Module Status Register 5 (Never Gated)	Section 3.2.7
0x818	MDSTAT6	Module Status Register 6 (DEBUGSS)	Section 3.2.7
0x81C	MDSTAT7	Module Status Register 7 (Serial RapidIO)	Section 3.2.7
0x820	MDSTAT8	Module Status Register 8 (TCP2_0)	Section 3.2.7
0x824	MDSTAT9	Module Status Register 9 (TCP2_1)	Section 3.2.7
0x828	MDSTAT10	Module Status Register 10 (VCP2)	Section 3.2.7
0xA00	MDCTL0	Module Control Register 0 (C64x+ Core RSAs)	Section 3.2.8
0xA04	MDCTL1	Module Control Register 1 (C64x+ Core)	Section 3.2.8
0xA08	MDCTL2	Module Control Register 2 (EMIF64)	Section 3.2.8
0xA0C	MDCTL3	Module Control Register 3 (HPI)	Section 3.2.8
0xA10	MDCTL4	Module Control Register 4 (UTOPIA)	Section 3.2.8
0xA14	MDCTL5	Module Control Register 5 (Never Gated)	Section 3.2.8
0xA18	MDCTL6	Module Control Register 6 (DEBUGSS)	Section 3.2.8
0xA1C	MDCTL7	Module Control Register 7 (Serial RapidIO)	Section 3.2.8
0xA20	MDCTL8	Module Control Register 8 (TCP2_0)	Section 3.2.8
0xA24	MDCTL9	Module Control Register 9 (TCP2_1)	Section 3.2.8
0xA28	MDCTL10	Module Control Register 10 (VCP2)	Section 3.2.8

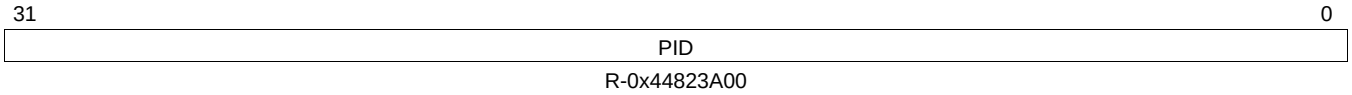
3.2 Register Descriptions

This section describes, in detail, the module registers with a register figure and a description table for each. Each register figure identifies the bit field, the register name, read/write capability, and the default.

3.2.1 Peripheral Identification Register (PID)

The peripheral identification register is shown in Figure 2 and described in Table 5. The PID offset is 0.

Figure 2. Peripheral Identification Register (PID)



LEGEND:R = Read only; -*n* = value after reset

Table 5. Peripheral Identification Register (PID) Field Descriptions

Bit	Field	Value	Description
31-0	PID		Peripheral ID used to differentiate different modules in the system

3.2.2 Voltage Control Identification Register (VCNTLID)

The TMS320TCI6484 device has four VCNTL output pins to control core voltage selection through the SmartReflex™ mechanism. These output values are also captured in the VCNTLID register. VCNTL3 through VCNTL0 pin values are reflected in VCNTLID[27:24]. For more details on SmartReflex and VCNTL pin mapping to the core voltage, see the *TMS320TCI6484 Hardware Design Guide* application report (SPRAAV7). The VCNTLID register is shown in Figure 3 and described in Table 6.

Figure 3. Voltage Control Identification Register (VCNTLID)

31 28	27 24	23 20	19 16
Reserved	VCNTL	VCNTL_MAX	VCNTL_MIN
R-0	R-0	R-0	R-0

15 0
Reserved
R-0

LEGEND: R = Read only; -*n* = value after reset

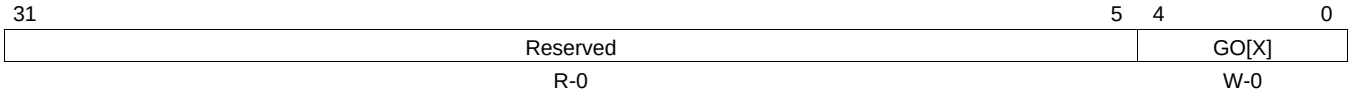
Table 6. Voltage Control Identification Register (VCNTLID) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved		Reserved
27-24	VCNTL	0x0	Current voltage control value. Mapped to VCNTL[3:0] chip output pins.
23-20	VCNTL_MAX	0x0	E-fuse voltage control value for Max temperature.
19-16	VCNTL_MIN	0x0	E-fuse voltage control value for Min temperature.
15-0	Reserved	0	Reserved

3.2.3 Power Domain Transition Command Register (PTCMD)

The power domain transition command register is shown in Figure 4 and described in Table 7.

Figure 4. Power Domain Transition Command Register (PTCMD)



LEGEND: R = Read only; W = Write only; -*n* = value after reset

Table 7. Power Domain Transition Command Register (PTCMD) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved		Reserved
4-0	GO[X]		Power domain GO transition command (X denotes power domain number).
		1	Write 1 to cause the state transition interrupt generation block to evaluate the new PTNEXT and MDCTL.NEXT states as the application desired states.

3.2.4 Power Domain Transition Status Register (PTSTAT)

The power domain transition status register is shown in Figure 5 and described in Table 8. PSTST offset is 0x128.

Figure 5. Power Domain Transition Status Register (PTSTAT)

31	5	4	0
Reserved		GOSTAT[X]	
R-0		R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 8. Power Domain Transition Status Register (PTSTAT) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved		Reserved
4-0	GOSTAT[X]		Power domain transition status (X denotes power domain number).
		0	No transition in progress.
		1	Power domain is transitioning (i.e., either the power domain is transitioning or modules in this power domain are transitioning).

3.2.5 Power Domain Status Register 0-4 (PDSTATx)

The power domain status register 0-4 is shown in Figure 6 and described in Table 9. PDSTAT[X] offset is 0x200.

Figure 6. Power Domain Status Register 0-4 (PDSTATx)

31	16
Reserved	
R-0	

15	10	9	8	7	2	1	0
Reserved		Rsvd		Reserved		STATE	
R-0		R-1		R-0		R(A)	

LEGEND: R = Read only; -*n* = value after reset

A. Default value after reset: AlwaysOn domain -1; other domains -0.

Table 9. Power Domain Status Register 0-4 (PDSTATx) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved		Reserved
1-0	STATE		Power domain status
		0	Power Domain is in the OFF state.
		1	ower Domain is in the ON state.

3.2.6 Power Domain Control Register 0-4 (PDCTLx)

The power domain control register 0-4 is shown in Figure 7 and described in Table 10. PDSTAT[X] offset is 0x300 - 0x310.

Figure 7. Power Domain Control Register 0-4 (PDCTLx)

31	30	29 28	27 24	23 16
Rsvd	Rsvd	Reserved	Reserved	Reserved
R/W-0	R-0	R/W-0	R-0	R/W(A)

15 12	11 10	9 8	7 1	0
Reserved	Reserved	Reserved	Reserved	NEXT
R/W(B)	R-0	RW-0	R-0	R/W(C)

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

A. Default value after reset: AlwaysOn domain -0x01; other domains -0x33.
B. Default value after reset: AlwaysOn domain -0xB; other domains -0x8.
C. Default value after reset: AlwaysOn domain -1; other domains -0.

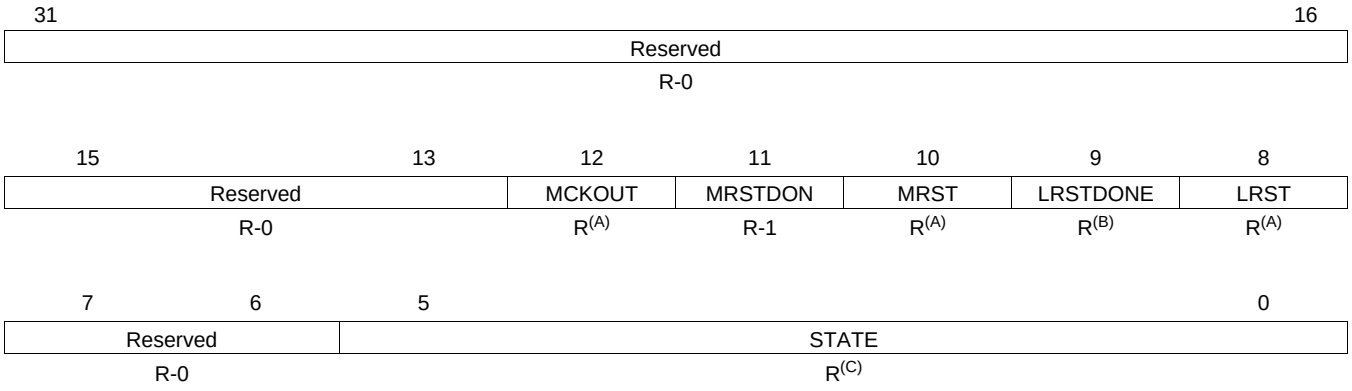
Table 10. Power Domain Control Register 0-4 (PDCTLx) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved		Reserved
0	NEXT		Power domain next state
		0	Power domain off.
		1	Power domain on.
		Others	Indicates transition.

3.2.7 Module Status Register 0-10 (MDSTATy)

The module status register 0-10 is shown in Figure 8 and described in Table 11. MDSTAT[Y] offset is 0x800 - 0x828.

Figure 8. Module Status Register 0-10 (MDSTATy)



LEGEND: R = Read only; -*n* = value after reset

A. Default value after reset: C64x+ domain and Never-Gated domain -1; other domains -0.
B. Default value after reset: C64x+ domain -0; other domains -1.
C. Default value after reset: C64x+ domain and Never-Gated domain -0x3; other domains -0.

Table 11. Module Status Register 0-10 (MDSTATy) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved		Reserved
12	MCKOUT		Module clock output status. Shows status of module clock; on/off.
		0	Module clock is off.
		1	Module clock is on.
11	MRSTDONE		Module reset done. Software is responsible for checking that mode reset is done before accessing the module.
		0	Module reset is not done.
		1	Module reset is done.
10	MRST		Module reset status. Reflects actual state of module reset.
		0	Module reset is asserted.
		1	Module reset is de-asserted.
9	LRSTDONE		Local reset done. Software is responsible for checking that local reset is done before accessing this module.
		0	Local reset is not done.
		1	Local reset is done.
8	LRST		Module local reset status. (This bit applies to C64x+ domains only.)
		0	Local reset is asserted.
		1	Local reset is de-asserted.
7-6	Reserved		Reserved
5-0	STATE		Module state status. Indicates current module status.
		0	SwRstDisable state.
		0x3	Enable state.
		Others	Reserved.

3.2.8 Module Control Register 0-10 (MDCTLy)

The module control register 0-10 is shown in Figure 9 and described in Table 12. MDCTL[Y] offset is 0xA00 - 0xA28.

Figure 9. Module Control Register 0-10 (MDCTLy)

31	30	16
Rsvd	Reserved	
R/W-0	R-0	

15	13	12	9	8	7	5	4	0
Reserved		Reserved		LRST	Reserved		NEXT	
R-0		R/W-0		R/W-1	R-0		R/W(A)	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

A. Default value after reset: C64x+ domain and Never-Gated domain -0x3; other domains -0.

Table 12. Module Control Register 0-10 (MDCTLy) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved		Reserved
8	LRST		Module local reset control. (This bit applies to C64x+ modules only.)
		0	Assert local reset.
		1	De-assert local reset.
7-5	Reserved		Reserved
4-0	NEXT		Module next state.
		0	SwRstDisable state.
		0x3	Enable state.
		Others	Reserved.

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