AM17x/AM18x ARM Microprocessor 64-Bit Timer Plus

User's Guide

Literature Number: SPRUFW2C
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About This Manual

This document describes the operation of the software-programmable 64-bit Timer Plus.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DSP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUGU3 — ***AM1705 ARM Microprocessor System Reference Guide.*** Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUGR6 — ***AM1707 ARM Microprocessor System Reference Guide.*** Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUGX5 — ***AM1802 ARM Microprocessor System Reference Guide.*** Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUGU4 — ***AM1806 ARM Microprocessor System Reference Guide.*** Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUGM9 — ***AM1808/AM1810 ARM Microprocessor System Reference Guide.*** Describes the ARM subsystem, system memory, memory protection unit (MPU), device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUFU0 — ***AM17x/AM18x ARM Microprocessor Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the AM17x/AM18x ARM Microprocessors.

64-Bit Timer Plus

1 Introduction

This document describes the operation of the software-programmable 64-bit Timer Plus. The number of supported Timer modules will vary between devices. The 64-bit Timer Plus can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode. Some Timer Plus implementations have signal connections to internal device reset that can be used in watchdog timer mode. New features over previous timers include: external clock/event input, period reload, external event capture, and timer counter register read reset.

1.1 Purpose of the Peripheral

The timer can support four basic modes of operation: a 64-bit general-purpose (GP) timer, dual unchained 32-bit GP timers, dual chained 32-bit timers, or a watchdog timer. The GP timer modes can be used to generate periodic interrupts and DMA synchronization events. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition (such as a non-exiting code loop).

1.2 Features

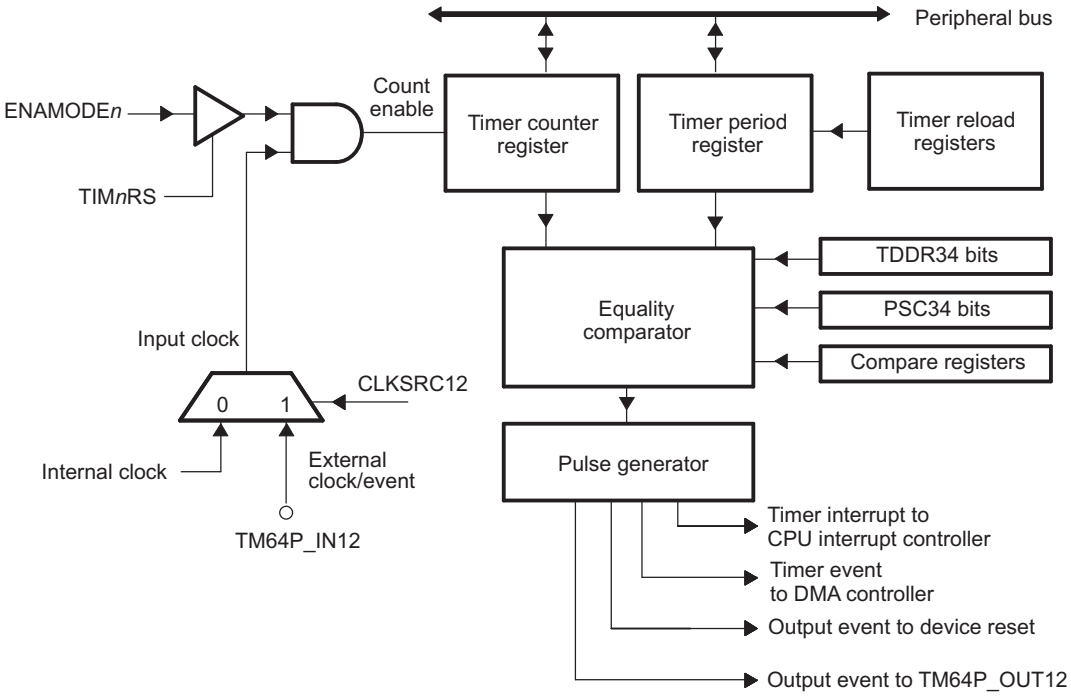
The 64-bit timer consists of the following features -- some features may not be supported on all timer instantiations (see your device-specific data manual for supported features):

- 64-bit count-up counter
- Timer modes:
  - 64-bit general-purpose timer mode
  - Dual 32-bit unchained general-purpose timer mode
  - Dual 32-bit chained timer mode
  - Watchdog timer mode
- 2 possible clock sources:
  - Internal clock
  - External clock/event input via timer input pins
- 3 possible operation modes:
  - One-time operation (timer runs for one period then stops)
  - Continuous operation (timer automatically resets to zero after each period and continues to operate)
  - Continuous operation with period reload (timer automatically assumes the value of the reload registers after each period and continues to operate)
- Generates interrupts to CPU
- Generates sync events to DMA
- Generates output event to device reset (watchdog only)
- Generates output event to timer output pins (if pins are available)
- External event capture via timer input pins (if pins are available)

1.3 Block Diagram

A block diagram of the timer is shown in Figure 1. Detailed information about the architecture and operation of the timers is in Section 2.1 and Section 2.2.

Figure 1. Timer Block Diagram



1.4 Industry Standard Compatibility Statement

This peripheral is not intended to conform to any specific industry standard.

2 Architecture

2.1 Architecture – General-Purpose Timer Mode

This section describes the timer in the general-purpose (GP) timer mode.

2.1.1 Backward Compatible Mode

The Timer Plus supports the following additional features over the other timers:

- External clock/event input
- Period reload
- External event capture mode
- Timer counter register read reset mode
- Timer counter capture registers
- Register for interrupt/DMA generation control and status

By default, period reload, external event capture mode, timer counter register read reset mode, timer counter capture registers, and interrupt/DMA/TM64P_OUT generation control and status are not available. To enable these features, you must set the PLUSEN bit in the timer global control register (TGCR). These features are described throughout the following sections. External clock/event input is always available, regardless of the state of the backward compatible bit.

2.1.2 Clock Control

The timer can use an internal or external clock source for the counter period. The following sections explain how to select the clock source.

As shown in Table 1 and Figure 2, the timer clock source is selected using the clock source (CLKSRC12) bit in the timer control register (TCR). Two clock sources are available to drive the timer clock:

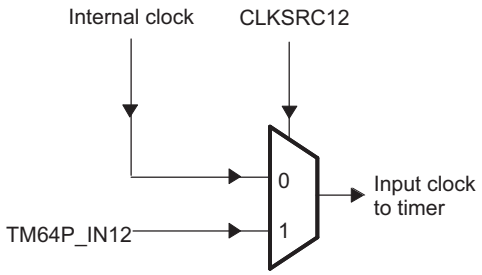
- internal clock by setting CLKSRC12 = 0.
- external clock on input pin TM64P_IN12 by setting CLKSRC12 = 1.

At reset, the clock source is the internal clock. Details on each of the clock source configuration options are included in the following sections.

Table 1. Timer Clock Source Selection

CLKSRC12	Input Clock
0	Internal clock (default)
1	External clock on timer input

Figure 2. Timer Clock Source Block Diagram



2.1.2.1 Using the Internal Clock Source to the Timer

The internal clock source to the timer is generated by the PLL controller. This clock source determines the speed of the timer since the timer counts up in units of source clock cycles. When determining the period and prescaler settings for the timer, choose the desired period in units of source clock cycles. For details on the generation of the on-chip clocks, see your device-specific *System Reference Guide*.

The CLKSRC12 parameter in the timer control register (TCR) determines whether an internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, CLKSRC12 controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 01 in TGCR), CLKSRC12 controls the timer 1:2 side of the timer only.

To select the internal clock as the clock source for the timer, CLKSRC12 in TCR must be cleared to 0.

2.1.2.2 Using the External Clock Source to the Timer

An external clock source can be provided to clock the timer through the timer input pin TM64P_IN12. The CLKSRC12 parameter in the timer control register (TCR) determines whether an internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, CLKSRC12 controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 01 in TGCR), CLKSRC12 controls the timer 1:2 side of the timer only.

At reset, the clock source defaults to the internal clock. Details on each of the clock source configuration options are included in the following sections. To select the external clock as the clock source for the timer, CLKSRC12 in TCR must be set to 1. The external clock source frequency must be no greater than the timer peripheral reference clock (see your device-specific data manual).

2.1.3 Signal Descriptions

As shown in Figure 2, the TM64P_IN12 pin may be used as input to the timer. This signal can be used to drive the clock/event count or be used as an external event input for event capture mode. Pin TM64P_OUT12 may be used as an output from the timer to generate a clock or pulse signal.

2.1.4 Timer Modes

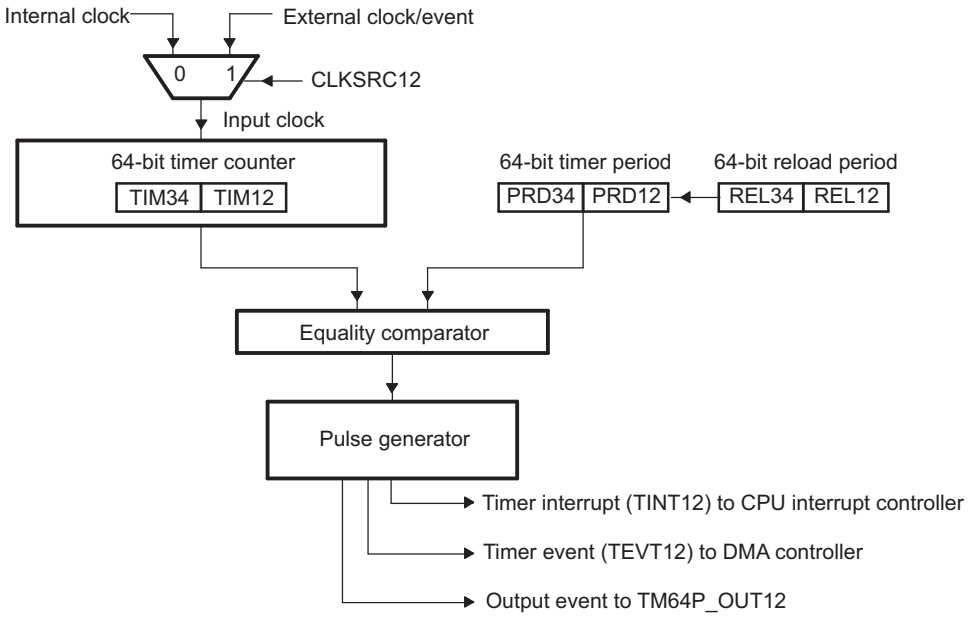
The following section describes the general-purpose (GP) timer modes.

2.1.4.1 64-Bit Timer Mode

The timer can be configured as a 64-bit timer by clearing the TIMMODE bit in the timer global control register (TGCR) to 0. At reset, 0 is the default setting for the TIMMODE bit.

In this mode, the timer operates as a single 64-bit up-counter (Figure 3). The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit timer period register. When the timer is enabled, the timer counter starts incrementing by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT12) and a timer EDMA (TEVT12) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using control bits in TGCR.

Figure 3. 64-Bit Timer Mode Block Diagram



2.1.4.1.1 Enabling the 64-Bit Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. For the timer to operate in 64-bit timer mode, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, enabled to run continuously, or enabled to run continuously with period reload; the ENAMODE34 bit has no effect in 64-bit timer mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again. When the timer is enabled for continuous operation with period reload (ENAMODE12 = 3h), the counter counts up until it reaches the period value, then resets itself to zero, reloads the period registers (PRD12 and PRD34) with the value in the period reload registers (REL12 and REL34), and begins counting again.

Table 2 shows the bit values in TGCR to configure the 64-bit timer.

Table 2. 64-Bit Timer Configurations

	TGCR Bit		TCR Bit
64-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**
To place the 64-bit timer in reset	0	0	0
To disable the 64-bit timer (out of reset)	1h	1h	0
To enable the 64-bit timer for one-time operation	1h	1h	1h
To enable the 64-bit timer for continuous operation	1h	1h	2h
To enable the 64-bit timer for continuous operation with period reload	1h	1h	3h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.1.4.1.2 Reading the Counter Registers

When reading the timer count in 64-bit timer mode, the CPU must first read TIM12 followed by TIM34. When TIM12 is read, the timer copies TIM34 into a shadow register. When reading TIM34, the hardware logic returns the shadow register value. This ensures that the values read from the registers are not affected by the fact that the timer may continue to run as the registers are read. When reading the timers in 32-bit mode, TIM12 and TIM34 may be read in any order.

2.1.4.1.3 64-Bit Timer Configuration Procedure

To configure the GP timer to operate as a 64-bit timer, follow the steps below:

1. Select 64-bit mode (TIMMODE in TGCR).
2. Remove the timer from reset (TIM12RS and TIM34RS in TGCR).
3. Select the desired timer period (PRD12 and PRD34).
4. Enable the timer (ENAMODE12 in TCR).
5. If ENAMODE12 = 3h, write the desired timer period for the next timer cycle in the period reload registers (REL12 and REL34). This step can be done at any time before the current timer cycle ends.

2.1.4.2 Dual 32-Bit Timer Modes

Each of the general-purpose timers can be configured as dual 32-bit timers by configuring the TIMMODE bit in the timer global control register (TGCR). In dual 32-bit timer mode, the two 32-bit timers can be operated independently (unchained mode) or in conjunction with each other (chained mode).

2.1.4.2.1 Chained Mode

The general-purpose timers can each be configured as a dual 32-bit chained timer by setting the TIMMODE bit to 3h in TGCR.

In the chained mode (Figure 4), one 32-bit timer (timer 3:4) is used as a 32-bit prescaler and the other 32-bit timer (timer 1:2) is used as a 32-bit timer. The 32-bit prescaler is used to clock the 32-bit timer. The 32-bit prescaler uses one counter register (TIM34) to form a 32-bit prescale counter register and one period register (PRD34) to form a 32-bit prescale period register.

When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated and the prescale counter register is reset to 0 (see the example in Figure 5).

The other 32-bit timer (timer 1:2) uses one counter register (TIM12) to form a 32-bit timer counter register and one period register (PRD12) to form a 32-bit timer period register. This timer is clocked by the output clock from the prescaler. The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT12) and a timer EDMA event (TEVT12) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS and TIM34RS bits in TGCR. In the chained mode, the upper 16-bits of the timer control register (TCR) are not used.

Figure 4. Dual 32-Bit Timers Chained Mode Block Diagram

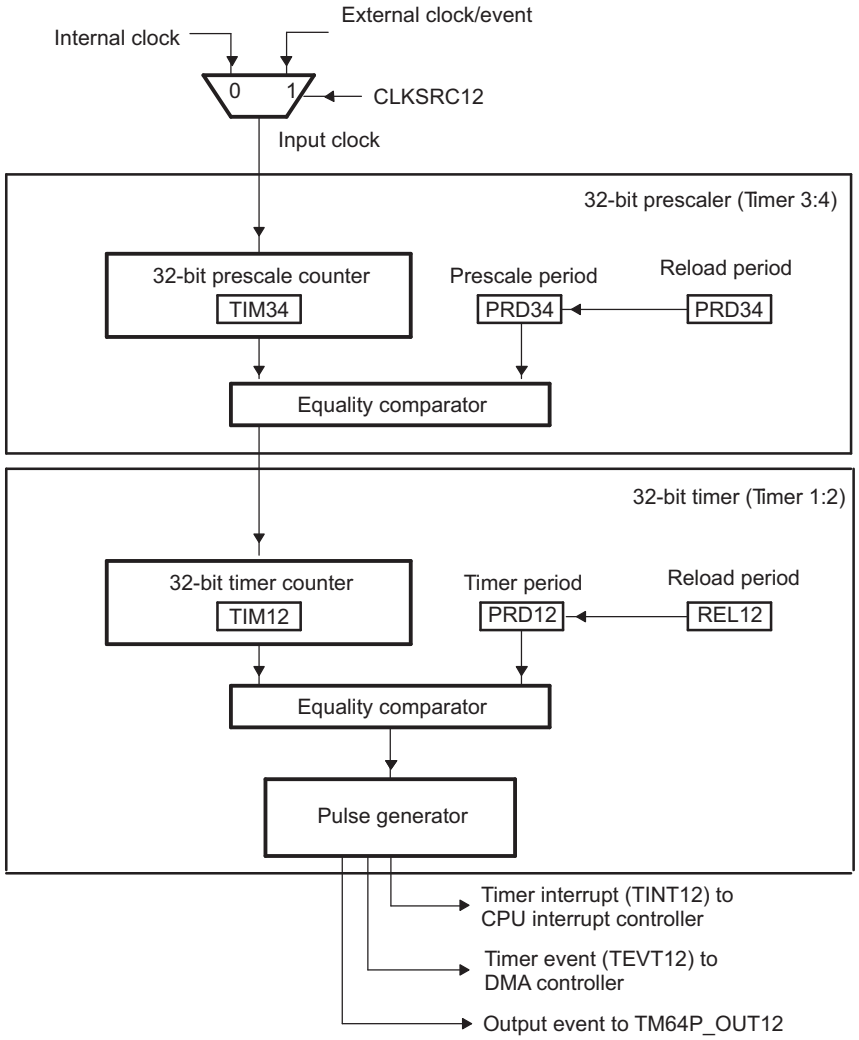
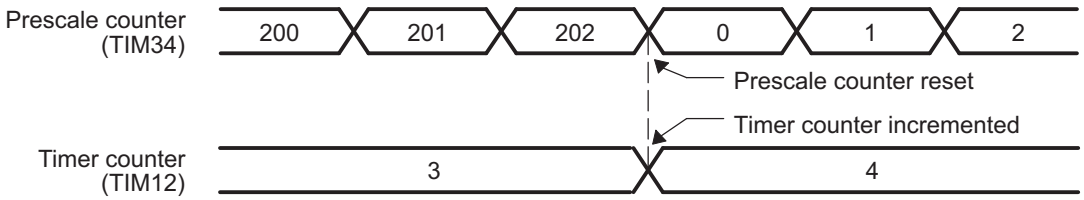


Figure 5. Dual 32-Bit Timers Chained Mode Example

32-bit prescaler settings: count = TIM34 = 200; period = PRD34 = 202
32-bit timer settings: count = TIM12 = 3; period = PRD12= 4



2.1.4.2.1.1 Enabling the 32-Bit Timer Chained Mode

The TIM12RS and TIM34RS bits in TGCR determine whether the timer is in reset, or if it is capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bits control the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, enabled to run continuously, or enabled to run continuously with period reload; the ENAMODE34 bit has no effect in 32-bit timer chained mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again. When the timer is enabled for continuous operation with period reload (ENAMODE12 = 3h), the counter counts up until it reaches the period value, then resets itself to zero, reloads the period registers (PRD12 and PRD34) with the value in the period reload registers (REL12 and REL34), and begins counting again.

Table 3 shows the bit values in TGCR to configure the 32-bit timer in chained mode.

Table 3. 32-Bit Timer Chained Mode Configurations

	TGCR Bit		TCR Bit
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**
To place the 32-bit timer chained mode in reset	0	0	0
To disable the 32-bit timer chained mode (out of reset)	1h	1h	0
To enable the 32-bit timer chained mode for one-time operation	1h	1h	1h
To enable the 32-bit timer chained mode for continuous operation	1h	1h	2h
To enable the 32-bit timer chained mode for continuous operation with period reload (Timer 3 only)	1h	1h	3h

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.1.4.2.1.2 32-Bit Timer Chained Mode Configuration Procedure

To configure the GP timer to operate as a dual 32-bit chained mode timer, follow the steps below:

1. Select 32-bit chained mode (TIMMODE in TGCR).
2. Remove the timer from reset (TIM12RS and TIM34RS in TGCR).
3. Select the desired timer period (PRD12).
4. Select the desired timer prescaler value (PRD34).
5. Enable the timer (ENAMODE12 in TCR).
6. If ENAMODE12 = 3h, write the desired timer period for the next timer cycle in the period reload registers (REL12 and REL34). This step can be done at any time before the current timer cycle ends.

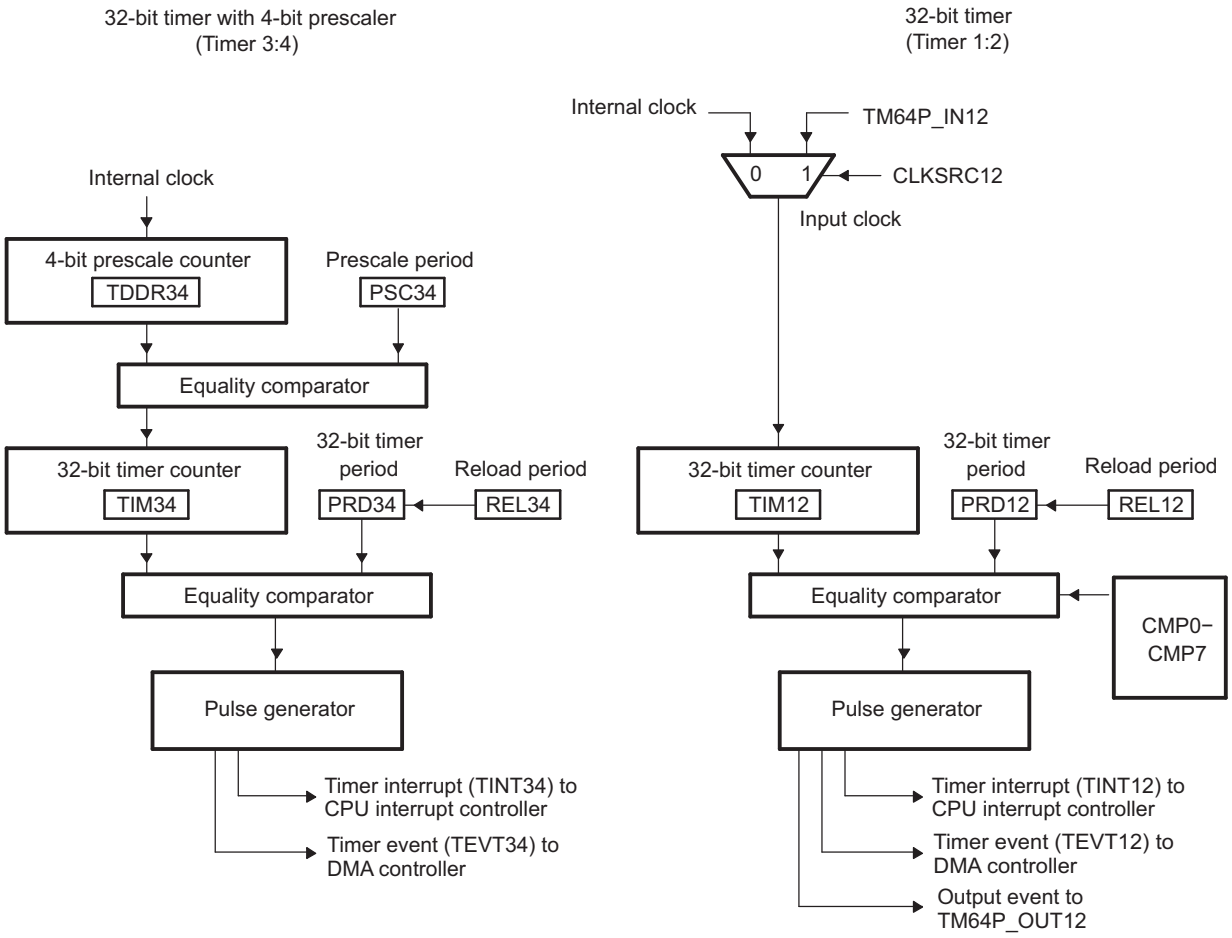
2.1.4.2.2 Unchained Mode

The general-purpose timers can be configured as a dual 32-bit unchained timers by setting the TIMMODE bit to 1 in TGCR.

In the unchained mode (Figure 6), the timer operates as two independent 32-bit timers. One 32-bit timer (timer 3:4) operates as a 32-bit timer being clocked by a 4-bit prescaler. The other 32-bit timer (timer 1:2) operates as a 32-bit timer with no prescaler.

Independent of the normal timer behavior, eight compare registers (CMP*n*) are compared against the value of the TIM12 register when the PLUSEN bit in TGCR is set. Upon a successful non-zero match, an interrupt and a DMA event are generated without affecting the TIM12 value, behavior, or associated counter registers. Note that some timer instantiations may not map the CMP interrupt and DMA events to the CPU and DMA engines (see your device-specific data manual for information).

Figure 6. Dual 32-Bit Timers Unchained Mode Block Diagram

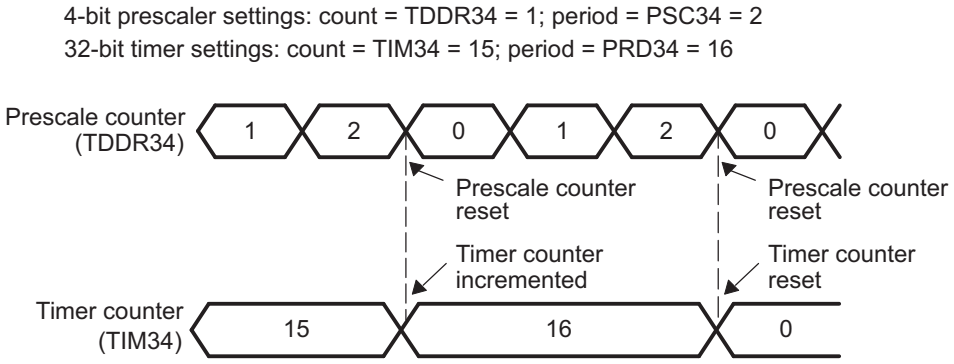


2.1.4.2.2.1 32-Bit Timer With a 4-Bit Prescaler

In the unchained mode, the 4-bit prescale is clocked by the internal clock. The 4-bit prescaler uses the timer divide-down ratio (TDDR34) bit in TGCR to form a 4-bit prescale counter register and the prescale counter bits (PSC34) to form a 4-bit prescale period register (see Figure 6). When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated for the 32-bit timer.

The 32-bit timer uses TIM34 as a 32-bit timer counter register and PRD34 as a 32-bit timer period register. The 32-bit timer is clocked by the output clock from the 4-bit prescaler (see the example in Figure 7). The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the period, a maskable timer interrupt (TINT34) and a timer DMA event (TEVT34) are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM34RS bit in TGCR. For timer 3:4, the lower 16 bits of the timer control register (TCR) have no control.

Figure 7. Dual 32-Bit Timers Unchained Mode Example



2.1.4.2.2.2 32-Bit Timer with No Prescaler

The other 32-bit timer (timer 1:2) uses TIM12 as the 32-bit counter register and PRD12 as a 32-bit timer period register (see Figure 6). When the timer is enabled, the timer counter increments by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt (TINT12), a timer DMA event (TEVT12), and a timer output event on TM64P_OUT12 are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS bit in TGCR. For timer 1:2, the upper 16 bit of the timer control register (TCR) have no control.

2.1.4.2.2.3 Enabling the 32-Bit Unchained Mode Timer

The TIM12RS and TIM34RS bits in TGCR determine whether the timer is in reset, or if it is capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bit controls the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and/or TIM34RS bits must be set to 1.

The ENAMODE*n* bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously.

- When the timer is disabled (ENAMODE*n* = 0), the timer does not run and maintains its current count value.
- When the timer is enabled for one time operation (ENAMODE*n* = 1), it counts up until the counter value equals the period value and then stops.
- When the timer is enabled for continuous operation (ENAMODE*n* = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.
- When the timer is enabled for continuous operation with period reload (ENAMODE*n* = 3h), the counter counts up until it reaches the period value, then resets itself to zero, reloads the period registers (PRD12 and/or PRD34) with the value in the period reload registers (REL12 and/or REL34), and begins counting again.

Table 4 shows the bit values in TGCR to configure the 32-bit timer in unchained mode.

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

Table 4. 32-Bit Timer Unchained Mode Configurations

	TGCR Bit		TCR Bit	
32-Bit Timer Configuration	**TIM12RS**	**TIM34RS**	**ENAMODE12**	**ENAMODE34**
To place the 32-bit timer unchained mode with 4-bit prescaler in reset	x	0	x	0
To disable the 32-bit timer unchained mode with 4-bit prescaler (out of reset)	x	1h	x	0
To enable the 32-bit timer unchained mode with 4-bit prescaler for one-time operation	x	1h	x	1h
To enable the 32-bit timer unchained mode with 4-bit prescaler for continuous operation	x	1h	x	2h
To enable the 32-bit timer unchained mode with 4-bit prescaler for continuous operation with period reload	x	1h	x	3h
To place the 32-bit timer unchained mode with no prescaler in reset	0	x	0	x
To disable the 32-bit timer unchained mode with no prescaler (out of reset)	1h	x	0	x
To enable the 32-bit timer unchained mode with no prescaler for one-time operation	1h	x	1h	x
To enable the 32-bit timer unchained mode with no prescaler for continuous operation	1h	x	2h	x
To enable the 32-bit timer unchained mode with no prescaler for continuous operation with period reload	1h	x	3h	x

2.1.4.2.2.4 32-Bit Timer Unchained Mode Configuration Procedure

To configure timer 1:2, follow the steps below:

1. Select 32-bit unchained mode (TIMMODE in TGCR).
2. Remove the timer 1:2 from reset (TIM12RS in TGCR).
3. Select the desired timer period for timer 1:2 (PRD12).
4. Select the desired clock source for timer 1:2 (CLKSRC12 in TCR).
5. Enable timer 1:2 (ENAMODE12 in TCR).
6. If ENAMODE12 = 3h, write the desired timer period for the next timer cycle in the period reload register (REL12). This step can be done at any time before the current timer cycle ends.

To configure timer 3:4, follow the steps below:

1. Select 32-bit unchained mode (TIMMODE in TGCR).
2. Remove the timer 3:4 from reset (TIM34RS in TGCR).
3. Select the desired timer period for timer 3:4 (PRD34).
4. Select the desired prescaler value for timer 3:4 (PSC34 in TGCR).
5. Enable timer 3:4 (ENAMODE34 in TCR).
6. If ENAMODE34 = 3h, write the desired timer period for the next timer cycle in the period reload register (REL34). This step can be done at any time before the current timer cycle ends.

2.1.4.2.2.5 Event Capture Mode

When the PLUSEN bit in the timer global control register (TGCR) is set, Event Capture Mode is available for TIM12 when the timer is configured in 32-bit unchained mode. When Event Capture Mode is enabled, the timer cycle is restarted when an external input event occurs on pin TM64P_IN12. In particular, when an external input event occurs, the timer stops counting, generates output events (TINT12, TEVT12, and TM64P_OUT12), copies values from the timer counter register TIM12 to the timer capture register CAP12, reloads the timer period register PRD12 if in continuous mode with period reload (ENAMODE = 3h), and then restarts counting in continuous mode. Event Capture Mode is available only when the timer clock source is the internal timer (CLKSRC = 0) and the timer is in continuous mode (ENAMODE = 2h or 3h).

Capture mode is enabled using the Capture mode enable bit CAPMODE12 in the timer control register (TCR). The type of input event is selected by the capture event mode bit CAPEVTMODE12 in the timer control register (TCR). All of the following input event types are available:

- Rising edge of input signal
- Falling edge of input signal
- Rising or falling edge of input signal

2.1.4.2.2.6 Timer Counter Register Read Reset Mode

Read Reset Mode is available when the PLUSEN bit in the timer global control register (TGCR) is set and the timer is configured in 32-bit unchained mode. When Read Reset Mode is enabled, the timer cycle will restart when the timer counter registers are read (TIM12 and/or TIM34). In particular, when the timer registers are read, the timer stops counting, copies values from the timer counter registers (TIM12 and/or TIM34) to the timer capture registers (CAP12 and/or CAP34), reloads the timer period registers (PRD12 and/or PRD34) if in continuous mode with period reload (ENAMODE = 3h), and then restarts counting in continuous mode. Timer output events (TINT*n*, TEVT*n*, and TM64P_OUT*n*) are not generated during this process. Read Reset Mode is enabled using the read reset mode enable bit (READRSTMODE) in the timer control register (TCR).

2.1.4.3 Timer Capture Registers

When the timer has a timeout due to a normal expiration of timer, external input event in Event Capture Mode, or read of timer counter registers in Read Reset Mode, the values of the timer counter registers (TIM12 and TIM34) are copied onto the timer counter capture registers (CAP12 and CAP34). Note that the value in TDDR is not captured when a read of TIM34 happens.

2.1.4.4 Counter and Period Registers Used in GP Timer Modes

Table 5 summarizes how the counter registers (TIM*n*) and period registers (PRD*n*) are used in each GP timer mode.

Table 5. Counter and Period Registers Used in GP Timer Modes

Timer Mode	Counter Registers	Period Registers
64-bit general-purpose	TIM34:TIM12	PRD34:PRD12
Dual 32-bit chained:		
Prescaler (Timer 3:4)	TIM34	PRD34
Timer (Timer 1:2)	TIM12	PRD12
Dual 32-bit unchained:		
Timer (Timer 1:2)	TIM12	PRD12
Timer with prescaler (Timer 3:4)	TDDR34 bits and TIM34	PSC34 bits and PRD34

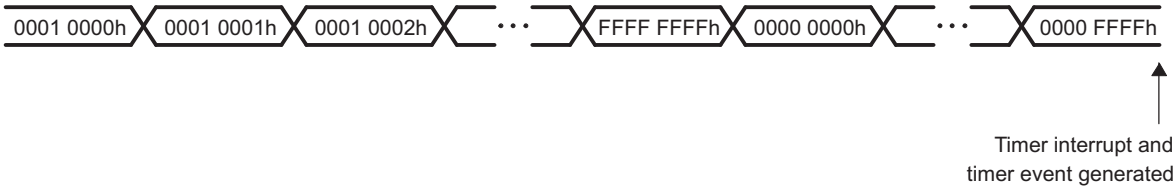
2.1.5 Timer Operation Boundary Conditions

The following boundary conditions affect the timer operation.

2.1.5.1 Timer Counter Overflow

Timer counter overflow can happen when the timer counter register is set to a value greater than the value in the timer period register. The counter reaches its maximum value (FFFF FFFFh or FFFF FFFF FFFF FFFFh), rolls over to 0, and continues counting until it reaches the timer period. An example is in Figure 8.

Figure 8. 32-Bit Timer Counter Overflow Example



2.1.5.2 Writing to Registers of an Active Timer

Writes to most timer registers are not allowed when the timer is active, except for setting the timer period reload registers (REL12 and REL34) and stopping and resetting the timers. In the 64-bit and dual 32-bit timer modes, registers that are protected by hardware are:

- TIM12
- TIM34
- PRD12
- PRD34
- TCR (except the ENAMODE bit)
- TGCR (except the TIM12RS and TIM34RS bits)

2.1.6 General-Purpose Timer Power Management

The timer can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see your device-specific *System Reference Guide*. The timer can be placed in an idle mode to conserve power when it is not being used.

2.2 Architecture – Watchdog Timer Mode

This section describes the use of the timer as a watchdog timer. In order to fully function in watchdog timer mode, the timer must be internally connected to the device hardware reset signal. For information on which timer instantiation can function as a watchdog timer, see your device-specific data manual.

2.2.1 Watchdog Timer

As a 64-bit watchdog timer, the peripheral can be used to prevent system lockup when the software becomes trapped in loops with no controlled exit.

After a hardware reset, the watchdog timer is disabled. The timer then can be configured as a watchdog timer using the timer mode (TIMMODE) bit in the timer global control register (TGCR) and the watchdog timer enable (WDEN) bit in the watchdog timer control register (WDTCR). In the watchdog timer mode, the timer requires a special service sequence to be executed periodically. Without this periodic servicing, the timer counter increments until it matches the timer period and causes a watchdog timeout event.

When the timeout event occurs, the watchdog timer resets the entire processor.

2.2.2 Watchdog Timer Mode Restrictions

The watchdog timer mode has the following restrictions:

- No external clock source
- No one-time enabling

2.2.3 Watchdog Timer Mode Operation

The watchdog timer mode is selected and enabled when:

- TIMMODE = 2h in TGCR
- WDEN = 1 in WDTCR

Figure 9 shows the timer when it is used in the watchdog timer mode. The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit period register. When the timer counter matches the timer period, the timer generates a watchdog timeout event which resets the entire processor.

To activate the watchdog timer, a certain sequence of events must be followed, as shown in the state diagram of Figure 10.

Once the watchdog timer is activated, it can be disabled only by a watchdog timeout event or by a hardware reset. A special key sequence is required to prevent the watchdog timer from being accidentally serviced while the software is trapped in a loop or by some other software failure.

To prevent a watchdog timeout event, the timer has to be serviced periodically by writing A5C6h followed by DA7Eh to the watchdog timer service key (WDKEY) bits in WDTCR before the timer finishes counting up. Both A5C6h and DA7Eh are allowed to be written to the WDKEY bits, but only the correct sequence of A5C6h followed by DA7Eh to the WDKEY bits services the watchdog timer. Any other writes to the WDKEY bits triggers the watchdog timeout event immediately.

When the watchdog timer is in the Timeout state, the watchdog timer is disabled, the WDEN bit is cleared to 0, and the timer is reset.

Figure 9. Watchdog Timer Mode Block Diagram

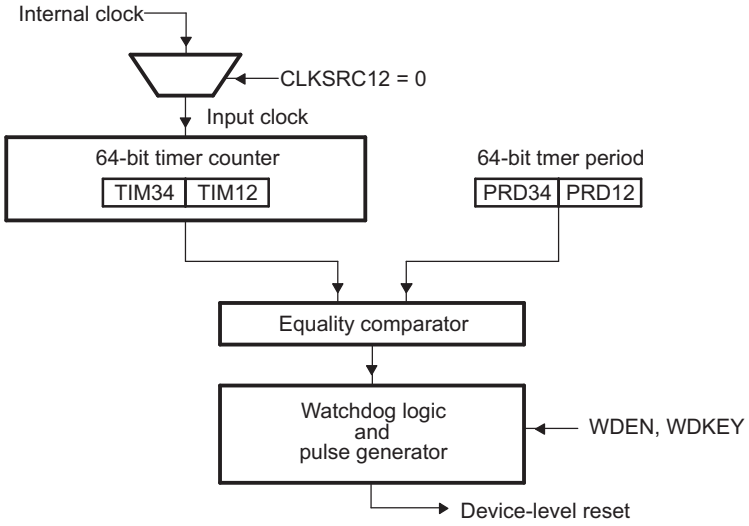
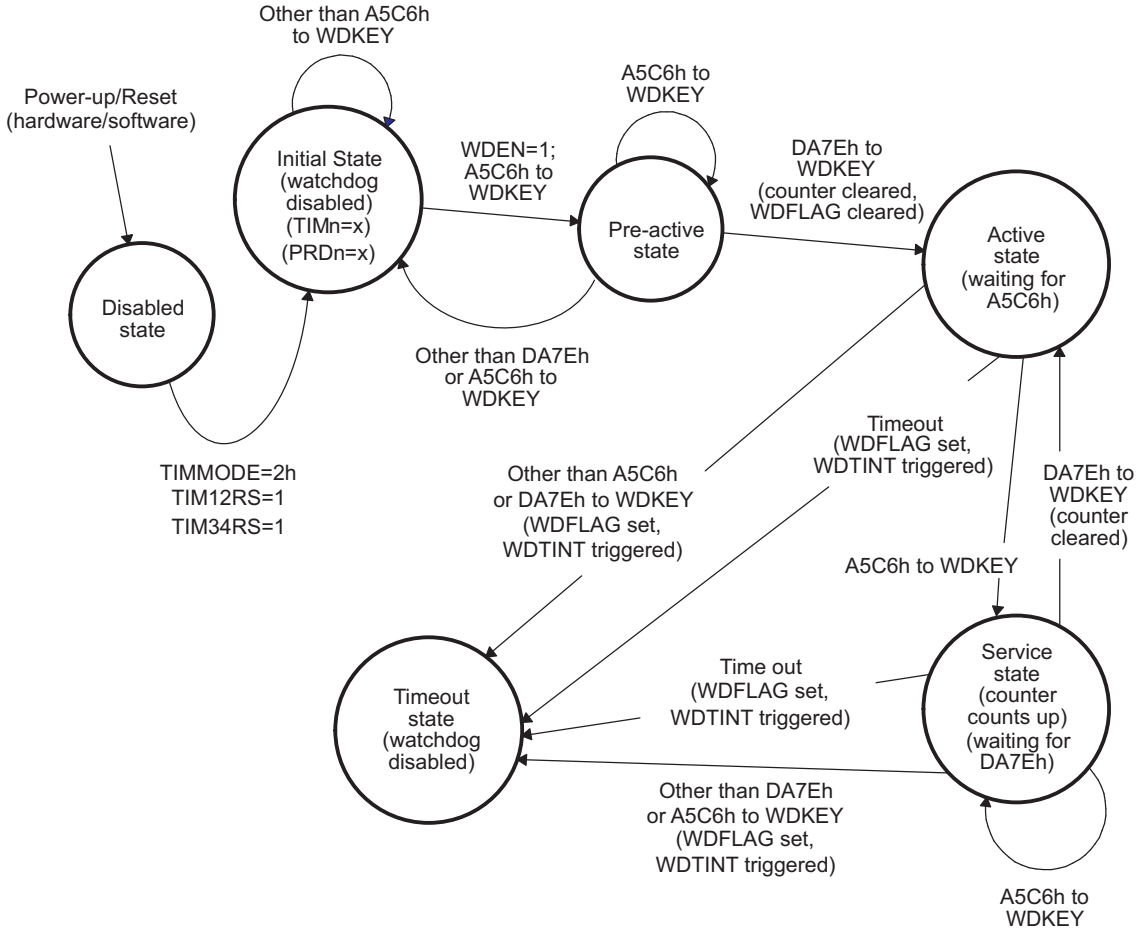


Figure 10. Watchdog Timer Operation State Diagram



After a hardware reset, the watchdog timer is disabled; however, reads or writes to the watchdog timer registers are allowed. Once the WDEN bit is set (enabling the watchdog timer) and A5C6h is written to the WDKEY bits, the watchdog timer enters the Pre-active state. In the Pre-active state:

- A write to WDTCR is allowed only when the write comes with the correct key (A5C6h or DA7Eh) to the WDKEY bits.
- A write of DA7Eh to the WDKEY bits when the WDEN bit is set to 1 resets the counters and activates the watchdog timer.

The watchdog timer must be configured before the watchdog timer enters the Active state. The WDEN bit must be set to 1 before writing DA7Eh to the WDKEY bits in the Pre-active state. Every time the watchdog timer is serviced by the correct WDKEY sequence, the watchdog timer counter is automatically reset.

2.2.4 Watchdog Timer Register Write Protection

Once the watchdog timer enters the Pre-active state (see Figure 10), writes to TIM12, TIM34, PRD12, PRD34, and WDTCR are write protected (except for the WDKEY field). While the watchdog timer is in the Timeout state, writing to the WDEN bit has no effect.

Once the watchdog timer enters its Initial state (see Figure 10), do not write to TGCR.

2.2.5 Watchdog Timer Power Management

The watchdog timer cannot be placed in power-down mode.

2.3 Reset Considerations

The timer has two reset sources: hardware reset and the timer reset (TIM12RS and TIM34RS) bits in the timer global control register (TGCR).

2.3.1 Software Reset Considerations

When the TIM12RS bit in TGCR is cleared to 0, the TIM12 register is held with the current value.

When the TIM34RS bit in TGCR is cleared to 0, the TIM34 register is held with the current value.

2.3.2 Hardware Reset Considerations

When a hardware reset is asserted, all timer registers are set to their default values.

2.4 Interrupt Support

Each of the timers can send either one of two separate interrupt events (TINT*n*) to the CPU, depending on the operating mode of the timer. The timer interrupts are generated when the count value in the counter register reaches the value specified in the period register. For supported interrupts, see your device-specific *System Reference Guide*.

When the PLUSEN bit in the timer global control register (TGCR) is set, matches between TIM12 and CMP*n* in dual 32-bit unchained mode will also generate interrupts. Setting the PLUSEN bit also enables additional features for control, status, and generation of interrupts. See Section 2.8 for more information.

2.5 DMA Event Support

Each of the timers can send either one of two separate timer events (TEVT*n*) to the DMA engine, depending on the operating mode the timer. The timer events are generated when the count value in the counters register reaches the value specified in the period register. For the supported DMA events, see your device-specific *System Reference Guide*.

When the PLUSEN bit in the timer global control register (TGCR) is set, matches between TIM12 and CMP*n* in dual 32-bit unchained mode will also generate DMA events. Setting the PLUSEN bit also enables additional features for control, status, and generation of dma events are enabled. See Section 2.8 for more information.

2.6 TM64P_OUT Event Support

The timer can generate an output pulse (Figure 11) or clock (Figure 12) signals on the TM64P_OUT12 pin. The output signal is generated when the count value in the counter registers reaches the value specified in the period registers (TSTAT12 drives the TM64P_OUT12 pin). Table 6 gives equations for various TSTAT12 timing parameters in pulse and clock modes.

The output mode is selected with the clock/pulse bit (CP*n*) in the timer control register (TCR). In pulse mode, the PWID12 bit in TCR sets the pulse width between 1 to 4 timer clock periods. The TM64P_OUT12 pin may be inverted using the INVOUTP12 bit in TCR.

Figure 11. Timer Operation in Pulse Mode (CP*n* = 0)

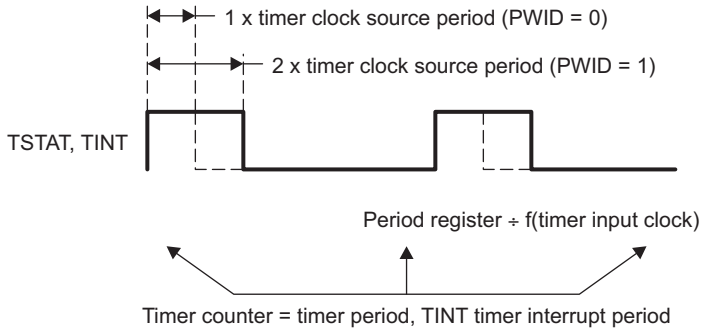


Figure 12. Timer Operation in Clock Mode (CP*n* = 1)

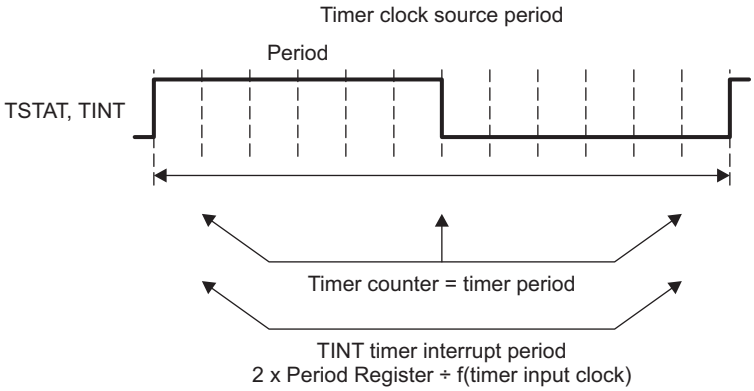


Table 6. TSTAT Parameters in Pulse and Clock Modes

Mode	Frequency	Period	Width High	Width Low
Pulse	$\frac{f\ (clock\ source)}{timer\ period\ register}$	$\frac{timer\ period\ register}{f\ (clock\ source)}$	$\frac{(PWID + 1)}{f\ (clock\ source)}$	$\frac{timer\ period\ register - (PWID + 1)}{f\ (clock\ source)}$
Clock	$\frac{f\ (clock\ source)}{2 \times timer\ period\ register}$	$\frac{2 \times timer\ period\ register}{f\ (clock\ source)}$	$\frac{timer\ period\ register}{f\ (clock\ source)}$	$\frac{timer\ period\ register}{f\ (clock\ source)}$

2.7 External Timer Pin GPIO Mode

The external timer pins (TM64P_IN12 and TM64P_OUT12) can be individually configured to function as general-purpose input/output (GPIO) pins. In GPIO mode, the pins are able to detect and drive arbitrary data. The pins are also able to source external interrupt events. Some timer instantiations may not have external pins, see your device-specific data manual for pin information.

The GPIO interrupt and GPIO enable register (GPINTGPEN) enables the GPIO mode and associated interrupts. The GPIO data and GPIO direction register (GPDATGPDIR) determines if GPIO-enabled pins are used as input or output pins; and it is the means by which data is read-from or written-to the GPIO pins.

Normal timer counting modes cannot be used when the GPIO mode is enabled -- TIM12RS in the timer global control register (TGCR) cannot be brought out of reset when either GPENO12 or GPENI12 in GPINTGPEN is asserted.

2.8 Interrupt/DMA Event Generation Control and Status

When the PLUSEN bit in the timer global control register (TGCR) is set, the timer supports additional features for control and status of interrupt and DMA event generation. Interrupt/DMA events are generated when the count value in the timer counter registers reaches the value specified in the timer period registers and interrupt/DMA events are also generated when the Event Capture Mode is enabled and an external event occurs.

To generate events in the case when the value in the timer counter registers equals the value specified in the timer period registers, set the period compare interrupt enable bit (PRDINTEN*n*) in the interrupt control and status register (INTCTLSTAT). The event status for this case is reflected in the period compare interrupt status bit (PRDINTSTAT*n*), which is also in INTCTLSTAT. The PRDINTSTAT*n* bit is cleared by writing a 1 to the bit.

Similarly, to generate events in Event Capture Mode, set the event interrupt enable bit (EVTINTEN*n*) in INTCTLSTAT. The event status for this case is reflected in the external interrupt status bit (EVTINTSTAT*n*) in INTCTLSTAT. The EVTINTSTAT*n* bit is cleared by writing a 1 to the bit.

2.9 Power Management

The general-purpose timers can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see your device-specific *System Reference Guide*.

2.10 Emulation Considerations

Each timer has an emulation management register (EMUMGT). As shown in Table 7, the FREE and SOFT bits of EMUMGT determine how the timer responds to an emulation suspend event. An emulation suspend event corresponds to any type of emulator access to the CPU, such as a hardware or software breakpoint or a probe point.

Note that during emulation, the timer count values will increment once every timer peripheral clock (not CPU clock). So when single-steeping though code, the timer values will not update on every CPU clock cycle.

The timer can respond to emulation events from the CPU based on the configuration of the emulation suspend source register (SUSPSRC) in the system configuration module. See your device-specific *System Reference Guide* for information on SUSPSRC and how it is configured.

Table 7. Timer Emulation Modes Selection

FREE	SOFT	Emulation Mode
0	0	The timer stops immediately.
0	1	The timer stops when the timer counter value increments and reaches the value in the timer period register.
1	x	The timer runs free regardless of SOFT bit status.

3 Registers

Table 8 lists the memory-mapped registers for the 64-bit Timer Plus. See your device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 8 should be considered as reserved locations and the register contents should not be modified.

Table 8. Timer Registers

Offset	Acronym	Register Description	Section
0h	REVID	Revision ID Register	Section 3.1
4h	EMUMGT	Emulation Management Register	Section 3.2
8h	GPINTGPEN	GPIO Interrupt and GPIO Enable Register	Section 3.3
Ch	GPDATGPDIR	GPIO Data and GPIO Direction Register	Section 3.4
10h	TIM12	Timer Counter Register 12	Section 3.5
14h	TIM34	Timer Counter Register 34	Section 3.5
18h	PRD12	Timer Period Register 12	Section 3.6
1Ch	PRD34	Timer Period Register 34	Section 3.6
20h	TCR	Timer Control Register	Section 3.7
24h	TGCR	Timer Global Control Register	Section 3.8
28h	WDTCR	Watchdog Timer Control Register	Section 3.9
34h	REL12	Timer Reload Register 12	Section 3.10
38h	REL34	Timer Reload Register 34	Section 3.11
3Ch	CAP12	Timer Capture Register 12	Section 3.12
40h	CAP34	Timer Capture Register 34	Section 3.13
44h	INTCTLSTAT	Timer Interrupt Control and Status Register	Section 3.14
60h	CMP0	Compare Register 0	Section 3.15
64h	CMP1	Compare Register 1	Section 3.15
68h	CMP2	Compare Register 2	Section 3.15
6Ch	CMP3	Compare Register 3	Section 3.15
70h	CMP4	Compare Register 4	Section 3.15
74h	CMP5	Compare Register 5	Section 3.15
78h	CMP6	Compare Register 6	Section 3.15
7Ch	CMP7	Compare Register 7	Section 3.15

3.1 Revision ID Register (REVID)

The revision ID register (REVID) contains the peripheral revision. The REVID is shown in Figure 13 and described in Table 9.

Figure 13. Revision ID Register (REVID)

31	0
REV	
R-4472 020Ch	

LEGEND: R = Read only; -*n* = value after reset

Table 9. Revision ID Register (REVID) Field Descriptions

Bit	Field	Value	Description
31-0	REV	4472 020Ch	Revision ID of the Timer.

3.2 Emulation Management Register (EMUMGT)

The emulation management register (EMUMGT) is shown in Figure 14 and described in Table 10.

Figure 14. Emulation Management Register (EMUMGT)

31	16
Reserved	
R-0	

15	2	1	0
Reserved		SOFT	FREE
R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. Emulation Management Register (EMUMGT) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Reserved
1	SOFT		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The timer stops immediately.
		1	The timer stops when the counter increments and reaches the value in the timer period register (PRD*n*).
0	FREE		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit selects the timer mode.
		0	The SOFT bit selects the timer mode.
		1	The timer runs free regardless of the SOFT bit.

3.3 GPIO Interrupt Control and Enable Register (GPINTGPEN)

The GPIO interrupt control and enable register (GPINTGPEN) is shown in Figure 15 and described in Table 11.

Figure 15. GPIO Interrupt Control and Enable Register (GPINTGPEN)

31	30	29	28	27	26	25	24
Reserved							
R/W-0							

23	22	21	20	19	18	17	16
Reserved						GPENO12	GPENI12
R/W-0						R/W-0	R/W-0

15	14	13	12	11	10	9	8
Reserved							
R/W-0							

7	6	5	4	3	2	1	0
Reserved		GPINT12INVO	GPINT12INVI	Reserved		GPINT12ENO	GPINT12ENI
R-0		R/W-0	R/W-0	R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 11. GPIO Interrupt Control and Enable Register (GPINTGPEN) Field Descriptions

Bit	Field	Value	Description
31-18	Reserved	0	Reserved
17	GPENO12		Enable TM64P_OUT12 to function in GPIO mode.
		0	TM64P_OUT12 is used as a TIMER output pin.
		1	TM64P_OUT12 is used as a GPIO pin.
16	GPENI12		Enable TM64P_IN12 to function in GPIO mode
		0	TM64P_IN12 is used as a TIMER input pin.
		1	TM64P_IN12 is used as a GPIO pin.
15-6	Reserved	0	Reserved
5	GPINT12INVO		Invert interrupt/event signal from TM64P_OUT12 when GPINT12ENO = 1.
		0	Rising signal edge on TM64P_OUT12 generates the interrupt/event.
		1	Falling signal edge on TM64P_OUT12 generates the interrupt/event.
4	GPINT12INVI		Invert interrupt/event signal for TM64P_IN12 when GPINT12ENI = 1.
		0	Rising signal edge on TM64P_IN12 generates the interrupt/event.
		1	Falling signal edge on TM64P_IN12 generates the interrupt/event.
3-2	Reserved	0	Reserved
1	GPINT12ENO		Enable TM64P_OUT12 to source interrupts/events in GPIO mode.
		0	Timer interrupts/events are sourced in TIMER mode.
		1	Timer interrupts/events are sourced externally from TM64P_OUT12.
0	GPINT12ENI		Enable TM64P_IN12 to source interrupts/events in GPIO mode.
		0	Timer interrupts/events are sourced in TIMER mode.
		1	Timer interrupts/events are sourced externally from TM64P_IN12.

3.4 GPIO Data and Direction Register (GPDATGPDIR)

The GPIO data and direction register (GPDATGPDIR) is shown in Figure 16 and described in Table 12.

Figure 16. GPIO Data and Direction Register (GPDATGPDIR)

31	18	17	16
Reserved		GPDIRO12	GPDIRI12
R/W-0		R/W-0	R/W-0

15	2	1	0
Reserved		GPDATO12	GPDATI12
R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. GPIO Data and Direction Register (GPDATGPDIR) Field Descriptions

Bit	Field	Value	Description
31-18	Reserved	0	Reserved
17	GPDIRO12		Select direction of TM64P_OUT12 in GPIO mode.
		0	TM64P_OUT12 functions as an input pin in GPIO mode.
		1	TM64P_OUT12 functions as an output pin in GPIO mode (TM64P_OUT12 cannot capture GPIO interrupt events when configured as output).
16	GPDIRI12		Select direction of TM64P_IN12 in GPIO mode.
		0	TM64P_IN12 functions as an input pin in GPIO mode.
		1	TM64P_IN12 functions as an output pin in GPIO mode (TM64P_IN12 cannot capture GPIO interrupt events when configured as output).
15-2	Reserved	0	Reserved
1	GPDATO12		Data on TM64P_OUT12 in GPIO mode. Only valid when GPENO12 = 1.
			When GPDIRO12 = 0 (input):
		0	TM64P_OUT12 is detected logic low.
		1	TM64P_OUT12 is detected logic high.
			When GPDIRO12 = 1 (output):
		0	TM64P_OUT12 is driven logic low.
		1	TM64P_OUT12 is driven logic high.
0	GPDATI12		Data on TM64P_IN12 in GPIO mode. Only valid when GPENI12 = 1.
			When GPDIRI12 = 0 (input):
		0	TM64P_IN12 is detected logic low.
		1	TM64P_IN12 is detected logic high.
			When GPDIRI12 = 1 (output):
		0	TM64P_IN12 is driven logic low.
		1	TM64P_IN12 is driven logic high.

3.5 Timer Counter Registers (TIM12 and TIM34)

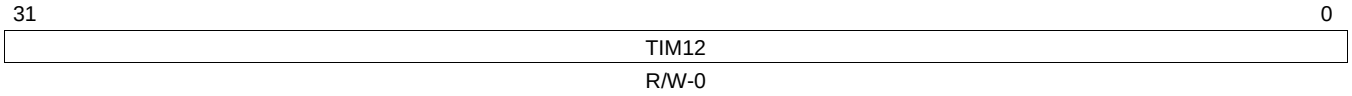
The timer counter register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, TIM12 and TIM34.

In the dual 32-bit timer mode, the 64-bit register is divided with TIM12 acting as one 32-bit counter and TIM34 acting as another. These two registers can be configured as chained or unchained.

3.5.1 Timer Counter Register 12 (TIM12)

The timer counter register 12 (TIM12) is shown in Figure 17 and described in Table 13

Figure 17. Timer Counter Register 12 (TIM12)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

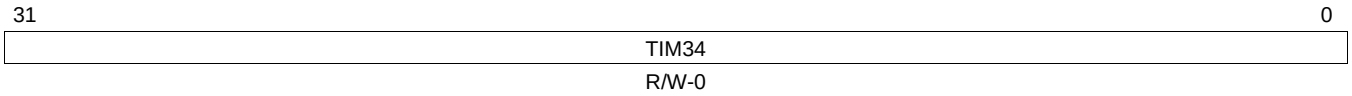
Table 13. Timer Counter Register 12 (TIM12) Field Descriptions

Bit	Field	Value	Description
31-0	TIM12	0-FFFF FFFFh	TIM12 count bits. This 32-bit value is the current count of the main counter.

3.5.2 Timer Counter Register 34 (TIM34)

The timer counter register 34 (TIM34) is shown in Figure 18 and described in Table 14.

Figure 18. Timer Counter Register 34 (TIM34)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Timer Counter Register 34 (TIM34) Field Descriptions

Bit	Field	Value	Description
31-0	TIM34	0-FFFF FFFFh	TIM34 count bits. This 32-bit value is the current count of the main counter.

3.6 Timer Period Registers (PRD12 and PRD34)

The timer period register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, PRD12 and PRD34.

Similar to TIM*n* in the dual 32-bit timer mode, PRD*n* can be divided into 2 registers: for timer 1:2, PRD12 and for timer 3:4, PRD34. These two registers can be used in conjunction with the two timer counter registers TIM12 and TIM34.

3.6.1 Timer Period Register 12 (PRD12)

The timer period register 12 (PRD12) is shown in Figure 19 and described in Table 15.

Figure 19. Timer Period Register 12 (PRD12)

31	0
PRD12	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. Timer Period Register (PRD12) Field Descriptions

Bit	Field	Value	Description
31-0	PRD12	0-FFFF FFFFh	PRD12 period bits. This 32-bit value is the number of timer input clock cycles to count.

3.6.2 Timer Period Register 34 (PRD34)

The timer period register 34 (PRD34) is shown in Figure 20 and described in Table 16.

Figure 20. Timer Period Register 34 (PRD34)

31	0
PRD34	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 16. Timer Period Register (PRD34) Field Descriptions

Bit	Field	Value	Description
31-0	PRD34	0-FFFF FFFFh	PRD34 period bits. This 32-bit value is the number of timer input clock cycles to count.

3.7 Timer Control Register (TCR)

The timer control register (TCR) is shown in Figure 21 and described in Table 17.

Figure 21. Timer Control Register (TCR)

31	27	26	25	24
Reserved		READRSTMODE34	Reserved	
R/W-0		R/W-0	R/W-0	

23	22	21	16
ENAMODE34		Reserved	
R/W-0		R/W-0	

15	14	13	12	11	10	9	8
Reserved		CAPVTMODE12		CAPMODE12	READRSTMODE12	TIEN12	CLKSRC12
R-0		R/W-0		R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
ENAMODE12		PWID12		CP12	INVINP12	INVOUTP12	TSTAT12
R/W-0		R/W-0		R/W-0	R/W-0	R/W-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 17. Timer Control Register (TCR) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26	READRSTMODE34		Read reset mode enable bit. Determines the effect of a timer counter read on TIM34. Read reset mode is only available in dual 32-bit unchained. Output events (interrupt/EDMA/other) are not generated when read reset occurs.
		0	There is no effect when timer counter register TIM34 is read.
		1	Timer counter is reset when timer counter register TIM34 is read.
25-24	Reserved	0	Reserved
23-22	ENAMODE34	0-3h	Enabling mode: determines the enabling modes fo the timer.
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM34 increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	The timer is enabled continuously with period reload, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching, reloads the period register with the values in the reload registers (REL*n*), and continues counting.
21-14	Reserved	0	Reserved
13-12	CAPEVTMODE12	0-3h	Capture event mode. Uses these bits to specify the type of event for Capture mode.
		0	Event occurs on timer input rising edge.
		1h	Event occurs on time input falling edge.
		2h	Event occurs on both rising and falling edges.
		3h	Reserved
11	CAPMODE12		Capture mode enable bit. Determines if external event can reset timer. Capture mode is only available in dual 32-bit unchained mode and when CLKSRC = 0 and ENAMODE = 2h or 3h. Output events (interrupt/EDMA/other) are generated when capture mode event occurs.
		0	Timer is not in capture mode.
		1	Timer is in capture mode. External event can reset timer.
10	READRSTMODE12		Read reset mode enable bit. Determines the effect of a timer counter read on TIM12. Read reset mode is only available in dual 32-bit unchained. Output events (interrupt/EDMA/other) are not generated when read reset occurs.
		0	There is no effect when timer counter register TIM12 is read.
		1	Timer counter is reset when timer counter register TIM12 is read.

Table 17. Timer Control Register (TCR) Field Descriptions (continued)

Bit	Field	Value	Description
9	TIEN12		Timer input gate enable bit. Allows timer input pin TM64P_IN12 to gate the internal timer clock source (CLKSRC = 0). Timer starts counting when TM64P_IN12 transitions from low to high. Timer stops counting when TM64P_IN12 transitions from high to low.
		0	Timer clock is not gated by TM64P_IN12.
		1	Timer clock is gated by TM64P_IN12.
8	CLKSRC12		CLKSRC determines the selected clock source for the timer.
		0	Internal clock
		1	External clock on TM64P_IN12
7-6	ENAMODE12	0-3h	Enabling mode: determines the enabling modes fo the timer.
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	The timer is enabled continuously with period reload, TIM*n* increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching, reloads the period register with the values in the reload registers (REL*n*), and continues counting.
5-4	PWID12	0-3h	Pulse width - Determines the pulse width on the TSTAT12 bit (and the TM64P_OUT12 pin) when the clock/pulse mode is set to pulse.
		0	TSTAT12 stays active for one timer clock cycle when the timer counter reaches the period.
		1h	TSTAT12 stays active for two timer clock cycles when the timer counter reaches the period.
		2h	TSTAT12 stays active for three timer clock cycles when the timer counter reaches the period.
		3h	TSTAT12 stays active for four timer clock cycles when the timer counter reaches the period.
3	CP12		Clock/Pulse bit - Determines whether the TM64P_OUT12 output event should behave as a 50% duty-cycle clock or a signal pulse.
		0	Pulse Mode. TM64P_OUT12 goes active after the timer counter reaches the period. The pulse width is determined by PWID12.
		1	Clock Mode. TM64P_OUT12 will behave as a 50% duty cycle signal. It toggles high-to-low or low-to-high when the timer counter reaches zero.
2	INVINP12		Invert TM64P_IN12. Only affects operation if CLKSRC = 1.
		0	Uninverted TM64P_IN12 signal drives timer.
		1	Inverted TM64P_IN12 signal drives timer.
1	INVOUTP12		Invert TM64P_OUT12.
		0	TM64P_OUT12 signal is not inverted.
		1	TM64P_OUT12 signal is inverted.
0	TSTAT12		Timer status. Drives the value of timer output TM64P_OUT12 when it is configured to function as timer output.
		0	TM64P_OUT12 signal is not asserted.
		1	TM64P_OUT12 signal is asserted.

3.8 Timer Global Control Register (TGCR)

The timer global control register (TGCR) is shown in Figure 22 and described in Table 18.

Figure 22. Timer Global Control Register (TGCR)

31						16
Reserved						
R-0						
15		12	11			8
TDDR34			PSC34			
R/W-0			R/W-0			
7	5	4	3	2	1	0
Reserved		PLUSEN	TIMMODE		TIM34RS	TIM12RS
R-0		R/W-0	R/W-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 18. Timer Global Control Register (TGCR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	TDDR34	0-Fh	Timer linear divide-down ratio specifies the timer divide-down ratio for timer 3:4. When the timer is enabled, TDDR34 increments every timer clock. The TIM34 counter increments on the cycle after TDDR34 matches PSC34. TDDR34 resets to 0 and continues. When TIM34 matches PRD34, timer 3:4 stops, if timer 3:4 is enabled one time; TIM34 resets to 0 on the cycle after matching PRD34 and timer 3:4 continues, if timer 3:4 is enabled continuously.
11-8	PSC34	0-Fh	TIM34 pre-scalar counter specifies the count for timer 3:4.
7-5	Reserved	0	Reserved
4	PLUSEN		Enable new timer plus features.
		0	Enable backward compatibility. New timer features are unavailable.
		1	Disable backward compatibility. New timer features are available.
3-2	TIMMODE	0-3h	TIMMODE determines the timer mode.
		0	The timer is in 64-bit GP timer mode.
		1h	The timer is in dual 32-bit timer unchained mode.
		2h	The timer is in 64-bit watchdog timer mode.
		3h	The timer is in dual 32-bit timer, chained mode.
1	TIM34RS		Timer 3:4 reset.
		0	Timer 3:4 is in reset.
		1	Timer 3:4 is not in reset. Timer 3:4 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.
0	TIM12RS		Timer 1:2 reset.
		0	Timer 1:2 is in reset.
		1	Timer 1:2 is not in reset. Timer 1:2 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.

3.9 Watchdog Timer Control Register (WDTCR)

The watchdog timer control register (WDTCR) is shown in Figure 23 and described in Table 19.

Figure 23. Watchdog Timer Control Register (WDTCR)

31	16
WDKEY	
R/W-0	

15	14	13	12	11	0
WDFLAG	WDEN	Reserved		Reserved	
R/W-0	R/W-0	R/W-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. Watchdog Timer Control Register (WDTCR) Field Descriptions

Bit	Field	Value	Description
31-16	WDKEY	0-FFFFh	16-bit watchdog timer service key. Only the sequence of an A5C6h followed by a DA7Eh services the watchdog. Not applicable in regular timer mode.
15	WDFLAG		Watchdog flag bit. WDFLAG can be cleared by enabling the watchdog timer, by device reset, or being written with 1. It is set by a watchdog time-out.
		0	No watchdog time-out occurred.
		1	Watchdog time-out occurred.
14	WDEN		Watchdog timer enable bit.
		0	Disable watchdog timer
		1	Enable watchdog timer
13-12	Reserved	0	Reserved. This bit field must be written as 00b.
11-0	Reserved	0	Reserved

3.10 Timer Reload Register 12 (REL12)

The timer reload register 12 (REL12) is shown in Figure 24 and described in Table 20.

Figure 24. Timer Reload Register 12 (REL12)

31	0
REL12	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. Timer Reload Register 12 (REL12) Field Descriptions

Bit	Field	Value	Description
31- 0	REL12	0-FFFF FFFFh	Period reload bits.

3.11 Timer Reload Register 34 (REL34)

The timer reload register 34 (REL34) is shown in Figure 25 and described in Table 21.

Figure 25. Timer Reload Register 34 (REL34)

31	0
REL34	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

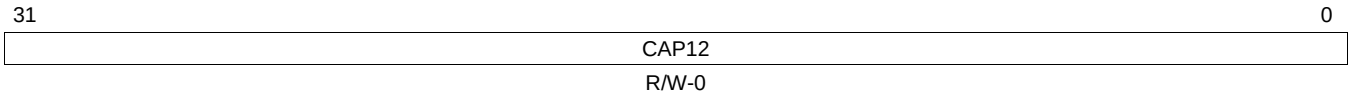
Table 21. Timer Reload Register 34 (REL34) Field Descriptions

Bit	Field	Value	Description
31- 0	REL34	0-FFFF FFFFh	Period reload bits.

3.12 Timer Capture Register 12 (CAP12)

The timer capture register 12 (CAP12) is shown in Figure 26 and described in Table 22.

Figure 26. Timer Capture Register 12 (CAP12)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

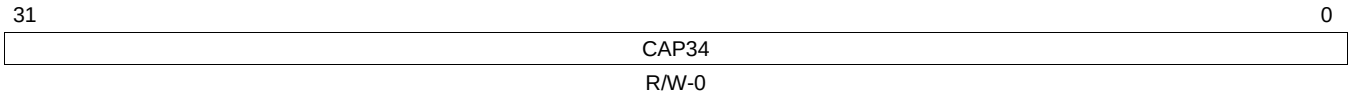
Table 22. Timer Capture Register 12 (CAP12) Field Descriptions

Bit	Field	Value	Description
31- 0	CAP12	0-FFFF FFFFh	Captured timer counter bits.

3.13 Timer Capture Register 34 (CAP34)

The timer capture register 34 (CAP34) is shown in Figure 27 and described in Table 23.

Figure 27. Timer Capture Register 34 (CAP34)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23. Timer Capture Register 34 (CAP34) Field Descriptions

Bit	Field	Value	Description
31- 0	CAP34	0-FFFF FFFFh	Captured timer counter bits.

3.14 Timer Interrupt Control and Status Register (INTCTLSTAT)

The timer interrupt control and status register (INTCTLSTAT) is shown in Figure 28 and described in Table 24.

Figure 28. Timer Interrupt Control and Status Register (INTCTLSTAT)

31	24
Reserved	
R-0	

23	20	19	18	17	16
Reserved		EVTINTSTAT34	EVTINTEN34	PRDINTSTAT34	PRDINTEN34
R-0		R/W1C-0	R/W-0	R/W1C-0	R/W-0

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved		EVTINTSTAT12	EVTINTEN12	PRDINTSTAT12	PRDINTEN12
R-0		R/W1C-0	R/W-0	R/W1C-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; W1C = Write 1 to clear bit; -*n* = value after reset

Table 24. Timer Interrupt Control and Status Register (INTCTLSTAT) Field Descriptions

Bit	Field	Value	Description
31-20	Reserved	0	Reserved
19	EVTINTSTAT34		Interrupt status which reflects the condition that an external event caused a timeout when timer is in capture mode. Write a 1 to clear this bit.
		0	Interrupt has not occurred.
		1	Interrupt has occurred.
18	EVTINTEN34		Enables the interrupt generation when timer is in capture mode.
		0	Disable interrupt when in event capture mode.
		1	Enable interrupt when in event capture mode.
17	PRDINTSTAT34		Interrupt status which reflects the condition that timer counter matched the period register when timer is enabled. Write a 1 to clear this bit.
		0	Interrupt has not occurred.
		1	Interrupt has occurred.
16	PRDINTEN34		Enable interrupt generation when timer is enabled in 64-bit/32-bit chained/unchained/watchdog modes.
		0	Disable interrupt
		1	Enable interrupt
15-4	Reserved	0	Reserved
3	EVTINTSTAT12		Interrupt status which reflects the condition that an external event caused a timeout when timer is in capture mode. Write a 1 to clear this bit.
		0	Interrupt has not occurred.
		1	Interrupt has occurred.
2	EVTINTEN12		Enables the interrupt generation when timer is in capture mode.
		0	Disable interrupt when in event capture mode.
		1	Enable interrupt when in event capture mode.
1	PRDINTSTAT12		Interrupt status which reflects the condition that timer counter matched the period register when timer is enabled. Write a 1 to clear this bit.
		0	Interrupt has not occurred.
		1	Interrupt has occurred.

Table 24. Timer Interrupt Control and Status Register (INTCTLSTAT) Field Descriptions (continued)

Bit	Field	Value	Description
0	PRDINTEN12		Enable interrupt generation when timer is enabled in 64-bit/32-bit chained/unchained/watchdog modes.
		0	Disable interrupt
		1	Enable interrupt

3.15 Timer Compare Registers (CMP0-CMP7)

The timer compare register (CMP*n*) is shown in Figure 29 and described in Table 25.

Figure 29. Timer Compare Register (CMP*n*)

31	0
CMP*n*	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 25. Timer Compare Register (CMP*n*) Field Descriptions

Bit	Field	Value	Description
31-0	CMP*n*	0-FFFF FFFFh	Timer compare register. When PLUSEN = 1 in the timer global control register (TGCR) and the timer is configured in 32-bit unchained mode, TIM12 is compared to all 8 compare registers (CMP0-CMP7). When CMP*n* matches TIM12, a timer CMP*n* interrupt and DMA event are generated. A CMP*n* match will not affect the TIM12 count or behavior.

Appendix A Revision History

Table 26 lists the changes made since the previous version of this document.

Table 26. Document Revision History

Reference	Additions/Modifications/Deletions
Figure 1	Changed figure.
Section 2.1.2	Changed second paragraph.
Figure 2	Changed figure.
Section 2.1.2.1	Changed second and third paragraphs.
Section 2.1.2.2	Changed first paragraph.
	Changed third sentence in second paragraph.
Section 2.1.3	Changed first sentence.
Figure 3	Changed figure.
Section 2.1.4.1.2	Changed paragraph.
Figure 4	Changed figure.
Figure 6	Changed figure.
Section 2.1.4.2.2.1	Changed first paragraph.
Section 2.1.4.2.2.5	Deleted second paragraph.
Section 2.6	Changed paragraphs.
Section 2.7	Changed third paragraph.
Figure 13	Changed Reset value.
Table 9	Changed Value field.
Figure 15	Changed bits 25, 24, 13, 12, 9, and 8
Table 11	Changed bits 25, 24, 13, 12, 9, and 8.
Figure 16	Changed bits 25, 24, 9, and 8.
Table 12	Changed bits 25, 24, 9, and 8.
Figure 21	Changed bits 27, 25, 24, and 21-16.
Table 17	Changed bits 27, 25, 24, and 21-16.

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