AM335x General-Purpose Evaluation Manual Hardware

This document describes the hardware architecture of the AM335x Evaluation Module (EVM) (Part # TMDXEVM3358), which is based on the Texas Instruments AM335x processor. This EVM is also commonly known as the AM335x general-purpose (GP) EVM.

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Trademarks

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1 Introduction

1.1 Description

The AM335x general-purpose EVM is a standalone test, development, and evaluation module system that enables developers to write software and develop hardware around an AM335x processor subsystem. The main elements of the AM335x subsystem are already available on the baseboard of the EVM, which gives developers the basic resources needed for most general purpose type projects that encompass the AM335x as the main processor. Furthermore, additional, "typical" type peripherals are built into the EVM such as memory, sensors, LCD, Ethernet PHY, and so forth, so that prospective systems can be modeled quickly without significant additional hardware resources. The following sections provide more details regarding the EVM.

1.2 EVM System View

The System View of the AM335x General Purpose EVM consists of the baseboard, daughterboard, and LCD display board stacked together and connected through standard throughhole connectors. Figure 1 and Figure 2 shows the EVM.

Figure 1. AM335x General Purpose EVM

Figure 2. AM335x Baseboard Bottom View

1.3 Schematics and Design Files

HW Documentation - Schematics, Design Files, and other related HW Documentation

2 System Description

2.1 System Board Diagram

The complete AM335x General Purpose EVM is partitioned across two different boards for modularity. The GP EVM consists of the baseboard (processor and main power supply) and daughterboard (external peripherals)), and the LCD display board (LCD and touchscreen) (see Figure 3).

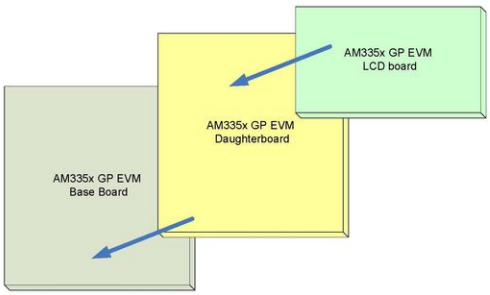


Figure 3. AM335x EVM System Board Diagram

The functional block diagram of the AM335x 15x15 baseboards is as shown in Figure 4.

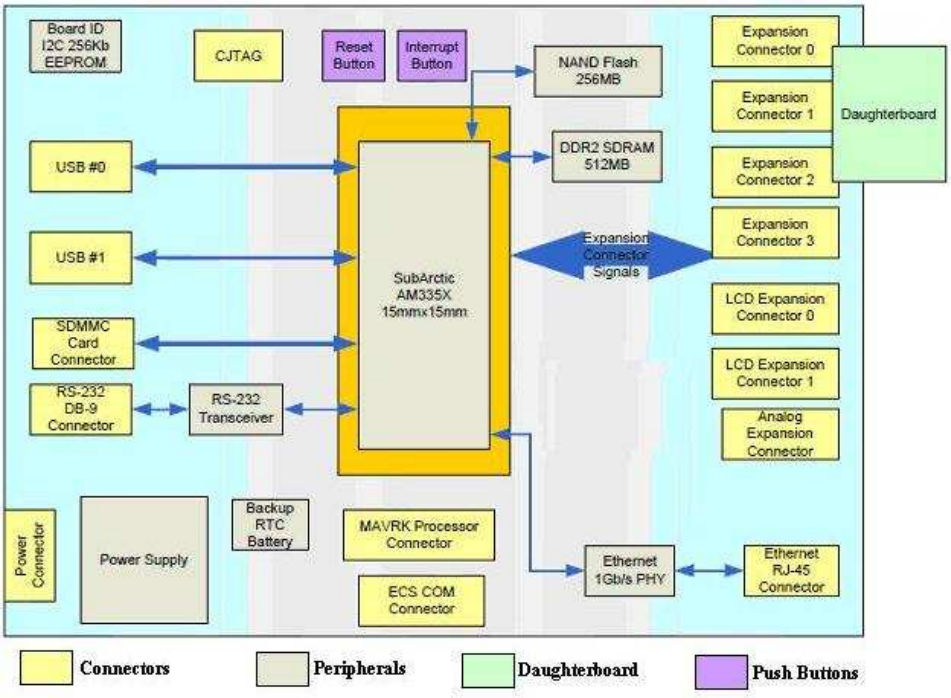


Figure 4. AM335x 15x15 Baseboard Block Diagram

The functional block diagram of the AM335x IDK Industrial Daughterboard is as shown in Figure 5.

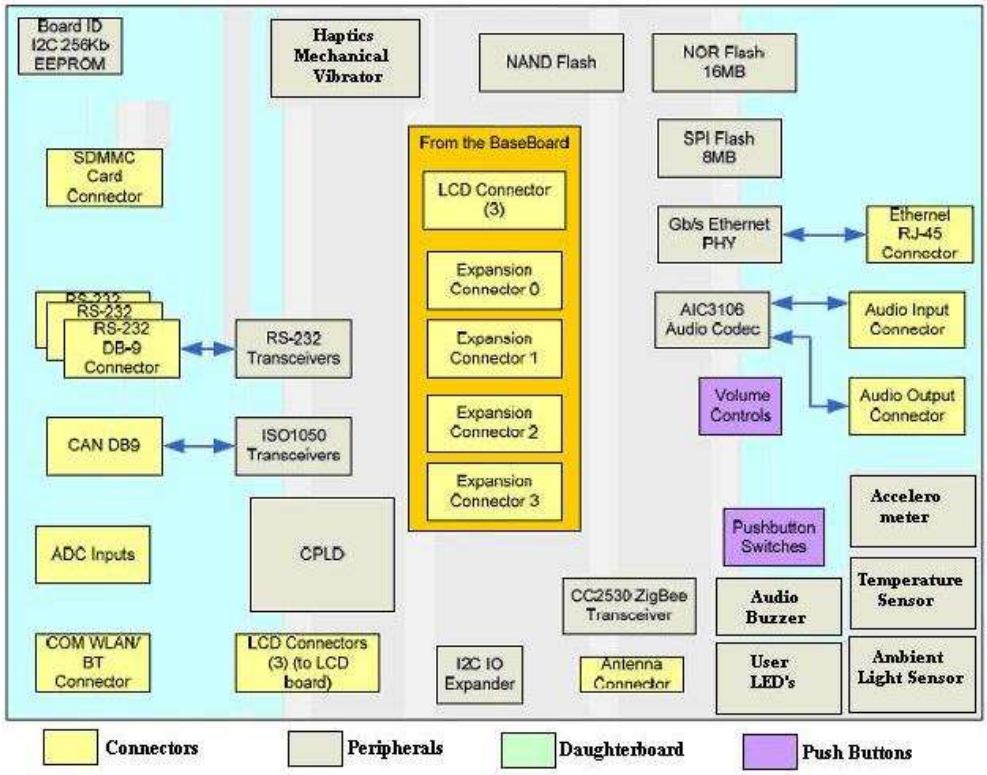


Figure 5. AM335x General Purpose Daughterboard Block Diagram

The block diagram of the AM335x LCD A Board is given in Figure 6.

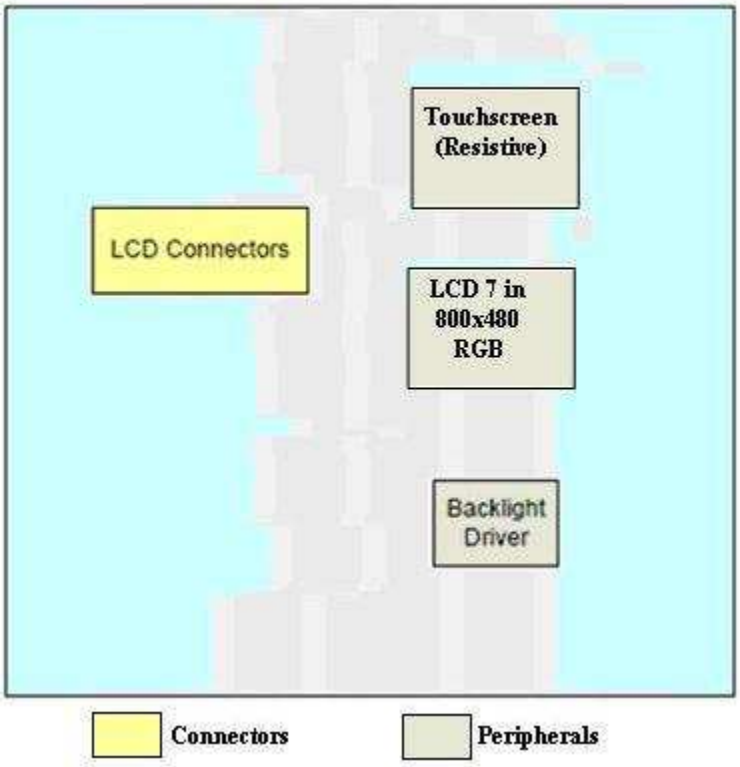


Figure 6. AM335x LCD A Block Diagram

2.2 Processor

The AM3359ZCZ processor is the central processor to this EVM. All the resources on the board surround the AM3359 processor to provide development capabilities for hardware and software. For the details about the processor, see the *Sitara AM335x ARM Cortex-A8 Microprocessors (MPUs) Data Manual* and *AM335x ARM Cortex-A8 Microprocessors (MPUs) Technical Reference Manual*.

There are system configuration signals, SYSBOOT, that can be set on the EVM to define some startup parameters on the AM335x processor. For more details, see Section 4.

2.3 Clocks

The EVM has several clocks to support the AM3359 processor. The main clock for the processor is derived from a 24 MHz crystal. An on-board oscillator in the AM3359 generates the base clock and subsequent module clocks as needed within the AM3359 processor. A 32 kHz clock for the RTC on the AM3359 is derived from a 32 kHz crystal on the board.

2.4 Reset Signals

SYS_RESETn is a signal running to several peripherals and AM335x that performs a reset on those peripherals. SYS_WARMRESETn is asserted by the pushbutton and is used to force a reset of the AM335x. AM335x can also pulldown on the RESET_INOUTn signal to cause the SYS_RESETn line to go active.

3 Power System

This section describes how the power supply is implemented.

3.1 Power Source

AM335x Baseboard uses an external AC to +5 VDC (rated 2.5A minimum) power adapter. The switch near to the power cable is used for power ON/OFF. The main power is off when the power switch is in the position away from the power supply jack. The main power is on when the power switch is in the position closest to the power supply jack.

NOTE: When powering this EVM, always use the recommended power supply (CUI/V-Infinity Part Number EMSA050300-P6P-SZ, Model 3A-182WP05) or equivalent model having output voltage of +5VDC, output current max 3.0 Amp, and Efficiency Level V as well as the applicable regional product regulatory/safety certification requirements such as (by example) UL, CSA, VDE, CCC, PSE, an so forth. Examples of equivalent models include SMI18-5-V-P6 or SWI18-5-N-P6. A power supply is no longer included in the kit.

NOTE: Mounted to this EVM is a UL-recognized component, RoHS-compliant Lithium rechargeable battery (Seiko MS920SE: Nominal voltage 3V, Nominal capacity 11.0 mAh, UL File No. MH15628).

- This battery should only be replaced by a trained technician.
- This battery is intended for use at ordinary temperatures where the EVM is not operated above a high temperature of 60°C or below a low temperature of -20°C.

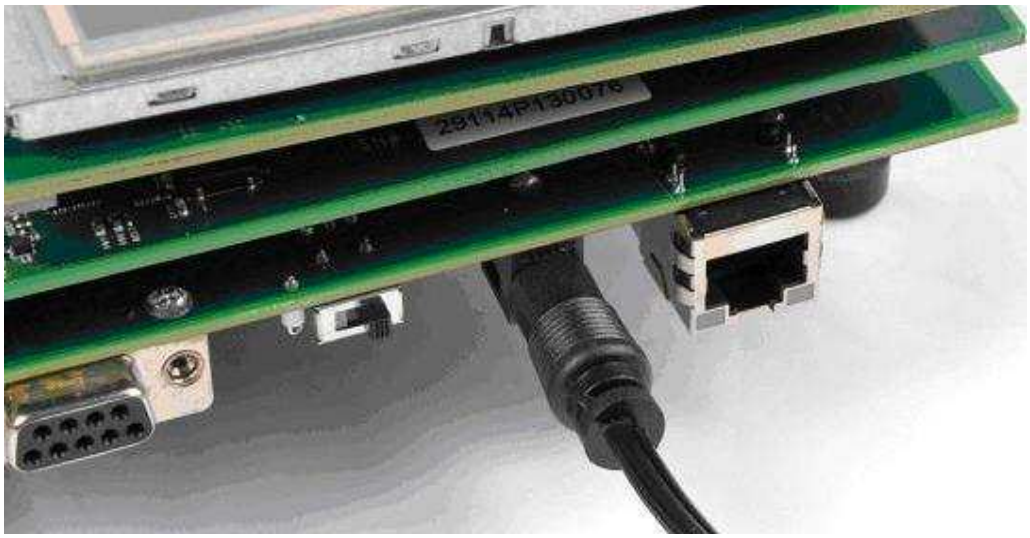
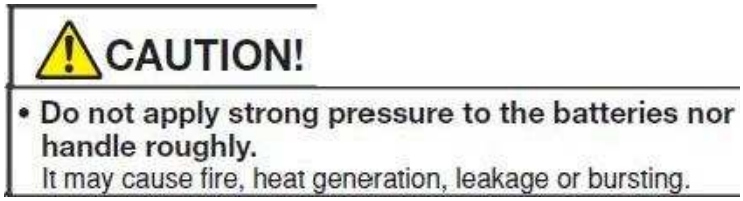


Figure 7. AM335x Power Adapter



3.2 Power Nets

The power nets used in the AM335x baseboard schematics are listed in Table 1 and Table 2.

Table 1. AM335x Baseboard Power Nets

Net	Description
V1_8DDR	Power supply for DDR2 SDRAM
GND_OSC0	Isolated ground for OSC0 main clock source
GND_OSCRTC	Isolated ground for RTC oscillator
DGND	Main ground reference net
V3_3D	Digital 3.3 V power
V5_0D	Digital 5.0 V power
GNDUSB0	Local ground for USB0 connector shield
GNDUSB1	Local ground for USB1 connector shield
V1_8D	Digital 1.8 V power
VSDMMC0	Digital SDMMC0 power supply (1.8 V or 3.3 V)
VBAT	Main unregulated power supply (may be tied to 5 V) (needs to be 3.7 to 5.5 V)
VCOM_BAT	COM connector VBAT supply (must be 3.6 V)
VEXPD	Unregulated power supply for expansion board
GND_ADC	Local ground for the ADC
VADC	Power supply for the ADC
GND_ETH	Ethernet Gb/s isolated ground
V1_2D	Power supply 1.2 V
VHDMI_IO	Power supply for HDMI transceiver I/O
V5_0USB	5.0 V power supply for the VBUS on USB
V1_1D	Power supply for AM335x core
GNDA_TSC	Local analog ground for touch screen
VDDH_PHY	Ethernet VDDH_REG power supply
VETH_AVDD_3_3	Ethernet 3.3V analog power supply
VETH_VDDIO	Ethernet I/O power supply
VDDL_PHY	Ethernet main digital supply
VADDL_PHY	Ethernet analog supply
VETH_LX	Ethernet LX power supply

Table 2. AM335x General Purpose Daughterboard Power Nets

Net	Description
DGND	Main ground reference net
V3_3D	Digital 3.3 V power
V5_0D	Digital 5.0 V power
V1_8D	Digital 1.8 V power
VSDMMC1	Digital SDMMC1 power supply (1.8 V or 3.3 V)
VBAT	Main unregulated power supply (may be tied to 5 V) (needs to be 3.7 to 5.5 V)
VEXPD	Variable power supply for expansion board
GND_ADC	Local ground for the ADC
VADC	Power supply for the ADC
V1_0PHY	Ethernet Gb/s 1.0 PHY supply
V1_0APHY	Ethernet Gb/s 1.0 V analog PHY supply
V2_5PHY	Ethernet Gb/s 2.5 V PHY supply
GND_ETH	Ethernet Gb/s isolated ground
VLCD_VCC	3.3 V power supply for LCD
VLCD_AVDD	Analog power supply for LCD 10 V
VLCD_VGH	LCD VGH TFT supply 15 V
VLCD_VGL	LCD VGL TFT supply -7 V

The power sequencing requirements of the AM335X processor are handled automatically by the TPS65910 PMIC. For more information, see the *Sitara AM335x ARM Cortex-A8 Microprocessors (MPUs) Data Manual*.

3.3 Power Management IC Power Supplies

The AM335x baseboard uses the TPS65910 power management IC.

The I2C0 on AM335x is used to control the Smart Reflex™ port and control port on the TPS65910.

For AM335x, the following power supplies from the TPS65910A are used.

Table 3. AM335x Power Supplies From TPS65910A

TPS65910 Power Supply	AM335x Power Rail	Voltage
VAUX2 (300mA)	VDDSHV1, 3, 5,6 (500 mA)	3.3 V (rails that are 3.3V)
VDIG1 (300 mA)	VDDSHV1, 3, 5, 6 (500 mA)	1.8 V (rails that are 1.8V)
VMMC (300 mA)	VDDSHV4 (60 mA) and VDDSHV2	1.8 V/3.3 V
VDD2 SMPS (1500 mA)	VDD_CORE (1000 mA)	1.1 V
VDD1 SMPS (1500 mA)	VDD_MPU (1500 mA)	1.2 V
No supply needed	VDD_RTC	1.1 V
VRTC	VDDS_RTC (10 mA)	1.8 V
VIO_SMPS (1000 mA)	VDDS_DDR (200 mA)	1.8 V (or 1.5 V for DDR3)
VIO_SMPS (1000mA)	VREFSSTL (10 mA)	0.9 V or 0.75 V
VDAC (150 mA)	VDDS (100 mA)	1.8 V
VDIG2 (300 mA)	VDDS_SRAM_CORE_BG (40 mA)||1.8 V	
VDIG2 (300 mA)	VDDS_SRAM_MPU_BB (40 mA)	1.8 V
VDIG2 (300 mA)	VDDS_PLL_DDR (25 mA)	1.8 V
VDIG2 (300 mA)	VDDS_PLL_CORE_LCD (25 mA)	1.8 V
VDIG2 (300 mA)	VDDS_PLL_MPU (25 mA)	1.8 V
VDIG2 (300 mA)	VDDS_OSC (10 mA)	1.8 V
VAUX1 (300 mA)	VDDA1P8V_USB0/1 (50 mA)	1.8 V
VAUX33 (150 mA)	VDDA3P3V_USB0/1 (10 mA)	3.3 V
VAUX33 (150 mA)	USB_VBUS0/1	3.3 V
VPLL (50 mA)	VDDA_ADC	1.8 V
VDD3 SMPS (100 mA)	Not Used	-
VIO_SMPS (1000 mA)	DDR2 SDRAM (320 mA)	1.8 V

3.4 APM Sense Resistors

The AM335x baseboard has the following subsystems with current sense resistors. These resistors allow the power to be measured on each power rail to check AM335x power requirements during real time software execution. The value of the resistors is selected to provide the best dynamic range when using a TI INA226 converter. In fact, an INA226 converter is installed on the baseboard for both the VDD_CORE and VDD_MPU power supply rails of the AM335x. The other power rails have sense resistors but have their measurement connections attached to 2-pin standard headers so that they can be read easily by a multi-meter or connected to an INA226 converter EVM.

Note the value of the sense resistors for the VDD_CORE and VDD_MPU were selected to give better dynamic range for active power modes rather than sleep and low power modes. If power is to be measured for VDD_CORE or VDD_MPU for sleep and low power modes, then this sense resistor value should be changed to give better shunt voltage values.

Table 4. AM335x Baseboard APM Sense Resistors

Voltage Net	Sense Resistor Value
VDD_CORE	0.05 Ω
VDD_MPU	0.05 Ω
VDDSPLLMPU	2 Ω
VDDS_SRAMMPU_BB	2 Ω
VDDS_SRAM_CORE_BG	2 Ω
VDDA1P8V_USB0	1 Ω
VDDA3P3V_USB0	2 Ω
VDDS_PLL_DDR	2 Ω
VDDS_DDR	0.24 Ω
SA_VDDSHV1	0.24 Ω
SA_VDDSHV2	0.24 Ω
SA_VDDSHV3	0.24 Ω
SA_VDDSHV4	0.24 Ω
SA_VDDSHV5	0.24 Ω
SA_VDDSHV6	0.24 Ω
SA_VDDS	0.24 Ω
SA_VDDA_ADC	1 Ω
VDDS_PLL_CORE_LCD	2 Ω
VDDS_RTC	2 Ω
VDDS_OSC	2 Ω

4 Configuration and Setup

The GP EVM has many different subsystems to allow development around the AM335x's capabilities. Most of these subsystems are fixed with regard to address locations and pin assignments. However, there are some functions that can be changed by configuring the EVM with switches. For the GP EVM, some of the AM335x pins are connected to different subsystems based on the CPLD profile number that is active. (The CPLD profile number is selected by a 4-bit DIP switch on the GP daughterboard.) The CPLD is used primarily as a pin mux switch.

Additionally, the AM335x has SYSBOOT pins that can be configured a certain way using two 8-bit DIP switches on the baseboard. These SYSBOOT switches will configure the AM335x to different settings. For instance, the boot method of the processor can be setup by setting certain of these DIP switches to particular settings. The SW3 DIP switch has the switches that set the SYSBOOT[0..7] and SW4 DIP switch has the switches that set the SYSBOOT[8..15]. For the actual definitions of each of the SYSBOOT signals, see the *AM335x ARM Cortex-A8 Microprocessors (MPUs) Technical Reference Manual* and *Sitara AM335x ARM Cortex-A8 Microprocessors (MPUs) Data Manual*. The SW3 DIP switch 1 corresponds to SYSBOOT(0), SW3 DIP2 = SYSBOOT(1), and so forth. The SW4 DIP switch 1 corresponds to SYSBOOT(8), SW4 DIP2 = SYSBOOT(9), and so forth. When the DIP switch is off, the corresponding SYSBOOT signal is pulled high. For more details, when the DIP switch is on, the corresponding SYSBOOT signal is pulled low. Also, see the GP EVM baseboard schematic.

4.1 CPLD

The general purpose daughterboard has a CPLD on it with connections to the major AM335x signals. The Altera EPM2210 is used to do active muxing of non-critical signals. It is also available for test logic that may be used for extra-EVM tests. AM335x can communicate and read the configuration of the muxes inside the CPLD by using the Inter-Integrated Circuit (I2C) bus. I2C0 of the AM335x is connected to the CPLD and an I2C slave is implemented within the CPLD. The I2C address is 0x35.

To control the configuration of the muxes inside the CPLD, the user can select the required profiles by using three switches as shown in Figure 8. Switches 1 to 3 control the required CPLD configurations and thereby the profile in which the EVM will operate. Switch 1 of the DIP switch is the lsb in the profile number and Switch 3 of the DIP switch is the msb of the profile number so possible profiles numbers are 0 to 7. For a description of the AM335x pin definitions for each of the 8 profiles, see the Pin Use Description Section 6 later in this document. The fourth DIP switch is reserved and should always be off.

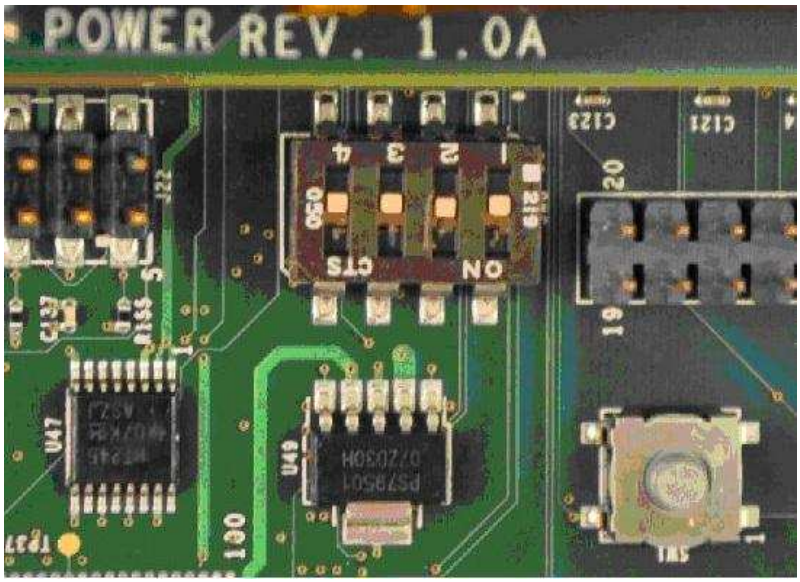


Figure 8. AM335x CPLD Profile Switch

4.2 I2C Address Assignments

In the AM335x GP EVM boards, each separate board has an I2C ID memory that contains the details of the identity of that board such as its configuration, and so forth. For more details on the memories' contents, see Section 4.3. All of the ID memories use I2C0 from AM335x (as does the Smart Reflex to the PMIC) so that software can always check I2C0 at the defined I2C addresses for the presence of a board and its contents. Therefore, the baseboard is the only board that has the ID memory set to 0x50, the daughterboard's addresses are all 0x51 (only one daughterboard is ever connected at a time), and the LCD (display board) is at 0x52.

Table 5. AM335x Baseboard I2C Bus Addresses

AM335x Baseboard Function	AM335x I2C Port	Address
Baseboard ID Memory	I2C0	0x50
AM335x PMIC Smart Reflex	I2C0	0x12
AM355x PMIC Control	I2C0	0x2D

Table 6. AM335x GP Daughterboard I2C Bus Addresses

AM335x GP Daughterboard Function	AM335x I2C Port	Address
AIC3106 Audio Codec	I2C1/I2C2	0x1B
General Purpose Daughterboard ID Memory	I2C0	0x51
Accelerometer	I2C1/I2C2	0x18
Ambient Light Sensor	I2C1/I2C2	0x39
Temperature Sensor	I2C1/I2C2	0x48
CPLD Control	I2C0	0x35
I/O Expander 0	I2C1/I2C2	0x20
I/O Expander 1	I2C1/I2C2	0x21

Table 7. AM335x LCD A Board I2C Bus Addresses

AM335x LCD A Board Function	AM335x I2C Port	Address
LCD A Board ID memory	I2C0	0x52
Touch Screen Controller	I2C0	0x4A
TLC59108	I2C0	0x40

4.3 I2C ID Memory

Each of the three boards in the EVM have a dedicated I2C EEPROM, which contains specific identity and configuration information for that board. In addition, there is available space in each memory for user-specific configuration information.

The part number of the memory device is pn#CAT24C256WI-GT3.

Table 8. AM335x 15x15 Baseboard EEPROM Data

Name	Size (bytes)	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for board in ASCII "A33515BB" = AM335x 15x15 Baseboard
Version	4	Hardware version code for board in ASCII "1.0A" = rev. 01.0A
Serial Number	12	Serial number of the board. This is a 12 character string which is: WWYY4P16nnnn where: WW = 2 digit week of the year of production YY = 2 digit year of production nnnn = incrementing board number
Configuration	32	Codes to show the configuration setup on this board. For the available EVM's supported, the following codes are used: ASCII "SKU#01" = baseboard for gen purpose evm ASCII "SKU#02" = baseboard for industrial motor control evm. Remaining 26 bytes are reserved.
Ethernet MAC Address #0	6	MAC Address for AM335x Ethernet MAC #1
Ethernet MAC Address #1	6	MAC Address for AM335x Ethernet MAC #2 or PRU #0
Ethernet MAC Address #2	6	MAC Address for AM335x PRU #1 (if used)
Available	32702	Available space for other non-volatile codes and data.

Table 9. AM335x General Purpose Daughterboard EEPROM Data

Name	Size (bytes)	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for board in ASCII "A335GPBD" = AM335x General Purpose Daughterboard
Version	4	Hardware version code for board in ASCII "1.0A" = rev. 01.0A
Serial Number	12	Serial number of the board. This is a 12 character string which is: WWYY4P13nnnn where: WW = 2 digit week of the year of production YY = 2 digit year of production nnnn = incrementing board number
Configuration	32	Codes to show the configuration setup on this board. For the available EVM's supported, the following codes are used: ASCII "SKU#00" = standard gp daughterboard configuration. Remaining 26 bytes are reserved.
CPLD Version	8	CPLD code version for board in ASCII "CPLD1.0A" = rev. 01.0A of the CPLD.
Available	32702	Available space for other non-volatile codes and data.

Table 10. AM335x LCD A Board EEPROM Data

Name	Size (bytes)	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for board in ASCII "A335LCDA" = AM335x LCD A Board
Version	4	Hardware version code for board in ASCII "1.0A" = rev. 01.0A
Serial Number	12	Serial number of the board. This is a 12 character string which is: WWYY4P15nnnn where: WW = 2 digit week of the year of production YY = 2 digit year of production nnnn = incrementing board number
Configuration	32	Codes to show the configuration setup on this board (codes to be assigned TBD)
Available	32708	Available space for other non-volatile codes and data.

5 AM335x EVM Functional Block Descriptions

This section describes major functional blocks of the AM335x EVM System.

5.1 Board Identity Memory

Each of the boards contains a serial EEPROM that contains board specific data that allows the processor to automatically detect which board is connected and the version of that board. Other hardware specific data can be stored on this memory device as well. The part number of the memory device is pn#CAT24C256WI-GT3. For details on the data in this memory, see Section 4.

5.2 SDMMC0 Connector

The SDMMC0 connector on the baseboard is a Morethanall card socket #MHC-W21-601. This is a standard SD/MMC Card type of connector. It is connected to the MMC0 port of the AM335x processor. For supported card types and densities, see the *AM335x ARM Cortex-A8 Microprocessors (MPUs) Technical Reference Manual* and the *Sitara AM335x ARM Cortex-A8 Microprocessors (MPUs) Data Manual*.

The Pin assignment is as shown in Table 11.

Table 11. AM335x SDMMC0 Connector Pin Details

Pin No	Memory Card PIN Number
MMC plus & MMC mobile & MMC & RS-MMC & SD#1	RSV/DAT3
MMC plus & MMC mobile & MMC & RS-MMC & SD#2	CMD
MMC plus & MMC mobile & MMC & RS-MMC & SD#3	GND
MMC plus & MMC mobile & MMC & RS-MMC & SD#4	V_{CC}
MMC plus & MMC mobile & MMC & RS-MMC & SD#5	CLK
MMC plus & MMC mobile & MMC & RS-MMC & SD#6	GND
MMC plus & MMC mobile & MMC & RS-MMC & SD#7	DAT0
MMC plus & MMC mobile & SD#8	DAT1
MMC plus & MMC mobile & SD#9	DAT2
MMC plus & MMC mobile#10	DAT4
MMC plus & MMC mobile#11	DAT5
MMC plus & MMC mobile#12	DAT6
MMC plus & MMC mobile#13	DAT7
miniSD#1	CD/DAT3
miniSD#2	CMD
miniSD#3	GND
miniSD#4	V_{CC}
miniSD#5	CLK
miniSD#6	GND
miniSD#7	DAT0
miniSD#8	DAT1
miniSD#9	DAT2
miniSD#10	NC
miniSD#11	NC

5.3 Gbit Ethernet

The AM335x baseboard has a Gbit Ethernet transceiver Atheros AR8031_AL1A that is connected to J15.

The reset on the transceiver is driven by the board system reset SYS_RESETn and the individual reset ETHER_RESETn signal that is controlled by GIO SA_GMII1_COL. A 25 MHz crystal drives the clock signal for the AR8031. The Ethernet INT pin is sent to the AM335x SA_GMII1_CRS pin for interrupt.

NOTE: The GP EVM PCB does not support external delay for the clock signals on the RGMII interface. The AR8031A PHY can be setup to use internal clock delay mode once booting is complete. Therefore, there may be problems in function and performance when booting in Gb mode or when running Gb Ethernet mode before the AR8031A PHY is configured properly. For more information, see the *AM335x General-Purpose EVM Errata*.

The PHYAD pins are left unconnected for setting the PHY's address so it is by default 0x01.

Table 12. AM335x Gbit Ethernet Pin Details

Pin Number	Signal Name	Description
1	DGND	Ground
2	V3_3D	Power 3.3V supply
3	ETHER_D3P	Ethernet Data 3 POSITIVE
4	ETHER_D3N	Ethernet Data 3 NEGATIVE
5	ETHER_D2P	Ethernet Data 2 POSITIVE
6	ETHER_D2N	Ethernet Data 2 NEGATIVE
7	ETHER_D1P	Ethernet Data 1 POSITIVE
8	ETHER_D1N	Ethernet Data 1 NEGATIVE
9	ETHER_D0P	Ethernet Data 0 POSITIVE
10	ETHER_D0N	Ethernet Data 0 NEGATIVE
D1	PHY_LED_ACTn	
D2	DGND	Ground
D3	DGND	Ground
D4	PHY_LED_1000n	
M1	NC	
M2	NC	
SHLD1	DGND	Ground
SHLD2	DGND	Ground

The baseboard has one Gb/s Ethernet PHY and RJ-45 connector for the MII1 port. The RJ-45 connector used to communicate with external Ethernet and for testing with external loopback cable.

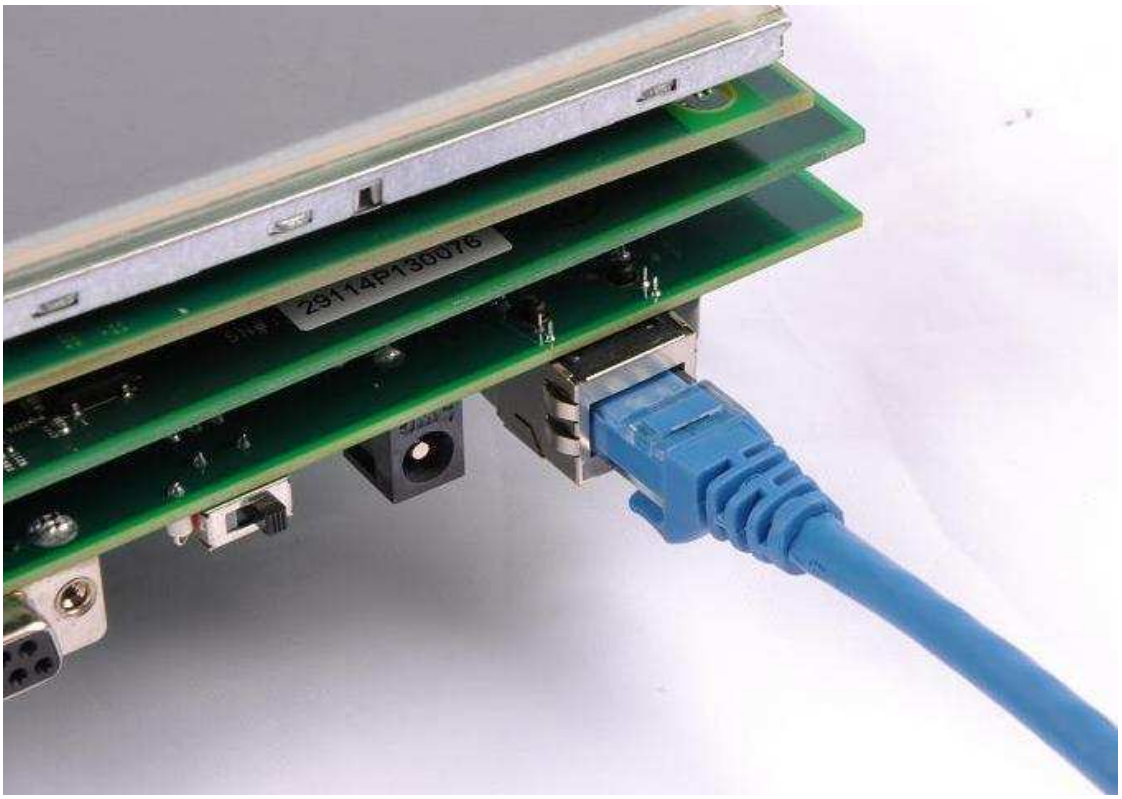


Figure 9. AM335x Baseboard Ethernet

5.4 USB

The AM335x ZCZ package supports 2 USB ports. The USB ports are on the baseboard and connected to a microUSB AB connector and a standard A connector. The ESD device TPD4012 and common choke filter ACM2012 (TDK) are used on the USB signals before they are connected to the AM335x pins. The microAB connector has its ID pin tied to ground through a 120K resistor by default so that the port looks like a B device.

Table 13. AM335x USB Port0

Pin Number	Signal Name	Description
1	VUSB_VBUS0	USB0 Bus Voltage
2	USB0_CONN_DM	USB0 Data Minus
3	USB0_CONN_DP	USB0 Data Plus
4	USB0_ID	USB0 Identification
5	DGND	Ground

Table 14. AM335x USB Port1

Pin Number	Signal Name	Description
1	VUSB_VBUS1	USB1 Bus Voltage
2	USB1_CONN_DM	USB1 Data Minus
3	USB1_CONN_DP	USB1 Data Plus
4	DGND	Ground

5.5 COM – Mobile Connectivity Expansion Connector

The AM335x baseboard supports TI MCS COM6/7 form factor wireless boards through the J11 COM connector, which is a Samtec card edge type connector pn# MEC. This connector supports COM6/7 types of boards, and more details about this connector can be found in the MCS COM6/7 board documents.

The COM connector requires 3.6 V 442 mA on the power supply. Therefore, a TPS79501 LDO regulator is used to provide this voltage supply from the base 5.0 V supply.

The signals on the COM board are all 1.8 V voltage level. Thus voltage translators are placed to convert to and from 3.3 V of the AM335x rail for a particular signal which is running at 3.3 V.

5.6 NOR Flash Memory

The GP daughterboard has Flash memory, which is a NOR type of Flash so that the AM335x's access to and from NOR Flash function can be tested. The part number of the memory used is Numonyx pn#M29W128GL, which is a 16MB (x16 width) Flash memory. The GPMC signals are used to communicate with this memory. The GPMC signals are muxed with other signals in AM335x. Also, several other devices connect to the GPMC signals on the baseboard and the daughterboard. Boot from NoR is currently not supported on EVM.

5.7 Ambient Light Sensor

The ambient light sensor on the GP daughterboard detects and reports the intensity of light luminescence in the human visual spectrum. The part number of the light sensor used is TAOS pn#TSL2550. The AM335x interfaces to the light sensor through I2C.

I2C1 is used and it is muxed in a TXS0102 using mux signal MUXCTRL_I2C1, which comes from the CPLD (based on the selected profile number).

5.8 RS-232 Connectors

The baseboard has one RS-232 connector (DB9 male) for one of the UART's. The general purpose daughterboard has 3 more DB9 RS-232 connectors (male). The muxes on this daughterboard (implemented in the CPLD) allow the UART's on the AM335x processor to be connected to these 3 connectors. UART0 is always connected to the DB9 connector on the baseboard. For the profiles that support connection of the UART's 1 through 5 to these connectors on the daughterboard, see Table 18. When a profile is selected that enables a UART for use, the UART's are assigned to the DB9 connectors from UART1 to UART5 starting at J10, then to J12, to J14, and then back around to J10. Therefore, when enabled by the profile selection:

AM335x UART1 => J10

AM335x UART2 => J12

AM335x UART3 => J14

AM335x UART4 => J10

AM335x UART5 => J12

Furthermore, these connectors can be connected together (through cable) to provide loopback testing. The MAX3232E is used for the RS-232 level translation.

5.9 SDMMC1 Connector

The baseboard has one SDMMC connector for the SDMMC0 port. This general purpose daughterboard has 1 more SDMMC connector for the MMC1 interface.

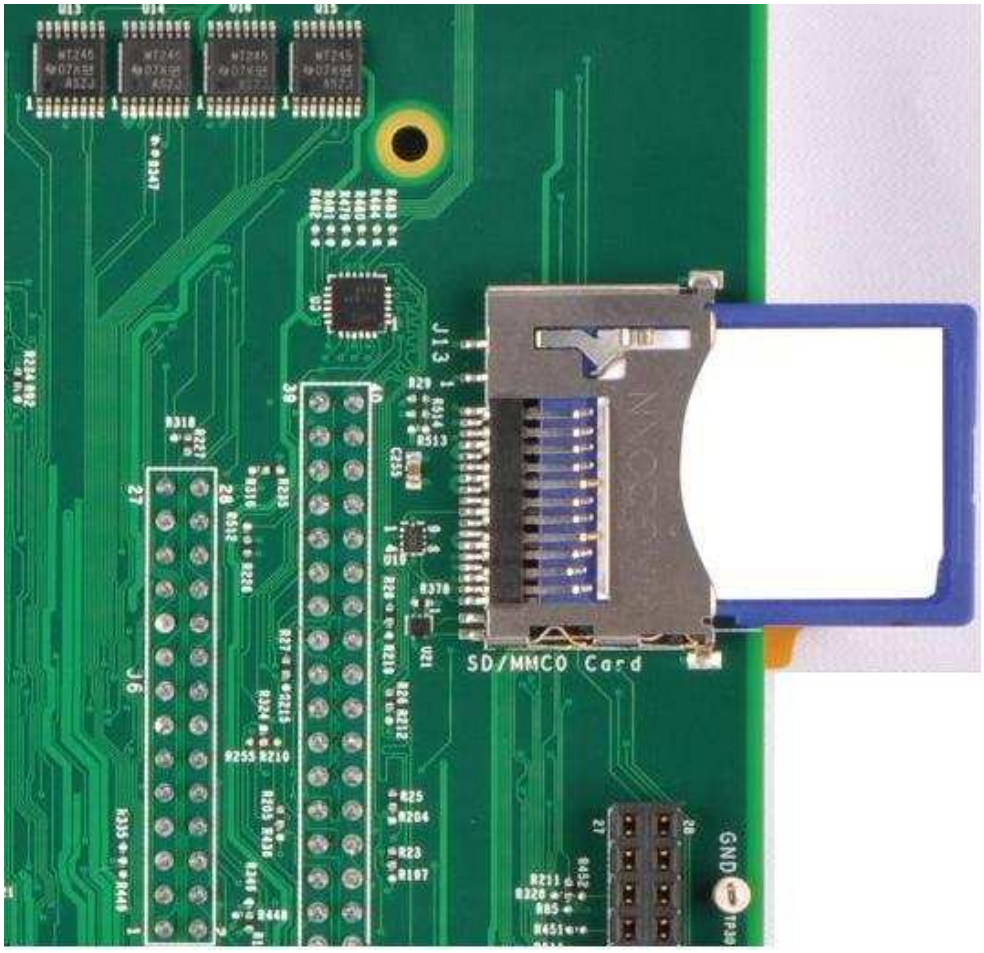


Figure 10. AM335x Baseboard SDMMC Connector

The Pin assignment of the GP daughterboard SDMMC1 connector is the same as the baseboard SDMMC0 connector. For signal assignments, see Table 11.

5.10 CAN

The general purpose daughterboard has 1 CAN transceiver and connector for the CAN0 interface. The CAN transceiver that is used is the TI ISO1050 and the connector is a DB9 male connector.

Table 15. AM335x General Purpose Daughterboard CAN Connector Pin Details

Pin Number	Signal Name	Description
1	Reserved	Upgrade Path
2	CAN_L	Dominant Low
3	CAN_GND	Ground
4	Reserved	Upgrade Path
5	CAN_SHLD	Shield, Optional
6	GND	Ground, Optional
7	CAN_H	Dominant High
8	Reserved	Upgrade Path
9	CAN_V+	Power, Optional

A PSM712 transient voltage suppressor and RSZ-3.305HP isolated voltage regulator are connected to the ISO1050 for full industrial connection. The AM335x side line filters are calculated for a max CAN transmission speed of 10 MHz.

5.11 I2C Expander

This general purpose daughterboard has two I2C I/O expanders. The I/O expander that is used is the TI TCA6408A. The I2C addresses of the expander chip are set to 0x20 and 0x21. Each I/O expander has 4 inputs and 4 outputs.

Table 16. AM335x General Purpose Daughterboard I2C Expander 0

I/O Number	In/Out	Description
0	In	Expansion Header
1	In	Expansion Header
2	In	Expansion Header
3	In	Expansion Header
4	Out	LED
5	Out	LED
6	Out	LED
7	Out	LED

Table 17. AM335x General Purpose Daughterboard I2C Expander 1

I/O Number	In/Out	Description
0	In	Expansion Header
1	In	Expansion Header
2	In	Expansion Header
3	In	Expansion Header
4	Out	LED
5	Out	LED
6	Out	LED
7	Out	LED

5.12 ADC Inputs

The general purpose LCD A board has a resistive touchscreen on the LCD (for more details, see Section 5.21). The touchscreen uses 4 of the 8 ADC input channels. The remaining 4 channels are connected to isolated connectors so that a signal can be input into them for testing. J8 connector on the GP daughterboard is used to get the analog data from the touch screen and also for manual testing,

5.13 Audio Volume Controls

In some of the profiles, audio is enabled. Switches for audio volume control are enabled in these profiles to aid in developing audio applications. These switches are connected to the eOEP. These switches are pushbutton switches to allow realistic actuation of the volume controls.

5.14 Accelerometer

An accelerometer is included on the GP daughterboard to allow motion data to be captured and used by the software. The accelerometer is mounted as close to the center of the board as possible to allow the most useful and dynamic data. The ST Micro model LIS331DLH accelerometer is used and is connected via I2C to the AM335x. The I2C address is 0x18. I2C1 is used and it is muxed in a TXS0102.

5.15 Keypad

Pushbutton switches (6) are attached to GIO's via a scanning method to allow a keypad to be used. These switches are powered and scanned to see if a switch is pressed (high) or if the switch is not pressed (low on scan line). The hardware debounce capacitors are not installed by default so software must handle the noise associated with the mechanical bouncing of the switches.

Table 18. AM335x GP Daughterboard GPIO Keypad Signals

Signal	Port Number	Pin Number	Event
See pin use document	1	25	Keypad SCN 0
See pin use document	1	26	Keypad SCN 1
See pin use document	1	27	Keypad SCN 2
See pin use document	1	21	Keypad POWER A
See pin use document	1	22	Keypad POWER B

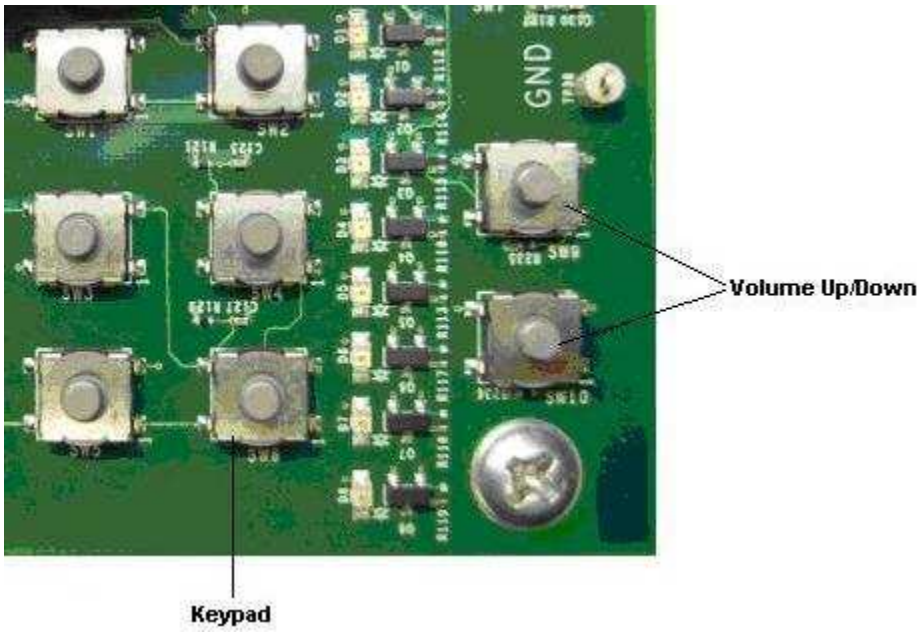


Figure 11. AM335x GP Keypad

5.16 Haptics Mechanical Vibrator

A Micro Precision pico haptics motor on the GP Daughterboard is used to signal events via mechanical vibration. This is a 304-100 PicoHaptic device that is triggered by a CPLD signal through a FET switch. Thus, the profile mode defines which AM335x GIO will turn on this haptics vibrator.

5.17 Audio Buzzer

The PUI Audio AI-1027-TWT on the GP Daughterboard is used as an audio buzzer. This is a 2700Hz continuous buzzer that is triggered via a signal from the CPLD through a FET switch. Thus, the profile mode defines which AM335x GIO will turn on this audio buzzer.

5.18 Temperature Sensor

A TI TMP275 temperature sensor on the GP Daughterboard is used to report ambient temperature. It is controlled by I2C and the I2C address is 0x48. I2C1 is used and it is muxed in a TXS0102.

5.19 NAND Flash Memory

The general purpose daughterboard has a Micron NAND Flash Memory. This is a MT29F2G08ABAEAWP 2Gb 8-bit wide Flash memory. The footprint is set to allow the 16-bit version to be placed instead although there is no plan for this. This memory was placed on the daughterboard to allow active muxing of its signals and allow NOR/MMC1 connection.

Table 19. AM335x NAND Pin Details

Pin Number	Signal	Description
1	NC	
2	NC	
3	NC	
4	NC	
5	NC	
6	NC	
7	NAND_WAIT	NAND wait
8	NAND_OEn	NAND output enable
9	NAND_CSn	NAND chip select
10	NC	
11	NC	
12	VDDSHV1	Power supply
13	DGND	Ground
14	NC	
15	NC	
16	NAND_BE0n_CLE	NAND Byte Enable 0 / Command Latch Enable
17	NAND_ADVN_ALE	NAND Address Valid / Address Latch Enable
18	NAND_WEn	NAND Write Enable
19	NAND_WPn	NAND Write Protect
20	NC	
21	NC	
22	NC	
23	NC	
24	NC	
25	DGND	Ground
26	NAND_D8	NAND Data
27	NAND_D9	NAND Data
28	NAND_D10	NAND Data

Table 19. AM335x NAND Pin Details (continued)

Pin Number	Signal	Description
29	NAND_D0	NAND Data
30	NAND_D1	NAND Data
31	NAND_D2	NAND Data
32	NAND_D3	NAND Data
33	NAND_D11	NAND Data
34	VDDSHV1	Power supply
35	NC	
36	DGND	Ground
37	VDDSHV1	Power supply
38	NC	
39	VDDSHV1	Power supply
40	NAND_D12	NAND Data
41	NAND_D4	NAND Data
42	NAND_D5	NAND Data
43	NAND_D6	NAND Data
44	NAND_D7	NAND Data
45	NAND_D13	NAND Data
46	NAND_D14	NAND Data
47	NAND_D15	NAND Data
48	DGND	Ground

5.20 Audio

The TLV320AIC3106 audio codec is used on the general purpose daughterboard. This codec is controlled from AM335x by I2C, which is at address 0x1B.

5.21 LCD Screen

The LCD is a Three Five 7in WVGA (800x480) RGB LCD panel part number #TFC-S9700RTWV43TR-01B. It is a 24-bit RGB TFT LCD with 27 white LED's for backlight (controlled by one power regulator). The connector is FPC 60-pin pn #FH28- 60S-0.5SH(05).

The LED backlight on the LCD is controlled by a TPS61081 PWM controlled LED driver.

5.22 Resistive Touch Screen

Table 20. LCD A Resistive Touch Screen Pin Details

Pin Name	Direction	Description
AN0 / XPUL	In	Analog input 1
AN1 / XNUR	In	Analog input 2
AN 2/ YPLL	In	Analog input 3
AN 3/ YNLR	In	Analog input 4
AN 4 / Wiper	In	Analog input 5

5.23 SPI Flash Memory

There is a SPI-based Flash Memory on the daughterboard of the EVM. This is a 64Mb memory Winbond W25Q64CV. For the profile that supports the connection to the SPI memory, see Section 6. Due to connection requirements for other devices that share the same pins as the SPI memory, the GP EVM is not designed to operate at the max SPI clock rate as shown in the *Sitara AM335x ARM Cortex-A8 Microprocessors (MPUs) Data Manual*.

5.24 WLAN/BT Module

There is a Wireless LAN and Bluetooth card connector on the GP EVM. This connector contains a card with a WL1271 WLAN/BT module and integrated antenna.

6 Pin Use Description

6.1 Functional Interface Mapping

Some signals of the AM335x are connected to a fixed device on the EVM where it cannot be changed. Some of the signals of the AM335x, however, are connected to devices on the EVM based on the profile setting.

Since AM335x processor has up to 8 different mux options for each signal, options have to exist on the EVM for allowing the supported subsets of these signals. The pinuse document shows only the signals, which are used on the expansion daughterboard.

In the schematics, the AM335x pin names are used for the net names up to the specific mux that connects the signal to the particular function. This is to allow easy knowledge of a single pin's connection to multiple functions through the muxes without burdening the net name to tell all the various functions.

See the additional columns in the pinmux document as there are preset profiles that define what peripherals on the hardware boards are connected and able to be used at a given time.

Table 21. Pin Use Assignment (1)

ddr_dqsn0	P2	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)
ddr_dqs1	L1	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)
ddr_dqsn1	L2	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)
ddr_vref	J4	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)
ddr_vtp	J3	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)	B(SDRAM)
ddr_strben0									
ddr_strben1									
AIN7	C9	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)
AIN6	A8	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)
AIN5	B8	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)
AIN4	C8	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)	GP(ADC)
AIN3	A7	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)
AIN2	B7	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)
AIN1	C7	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)
AIN0	B6	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)
VREFP	B9	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)
VREFN	A9	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)	L(Touch)
iforce									
vsense									
testout	A3								

(1) Key:
B - Base Board
GP - GP Daughter Board
L - LCD Board
C - COM Board

6.2 GPIO Definitions

See the updated pinmux documents that show use case columns for GPIO's. The developer can select and enable pins based on the selective peripheral pins as output or input. For the GP EVM, each single pin is muxed based on the CPLD profile number that is active. (The CPLD profile number is selected by a DIP switch.)

7 Board Connectors

7.1 Expansion Connectors

The expansion connector details are listed in Table 22 through Table 25.

Table 22. AM335x EXP0 Connector

Pin Number	Signal	Description
1	V1_8D	Power 1.8 V supply
2	V5_0D	Power 5.0 V rail
3	GPMC_AD7	GPMC Address and Data
4	RMII1_RXD3	RMII Receive Data bit 3
5	GPMC_AD6	GPMC Address and Data
6	RMII1_TXCLK	RMII Transmit Clock
7	GPMC_AD5	GPMC Address and Data
8	RMII1_RXCLK	RMII Receive Clock
9	GPMC_AD4	GPMC Address and Data
10	RMII1_RXD2	RMII Receive Data bit 2
11	GPMC_AD3	GPMC Address and Data
12	RMII1_TXD2	RMII Transmit Data bit 2
13	GPMC_AD2	GPMC Address and Data
14	RMII1_RXDV	RMII Receive Data Valid
15	GPMC_AD1	GPMC Address and Data
16	RMII1_TXD3	RMII Transmit Data bit 3
17	GPMC_AD0	GPMC Address and Data
18	RMII1_TXD1	RMII Transmit Data bit 1
19	GPMC_CS2n	GPMC Chip Select
20	RMII1_TXD0	RMII Transmit Data bit 0
21	GPMC_CS1n	GPMC Chip Select
22	RMII1_RXD1	RMII Receive Data bit 1
23	SPI0_D1	SPI Data
24	SPI0_CS0	SPI Chip Select
25	PMIC_PWR_EN	
26	SYS_RESETn	System reset
27	DGND	Ground
28	DGND	Ground

Table 23. AM335x EXP1 Connector

Pin Number	Signal	Description
1	NOT USED	
2	NOT USED	
3	NOT USED	
4	NOT USED	
5	NOT USED	
6	NOT USED	
7	DGND	Ground
8	DGND	Ground
9	NOT USED	
10	NOT USED	
11	SYS_WARMRESETn	System warm reset
12	EXP_PB_POWERON	Power ON
13	NOT USED	
14	NOT USED	
15	NOT USED	
16	NOT USED	
17	NOT USED	
18	NOT USED	
19	GPMC_WAIT	GPMC Wait
20	NOT USED	
21	GPMC_WPn	GPMC Write Protect
22	NOT USED	
23	GPMC_CLK	GPMC Clock
24	NOT USED	
25	GPMC_CS0n	GPMC Chip Select
26	GPMC_ADVn_ALE	GPMC Address Valid / Address Latch Enable
27	NOT USED	
28	GPMC_BE0n_CLE	GPMC Byte Enable 0 / Command Latch Enable

Table 24. AM335x EXP2 Connector

Pin Number	Signal	Description
1	DGND	Ground
2	GPMC_BE1n	GPMC Byte Enable 1
3	RMII1_REFCLK	RMII Reference Clock
4	GPMC_CS3n	GPMC Chip Select
5	RMII1_RXD0	RMII Receive Data bit 0
6	GPMC_OEn_REn	GPMC Output / Read Enable
7	MDIO_DATA	MDIO Data
8	GPMC_WEn	GPMC Write Enable
9	MDIO_CLK	MDIO Clk
10	DGND	Ground
11	DGND	Ground
12	MMC0_CLK	MMC Clock
13	SPI0_CLK	SPI Clock
14	MMC0_CMD	MMC Command
15	SPI0_D0	SPI Data
16	MMC0_DAT0	MMC Data Bus
17	SPI0_CS1	SPI Chip Select
18	WAKEUP	
19	ECAP0_IN_PWM0_OUT	Enhanced capture 0 input or Auxiliary PWM0 out
20	DGND	Ground
21	UART0_CTSn	UART Clear to Send
22	MMC0_DAT1	MMC Data Bus
23	UART0_RTSn	UART Request to Send
24	MMC0_DAT2	MMC Data Bus
25	UART0_RXD	UART Receive Data
26	MMC0_DAT3	MMC Data Bus
27	UART0_TXD	UART Transmit Data
28	XDMA_EVENT_INTR0	External DMA Event or Interrupt 0
29	UART1_CTSn	UART Clear to Send
30	DGND	Ground
31	UART1_RTSn	UART Request to Send
32	XDMA_EVENT_INTR1	External DMA Event or Interrupt 1
33	UART1_RXD	UART Receive Data
34	RMII1_COL	RMII Collision
35	UART1_TXD	UART Transmit Data
36	RMII1_CRS	RMII Carrier Sense
37	DGND	Ground
38	RMII1_RXERR	RMII Receive Data Error
39	V3_3D	Power 3.3V supply
40	RMII1_TXEN	RMII Transmit Enable

Table 25. AM335x EXP3 Connector

Pin Number	Signal	Description
1	MCASP0_ACLKX	McASP0 Transmit Bit Clock
2	GPMC_A0	GPMC Address
3	DGND	Ground
4	GPMC_A1	GPMC Address
5	MCASP0_FSX	McASP0 Transmit Frame Sync
6	GPMC_A2	GPMC Address
7	MCASP0_AXR0	McASP0 Serial Data (IN/OUT)
8	GPMC_A3	GPMC Address
9	EXP3_P9	
10	GPMC_A4	GPMC Address
11	VDDSHV2	Power supply for SDMMC cards
12	GPMC_A5	GPMC Address
13	MCASP0_AHCLKR	McASP0 Receive Master Clock
14	DGND	Ground
15	V3_3D	Power 3.3 V supply
16	GPMC_A6	GPMC Address
17	MCASP0_ACLKR	McASP0 Receive Bit Clock
18	GPMC_A7	GPMC Address
19	VEXPD	VBAT spower
20	DGND	Ground
21	MCASP0_FSR	McASP0 Receive Frame Sync
22	GPMC_A8	GPMC Address
23	MCASP0_AXR1	McASP0 Serial Data (IN/OUT)
24	GPMC_A9	GPMC Address
25	DGND	Ground
26	GPMC_A10	GPMC Address
27	MCASP0_AHCLKX	McASP0 Transmit Master Clock
28	GPMC_A11	GPMC Address

7.2 LCD Connectors

The connector details of LCD are described in Table 26 and Table 27.

Table 26. AM335x LCD Connector 1

Pin Number	Signal	Description
1	V5_0D	Power 5.0 V rail
2	V5_0D	Power 5.0 V rail
3	LCD_DATA1	LCD data bus
4	LCD_DATA0	LCD data bus
5	LCD_DATA3	LCD data bus
6	LCD_DATA2	LCD data bus
7	LCD_DATA5	LCD data bus
8	LCD_DATA4	LCD data bus
9	LCD_DATA12	LCD data bus
10	LCD_DATA10	LCD data bus
11	LCD_DATA23	LCD data bus
12	LCD_DATA14	LCD data bus
13	LCD_DATA19	LCD data bus
14	LCD_DATA22	LCD data bus
15	I2C0_SDA	I2C0 Data
16	LCD_DATA11	LCD data bus
17	LCD_VSYNC	LCD Vertical Sync
18	DGND	Ground
19	DGND	Ground
20	DGND	Ground

Table 27. AM335x LCD Connector 2

Pin Number	Signal	Description
1	VEXPD	Power variable supply
2	V1_8D	Power 1.8V supply
3	LCD_DATA20	LCD data bus
4	LCD_DATA21	LCD data bus
5	LCD_DATA17	LCD data bus
6	LCD_DATA18	LCD data bus
7	LCD_DATA15	LCD data bus
8	LCD_DATA16	LCD data bus
9	LCD_DATA7	LCD data bus
10	LCD_DATA13	LCD data bus
11	LCD_DATA8	LCD data bus
12	V5_0D	Power 5.0V rail
13	LCD_DATA9	LCD data bus
14	I2C0_SCL	I2C0 Clock
15	LCD_DATA6	LCD data bus
16	LCD_PCLK	LCD pixel clock
17	LCD_DEN	
18	LCD_HSYNC	LCD Horizontal Sync
19	DGND	Ground
20	DGND	Ground

The touchscreen connector details are shown in Table 28.

Table 28. AM335x Touchscreen Connector

Pin Number	Signal	Description
1	TSC_GIO0	GIO0
2	V3_3D	Power 3.3V supply
3	TSC_GIO1	GIO1
4	TSC_I2CSCL	I2C SCLK for touchscreen
5	TSC_CLK	Source clock for touchscreen controller
6	TSC_I2CSDA	I2C SDATA for touchscreen
7	TSC_RSV0	Reserved
8	TSC_GIO2	GIO2
9	TSC_RSV1_VREF	Reserved power pin
10	DGND	Ground
11	GNDA_TSC	Analog ground
12	GNDA_TSC	Analog ground
13	TSC_AIN4	ADC4 input
14	TSC_AIN0	ADC0 input
15	TSC_AIN5	ADC5 input
16	TSC_AIN1	ADC1 input
17	TSC_AIN6	ADC6 input
18	TSC_AIN2	ADC2 input
19	TSC_AIN7	ADC7 input
20	TSC_AIN3	ADC3 input

7.3 JTAG Connector

Other JTAG adaptors are available at the TI e-store and can be purchased from here.

8 References

- *Sitara AM335x ARM Cortex-A8 Microprocessors (MPUs) Data Manual*
- *AM335x ARM Cortex-A8 Microprocessors (MPUs) Technical Reference Manual*
- *AM335x General-Purpose EVM Errata*

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