User's Guide

AM64x/AM243x GP EVM User's Guide

TEXAS INSTRUMENTS

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1 Introduction

The AM64x/AM243x GP EVM is a standalone test, development, and evaluation module (EVM) that lets developers evaluate the AM64x/AM243x functionality and develop prototypes for a variety of applications. The EVM implements either the Sitara™ AM6442 MPU or the AM2434 MCU. Additional supporting components allow the user to make use of the various device interfaces including Industrial Ethernet, standard Ethernet, PCIe, Fast Serial Interface (FSI) and others to easily create prototypes. An on-board display makes use of AM64x/AM243x serial peripheral interface (SPI) ports to provide the ability for local visual outputs in addition to the various LED provided. On-board current measurement capabilities are available to monitor power consumption for power-conscious applications. The supplied USB cable paired with embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ software from TI.

1.1 EVM Revisions and Assembly Variants

The various AM64x/AM243x GP EVM PCB design revisions, and asssembly variants are listed in the table below. Specific PCB revision is indicated in silkscreen on the PCB. Specific assembly variant is indicated with additional sticker label.

Table 1-1. AM64x/AM243x GP EVM PCB design revisions, and asssembly variants

PCB Revison	Assembly Variant	Revision and Assembly Variant Description
PROC101E2	N/A (single variant produced)	First prototype, early release revision of the AM64x/AM243x GP EVM. Implements the Sitara™ AM6442 MPU.
PROC101A	001	First production release of the AM64x/AM243x GP EVM. Implements the Sitara™ AM6442 MPU.
PROC101A	002	First production release of the AM64x/AM243x GP EVM. Implements the Sitara™ AM2434 MCU in the ALV package.

Note

Throughout this document, the AM6442 and AM2434 devices are interchangable in diagrams and other tables, other than explicitly defined exception. The AM2434 MCU in the ALV package and the AM6442 MPU are footprint and pinout compatible and the PCB has been designed to accommodate both.

2 Important Usage Notes

2.1 Power-On Usage Note

CAUTION

To avoid high inrush currents and prevent possible damage to the AM64x/AM243x GP EVM components, the proper EVM power on and power off procedures are required. For more details, see Section 3.3.

3 System Description

The following sections describe the AM64x/AM243x GP EVM design. Top-down and bottom-up views of the PCB are provided in Figure 3-1 and Figure 3-2 for reference to major IC and connector component locations.

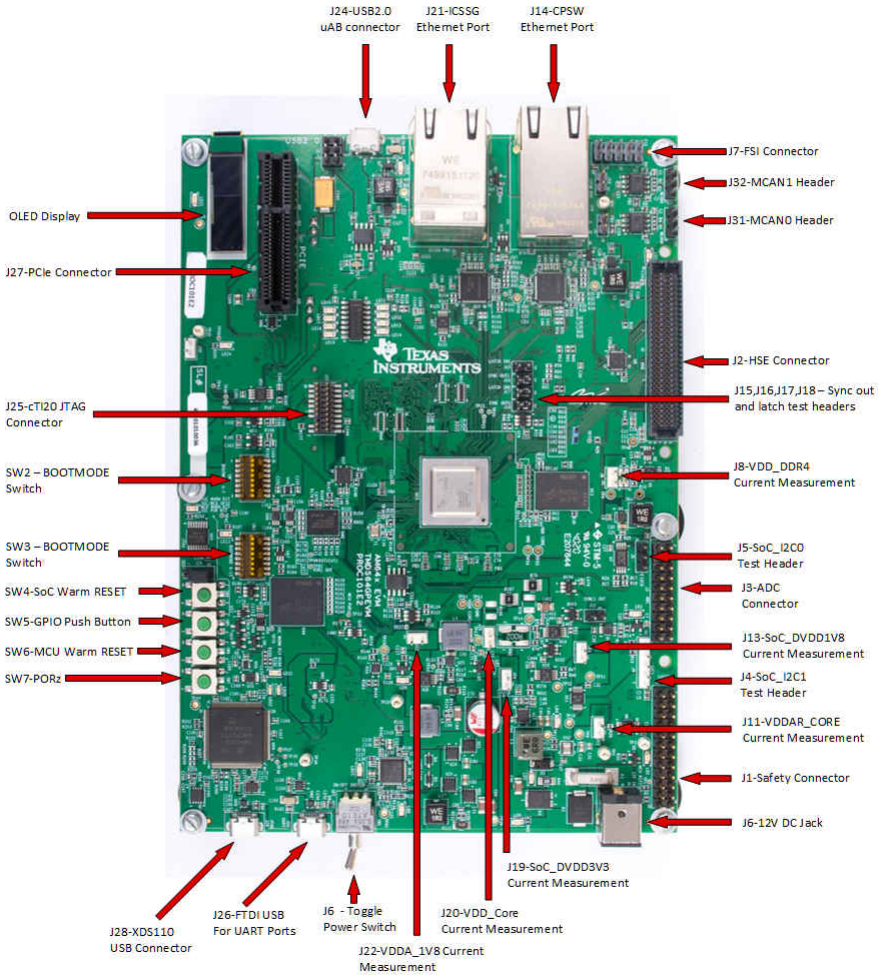


Figure 3-1. Top View of the AM64x/AM243x GP EVM Board

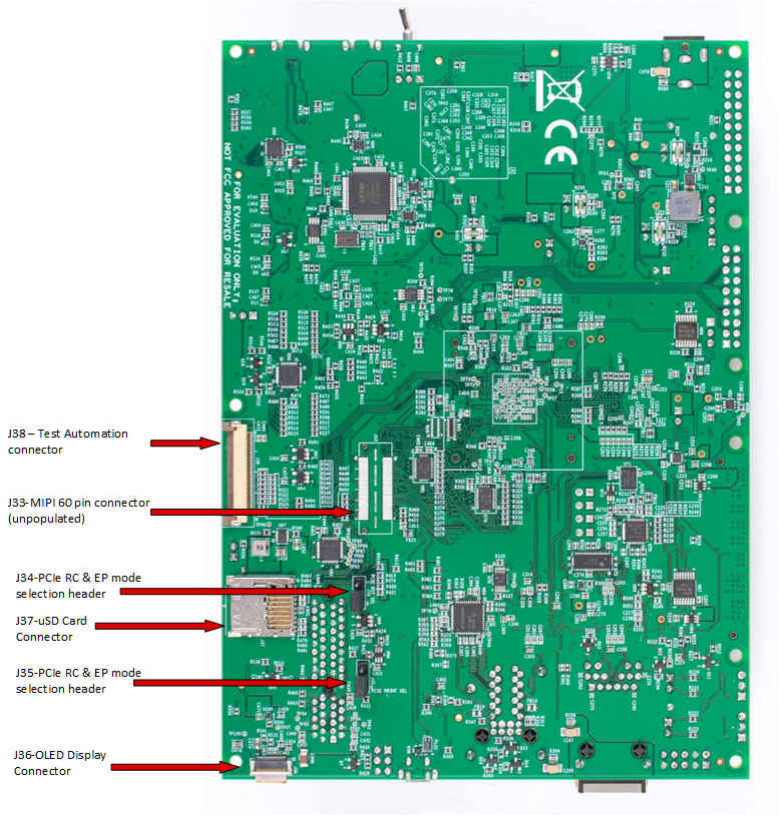


Figure 3-2. Bottom View of the AM64x/AM243x GP EVM Board

3.1 Key Features

AM64x System-on-Chip (SoC):

- AM64x combines two instances of Sitara's gigabit TSN-enabled PRU-ICSSG with up to two Arm® Cortex®-A53 cores, up to four Cortex-R5F MCUs, and a single Cortex-M4F MCU

AM243x Microcontroller (MCU):

- AM243x combines two instances of Sitara's gigabit TSN-enabled PRU-ICSSG with up to two Cortex-R5F MCU, and a single Cortex-M4F MCU

Memory

- 2GB DDR4 supporting data rate up to 1600MT/s
- 16GB eMMC Flash which can support HS400 speed of operation
- Micro Secure Digital (SD) Card with UHS-1 support
- 1 Kbit Serial Peripheral Interface (SPI) EEPROM
- 512 Mbit OSPI EEPROM
- 1 Mbit Inter-Integrated Circuit (I2C) Boot EEPROM

I/O Interface:

- One CPSW Gigabit Ethernet port and two Industrial Ethernet ports based on the Gigabit Industrial Communication Subsystem (PRU-ICSS-Gb) paired with Texas Instruments Gigabit Ethernet PHY
- One USB2.0 interface with Micro AB connector

Expansion Bus:

- 10051922-1410ELF - 14-Pin FPC connector to interface with the OSD9616P0992-10 display
- High Speed Expansion (HSE) connector to connect application cards
- 2x5 header - 67997-410HLF FSI connector to connect with the C2000 EVM
- x4 PCIe connector to support 1 lane PCIe Card

Debug:

- XDS110 On-Board Emulator
- Supports 20-pin JTAG connection from external emulator
- Automatic selection between on-board and external emulator (higher priority)
- Quad port Universal Asynchronous Receiver/Transmitter (UART) to USB circuit over microB USB connector
- Two I2C ports SoC_I2C0 and SoC_I2C1 connected to test headers for peripheral testing of the AM64x device
- 4x Push Buttons:
  - 1x SoC Warm RESET
  - 1x User GPIO
  - 1x MCU Warm RESET
  - 1x MCU/SoC PORz RESET

Power Supply:

Note

Please ensure that you are using the appropriately sized DC barrel jack for your particular EVM revision, as these have changed from the E2 to the A revision. An E2 Power Supply can be adapted to a Rev A GP EVM by using an adapter of part number DC PLUG-P1J-P1M

- DC Input: 12V
- Revision A and later:
  - The GP EVM Revision A implement a center positive 5.5mm x **2.5mm** x 9.5mm Barrel Jack.
  - Recommended mating connector - PJ-080BH.
  - Recommended Power Supply - GlobTek Inc. RR9LE5000LCPCIMR6B (IEC 320-C6 adapter cords sold separately).
- Revision E2:
  - The GP EVM Revision E2 implements a center positive 5.5mm x **2.1mm** x 9.5mm Barrel Jack.
  - Recommended mating connector - CUI In. PP3-002AH. (“tuning fork” style plug recommended to avoid the possibility of intermittent connections)
  - Recommended Power Supply - CUI In. SDI65-12-UD-P5 (adapter cords sold separately).
  - Example Adapter Cords:
    - CUI In. AC-C7 NA
    - Phihong USA AC15WNA
    - CUI In. AC-C7 UK
- Status Output: LEDs to indicate power status
- INA devices for current monitoring

Compliance:

- RoHS Compliant
- REACH Compliant

3.2 Functional Block Diagram

Figure 3-3 shows the functional block diagram of the AM64x/AM243x GP EVM.

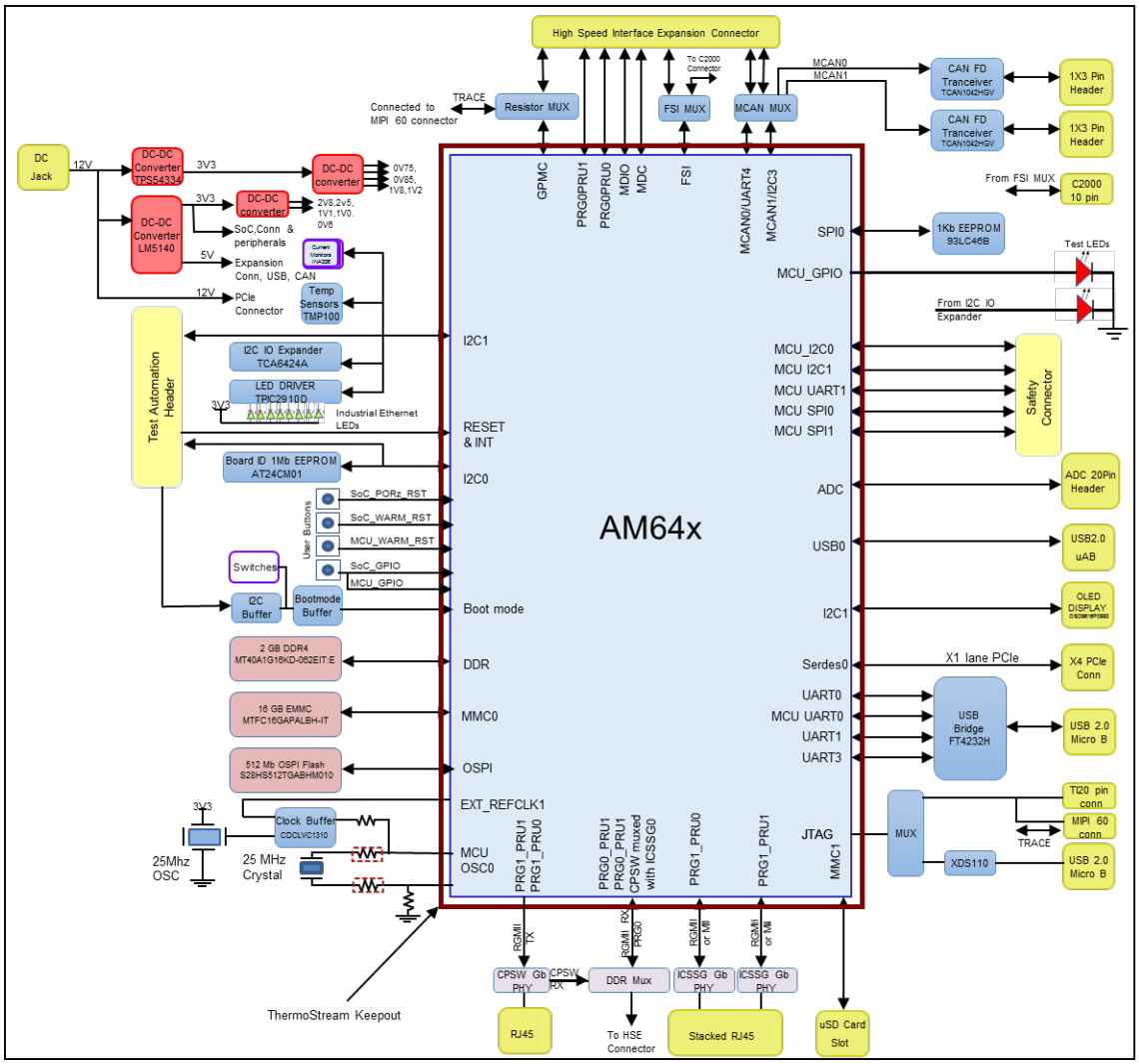


Figure 3-3. General Processor Board Functional Block Diagram

Note

Diagram is compatible with both the AM6442 MPU and the AM2434 MCU version of the system.

3.3 Power-On/Off Procedures

Power to the EVM is provided through an external AC/DC converter providing 12 Volt, 5A (max) DC voltage to the J6 power jack.

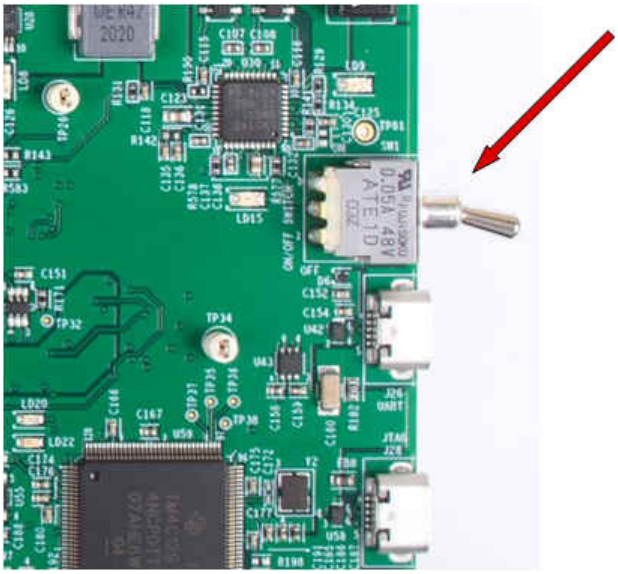
See the "Power Supply" list in Section 3.1 for TI's recommendation on an appropriate AC/DC power converter for your EVM revision.

CAUTION

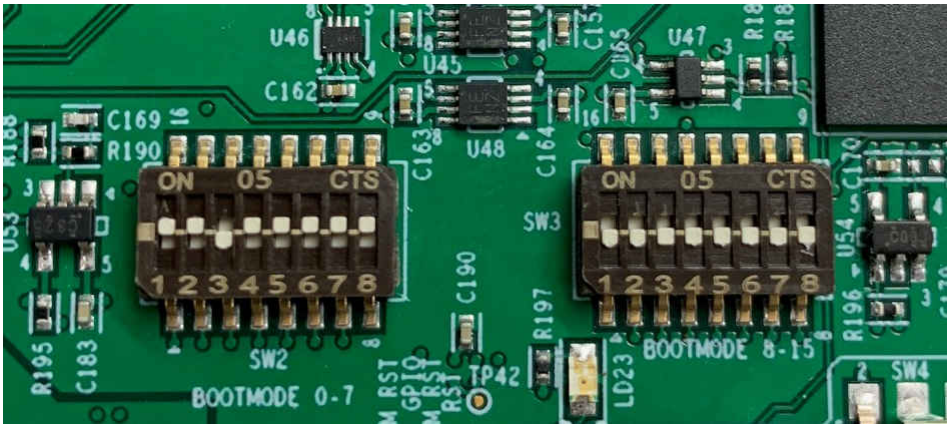
To avoid high inrush currents, and prevent possible damage to the AM64x/AM243x GP EVM components, the following EVM power on and power off procedures should be utilized.

3.3.1 Power-On Procedure

1. Place EVM power **(SW1)** switch in **OFF** position as shown in the figure below.



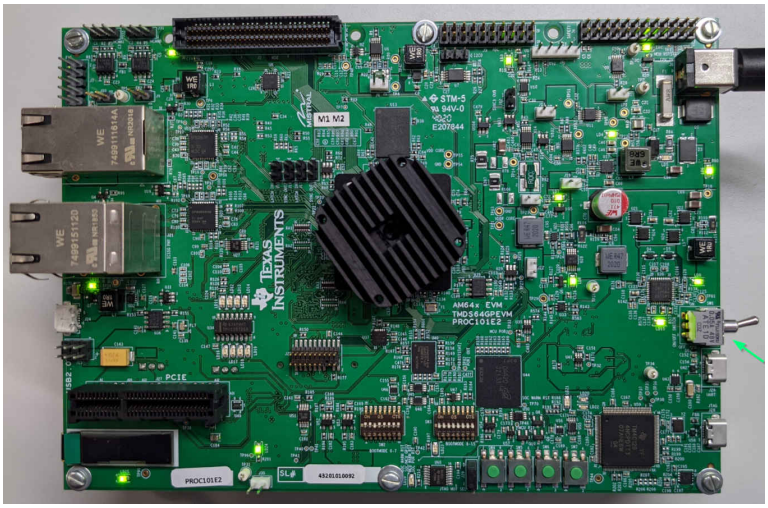
2. Place EVM boot switch selectors **(SW2, SW3)** into selected boot mode. For more details, see Section 3.4.4.1.



3. Attach 12 V AC/DC regulator plug to EVM power jack **(J6)**, **but do not power converter from AC power.**

4. Apply AC power to AC/DC converter. 12 V power LED **(LD6 and LD12)** should illuminate.

5. Place EVM power **(SW1)** switch in **ON** position as shown below.



6. Visually inspect LED against reference photo above. The following LED should be illuminated:
   - LD1, LD2, LD3, LD4, LD6, LD7, LD8, LD9, LD10, LD15, LD24, LD25

Note

If using an AM243x GP EVM, LD2 will not be illuminated.

3.3.2 Power-Off Procedure

1. Switch EVM power switch **(SW1)** to **OFF** position.
2. Disconnect AC power from AC/DC converter.
3. Remove DC power plug from EVM power jack **(J6)**.

3.4 Peripheral and Major Component Description

The following sections provide an overview of the different interfaces and circuits on the AM64x/AM243x GP EVM.

3.4.1 Clocking

3.4.1.1 Ethernet PHY Clock

A clock generator of part number **CDCLVC1310** is used to drive 25 MHz clock to the Ethernet PHYs. CDCLVC1310 is a 1:10 LVCMOS clock buffer, which takes 25 MHz crystal/LVCMOS reference input and provides ten 25 MHz LVCMOS clock outputs. The source for the clock buffer is either the CLKOUT0 pin from the SoC or a 25 MHz oscillator **(ASFLMB-25.000MHZ-LY-T)**, the selection is made using a set of resistors. This selection can be made through the select lines of the clock buffer.

1. **IN_SEL0, IN_SEL1 = [00]** for selecting CLKOUT0.
2. **IN_SEL0, IN_SEL1 = [01]** for selecting oscillator input. This is the default condition.

The resistor termination for single ended Crystal input is provided as per device-specific data sheet.

Table 3-1. Source Clock Selection for the Clock Buffer

IN_SEL1	IN_SEL0	Clock Chosen	Mount	Unmount
0	0	EXT_REFCLK from SoC	R40, R45	R248, R253
1	0	Oscillator input	R253, R40	R45, R248

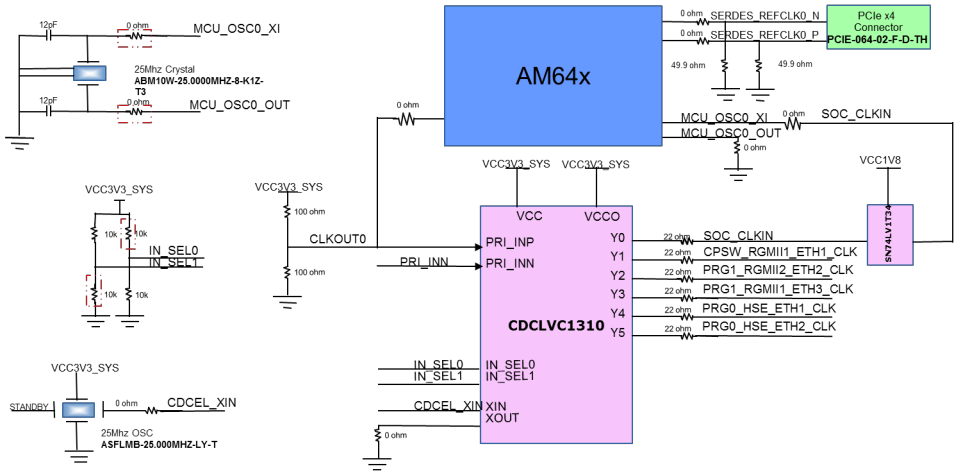


Figure 3-4. AM64x/AM243x GP EVM Clock Tree

Note

Resistors that are marked with red color box are DNI.

3.4.1.2 AM64x/AM243x Clock

Crystal of 25 MHz **(ABM10W-25.0000MHZ-8-K1Z-T3)** is provided on EVM as reference clock for the AM64x/ AM243x device. An optional output from the buffer driving the AM64x/AM243x is provided. Selection of clock for SoC is done using resistors. By default, an output from clock buffer SoC_CLKIN is provided to SoC.

3.4.1.3 PCIe Clock

The PCIe reference clock to the SoC will be provided by the PCIe slot connector when processor is configured as downstream port and PCIe reference clock from the SoC (SERDES0_REFCLK0) will be provided to the PCIe slot connector during root complex mode of operation.

3.4.2 Reset

The AM64x/AM243x device has the following reset signals:

- RESET_REQz is the warm reset input for MAIN domain.
- RESETSTATz is the warm reset status output for MAIN domain.
- PORz_OUT is the power ON reset status output from MAIN and MCU domain.
- MCU_PORz is the power ON/Cold Reset input for MCU and MAIN domain.
- MCU_RESETz is the Warm Reset input for MCU domain.
- MCU_RESETSTATz is the Warm Reset status output for MCU domain.

The two supervisor outputs and reset from JTAG are input to an AND gate to generate the PORz signal. This PORz, the CONN_MCU_PORz from safety connector, and PCIe_MCU_PORz from PCIe connector are input to another AND gate to generate the MCU_PORz signal.

Three push button switches are available to provide reset for MCU_PORz, MCU_RESETz and RESET_REQz.

Warm reset can also be applied through Test automation header or manual reset switches SW4(SoC) and SW6(MCU).

MCU_PORz input can be applied though switch SW7.

The CONN_MCU_RESETz and CONN_MCU_PORz from the safety connector are routed to MCU_RESETz and MCU_PORz respectively thereby providing option for safety connector to create a warm reset and a cold reset as shown in the Figure 3-5.

Most peripheral resets are “ANDED” with the RESETSTATz output from the SoC along with a GPIO control as shown in Figure 3-5. This ensures that the peripheral reset is asserted until the SoC is out of reset and allows the AM64x to manually assert reset to the peripheral.

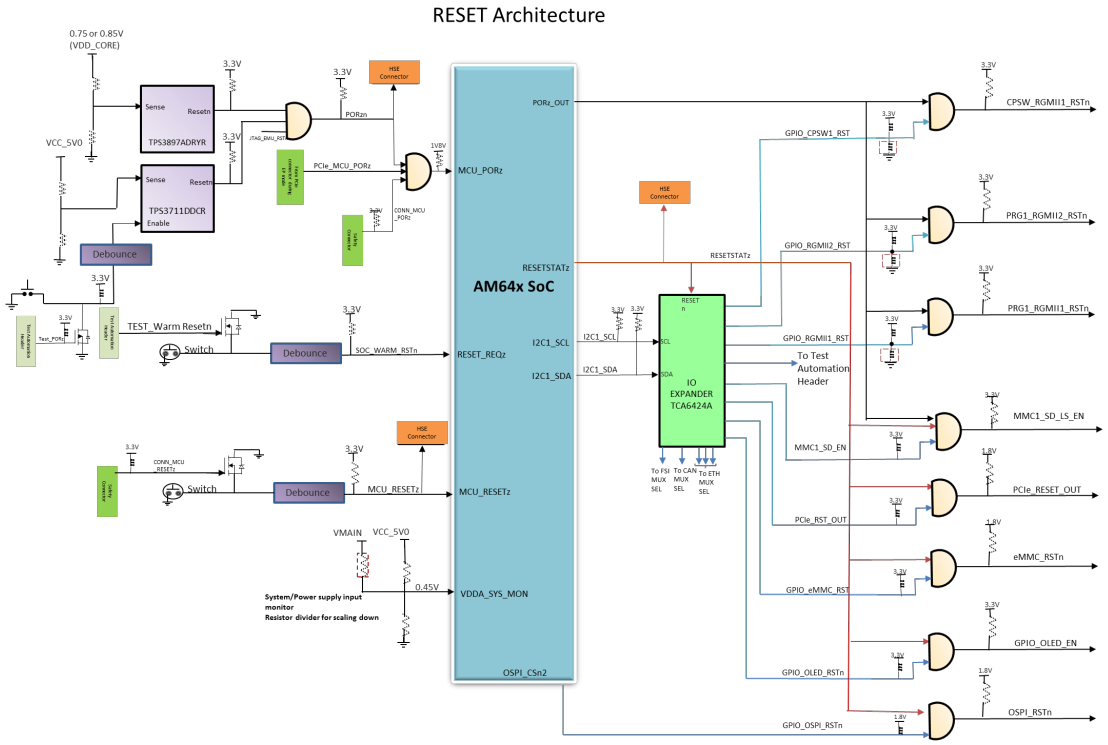


Figure 3-5. Overall Reset Architecture of the AM64x/AM243x GP EVM

3.4.3 Power

3.4.3.1 Power Input

The following sections describe the power distribution network topology that supplies the GP EVM board, supporting components and reference voltages.

The AM64x/AM243x GP EVM board includes a power solution based on discrete power supply components. The initial stage of the power supply will be 12 V from a barrel jack connector with part reference J6. J6 supports 8A current rating and necessary diodes for reverse polarity protection and voltage surge protection. The 12 V input (VMAIN) of the EVM that is used to generate all necessary voltages required by the EVM.

A ON/OFF switch with part reference SW1 is provided to turn ON/OFF the EVM by connecting this switch to Enable pin of LM5140, thereby, allowing the switch to turn on or off the board based on the switch position. The board is in off condition when switch is grounded position 1-2 and in on condition when the switch is in position 2-3. Additionally GPIO from the test automation header is also connected to the switch to control ON/OFF of the EVM via the test automation board. A fault indication LED LD5 will be in ON status in case of reverse polarity. LD6 will be in ON status to indicate VMAIN power good.

Note

The Switch SW1 does not turn of VMAIN. It only disables the VCC_5V0 output of LM5140 from which all other power supplies are derived.

3.4.3.2 Reverse Polarity Protection

A Schottky barrier rectifier with reference D3 is kept for reverse polarity protection, which has average forward current: IF(AV) ≤ 15 A, reverse voltage: VR ≤ 45 V. LD6 status will give power polarity.

Table 3-2. VMAIN LED

LED	ON Status	OFF Status
LD5	Power polarity reversed	Power polarity good
LD6	Board Power on	Board Power off

3.4.3.3 Current Monitoring

INA226 power monitor devices are used to monitor current and voltage of various power rails of AM64x/AM243x processor. The INA226 interfaces to the AM64x/AM243x through I2C interface. Four terminal, high precision shunt resistors are provided to measure load current.

Table 3-3. INA Devices I2C Slave Address

Power Source	Supply Net	Slave Address (IN HEX)	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	40	2mΩ ±1%
VDD_0V85	VDDAR_CORE	41	10mΩ ± 0.5%
VCC_3V3_SYS	SoC_DVDD3V3	4C	10mΩ ± 0.5%
VCC1V8	SoC_DVDD1V8	4B	10mΩ ± 0.5%
VDDA1V8	VDDA_1V8	4E	10mΩ ± 0.5%
VCC1V2_DDR	VDD_DDR4	46	10mΩ ± 0.5%

3.4.3.4 Power Supply

The GP EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SoC and other components on the card with the necessary voltage and the power required. Table 3-5 gives power-good LEDs provided on EVM board to give users positive confirmation of the status of output of each supply.

Test points for each power outputs are provided on the EVM Board and are mentioned in the below Table 3-4.

Table 3-4. Power Test Points

Sl.No	Power Supply	Test Point	Voltage
Top Side			
1	VMAIN	TP81	12 V
2	VCC_5V0	TP18	5 V
3	VCC3V3_PREREG	TP12	3.3 V
4	VCC_3V3_SYS	TP44	3.3 V
5	VDD_2V5	TP6	2.5 V
6	VDD_1V1	TP28	1.1 V
7	VDDA1V8	TP29	1.8 V
8	VDD_CORE	TP14	0.75 V (1)
9	VCC_CORE	TP23	0.75 V
10	VDD_0V85	TP8	0.85 V
11	VDDAR_CORE	TP10	0.85 V
12	VCC1V2_DDR	TP4	1.2 V
13	VDD_2V8	TP99	2.8 V
14	VCC3V3_TA	TP96	3.3 V
15	VDD_1V0	TP56	1 V
16	VPP_DDR_2V5	TP47	2.5 V
17	VDDR_VTT	TP48	0.6 V
18	VCC1V8	TP51	1.8 V
19	VPP_1V8	TP52	1.8 V

(1) AM243x EVM should be 0.85 V.

Table 3-5. Power LEDs

Sl.No	Power Supply	LED REF
Before SW1 TURN ON		
1	VMAIN	LD6
2	VCC3V3_TA	LD24
After SW1 TURN ON		
3	VCC_5V0	LD15
4	VCC3V3_PREREG	LD4
5	VCC_3V3_SYS	LD9
6	VDD_2V5	LD1
7	VDD_1V1	LD10
8	VDDA1V8	LD8
9	VDD_CORE	LD2
10	VCC_CORE	LD7
11	VDD_2V8	LD25
12	VCC1V2_DDR	LD3

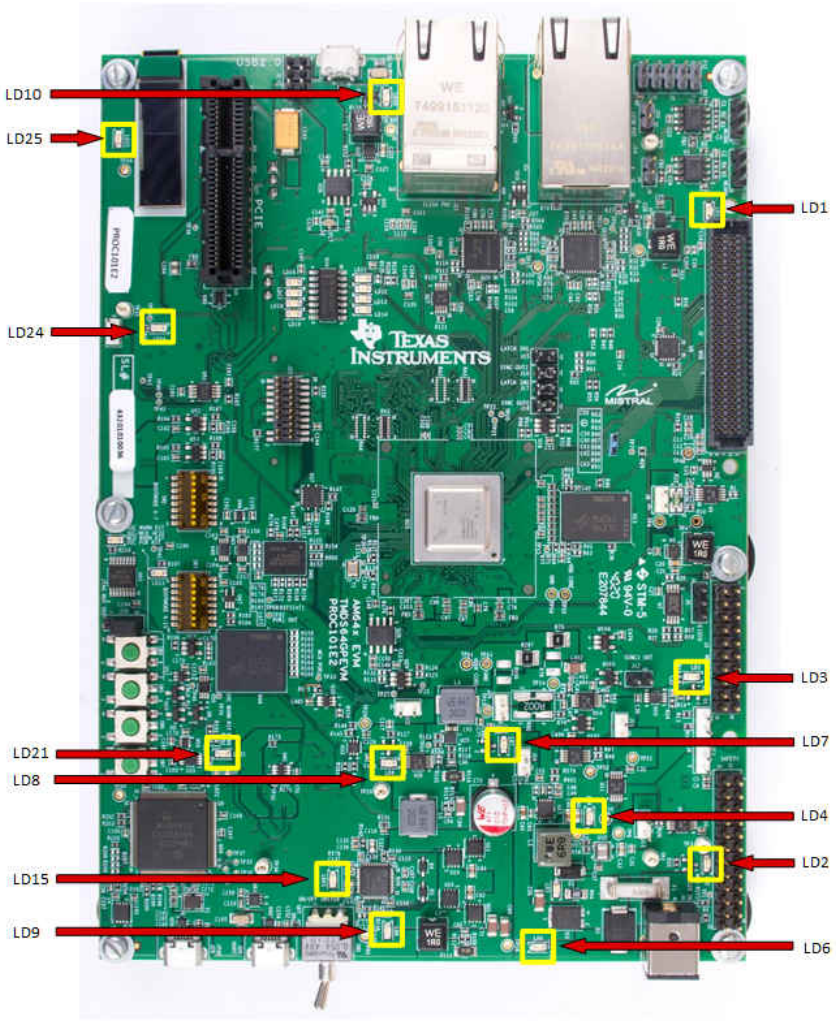


Figure 3-6. Power Good LEDs

3.4.3.5 Power Sequencing

Figure 3-7 shows the Power Up and Power Down sequence of all the Power supplies present on the EVM Board.

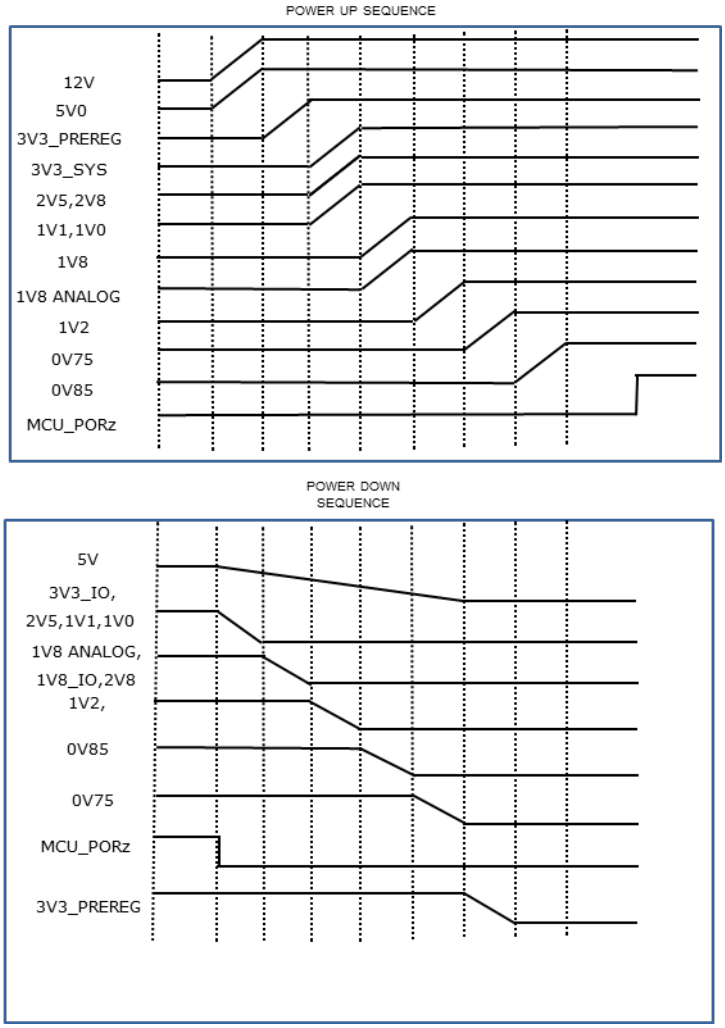
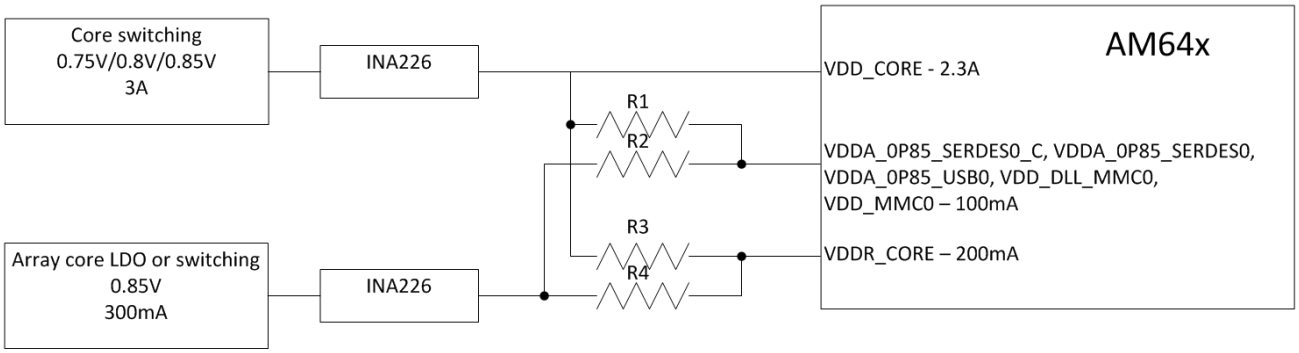


Figure 3-7. Power ON and OFF Sequencing

3.4.3.6 AM64x/AM243x Power

The Core voltage of the AM64x/AM243x can be powered by 0.75 V or 0.8 V or 0.85 V based on the power optimization requirement. It is recommended to use a single voltage source when the SoC Core voltage (VDD_CORE) and SoC Array Core Voltage (VDDR_CORE) and other array core voltages (VDDA_0P85_SERDES0_C, VDDA_0P85_SERDES0, VDDA_0P85_USB0, VDD_DLL_MMC0, VDD_MMC0) is 0.85 V. In cases where the SoC Core voltage is required to be 0.75 V or 0.8 V and SoC Array Core Voltage and other Array Core voltages is required to be 0.85 V then there needs to be separate voltage supply for the SoC Core voltage and an separate supply for the SoC Array Core voltages.

This EVM has a provision for providing single voltage supply or different voltage supply to the SoC Core and SoC Array Core and other Array Core Voltages and based requirement. This can be configured by the placement of resistors as mentioned in Figure 3-8.



Possible Configurations

Core supply	Array Core Supply	Steering resistors
0.75V VDD_CORE	0.85V VDDR_CORE & Others	R2 & R4 installed
0.8V VDD_CORE	0.85V VDDR_CORE & Others	R2 & R4 installed
0.8V VDD_CORE & Others	0.85V VDDR_CORE	R1 & R4 installed
0.85V VDD_CORE & VDDR_CORE & Others	none	R1 & R3 installed

Figure 3-8. AM64x/AM243x Core Supply and Array Core Supply Options

Note

- PROC101x-001 BOM variant, implements the AM6442 and requires 0.75 V supplied to the VDD_CORE and 0.85 V supplied to VDDR_CORE. In this variant R2 and R4 are installed by default and VDD_CORE supply (U25) is setup for 0.75 V operation.
- PROC101x-002 BOM variant, implements the AM2434 and requires 0.85 V supplied to VDD_CORE and VDDR_CORE. In this variant R1 and R3 are installed by default and VDD_CORE supply (U25) is setup for 0.85 V operation.

The SoC has different IO groups. Each IO group is powered by specific power supplies as shown in Table 3-6.

Table 3-6. SoC Power Supply

Sl.No.	Power Supply	SoC Supply Rails	IO Power Group	Power
1	VDDA_CORE	VDDA_0P85_SERDES0	SERDES0	0.85
		VDDA_0P85_SERDES0_C		0.85
		VDDA_0P85_USB0	USB0	0.85
		VDD_MMC0	MMC0	0.85
2	SoC_DVDD3V3	VDDS_MCU	MCU	3.3
		VDDA_3P3_USB0	USB0	3.3
		VDDSHV0	General	3.3
		VDDSHV1	PRG0	3.3
		VDDSHV2	PRG1	3.3
		VDDSHV3	GPMC	3.3
3	VDDA_1V8_MCU	VDDA_MCU	MCU	1.8
4	VDDA_MCU_ADC	VDDA_ADC	ADC0	1.8
5	VDDA_1V8_SERDES	VDDA_1P8_SERDES0	SERDES0	1.8
6	VDDA_1V8_USB0	VDDA_1P8_USB0	USB0	1.8
7	VDDA_1V8	VDDS_OSC	OSC0	1.8
		VDDA_TEMP_0/1		1.8
		VDDA_PLL_0/1/2		1.8
8	VDD_DDR4	VDDS_DDR	DDR0	1.2
		VDDS_DDR_C		1.2
9	SOC_DVDD1V8	VDDSHV4	FLASH	1.8
		VDDS_MMC0	MMC0	1.8
10	VDDSHV_SD_IO	VDDSHV5	MMC1	1.8

3.4.4 Configuration

3.4.4.1 Boot Modes

The boot mode for the EVM is defined by either a bank of switches **SW2** and **SW3** or by the I2C buffer (**U96**) connected to the test automation connector (**J38**). All the boot mode pins have a weak pull-down resistor and a switch capable of connecting to a strong pull up resistor. Switch set to “ON” corresponds to logic “HIGH” while “OFF” corresponds to logic “LOW”.

For a full description of all AM64x SoC supported bootmodes, see the *AM64x Sitara™ Processors Data Manual* and *AM64x Processors Silicon Revision 1.0 Texas Instruments Families of Products Technical Reference Manual*.

The following boot modes are supported by EVM (and subject to change):

1. OSPI
2. MMC1 - SD Card
3. MMC0 - eMMC installed
4. USB - boot using host mode with bulk storage. USB 2.0 mass storage using FAT16/32 (thumb drive)
5. USB - device boot DFU
6. UART
7. No-Boot

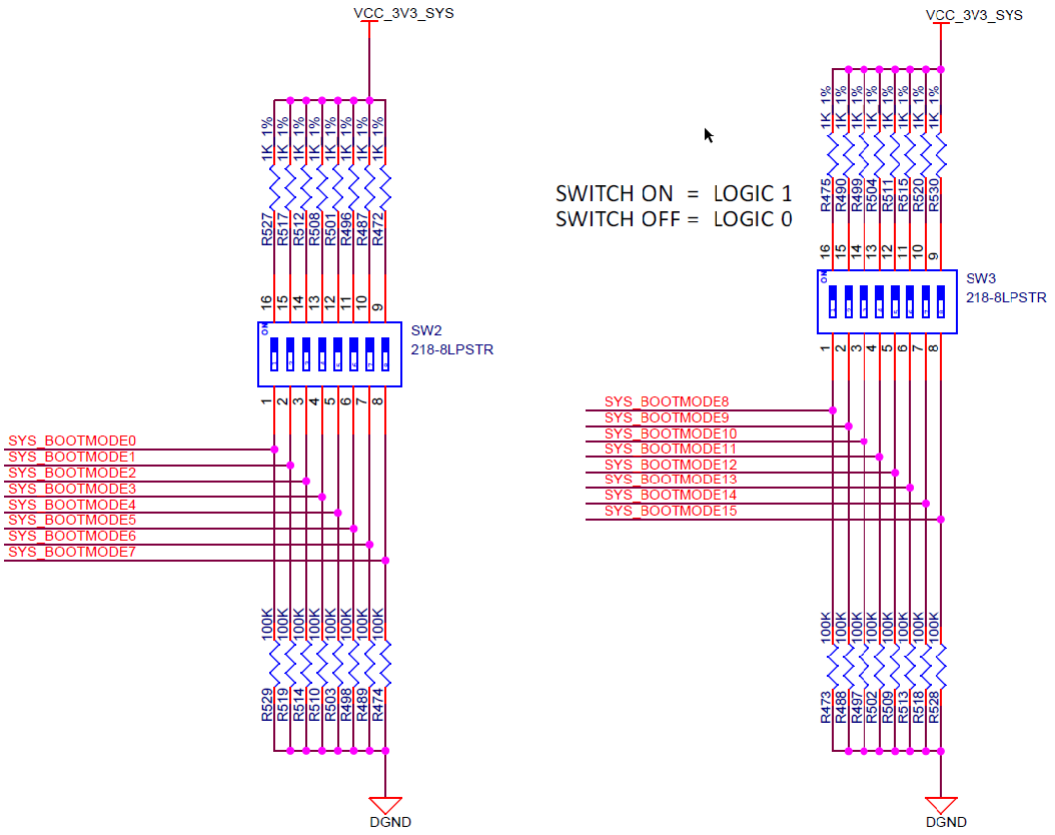


Figure 3-9. AM64x/AM243x GP EVM Schematic Excerpt, Boot Mode Selection Switches (SW2, SW3)

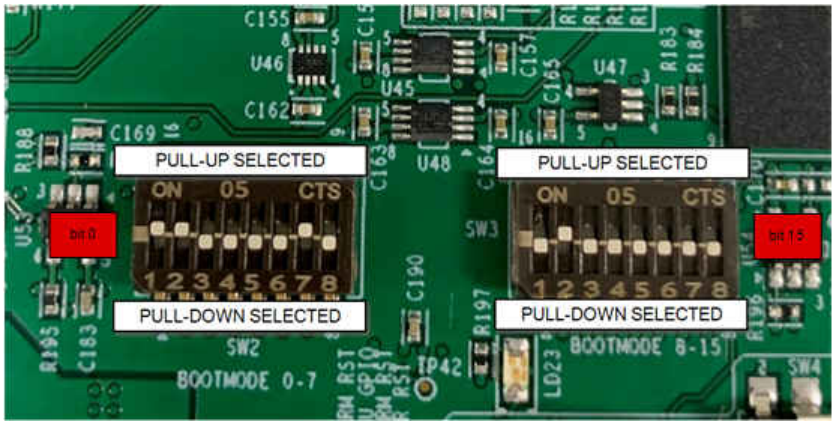


Figure 3-10. AM64x/AM243x GP EVP PCB, Boot Mode Selection Switches (SW2, SW3)

The BOOTMODE pins provide means to select the boot mode before the device is powered up. They are divided into the following categories:

Note

The following bit pattern is reversed in the table from the switch order.

Table 3-7. BOOTMODE Bits

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSVD	RSVD	Backup Boot Mode Config	Backup Boot Mode			Primary Boot Mode Config			Primary Boot Mode				PLL Config		

BOOTMODE[2:0] - Denote system clock frequency for PLL configuration. By default, these bits are set for 25 MHz.

Table 3-8. PLL Reference Clock Selection BOOTMODE[2:0]

SW2.3	SW2.2	SW2.1	PLL REF CLK (MHz)
off	off	off	19.2
off	off	on	20
off	on	off	24
off	on	on	25
on	off	off	26
on	off	on	27
on	on	off	RSVD
on	on	on	RSVD

BOOTMODE[6:3] - This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from.

Table 3-9. Boot Device Selection BOOTMODE[6:3]

SW2.7	SW2.6	SW2.5	SW2.4	Primary Boot Device Selected
off	off	off	off	RSVD
off	off	off	on	OSPI
off	off	on	off	QSPI
off	off	on	on	SPI
off	on	off	off	RSVD
off	on	off	on	RSVD
off	on	on	off	I2C
off	on	on	on	UART
on	off	off	off	MMC/SD Card
on	off	off	on	eMMC
on	off	on	off	USB
on	off	on	on	GPMC NAND
on	on	off	off	GPMC NOR
on	on	off	on	PCIe
on	on	on	off	xSPI
on	on	on	on	No-boot / Dev-boot

BOOTMODE[9:7] - These pins provide optional settings and are used in conjunction with the primary boot device selected. For more details, see the device-specific TRM.

Table 3-10. Primary Boot Media Configuration BOOTMODE[9:7]

SW3.2	SW3.1	SW2.8	Primary Boot Device
RSVD	RSVD	RSVD	RSVD
RSVD	Iclk	Csel	OSPI
RSVD	Iclk	Csel	QSPI
RSVD	Mode	Csel	SPI
RSVD	RSVD	RSVD	RSVD
RSVD	RSVD	RSVD	RSVD
Bus Reset	Don't Care	Addr	I2C
RSVD	RSVD	RSVD	UART
Port	RSVD	Fs/raw	MMC / SD Card
RSVD	RSVD	RSVD	eMMC
Core Volt	Mode	Lane Swap	USB
RSVD	RSVD	RSVD	GPMC NAND
RSVD	RSVD	RSVD	GPMC NOR
RSVD	RSVD	RSVD	PCIe
SFDP	Read Cmd	Mode	xSPI
RSVD	RSVD	RSVD	No-boot / Dev-boot

BOOTMODE[12:10] - Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.

Table 3-11. Backup Boot Mode Selection BOOTMODE[12:10]

SW3.2	SW3.1	SW2.8	Backup Boot Device Selected
off	off	off	None (No backup mode)
off	off	on	USB
off	on	off	RSVD
off	on	on	UART
on	off	off	RSVD
on	off	on	MMC/SD
on	on	off	SPI
on	on	on	I2C

BOOTMODE[13] - These pins provide optional settings and are used in conjunction with the backup boot device devices. For more details on bit details, see the device-specific TRM. When on, switches SW3.6 sets 1 and, when off, sets 0.

Table 3-12. Backup Boot Media Configuration BOOTMODE[13]

SW3.6	Boot Device
RSVD	None
Mode	USB
RSVD	RSVD
RSVD	UART
RSVD	RSVD
Port	MMC/SD
RSVD	SPI
RSVD	I2C

BOOTMODE[14:15] - Reserved

3.4.5 JTAG

The GP EVM includes XDS110 class embedded JTAG emulation through the micro B connector J28. It also has an optional TI20 pin (J25) connector to support external JTAG emulation. When an external emulator is connected, internal emulation circuitry will be disabled.

The design includes the footprint for a MIPI60 (J33) connector with connections for JTAG and trace capabilities. The trace pins are pinmuxed with GPMC signals which, by default, are connected to HSE connector on the processor board. Resistor networks are used to steer these signals to either the HSE connector or to the MIPI60 connector. The MIPI60 is not installed as delivered.

Resistor options are provided to connect these signals to the HSE or Trace connector as mentioned in the Table 3-13.

The pinout of TI20 pin connector and MIPI60 pin connector are given in Table 3-13 and Table 3-15, respectively.

Table 3-13. Selection of HSE Connector and JTAG TRACE Functionality

Signals Selected	Mount	Un Mount
HSE Connector (default)	RA1	RA2
	RA3	RA4
	RA5	RA6
	R390	R391
	R393	R392
JTAG Trace signals to J33	RA2	RA1
	RA4	RA3
	RA6	RA5
	R391	R390
	R392	R393

Table 3-14. TI20 Pin Connector (J25) Pin-Out

Pin No.	Signal	Pin No.	Signal
1	JTAG_CTI_TMS	11	JTAG_CTI_TCK
2	JTAG_TRSTN	12	DGND
3	JTAG_CTI_TDI	13	JTAG_EMU0
4	JTAG_TDIS	14	JTAG_EMU1
5	VCC_3V3_SYS	15	JTAG_EMU_RSTN
6	NC	16	DGND
7	JTAG_TDO	17	NC
8	SEL_XDS110_INV	18	NC
9	JTAG_CTI_RTCK	19	NC
10	DGND	20	DGND

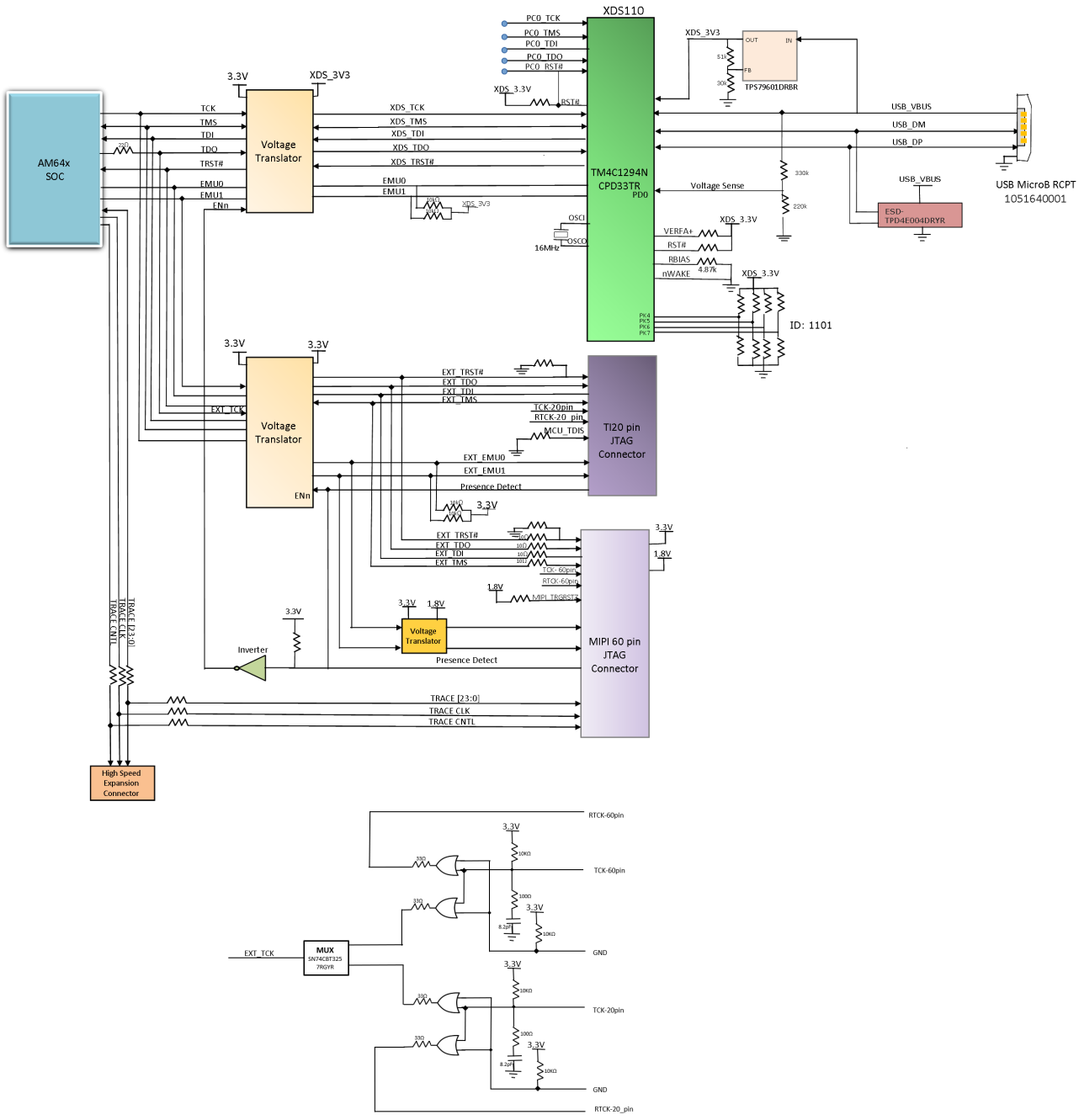


Figure 3-11. JTAG Interface

Table 3-15. TI 60-Pin Connector (J33) Pin-Out

Pin No.	Signal	Pin No.	Signal
1	VCC3V3_R	31	MIPI_TRC_DAT06
2	MIPI_TMS_R	32	NC
3	JTAG_MIPI_TCK	33	MIPI_TRC_DAT07
4	MIPI_TDO_R	34	NC
5	MIPI_TDI_R	35	MIPI_TRC_DAT08
6	MIPI_EMU_RSTn	36	NC
7	MIPI_RTCK	37	MIPI_TRC_DAT09
8	MIPI_TRST#_R	38	JTAG_MIPI_EMU0
9	NC	39	MIPI_TRC_DAT10
10	NC	40	JTAG_MIPI_EMU1
11	NC	41	MIPI_TRC_DAT11
12	VCC_3V3_MIPI	42	NC
13	MIPI_TRC_CLK	43	MIPI_TRC_DAT12
14	NC	44	NC
15	DGND	45	MIPI_TRC_DAT13
16	DGND	46	NC
17	MIPI_TRC_CTL	47	MIPI_TRC_DAT14
18	MIPI_TRC_DAT19	48	NC
19	MIPI_TRC_DAT00	49	MIPI_TRC_DAT15
20	MIPI_TRC_DAT20	50	NC
21	MIPI_TRC_DAT01	51	MIPI_TRC_DAT16
22	MIPI_TRC_DAT21	52	NC
23	MIPI_TRC_DAT02	53	MIPI_TRC_DAT17
24	MIPI_TRC_DAT22	54	NC
25	MIPI_TRC_DAT03	55	MIPI_TRC_DAT18
26	MIPI_TRC_DAT23	56	NC
27	MIPI_TRC_DAT04	57	DGND
28	NC	58	SEL_XDS100_INV
29	MIPI_TRC_DAT05	59	NC
30	NC	60	NC

3.4.6 Test Automation

A Test automation header J38 is provided to allow an external controller to control the power on/off, boot modes, reset functionality and current measurement to support automated testing. The test automation header includes four GPIOs, two I2C interfaces. The basic controls as shown in Table 3-16.

Table 3-16. List of Signals Routed to Test Automation Header

Signal	Signal Type	Function
POWER_DOWN	GPIO	Instructs the EVM to power down all circuits
POR	GPIO	Creates a PORz into the AM64x SoC
WARM_RESET	GPIO	Creates a RESETz into the AM64x SoC
GPIO1	GPIO	GPIO for communication with AM64x SoC
GPIO2	GPIO	Connected to I2C IO Expander
GPIO3	GPIO	Used to Enable the BOOTMODE Buffer
GPIO4	GPIO	Used to Reset the Boot mode IO Expander
I2C0	I2C	Commnicates with Boot mode I2C buffer
I2C2	I2C	Communicates with INA226 current measurement devices

One of the I2C interface from Test automation header is connected to an I2C IO expander, which can drive the Boot mode pins of the processor.

Note

The bootmode selection switches should be in the OFF condition and GPIO3 should be set to logic low to enable this mode.

The other I2C interface is connected to the current measurement and temperature sensing devices present on the I2C1 port of the SoC.

The Test Automation connector is used by Texas Instruments for control of software regression testing and comparative power measurements. The connector is provided to allow customers to develop their own testing and power measurements of customer applications.

Note

The power measurements are not a substitute for the AM64x/AM243x Power Estimation Tool and should not be used for the design of power supply solutions.

Power measurements will vary based on silicon process and environment and measurements should only be used for comparison with other measurements taken on the same EVM.

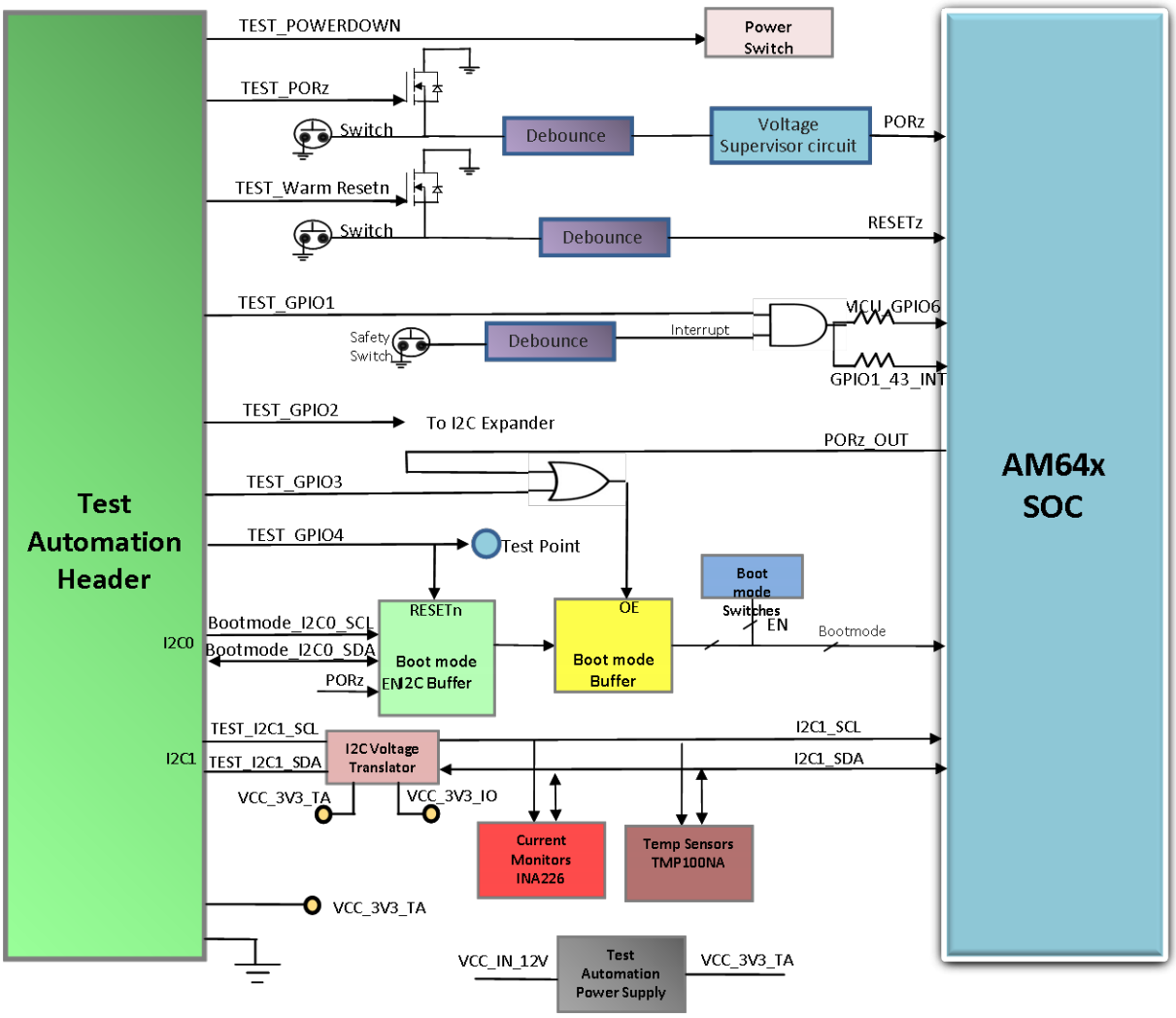


Figure 3-12. Test Automation Header

Table 3-17. Test Automation Header (J38) Pin-out

Pin No.	Signal	IO Direction (to CP board)
1	VCC3V3_1	Power (out)
2	VCC3V3_1	Power (out)
3	VCC3V3_1	Power (out)
4	NC	NA
5	NC	NA
6	NC	NA
7	DGND	Ground
8	NC	NA
9	NC	NA
10	NC	NA
11	NC	NA
12	NC	NA
13	NC	NA
14	NC	NA
15	NC	NA
16	DGND	Ground
17	NC	NA
18	NC	NA
19	NC	NA
20	NC	NA
21	NC	NA
22	NC	NA
23	NC	NA
24	NC	NA
25	DGND	Ground
26	TEST_POWERDOWN	Input
27	TEST_PORz	Input
28	TEST_WARMRESETn	Input
29	NC	NA
30	TEST_GPIO1	Bidirectional
31	TEST_GPIO2	Bidirectional
32	TEST_GPIO3	Input
33	TEST_GPIO4	Input
34	DGND	Ground
35	NC	NA
36	SOC_I2C1_SCL	Bidirectional
37	BOOTMODE_I2C_SCL	Bidirectional
38	SOC_I2C1_SDA	Bidirectional
39	BOOTMODE_I2C_SDA	Bidirectional
40	DGND	Ground
41	DGND	Ground
42	DGND	Ground

3.4.7 UART Interfaces

Four UART ports of the SoC are interfaced with FT4232H for UART-to-USB functionality and terminated on a micro B connector (J26). When the EVM is connected to a Host using the provided USB cable, the host can establish a Virtual Com Port which can be used with any terminal emulation application. The FT4232H is bus powered. Virtual Com Port drivers for the FT4232H can be obtained from https://www.ftdichip.com/Products/ICs/FT4232H.htm.

The FT_Prog has three modes of operation: Idle Mode, Program Mode and Edit Mode. FT_Prog programming parameters can be saved in files referred as EEPROM templates. Once defined, these EEPROM templates can be loaded by FT_Prog and used to program EEPROMs.

- Idle Mode is the initial mode of operation when the program is launched.
- Edit Mode is used to edit the settings of an EEPROM template
- Program Mode is used to Program and Erase the device EEPROM(s).

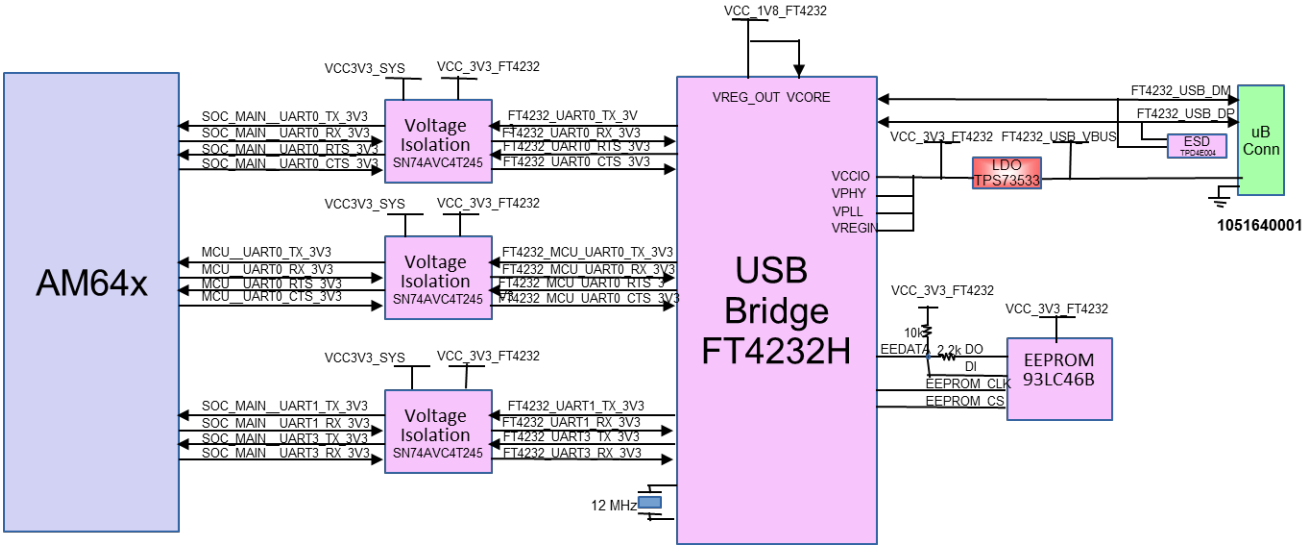


Figure 3-13. AM64x/AM243xUART Interfaces

3.4.8 Memory Interfaces

3.4.8.1 DDR4 Interface

The GP EVM has 2GB, 16bit wide DDR4 memory with operating speed of up to 1600MT/s. Micron's MT40A1G16KD-062E:E is used. This uses two x8 8Gb Micron dies to make one x16. The DDR memory is mounted on-board (single chip). The placement and routing of the DDR4 device will be point to point with VTT termination. The DDR4 requires 1.2V and thus reduces power demand.

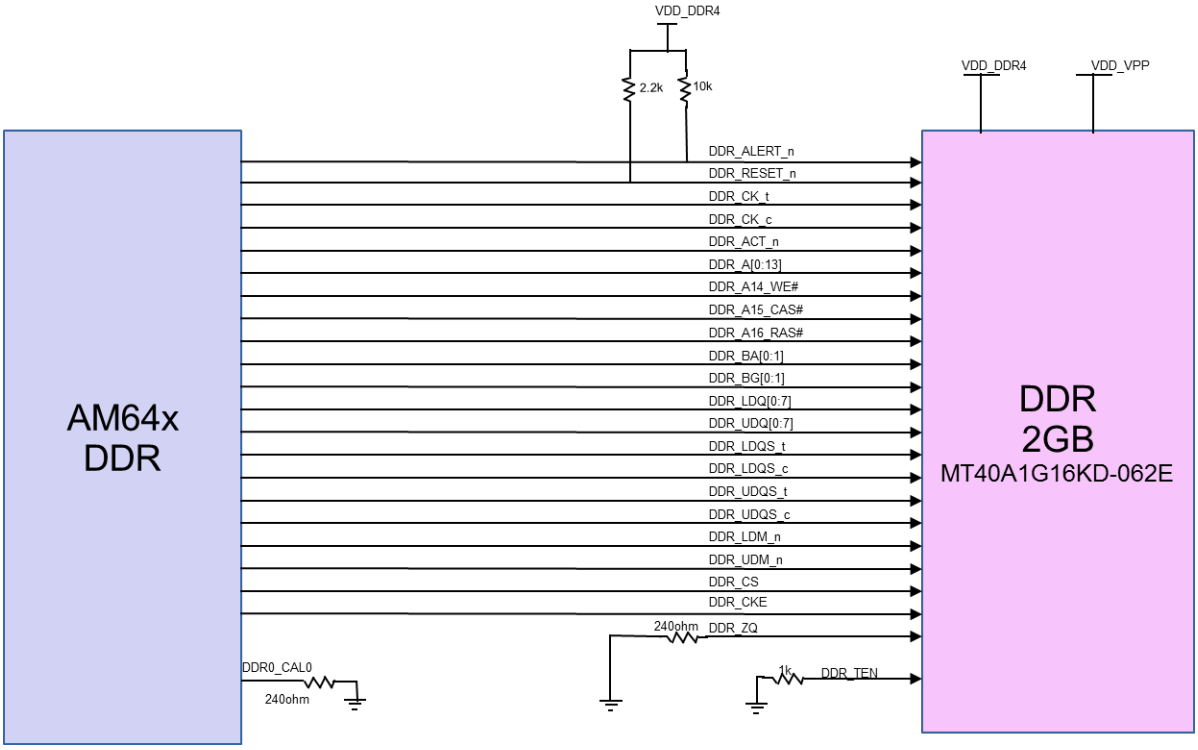


Figure 3-14. AM64x/AM243x DDR4 Interface

3.4.8.2 MMC Interfaces

The AM64x/AM243x processor provides two MMC interfaces. One MMC interface is connected to eMMC flash and the other is used for the micro SD card interface.

3.4.8.2.1 Micro SD Interface

The processor board provides an uSD card interface connected to MMC1 port of AM64x SoC. The uSD card interface supports UHS1 operation including operations at both 1.8V and 3.3V IO levels.. The AM64x SoC includes a circuit to generate the uSD voltage based on IO level negotiation with the uSD card. For high-speed cards, ROM code of the SoC attempts to find the fastest speed that the card and controller can support and can have a transition to 1.8V. The internal SDIO LDO output from the SoC is provided on the CAP_VDDSHV_SDLDO pin. CAP_VDDSHV_SDLDO is connected to both the IO voltage of SD signals and VDDSHV_MMC1 power pins of the SoC.

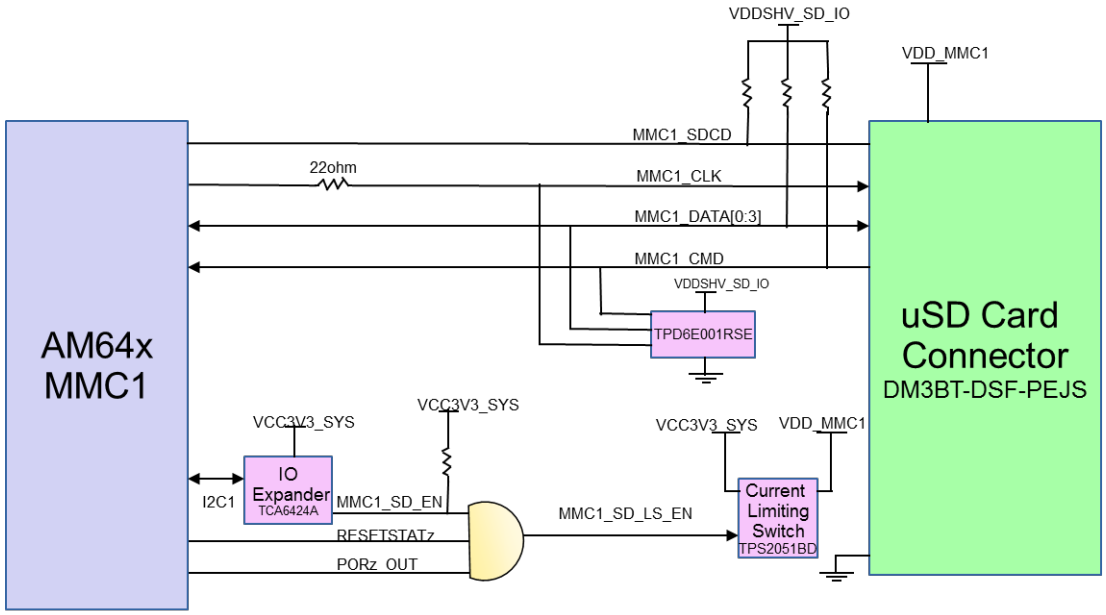


Figure 3-15. Micro SD Interface

3.4.8.2.2 eMMC Interface

The processor card supports eMMC Flash memory (part number Micron MTFC16GAPALBH-IT), connected to MMC0 port of the AM64x processor. The flash is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200 MHz.

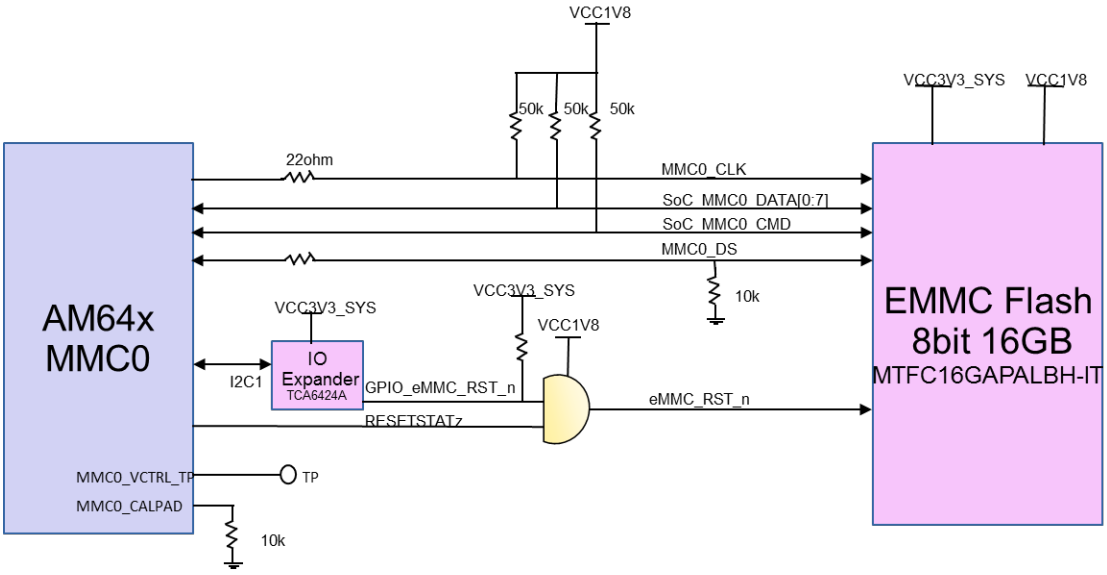


Figure 3-16. eMMC Interface

3.4.8.3 OSPI Interface

The GP EVM has 512 Mbit OSPI memory device of part number S28HS512TGABHM010 from Cypress is connected to OSPI0 interface of AM64x/AM243x SoC. The OSPI interface supports single and double data rates with memory speed up to 200 MBps SDR and 400 MBps DDR (200 MHz clock speed).

Two signals are routed to OSPI0_DQS:

1. OSPI0_DQS from the memory device
2. OSPI0_LBCLK from SoC

To route DQS from memory device: Mount R601 and R592 and DNI R600 and R591.

To route OSPI0_LBCLK from SoC: Mount R600 and R591 and DNI R601 and R592

Note

For more information, see the *OSPI and QSPI Board Design and Layout Guidelines* section in the *AM64x Sitara™ Processors Data Manual*.

OSPI and QSPI implementation: 0 Ω resistors are provided for DATA[7:0], DQS, INT# and CLK signals. Footprints to mount external pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. S25FL256SABHI200 from Cypress should be used in variants where QSPI flash is required. The 0 ohm resistors used in pins OSPI_DATA[4:7] will be removed if QSPI flash is mounted

Note

For QSPI Configuration

Remove 0E resistors from the following

1. OSPI_DQ4 to OSPI_DQ7 nets (R432, R441, R442, R443)
2. OSPI_INTn (R158)

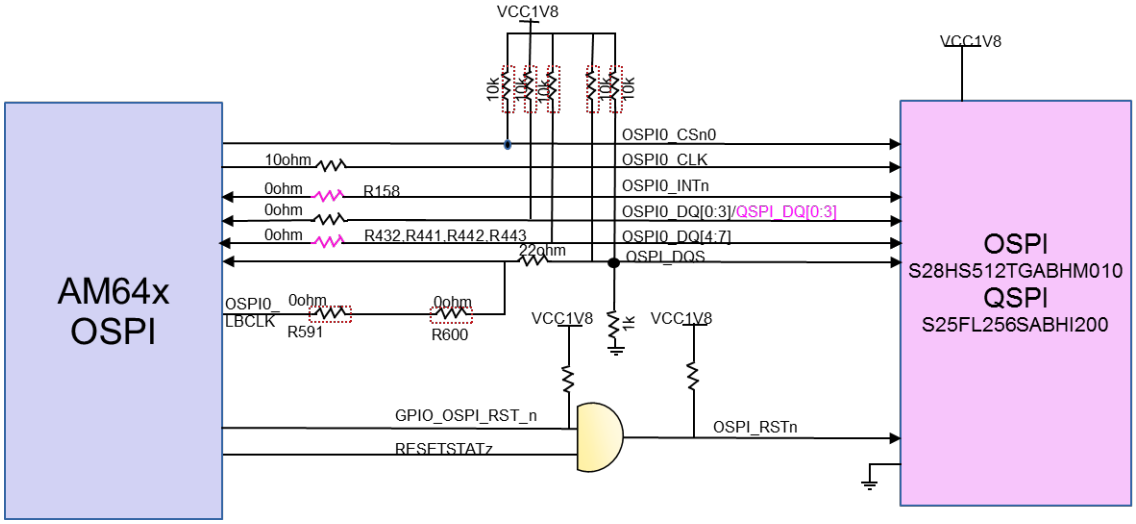


Figure 3-17. AM64x/AM243x OSPI Interface

3.4.8.4 SPI EEPROM Interface

A 1-Kbit SPI EEPROM (93LC46B) is interfaced to SPI0 port of AM64x/AM243x processor. It is used for testing purpose.

3.4.8.5 Board ID EEPROM Interface

The GP EVM includes an onboard EEPROM (U7). This EEPROM holds identifying information include the EVM version and serial number. PHY MAC ID and other static information about the EVM are also stored in this memory.

The Board ID memory shall be configured to respond to address 0x50 and 0X51 programmed with the header description and DDR information of this card. AT24CM01 from Microchip is used, this will be interfaced to I2C0 port of the SOCI2C address of the EEPROM can be modified by driving the A0, A1, A2 pins to LOW. The first 259 bytes of addressable EEPROM memory are preprogrammed with identification information for each board. The remaining 32509 bytes are available to the user for data or code storage.

Table 3-18. Board ID Memory Header Information

Header	Field Name	Size (bytes)	Comments
EE3355AA	MAGIC	4	Magic Number
	TYPE	1	Fixed length and variable position board ID header
		2	Size of payload
BRD_INFO	TYPE	1	Payload type
	Length	2	Offset to next header
	Board_Name	16	Name of the board
	Design_rev	2	Revision number of the design
	PROC_Nbr	4	PROC number
	Variant	2	Design variant number
	PCB_Rev	2	Revision number of the PCB
	SCHBOM_Rev	2	Revision number of the schematic
	SWR_Rev	2	First software release number
	VendorID	2	
	Build_Week	2	Week of the year of production
	Build_Year	2	Year of production
	BoardID	6	
	Serial_Nbr	4	Incrementing board number

Table 3-18. Board ID Memory Header Information (continued)

Header	Field Name	Size (bytes)	Comments
DDR_INFO	TYPE	1	
	Length	2	Offset to next header
	DDR control	2	DDR Control Word
MAC_ADDR	TYPE	1	Payload type
	Length	2	Size of payload
	MAC control	2	MAC header control word
	MAC_adrs	192	MAC address of AM64x/AM243x PRG2
END_LIST	TYPE	1	End Marker

3.4.9 Ethernet Interface

Three Ethernet PHYs terminated to RJ45 connectors with integrated magnetics is supported on the EVM.

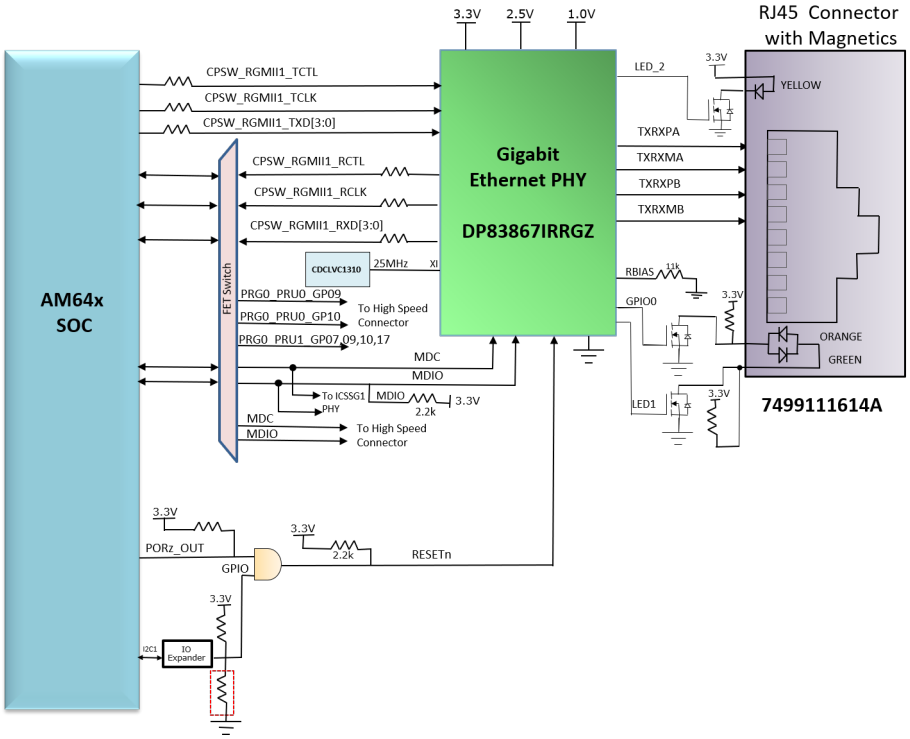


Figure 3-18. Ethernet Interface - CPSW Domain

The first PHY (connected to RJ45 connector J14) is interfaced to the CPSW_RGMII1 port of the SoC. The DP83867 PHY has been selected for this interface based on its ability to configure the Tx and Rx Delays. Since the CPSW_RGMII1_RX port is also multiplexed with PRG0 signals, a mux is needed to select the path from the SoC to this PHY (in CPSW mode) or to the HSE connector (PRG0 mode). The selection is done using a GPIO from the 24 bit IO expander.

The second PHY (connected to stacked RJ45 connector J21B) is interfaced to the PRG1_RGMII2 port of the SoC. This port is directly multiplexed with the CPSW_RGMII2 port. In order to select between CPSW and PRG operation, we need to multiplex the MDIO MDC signals from each controller to this PHY and the mux shall be controlled by a GPIO from IO expander. PRG1_RGMII2 is also internally multiplexed with PRG1_MII signals. The objective of the PHY used to connect this port is that the PHY should support both RGMII and MII modes, hence DP83869 (48 pin) PHY is selected.

The third PHY (connected to stacked RJ45 connector J21A) is interfaced to the PRG1_RGMII1 port of the SoC. ICSSG ports support internal multiplexing of GPI, GPO, RGMII, MII etc. The objective of this PHY used to connect to this port is that it should support both RGMII and MII modes (without the use of CRS and COL signals as they are multiplexed with the CPSW_RGMII1 used for the first PHY). Hence the same DP83869 (48pin) PHY is used for this port as well.

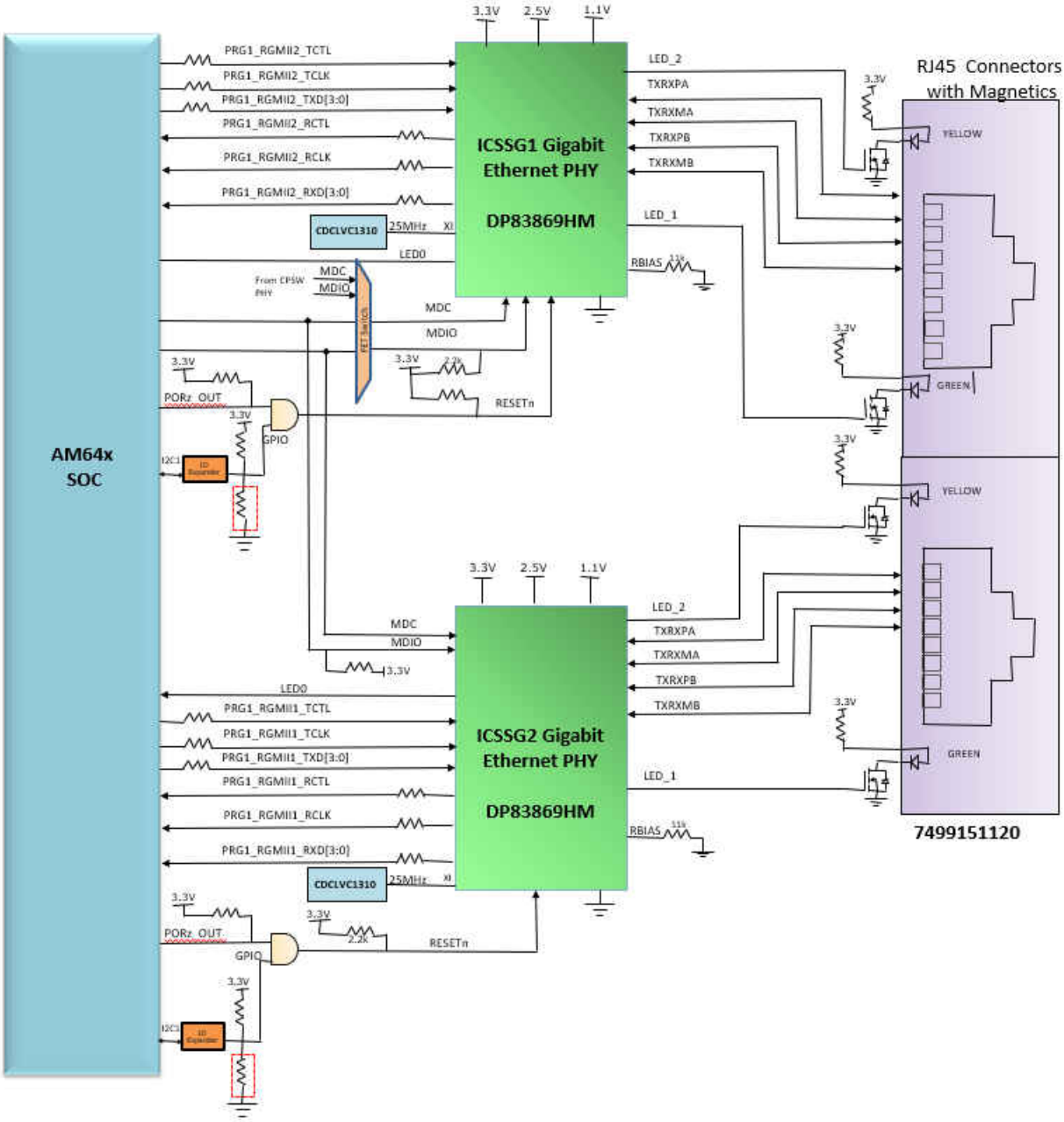


Figure 3-19. Ethernet Interface - ICSSG Domain

3.4.9.1 DP83867 PHY Default Configuration

The DP83867 PHY uses four level configurations based on resistor strapping, which generates four distinct voltages ranges. The resistors are connected to the RX data and control pins that are normally driven by the PHY and are inputs to the AM64x. The voltage range for each mode is shown below:

Mode 1 - 0 V to 0.3234 V

Mode 2 – 0.462 V to 0.6303 V

Mode 3 – 0.7425 V to 0.9372 V

Mode 4 – 2.2902 V to 2.904 V

DP83867 device includes internal pull-down resistor. The value of the external pull resistors is selected to provide voltage at the pins of the AM64x/AM243x as close to ground or 3.3V as possible. The strapping is shown in Figure 3-21 and strap values shown in Table 3-19.

Address strapping is provided for CPSW PHY to set address -00000 (0h) by default, as strapping pins has internal pull-down resistors. Footprint for both pull up and pull down is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to mode 1 by default, Mode 4 is not applicable and Mode2, Mode3 option is not desired.

3.4.9.2 DP83869 PHY Default Configuration

The DP83869 PHY uses four level configurations for I/O, RX_D0 and RX_D1 pins and two-level configurations for all other pins. The four level strap pins based on resistor strapping generates four distinct voltages ranges. The resistors are connected to the RX data pins, which are normally driven by the PHY and are inputs to the AM64x/AM243x. The voltage range for each mode is shown below:

Mode 0 - 0 V to 0.3069 V

Mode 1 – 0.4488 V to 0.6072 V

Mode 2 – 0.7227 V to 0.924 V

Mode 3 – 1.98 V to 2.9304 V

The two level strap pins based on resistor strapping generates two distinct voltage ranges. The resistors are connected to the LED pins. Because the LED output pins are also used as straps, the external components required for strapping and LED usage must be considered to avoid contention. Specifically, this may be an issue when the LED outputs are used to drive LED directly. The voltage range for each mode is shown below:

Mode 0 - 0 V to 0.594 V

Mode 1 – 1.65 V to 2.904 V

DP83869 device includes internal pull-down resistor. The value of the external pull resistors is selected to provide voltage at the pins of the AM64x/AM243x as close to ground or 3.3 V as possible. The strapping is shown in Figure 3-21 and the strap values are given in Table 3-20.

Address strapping is provided for ICSSG1 PHY to set address of 00011 (03h) and ICSSG2 PHY to set address of 01111 (0Fh) using the strap resistors. Footprint for both pull up and pull down is provided on all the strapping pins.

Table 3-19. Default Strap Setting of CPSW Ethernet PHY

Strap Setting	Pin Name	Strap Function	Mode for PRG0_PRU1, PRG0_PRU0, PRG1_PRU1, PRG1_PRU0	Value of Strap Function for PRG0 and PRG1	Description
PHY Address	RX_D2	PHY_AD3	1	0	PHY Address: 0000
		PHY_AD2	1	0	
	RX_D0	PHY_AD1	1	0	
		PHY_AD0	1	0	
Auto Negotiation	RX_DV/RX_CTRL	Auto-neg	3	0	Auto neg Disable=0
Modes of Operation	LED_2	RGMII Clock Skew TX[1]	1	0	RGMII TX Clock Skew is set to 2 ns
		RGMII Clock Skew TX[0]	1	0	
	LED_1	RGMII Clock Skew TX[2]	1	0	
		ANEG_SEL	1	0	advertise ability of 10/100/1000
	LED_0	Mirror Enable	1	0	Mirror Enable Disabled
	GPIO_1	RGMII Clock Skew RX[2]	1	0	RGMII RX Clock Skew is set to 2 ns
		RGMII clock Skew TX[1]	1	0	
	GPIO_0	RGMII clock Skew RX[0]	1	0	

Table 3-20. Default Strap Setting of ICSSG Ethernet PHYs

Strap Setting	Pin Name	Strap Function	Mode for PRG1_RGMII2 (ICSSG1)	Value of Strap Function for PRG1_RGMII2 (ICSSG1)	Mode for PRG1_RGMII1 (ICSSG2)	Value of Strap Function for PRG1_RGMII1 (ICSSG2)	Description
PHY Address	RX_D1	PHY_AD3	3	1	3	1	ICSSG1 PHY Address: 00011
		PHY_AD2	3	1	3	1	
	RX_D0	PHY_AD1	0	0	3	1	ICSSG2PHY Address: 01111
		PHY_AD0	0	0	3	1	
Modes of Operation	RX_CNTL	Mirror Enable	0	0	0	0	Mirror Enable Disabled
	LED_2	ANEGSEL_1	0	0	0	0	Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
	LED_1	ANEGSEL_0	0	0	0	0	
	LED_0	ANEG_DIS	0	0	0	0	
	JTAG_TDO/ GPIO_1	OPMODE_0	0	0	0	0	RGMII to Copper (1000BaseT/ 100Base-TX/ 10Base-Te)

The PHY devices include integrated MDI termination resistors, so external termination is not provided.

Interrupt: The interrupt from two ICSSG PHYs from PRG1 domain are tied together and is connected to EXTINTN pin of the AM64x/AM243x. An option for connecting the interrupt from CPSW PHY to the PRG1 ICSSG Interrupt pins is also provided.

Three configurable LED pins and a GPIO of Ethernet PHY are used to indicate link status. Several functions can be multiplexed onto the LEDs for different modes of operation. The LED operation mode can be selected using

the LEDCR1 register address 0x0018 on the DP83867 device and LEDS_CFG1 register address 0x0018 on the DP83869 device. The default configuration are as follows.

LED0: By default, this pin indicates that link is established. Additional functionality is configurable via LEDCR1[3:0] register bits in the DP83867 device and LEDS_CFG1[3:0] register bits in the DP83869 device. LDE0 is not used in the CPSW PHY (DP83867), this is also a strap pin which is used to set mirror enable. Since these features are not required the strapping for the LED0 is not provided. In the DP83869 ICSSG PHY the LED0 is connected to PRG1_PRU1_GPO8 and PRG1_PRU0_GPO8 of SoC for link status. This pin is also a strap pin which is having internal pulldown resistor to set Auto Negotiation Disable option in the DP83869 device. The default condition is to auto negotiate and advertise link as 10/100/1000Mbps

LED_1: By default, this pin indicates that 1000BASE-T link is established. This setting can be changed to Auto negotiate to 10/100Mbps using the strap resistors. Additional functionality is configurable via LEDCR1[7:4] register bits in the DP83867 device and LEDS_CFG1[7:4] register bits in the DP83869 device. LED_1 is a also an strap pin which is having internal pulldown resistor to set RGMII TX Clock Skew in the DP83867 device and to select Auto Negotiation mode in the DP83869 device. Since this pin will be set to active on both the devices this would result in dim LED lighting when LED is driven directly. So a MOSFET is used to drive LED as shown in Figure 3-23.

LED_2: By default, this pin indicates receive or transmit activity. Additional functionality is configurable via LEDCR1[11:18] register bits in the DP83867 device and LEDS_CFG1[11:18] register bits in the DP83869 device. LED_2 is also a strap pin, which is having internal pulldown resistor to set RGMII TX Clock Skew in the DP83867 device and to select Auto Negotiation mode in the DP83869 device. The default condition is to auto negotiate and advertise link as 10/100/1000Mbps, this can be changed using the strap resistors provided. The pull up resistor used for strap setting results in dim LED lighting when LED is driven directly. So a MOSFET is used to drive LED .

GPIO1: In the DP83867 PHY, the GPIO can be configured to function as LED3 through GPIO Mux Control Register 1 (GPIO_MUX_CTRL1) and the LED configuration can be set by programming LEDCR1 register this is also a strap pin which is used to set fast link drop (FDP), currently this is disabled. In the DP83869 PHY The GPIO can be configured to function as LED_GPIO(3) through GPIO Mux Control Register (GPIO_MUX_CTRL) and the LED configuration can be set by programming LEDS_CFG1 register, this is also a strap pin which is used to select RGMII to copper mode of operation on startup. This can be changed to MII mode using the MDC &MDIO pin to update the GEN_CFG1 register – 0x9 (gigabit Ethernet advertising should be disabled when using MII mode as the PHY would not link up at 1000Mbps speed)

RJ45 Connector LED Indication -CPSW (DP83867):

LED1 and GPIO1 is connected to dual LEDs of RJ45 to indicate 10/100 or 1000 MHz link. Orange LED indicates 10/100 speed and Green LED is to indicate 1000 MHz speed

LED2 is connected to RJ45 LED (Yellow) to indicate transmit/receive activity.

RJ45 Connector LED Indication -ICSSG (DP83869):

LED1 is connected to RJ45 LED (Green) to indicate 1000 MHz speed

LED2 is connected to RJ45 LED (Yellow) to indicate transmit/receive activity.

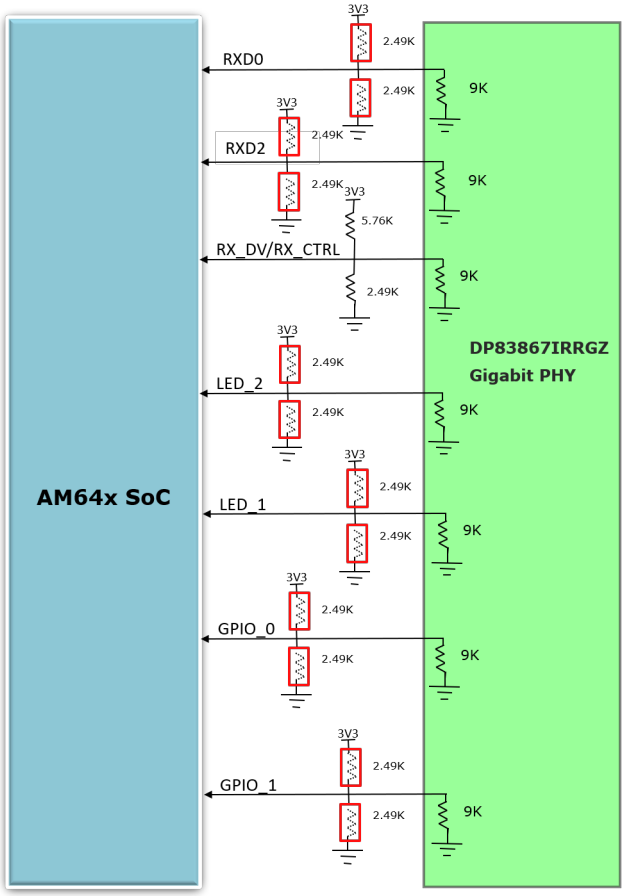


Figure 3-20. AM64x/AM243xEthernet Interfaces - CPSW Ethernet Strap Settings

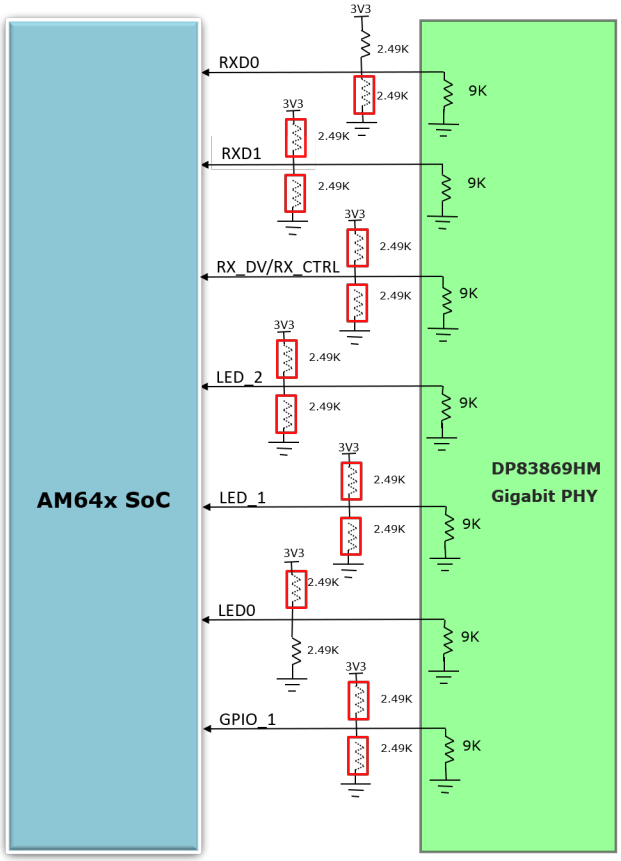


Figure 3-21. AM64x/AM243x Ethernet Interfaces - ICSSG1 Ethernet Strap Settings

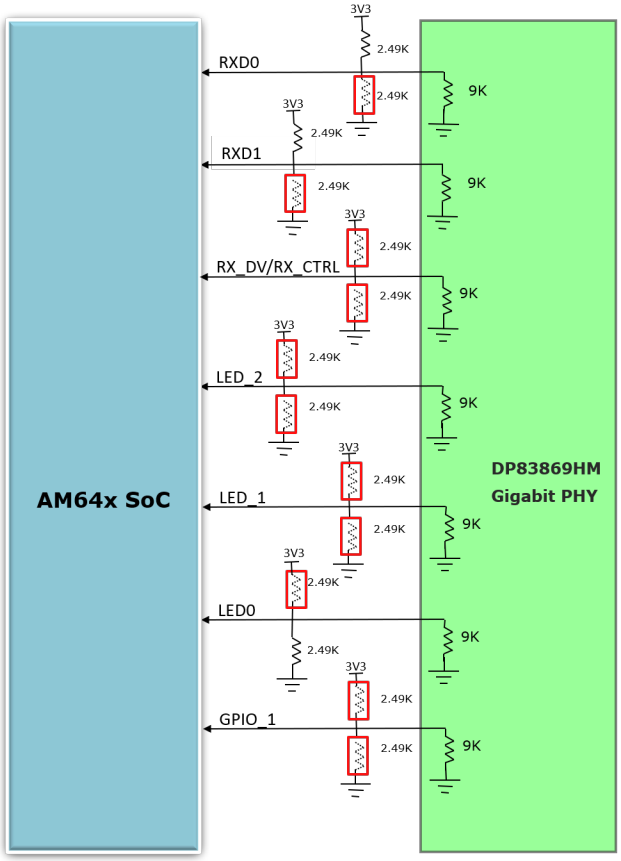


Figure 3-22. AM64x/AM243x Ethernet Interfaces - ICSSG2 Ethernet Strap Settings

Note

Resistors that are highlighted by red color box are DNI components.

3.4.9.3 Ethernet LED

The EVM card has multiple LED to indicate status of Ethernet link, Ethernet Activity and Ethernet Speed Set. Figure 3-23 shows the LED used for ICSSG PRG1 Ethernet activity and CPSW Ethernet activity. Additionally, there are eight LED's that are connected to an IO Expander, which is controlled by the SoC via the I2C1 port. These eight LED can be toggled based on the user application.

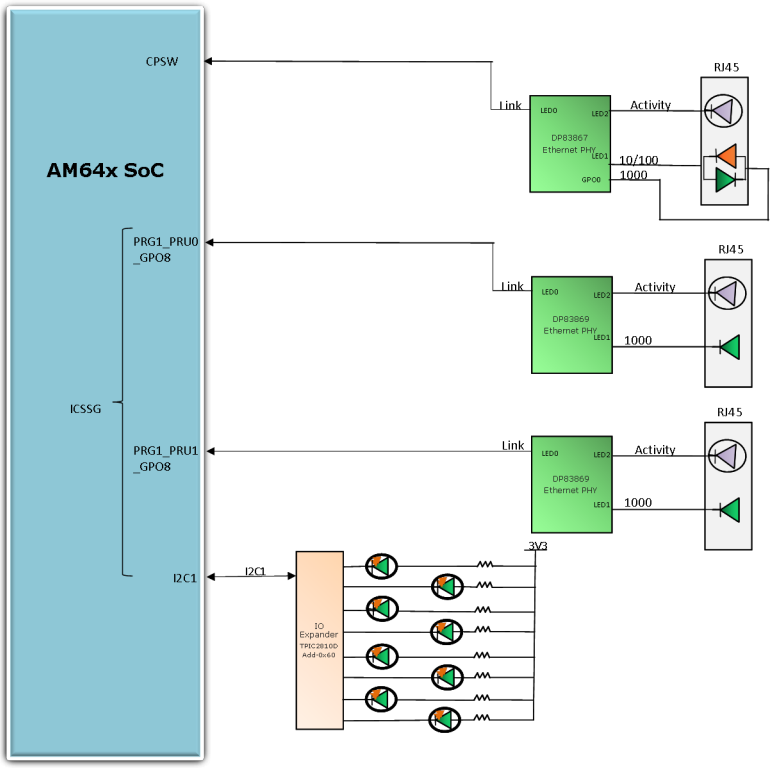


Figure 3-23. AM64x/AM243x GP EVM Ethernet Interface LED

3.4.10 Display Interface

The display device used on the EVM is an OSD9616P0992-10 from OSD Displays. This is a passive matrix PMOLED display with monochrome (light blue) backlight. The display has a pixel array of 96X16 and a panel size of 29.10 X 9.20 X 1.30 (mm) and an active area of 21.1 X 3.5 (mm). The display is connected to the 14-Pin FPC connector on the EVM having part number 10051922-1410ELF from Amphenol ICC and the pin details are mentioned in Table 3-21.

Table 3-21. Display Connector (J36) Pin-Out

Pin No.	Signal
1	C2P
2	C2N
3	C1P
4	C1N
5	VDDB
6	NC
7	VSS
8	VDD
9	RES#
10	SCL
11	SDA
12	IREF
13	VCOMH
14	VCC

3.4.11 USB 2.0 Interface

The USB0 port of AM64x/AM243x is used for USB 2.0 interface. The USB signals are terminated to a uAB connector and supporting circuitry is included to allow the USB interface to be configured as either host or a self-powered slave device.

In the host mode, up to 500 mA, 5 V is supported for the slave device. A power switch is included that is controlled by DRV_VBUS signal from the AM64x/AM243x.

A 2x3 header (J23) is provided to install the 2-position ganged shunt to configure the port for host mode as shown in Figure 3-24. Place the shunt on pin no. 1 and 2 to enable bulk capacitance on VBUS and place the shunt on pin 5 and 6 to connect ID pin to ground.

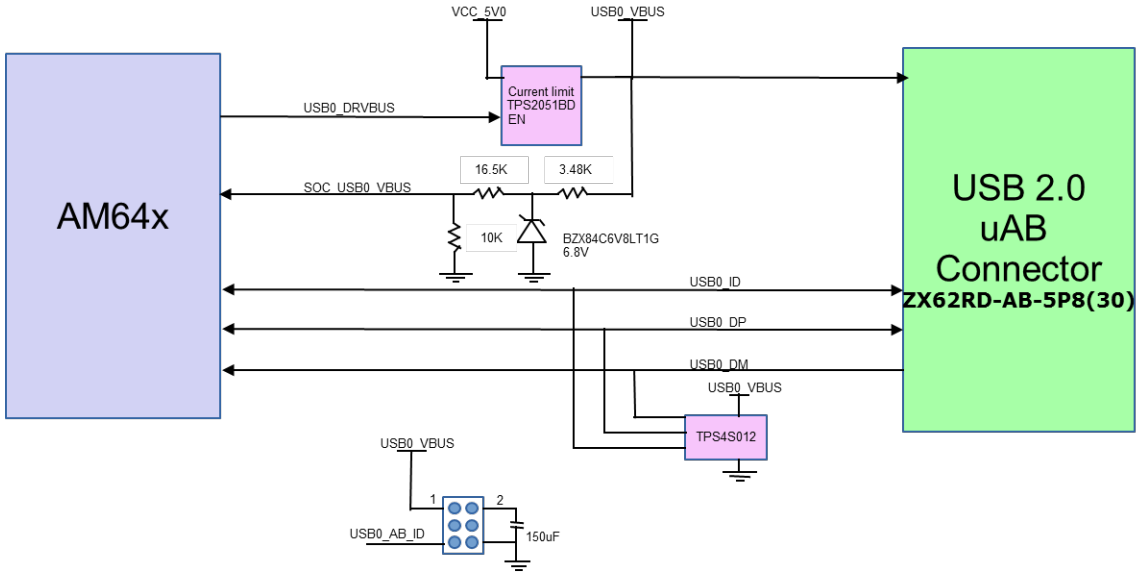


Figure 3-24. AM64x/AM243x USB 2.0 Host Interface

3.4.12 PCIe Interface

The Serdes0 interface of AM64x/AM243x is used to implement a x1 lane PCIe interface with the signals routed to a x4 PCIe slot connector. **PCIE-064-02-F-D-TH** connector from Samtec is be used for the PCIe interface and this connector meets the PCIe CEM v2.0 specification both physically and electrically and it is designed to support a 25W slot including 2.1A for the 12 V rail and 3A for the 3.3 V rail. The PCIe interface is designed to support either root complex operation or endpoint operation with a cross over cable. SoC_I2C1 is used for control purpose. The link activation signal from PCIe connectors is pulled up to VCC3V3_SYS.

Clock: SERDES REFCLK is routed to the PCIe REF CLK pins to allow either receiving or providing a clock from the connector (no separate PLL to generate PCIe REF CLK available on the EVM).

Hot plug: The PRSNT1# and PRSNT2# signals are the hot plug presence detect signals. The PRSNT2# is pulled up and PRSNT1# is connected to ground so that PRSNT2# will be pulled low when a daughter card is plugged in. A 3 pin header (J35) is provided to choose between RC and EP mode.

Reset: A 3 pin header (J34) is provided to select the reset source for host and endpoint PCIe operation. In case of host mode, PCIe_RST_OUT signal from IO Expander and RESETSTATz signal from SoC are ANDed and the output is connected to PCIe connector through 3 pin header. A jumper is mounted for the connectivity. Whereas in case of PCIe end point operation, the AM64x SoC receives reset signal from the add-on card and passed on to the MCU_PORz pin. The reset signal is connected to 3 pin header and the selection should be made with a jumper.

The PCIe x4 Connector JTAG signals are unused and test points are provided on the signals.

Table 3-22 describes the jumper options used to select if the GP EVM will operate in Root Complex mode or in End Point mode.

Table 3-22. PCIe Jumper Options to Enable Root Complex and Endpoint Mode

	Root Complex	End Point
1x3 header J34 and J35	Short 1 and 2	Short 2 and 3

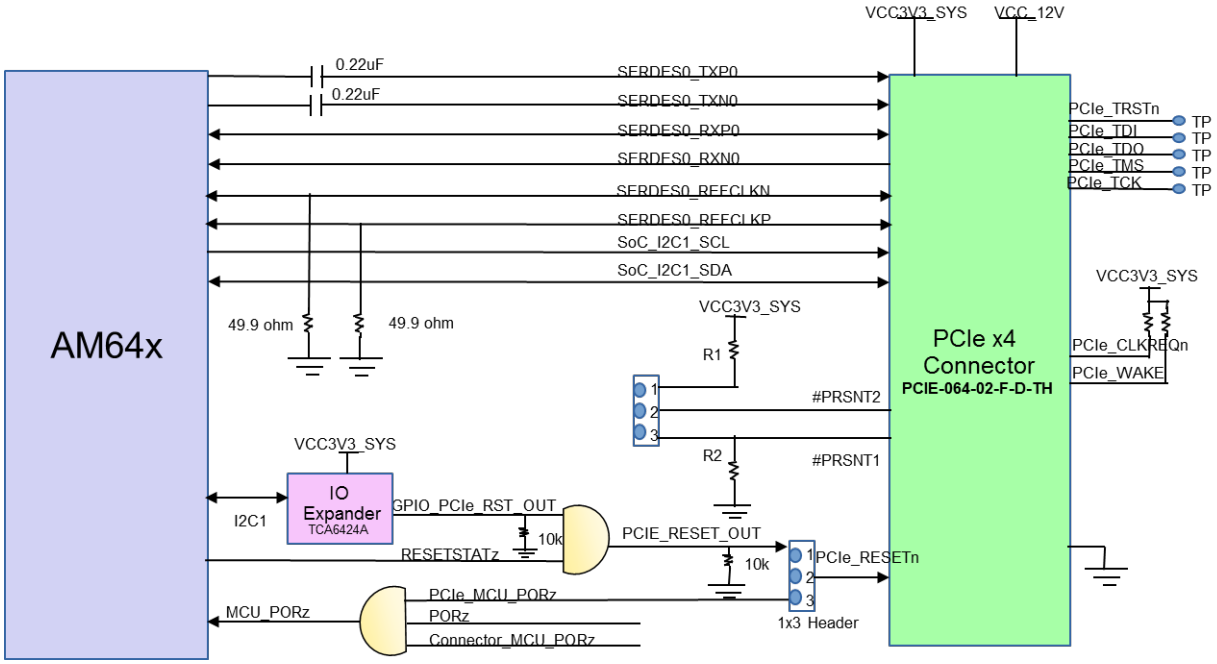


Figure 3-25. AM64x/AM243x PCIe Interface

Table 3-23. PCIe Connector (J27) Pin-out

Pin No.	Side A of PCIe Connector	GP Board Signal	Side B of PCIe Connector	GP Board Signal
1	PRSNT1#	J35.3	+12V	VDD_12V
2	+12V	VDD_12V	+12V	VDD_12V
3	+12V	VDD_12V	+12V	VDD_12V
4	GND	GROUND	GND	GROUND
5	JTAG2	TP	SMCLK	SoC_I2C1_CLK
6	JTAG3	TP	SMDATA	SoC_I2C1_SDA
7	JTAG4	TP	GND	GROUND
8	JTAG5	TP	+3V3	VCC3V3_SYS
9	+3V3	VCC3V3_SYS	JTAG1	TP
10	+3V3	VCC3V3_SYS	3V3 VAUX	VCC3V3_SYS
11	PERST#	J24.2	WAKE#	Pulled up to VCC3V3_SYS
12	GND	GROUND	RSVD4	Pulled up to VCC3V3_SYS
13	REFCLK+	SERDES_REFCLK0P	GND	GROUND
14	REFCLK-	SERDER_REFCLK0N	PETp0	SERDES_TXP0
15	GND	GROUND	PETn0	SERDES_TXN0
16	PERp0	SERDES_RXP0	GND	GND
17	PERn0	SERDES_RXN0	PRSNT2#_1	J35.2
18	GND	GROUND	GND	GROUND
19	RSVD1	NC	PETp1	NC

Table 3-23. PCIe Connector (J27) Pin-out (continued)

Pin No.	Side A of PCIe Connector	GP Board Signal	Side B of PCIe Connector	GP Board Signal
20	GND	GROUND	PETn1	NC
21	PERp1	NC	GND	GROUND
22	PERn1	NC	GND	GROUND
23	GND	GROUND	PETp2	NC
24	GND	GROUND	PETn2	NC
25	PERp2	NC	GND	GROUND
26	PERn2	NC	GND	GROUND
27	GND	GROUND	PETp3	NC
28	GND	GROUND	PETn3	NC
29	PERp3	NC	GND	GROUND
30	PERn3	NC	RSVD3	NC
31	GND	GROUND	PRSNT2#_2	NC
32	RSVD2	NC	GND	GROUND

3.4.13 High Speed Expansion Interface

The GP board has a high-speed expansion connector allowing connections to the ICSSG and GPMC capabilities of the AM64x/AM243x. A single high speed connector with part number **SEAF-30-06.0-L-05-2-A-K-TR** is used on the EVM. All the signals associated with the ICSSG0 interface is routed to the expansion connector. In addition, the data and command signals for the GPMC are routed to the AM64x/AM243x as well.

The trace signal is routed to either the high-speed expansion connector or the MIPI60 connector. Zero-Ohm resistor are used to minimize the disruption to the routing. The default configuration will have the resistors installed thereby routing the signals to the HSE connector. The MIPI60 is not installed by default.

One FSI transmit channel and one FSI receive channel is required to connect with the C2000 EVM. These signals from SoC are terminated on 2x5 header with part number **67997-410HLF** from Amphenol ICC (FCI). These signals are muxed so that they are available to both the FSI connector and the expansion connector. FSI_TX0 signals and FSI_RX0 signals are connected to the mux. The mux is controlled by jumper. The default state drives the signals from the AM64x/AM243x to the HSE connector unless the jumper is installed. The boards will be delivered with the jumper installed.

Additional signals like UART4, I2C0, SPI1 and GPIOs are connected to the HSE connector to provide additional connectivity options.

Necessary voltages such as 5 V, 3V3, 1V8 are provided to the HSE connector and these voltages are connected through current limiting switches ensuring that an accidental short on the connector will not damage the EVM. The connector includes a presence detect pin that will be grounded on the application board. This is connected to the ExpBrdDetect signal on the I2C presence detect buffer. A board ID memory is included in external HSE board and programmed to identify the board. I2C3 Pinmuxed with MCAN1 and UART4 pinmuxed with MCAN0 are routed to HSE Connector.

Note

The following net names do not indicate an exhaustive list of pin capabilities and available signal functions. For a full list of available secondary multiplexing of signal functions implemented in device subsystems, see the EVM Schematic, Sysconfig Tool and device-specific data sheet.

Table 3-24. Selection of PRG0 Signals on Application Connector

Connector Pin	SoC Ball	Net Name	Pin Multiplexed Signal Functions
A1	-	VCC_5V0_HSE	-
A2	-	VCC_5V0_HSE	-
A3	-	VCC_5V0_HSE	-
A4	P2	PRG0_MDIO0_MDIO	GPIO1_40, GPMC0_A12
A5	P3	PRG0_MDIO0_MDC	GPIO1_41, GPMC0_A13
A6	-	DGND	-
A7	T2	PRG0_PRU0GPO8	PRG0_PRU0_GPI8, PRG0_PWM2_A1, GPIO1_8,GPMC0_A2, UART4_RTSn
A8	U2	PRG0_PRU0GPO2	PRG0_PRU0_GPI2,PRG0_RGMII1_RD2, PRG0_PWM2_A0,GPIO1_2 GPMC0_A0, UART2_RTSn
A9	V2	PRG0_PRU0GPO3	PRG0_PRU0_GPI3,PRG0_RGMII1_RD3, PRG0_PWM3_A2, GPIO1_3, UART3_CTSn
A10	-	DGND	-
A11	W2	PRG0_PRU1GPO1	PRG0_PRU1_GPI1, PRG0_RGMII2_RD1, GPIO1_21, EQEP0_B,UART5_TXD
A12	Y2	PRG0_PRU1GPO0	PRG0_PRU1_GPI0,PRG0_RGMII2_RD0, GPIO1_20, EQEP0_A, UART5_CTSn
A13	AA2	PRG0_PRU0GPO4	PRG0_PRU0_GPI4,PRG0_RGMII1_RX_CTL, PRG0_PWM2_B0, GPIO1_4,GPMC0_A1, UART3_TXD
A14	AA3	PRG0_PRU0GPO12	PRG0_PRU0_GPI12,PRG0_RGMII1_TD1, PRG0_PWM0_A0, GPIO1_12, GPMC0_A14
A15	AA4	PRG0_PRU1GPO16	PRG0_PRU1_GPI16,PRG0_RGMII2_TXC, PRG0_PWM1_A2 , GPIO1_36, GPMC0_A11, PRG0_ECAP0_SYNC_OUT
A16	-	DGND	-
A17	-	PRG0_HSE_ETH1_CLK	-
A18	-	DGND	-
A19	Y20	GPMC0_AD15	FSI_TX0_D1, UART6_TXD, EHRPWM3_SYNCI, TRC_DATA13, GPIO0_30, BOOTMODE15
A20	-	HSE_GPIO0_36	-
A21	T17	GPMC0_AD9	FSI_RX0_D0, UART3_CTSn, EHRPWM2_B, TRC_DATA7, GPIO0_24, PRG0_PWM2_B2, BOOTMODE09
A22	V19	GPMC0_AD8	FSI_RX0_CLK , UART2_CTSn, EHRPWM2_A, TRC_DATA6, GPIO0_23, PRG0_PWM2_A2, BOOTMODE08
A23	-	DGND	-
A24	-	DGND	-
A25	-	DGND	-
A26	-	-	-
A27	-	VCC3V3_IO_HSE	-
A28	-	VCC3V3_IO_HSE	-
A29	-	VCC3V3_IO_HSE	-
A30	-	-	-
C1	C14	SOC_SPI1_CLK	EHRPWM6_SYNCI, GPIO1_49
C2	-	VCC1V8_HSE	-
C3	-	VCC1V8_HSE	-
C4	-	DGND	-

Table 3-24. Selection of PRG0 Signals on Application Connector (continued)

Connector Pin	SoC Ball	Net Name	Pin Multiplexed Signal Functions
C5	R6	PRG0_PRU0GPO13	PRG0_PRU0_GPI13, PRG0_RGMII1_TD2 ,PRG0_PWM0_B0, SPI3_D0, GPIO1_13, GPMC0_A15
C6	R3	PRG0_PRU0GPO5	PRG0_PRU0_GPI5, PRG0_PWM3_B2, GPIO1_5, UART3_RTSn
C7	-	DGND	-
C8	T4	PRG0_PRU1GPO3	PRG0_PRU1_GPI3, PRG0_RGMII2_RD3, GPIO1_23, EQEP1_A, GPMC0_A18, UART6_CTSn
C9	V4	PRG0_PRU0GPO14	PRG0_PRU0_GPI14, PRG0_RGMII1_TD3,PRG0_PWM0_A1, SPI3_D1, GPIO1_14, GPMC0_A3
C10	-	DGND	-
C11	U5	PRG0_PRU1GPO15	PRG0_PRU1_GPI15, PRG0_RGMII2_TX_CTL, PRG0_PWM1_B1, GPIO1_35 , GPMC0_A10, PRG0_ECAP0_IN_APWM_OUT
C12	V12	PRG1_PRU1GPO19	PRG1_PRU1_GPI19, PRG1_IEP1_EDC_SYNC_OUT0, PRG1_PWM1_TZ_OUT, RGMII1_RD3, RMII1_CRS_DV, SPI3_CS2, GPIO0_84, UART5_RTSn, PRG1_ECAP0_IN_APWM_OUT
C13	-	DGND	-
C14	T18	GPMC0_AD2	FSI_RX2_D1 , UART2_RTSn, EHRPWM_TZn_IN0, TRC_DATA0, GPIO0_17, PRG0_PWM2_TZ_IN, BOOTMODE02
C15	U19	GPMC0_AD5	FSI_RX3_D1, UART3_RTSn, EHRPWM1_A, TRC_DATA3, GPIO0_83, PRG0_PWM2_A1, BOOTMODE05
C16	-	DGND	-
C17	-	DGND	-
C18	-	DGND	-
C19	-	DGND	-
C20	-	DGND	-
C21	W21	GPMC0_AD12	FSI_RX1_D0, UART6_CTSn, EQEP1_B, TRC_DATA10, GPIO0_27, EHRPWM7_B, BOOTMODE12
C22	-	HSE_GPIO0_32	-
C23	-	HSE_GPIO0_34	-
C24	-	HSE_GPIO0_37	-
C25	-	DGND	-
C26	-	HSE_GPIO0_39	-
C27	R2	HSE_PRG0_PRU1_GPO19	PRG0_PRU1_GPI19, PRG0_IEP1_EDC_SYNC_OUT0, PRG0_PWM1_TZ_OUT, MDIO0_MDC, RMII1_CRS_DV, EHRPWM7_B, GPIO1_39, PRG0_ECAP0_IN_APWM_OUT
C28	V5	HSE_PRG0_PRU1_GPO17	PRG0_PRU1_GPI17, PRG0_IEP1_EDC_SYNC_OUT1 , PRG0_PWM1_B2, RGMII1_RD3, RMII1_TXD1, GPIO1_37, PRG0_ECAP0_SYNC_OUT, PRG0_ECAP0_SYNC_IN
C29	D17	HSE_MCAN1_RX/I2C3_SDA	ECAP2_IN_APWM_OUT, OBSCLK0, TIMER_IO5, UART5_TXD, EHRPWM_SOCB, GPIO1_63, EQEP2_B, UART0_DSRn
C30	-	DGND	-
E1	A18	SOC_I2C0_SCL	UART6_CTS, GPIO1_64

Table 3-24. Selection of PRG0 Signals on Application Connector (continued)

Connector Pin	SoC Ball	Net Name	Pin Multiplexed Signal Functions
E2	B18	SOC_I2C0_SDA	UART6_RTSn, GPIO1_65
E3	B13	MCU_RESETSTATZ	MCU_GPIO0_22
E4	-	HSE_DETECT	-
E5	-	DGND	-
E6	-	DGND	-
E7	-	DGND	-
E8	R4	PRG0_PRU0GPO1	PRG0_PRU0_GPI1, PRG0_RGMII1_RD1, PRG0_PWM3_B0, GPIO1_1, UART2_TXD
E9	U4	PRG0_PRU0GPO16	PRG0_PRU0_GPI16, PRG0_RGMII1_TXC, 2 IO 0 0/1 PRG0_PWM0_A2, SPI3_CLK, GPIO1_16, GPMC0_A4
E10	-	DGND	-
E11	R5	PRG0_PRU1GPO6	PRG0_PRU1_GPI6, PRG0_RGMII2_RXC, GPIO1_26, EQEP2_A, GPMC0_A19, UART4_CTSn
E12	U6	PRG0_PRU1GPO14	PRG0_PRU1_GPI14, PRG0_RGMII2_TD3, PRG0_PWM1_A1, GPIO1_34, EQEP1_I , GPMC0_A9, UART6_RXD
E13	Y13	PRG1_PRU1GPO18	PRG1_PRU1_GPI18, PRG1_IEP1_EDC_LATCH_IN0, PRG1_PWM1_TZ_IN, RGMII1_RD2, RMII1_TX_EN, GPIO0_20 , UART5_CTSn, PRG1_ECAP0_SYNC_IN
E14	T20	GPMC0_AD0	FSI_RX2_CLK, UART2_RXD, EHRPWM0_SYNCI, TRC_CLK, GPIO0_15, BOOTMODE00
E15	U20	GPMC0_AD3	FSI_RX3_CLK, UART3_RXD, EHRPWM0_A, TRC_DATA1, GPIO0_18, PRG0_PWM2_A0, BOOTMODE03
B1	A15	SOC_SPI1_MISO	EHRPWM6_B, GPIO1_51
B2	B15	SOC_SPI1_MOSI	EHRPWM6_SYNCO, GPIO1_50
B3	-	DGND	-
B4	R1	PRG0_PRU1GPO8	PRG0_PRU1_GPI8, PRG0_PWM2_TZ_OUT, GPIO1_28, EQEP2_S, UART4_RTSn
B5	-	DGND	-
B6	-	DGND	-
B7	T1	PRG0_PRU0GPO7	PRG0_PRU0_GPI7, PRG0_IEP0_EDC_LATCH_IN1, PRG0_PWM3_B1, CPTS0_HW2TSPUSH, CP_GEMAC_CPTS0_HW2TSPUSH, TIMER_IO6, GPIO1_7, UART4_TXD
B8	U1	PRG0_PRU0GPO17	PRG0_PRU0_GPI17, PRG0_IEP0_EDC_SYNC_OUT1, PRG0_PWM0_B2, CPTS0_TS_SYNC, CP_GEMAC_CPTS0_TS_SYNC, SPI3_CS0, GPIO1_17, TIMER_IO11, GPMC0_A17
B9	V1	PRG0_PRU0GPO18	PRG0_PRU0_GPI18, PRG0_IEP0_EDC_LATCH_IN0, PRG0_PWM0_TZ_IN, CPTS0_HW1TSPUSH, CP_GEMAC_CPTS0_HW1TSPUSH, EHRPWM8_A, GPIO1_18, UART4_CTSn, GPMC0_A5, UART2_RXD
B10	-	DGND	-
B11	W1	PRG0_PRU0GPO19	PRG0_PRU0_GPI19, PRG0_IEP0_EDC_SYNC_OUT0, PRG0_PWM0_TZ_OUT, CPTS0_TS_COMP, CP_GEMAC_CPTS0_TS_COMP, EHRPWM8_B, GPIO1_19, UART4_RTSn, GPMC0_A6, UART3_RXD
B12	Y1	PRG0_PRU0GPO0	PRG0_PRU0_GPI0, PRG0_RGMII1_RD0, PRG0_PWM3_A0, GPIO1_0, UART2_CTSn
B13	W3	PRG0_PRU1GPO4	PRG0_PRU1_GPI4, PRG0_RGMII2_RX_CTL, PRG0_PWM2_B2, GPIO1_24, EQEP1_B, UART6_TXD

Table 3-24. Selection of PRG0 Signals on Application Connector (continued)

Connector Pin	SoC Ball	Net Name	Pin Multiplexed Signal Functions
B14	Y3	PRG0_PRU0GPO11	PRG0_PRU0_GPI11, PRG0_RGMII1_TD0, PRG0_PWM3_TZ_OUT, GPIO1_11, UART4_RXD
B15	Y4	PRG0_PRU1GPO12	PRG0_PRU1_GPI12, PRG0_RGMII2_TD1, PRG0_PWM1_A0, GPIO1_32, EQEP2_B, GPMC0_A7, UART4_TXD
B16	-	DGND	-
B17	-	PRG0_HSE_ETH2_CLK	-
B18	-	DGND	-
B19	-	DGND	-
B20	Y21	GPMC0_AD14	FSI_TX0_D0, UART6_RXD,EHRPWM3_B, TRC_DATA12, GPIO0_29, PRG0_PWM3_B0, BOOTMODE14
B21	R16	GPMC0_AD10	FSI_RX0_D1, UART4_CTSn, EHRPWM_TZn_IN2, EHRPWM8_B, TRC_DATA8, GPIO0_25, PRG1_PWM2_B2, BOOTMODE10
B22	-	HSE_GPIO0_31	-
B23	-	DGND	-
B24	-	HSE_GPIO0_35	-
B25	-	DGND	-
B26	-	DGND	-
B27	-	DGND	-
B28	-	DGND	-
B29	AA5	HSE_PRG0_PRU0_GPO10	PRG0_PRU0_GPI10, PRG0_UART0_RTSn, PRG0_PWM2_B1, RGMII1_RXC, RMII_REF_CLK, PRG0_IEP0_EDIO_DATA_IN_OUT29,GPIO1_10, UART3_RXD
B30	-	DGND	-
D1	B14	SOC_SPI1_CS0	EHRPWM6_A, GPIO1_47
D2	D14	SOC_SPI1_CS1	CPTS0_TS_SYNC, I2C2_SDA, PRG1_IEP0_EDIO_OUTVALID, UART6_TXD, ADC_EXT_TRIGGER1, GPIO1_48, TIMER_IO11
D3	B12	MCU_RESETZ	-
D4	-	DGND	-
D5	T6	PRG0_PRU1GPO13	PRG0_PRU1_GPI13, PRG0_RGMII2_TD2, PRG0_PWM1_B0, GPIO1_33, EQEP0_I, GPMC0_A8, UART5_RXD
D6	P4	PRG0_PRU1GPO5	PRG0_PRU1_GPI5, GPIO1_25, EQEP1_S, UART6_RTSn
D7	-	DGND	-
D8	T3	PRG0_PRU0GPO6	PRG0_PRU0_GPI6, PRG0_RGMII1_RXC, PRG0_PWM3_A1, GPIO1_6, UART4_CTSn
D9	V3	PRG0_PRU1GPO2	PRG0_PRU1_GPI2, PRG0_RGMII2_RD2, PRG0_PWM2_A2, GPIO1_22, EQEP0_S, UART5_RTSn
D10	-	DGND	-
D11	W4	PRG0_PRU1GPO11	PRG0_PRU1_GPI11, PRG0_RGMII2_TD0, GPIO1_31, EQEP2_I, UART4_RXD
D12	T5	PRG0_PRU0GPO15	PRG0_PRU0_GPI15, PRG0_RGMII1_TX_CTL, PRG0_PWM0_B1, SPI3_CS1, GPIO1_15, GPMC0_A16
D13	-	DGND	-

Table 3-24. Selection of PRG0 Signals on Application Connector (continued)

Connector Pin	SoC Ball	Net Name	Pin Multiplexed Signal Functions
D14	U21	GPMC0_AD1	FSI_RX2_D0, UART2_TXD, EHRPWM0_SYNCO, TRC_CTL, GPIO0_16, PRG0_PWM2_TZ_OUT, BOOTMODE01
D15	U18	GPMC0_AD4	FSI_RX3_D0, UART3_TXD, EHRPWM0_B, TRC_DATA2, GPIO0_82, PRG0_PWM2_B0, BOOTMODE04
D16	-	DGND	-
D17	V21	GPMC0_AD7	FSI_RX4_D1, UART4_TXD, EHRPWM_TZn_IN1, EHRPWM8_A, TRC_DATA5, GPIO0_22, PRG1_PWM2_A2, BOOTMODE07
D18	P19	GPMC0_CSN2	I2C2_SCL, TIMER_IO8, EQEP1_S, EHRPWM_TZn_IN4, GPIO0_43, PRG1_PWM2_TZ_IN
D19	R21	GPMC0_CSN3	I2C2_SDA, TIMER_IO9, EQEP1_I, GPMC0_A20, EHRPWM_TZn_IN5, GPIO0_44
D20	-	DGND	-
D21	V18	GPMC0_AD13	FSI_RX1_D1, EHRPWM3_A, TRC_DATA11, GPIO0_28, PRG0_PWM3_A0, BOOTMODE13
D22	-	HSE_GPIO0_33	-
D23	W5	HSE_PRG0_PRU1_GPO7	PRG0_PRU1_GPI7, PRG0_IEP1_EDC_LATCH_IN1, RGMII1_RD0, RMII1_RXD0, GPIO1_27, EQEP2_B, UART4_TXD
D24	A17	HSE_MCAN0_TX/UART4_RXD	TIMER_IO2, SYNC2_OUT, SPI4_CS1, GPIO1_60, EQEP2_I, UART0_DTRn
D25	-	DGND	-
D26	-	HSE_GPIO0_41	-
D27	P5	HSE_PRG0_PRU1_GPO18	PRG0_PRU1_GPI18, PRG0_IEP1_EDC_LATCH_IN0, PRG0_PWM1_TZ_IN, MDIO0_MDIO, RMII1_TX_EN, EHRPWM7_A, GPIO1_38, PRG0_ECAP0_SYNC_IN
D28	W6	HSE_PRG0_PRU0_GPO9	PRG0_PRU0_GPI9, PRG0_UART0_CTSn, PRG0_PWM3_TZ_IN, RGMII1_RX_CTL, RMII1_RX_ER, PRG0_IEP0_EDIO_DATA_IN_OUT28, GPIO1_9, UART2_RXD
D29	C17	HSE_MCAN1_TX/I2C3_SCL	ECAP1_IN_APWM_OUT, SYSCLKOUT0, TIMER_IO4, UART5_RXD, EHRPWM_SOCA, GPIO1_62, EQEP2_A, UART0_DCDn
D30	-	DGND	-
E16	-	DGND	-
E17	V20	GPMC0_AD6	FSI_RX4_D0, UART4_RXD, EHRPWM1_B, TRC_DATA4, GPIO0_21, PRG0_PWM2_B1, BOOTMODE06
E18	N17	GPMC0_DIR	EQEP0_B, GPIO0_40, EHRPWM6_B, PRG1_PWM2_B0
E19	R20	GPMC0_CSN1	EQEP0_I, EHRPWM_TZn_IN2, GPIO0_42, EHRPWM6_SYNCO, PRG1_PWM2_TZ_OUT
E20	-	DGND	-
E21	W20	GPMC0_AD11	FSI_RX1_CLK, UART5_CTSn, EQEP1_A, TRC_DATA9, GPIO0_26, EHRPWM7_A, BOOTMODE11
E22	-	DGND	-
E23	Y5	HSE_PRG0_PRU1_GPO9	PRG0_PRU1_GPI9, PRG0_UART0_RXD, RGMII1_RD1, PRG0_IEP0_EDIO_DATA_IN_OUT30, GPIO1_29, EQEP0_I, UART5_RXD
E24	B17	HSE_MCAN0_RX/UART4_TXD	UART4_TXD, TIMER_IO3, SYNC3_OUT, SPI4_CS2, GPIO1_61, EQEP2_S, UART0_RIn

Table 3-24. Selection of PRG0 Signals on Application Connector (continued)

Connector Pin	SoC Ball	Net Name	Pin Multiplexed Signal Functions
E25	-	DGND	-
E26	-	HSE_GPIO0_38	-
E27	V6	HSE_PRG0_PRU1_GPO10	PRG0_PRU1_GPI10, PRG0_UART0_TXD, PRG0_PWM2_TZ_IN, RGMII1_RD2, RMII1_TXD0, PRG0_IEP0_EDIO_DATA_IN_OUT31, GPIO1_30, EQEP1_I, UART6_RXD
E28	-	DGND	-
E29	-	DGND	-
E30	B21	MCU_PORZ	-

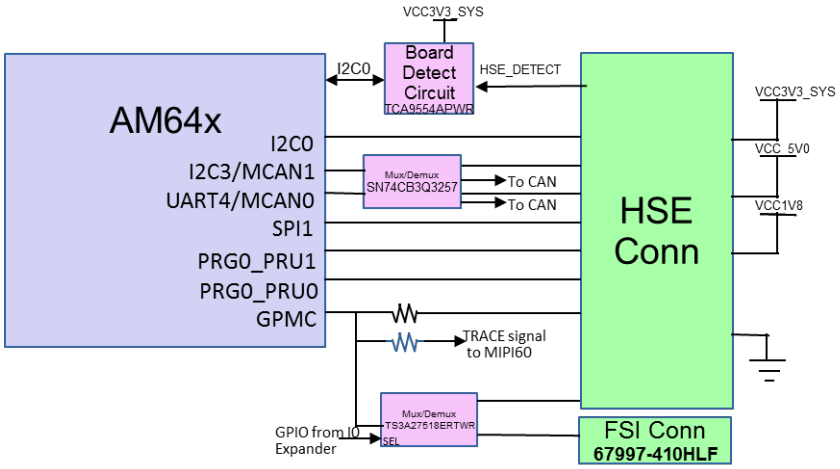


Figure 3-26. AM64x/AM243x High Speed Expansion Connector

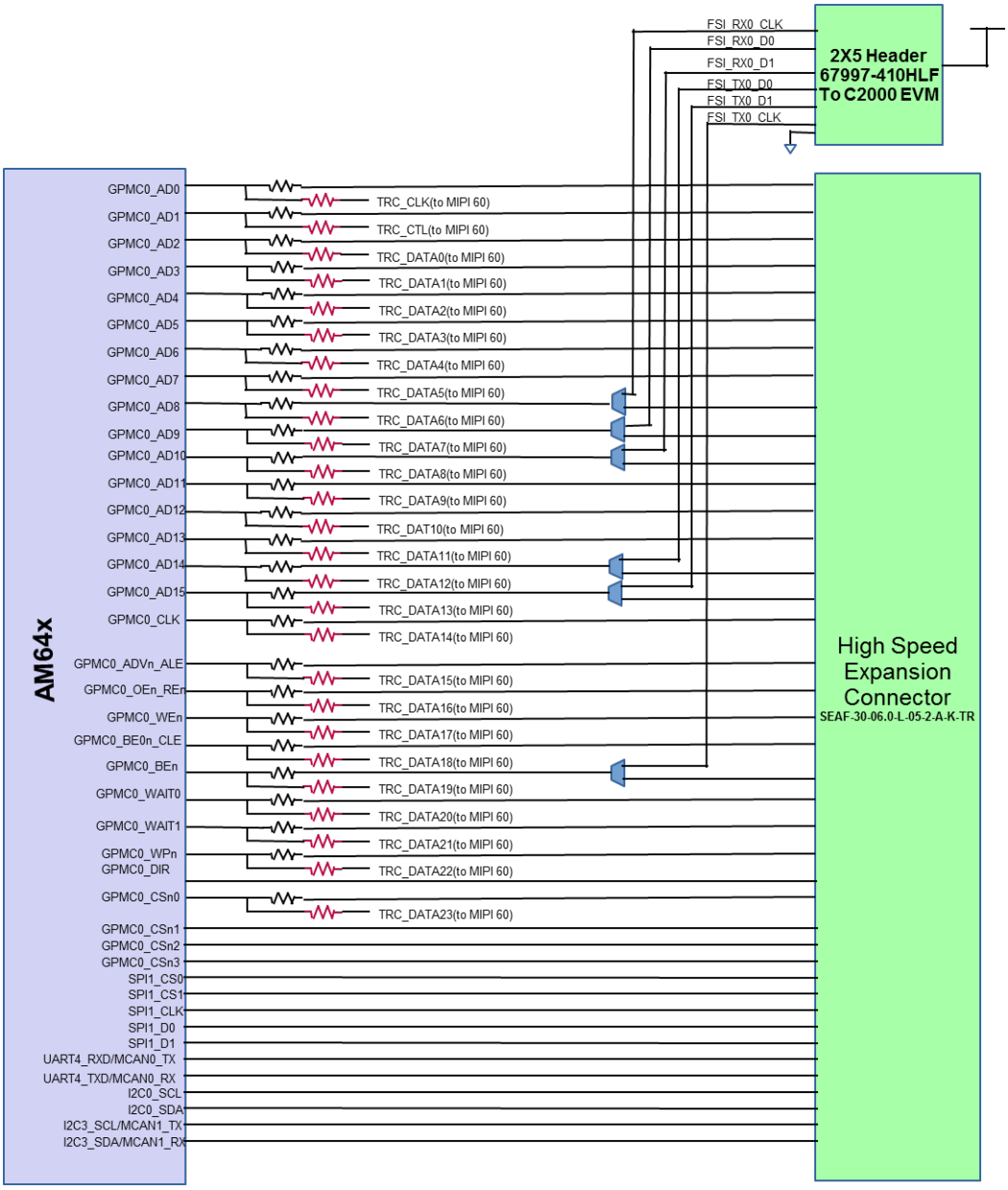


Figure 3-27. AM64x/AM243x High Speed Expansion Connector - Part 1

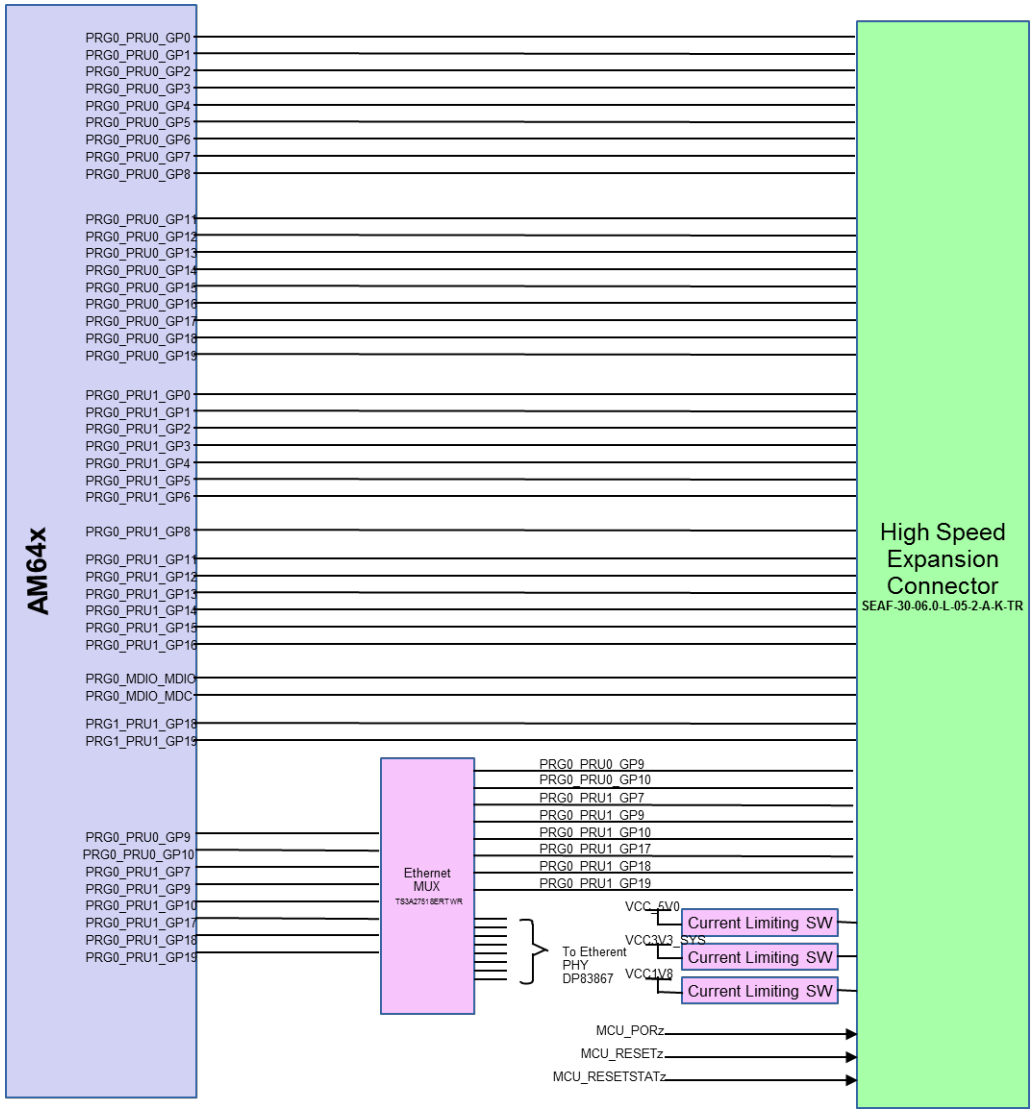


Figure 3-28. AM64x/AM243x High Speed Expansion Connector - Part 2

3.4.14 CAN Interface

The GP EVM includes two CAN interfaces. The MCAN0 and MCAN1 pins are muxed internally with UART4 and I2C3 respectively. These signals are connected to an on board MUX to route the signals to either the MCAN Transceiver or to the HSE connector, this MUX is controlled by the IO Expander. Figure 3-29 depicts the implementation of CAN interface using TCAN1042HGV. RXD and TXD pins are connected to MCAN0_RX/ UART4_TXD and MCAN0_TX/UART4_RXD pins of AM64x respectively. STB pin of the IC is by default connected to ground to avoid IC entering stand-by mode. The STB pin is controlled by GPIO to enable Standby mode.

The pin-out of CAN connector is shown in Table 3-25.

Table 3-25. CAN (J31 and J32) Pin-out

CAN0 J31		CAN1 J32	
Pin No.	Signal	Pin No.	Signal
1	MCAN0_H	1	MCAN0_H
2	GND	2	GND
3	MCAN0_L	3	MCAN0_L

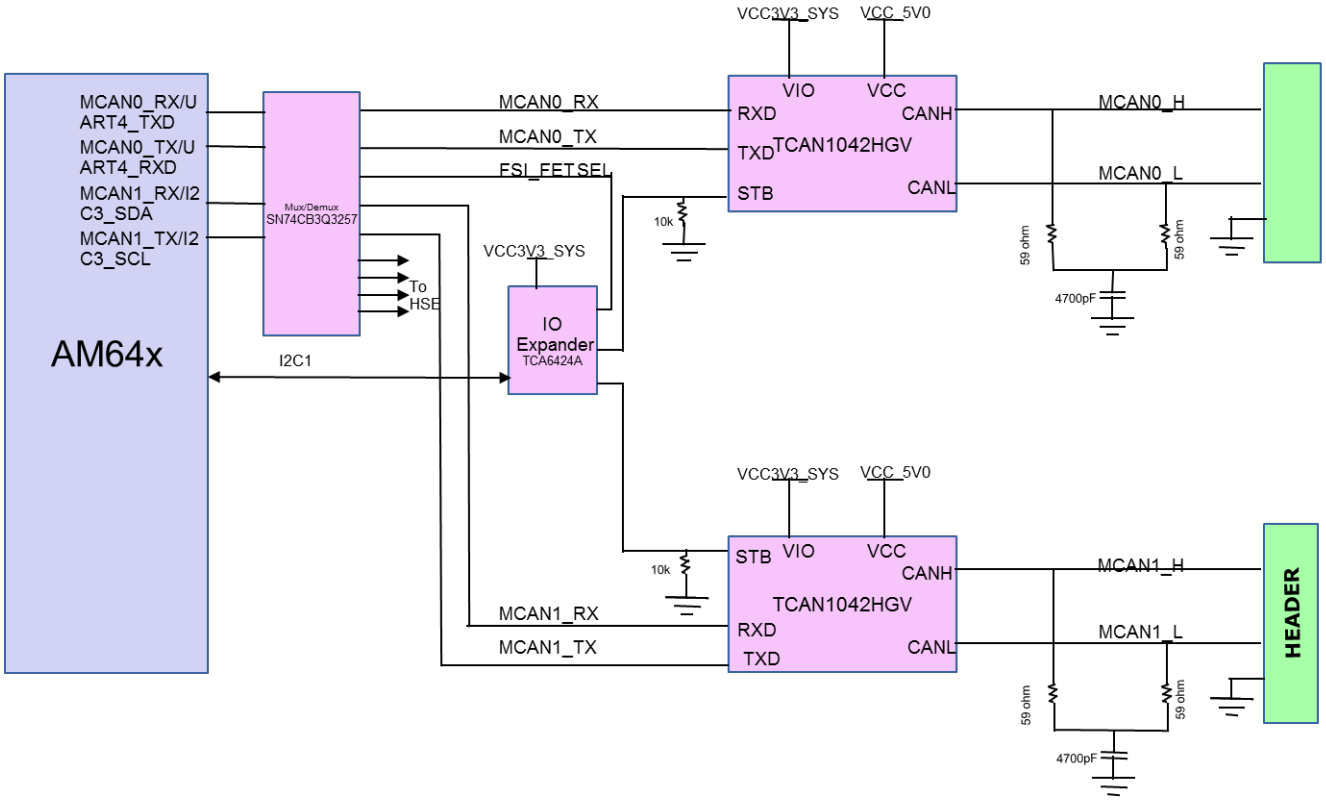


Figure 3-29. AM64x/AM243x CAN Interfaces

3.4.15 Interrupt

The GP EVM supports the following timer and interrupt options.

Three push button switches are available to provide reset for MCU_PORz and MCU_RESETz and RESET_REQz. One push button switch is available for GPIO interrupt, which is connected to both main domain and MCU domain GPIO pin.

Warm reset can also be applied through Test automation header or manual reset switches SW4 (SoC) and SW6 (MCU).

Power on reset input can be applied though switch SW7.

3.4.16 ADC Interface

A 20-pin connector J3 of part number TSW-110-07-S-D for connecting ADC signals of the AM64x/AM243x. The connector includes ADC0_AIN0-7, VDDA_ADC connections and ground connections.

Table 3-26. ADC Connector (J3) Pin-out

Pin No.	Signal	Pin No.	Signal
1	DGND	11	ADC0_AIN7
2	NC	12	DGND
3	ADC0_AIN6	13	DGND
4	VDDA_ADC	14	ADC0_AIN1
5	DGND	15	ADC0_AIN0
6	ADC0_AIN2	16	DGND
7	ADC0_AIN5	17	VDDA_ADC
8	DGND	18	ADC0_AIN3
9	DGND	19	NC
10	ADC0_AIN4	20	DGND

3.4.17 Safety Connector

A 12x2 standard 0.1” spaced header- TSW-112-07-S-D is included as a safety signal connector. The safety connector includes signals connected to the MCU. The 24 pins include MCU_I2C0, MCI_I2C1, MCU_UART1, MCU_SPI0 and MCU_SPI1 signals. This provides eighteen signals that can be used as either the specified interface or as MCU_GPIOs. In addition the CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz and MCU_SAFETY_ERRORn signals are supported with the connector.

Table 3-27. Safety Connector Pinouts

Pin No.	Signal	Pin No.	Signal
1	VCC_3V3_SYS	13	MCU_UART1_RTS_3V3
2	MCU_SPI0_D1	14	MCU_I2C1_SDA
3	MCU_SPI0_CS1	15	MCU_UART1_TX_3V3
4	MCU_SPI0_D0	16	MCU_SPI0_CLK
5	MCU_GPIO0_8	17	MCU_I2C0_SDA
6	MCU_SPI0_CS0	18	MCU_I2C1_SCL
7	TEST_LED2	19	MCU_RESETSTATZ
8	MCU_GPIO0_6	20	MCU_I2C0_SCL
9	MCU_GPIO0_7	21	CONN_MCU_RESETZ
10	MCU_UART1_CTS_3V3	22	MCU_SAFETY_ERRORZ_3V3
11	MCU_UART1_RX_3V3	23	DGND
12	MCU_GPIO0_9	24	CONN_MCU_PORZ

3.4.18 SPI Interfaces

- SPI0: A 1Kbit SPI EEPROM (93LC46B) is interfaced to SPI0 port of the AM64x/AM243x. It is used for testing purposes.
- SPI1: This interface is routed to the HSE Connector. The SPI1 interface signals are at a 3.3 V IO level.
  - SPI1_CS0 is routed to the HSE expansion header (J2)
  - SPI1_CS1 is routed to the HSE expansion header (J2)

3.4.19 I2C Interfaces

There are five I2C interfaces used in the GP EVM board.

1. MAIN_I2C0: This interface is used by the software to identify the EVM and to control the power supply circuit. It is interfaced to presence detect latch to identify the daughter cards which are presently installed, Board ID memory device, board ID memories of the daughter cards and HSE connector. This I2C is also connected to a test header J5 for AM64x/AM243x processor slave operation. Pin outs of I2C test header is given in Table 3-28.

Table 3-28. I2C Test Header (J5) Pin-out

Pin No.	Signal
1	DGND
2	SoC_I2C0_SDA
3	SoC_I2C0_SCL

2. MAIN_I2C1: This is interfaced to 16 bit GPIO expanders that is being used for all control signals and LED controls, 8bit LED Driver with part number **TPIC2810,** Current Monitors with part number **INA226** to monitor current of VDD_CORE, VDDAR_CORE, SoC_DVDD3V3, SoC_DVDD1V8, VDDA_1V8, VDD_DDR4 , Temperature sensor with part number **TMP100**, Display Interface with part number **OSD9616P0992-10**, Test automation connector via voltage isolation. This I2C is also connected to a test header J4 for AM64x processor slave operation. Pin outs of I2C test header is given in Table 3-29.

Table 3-29. I2C Test Header (J4) Pin-out

Pin No.	Signal
1	SoC_I2C1_SCL
2	SoC_I2C0_SDA
3	DGND
4	INA_ALERT
5	NC

3. MAIN_I2C3: This is connected to the expansion board connector from a mux. I2C3 is muxed with the MCAN signals. The default state of the mux is MCAN.
4. MCU_I2C0: This is connected to the safety connector.
5. MCU_I2C1: This is connected to the safety connector.

Figure 3-30 depicts the I2C tree.

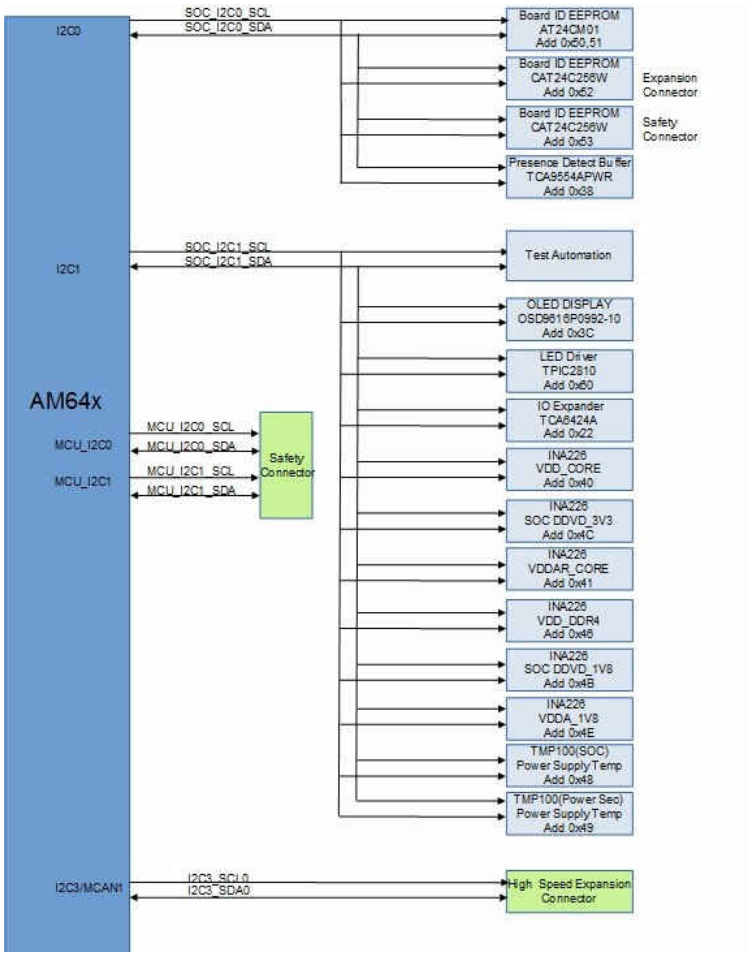


Figure 3-30. AM64x/AM243x I2C Interfaces and Address Assignment of Peripherals

3.4.20 FSI Interface

One FSI Interface (1Tx and 1Rx) from SoC is terminated on 2x5 header with part number **67997-410HLF** from Amphenol ICC (FCI) having connections which can be interfaced to C2000 EVM. FSI_TX0 signals and FSI_RX0 signals are connected to the mux so that they are available to both the FSI connector and the expansion connector. The TS3A27518E mux-demux is used for this purpose and it is controlled by GPIO from IO Expander. A logic low in Mux select pin connects port A and Port B1 whereas a logic high connects A port to B2 port. The default state of mux drives the signals from A port to B1 port, which is connected to HSE connector.

Table 3-30. FSI (J5) Connector Pin-out

Pin No.	Signal
1	FSI_TX0_CLK
2	FSI_RX0_CLK
3	DGND
4	DGND
5	FSI_TX0_D0
6	FSI_RX0_D0
7	FSI_TX0_D1
8	FSI_RX0_D1
9	DGND
10	VCC_3V3_SYS

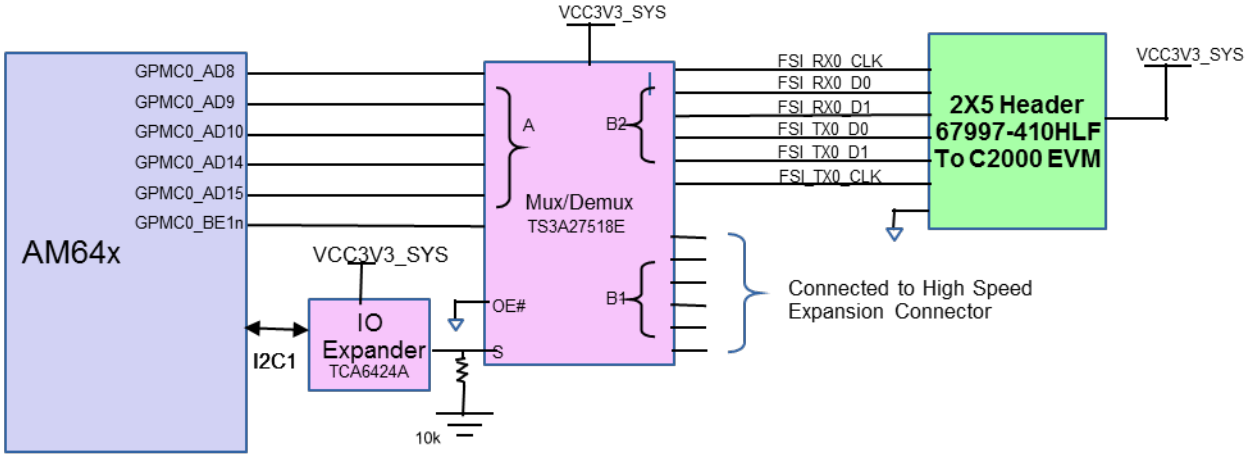


Figure 3-31. AM64x/AM243x FSI Interface

4 Known Issues and Modifications

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched will have modification labels attached to the EVM assembly. These modification labels can be found as shown in Table 4-1 and Figure 4-1.

Table 4-1. AM64x/AM243x GP EVM Known Issues and Modifications

Issue Number	Modification Label Number	Issue Title	Issue Description
1	N/A	Embedded XDS110 connection issue	Embedded XDS110 fails to connect to AM64x target in CCS after first EVM power cycle.
2	4, 5	MDIO Ethernet PHY Communications	Intermittent MDIO communications to the CPSW and ICSSG1 PHY

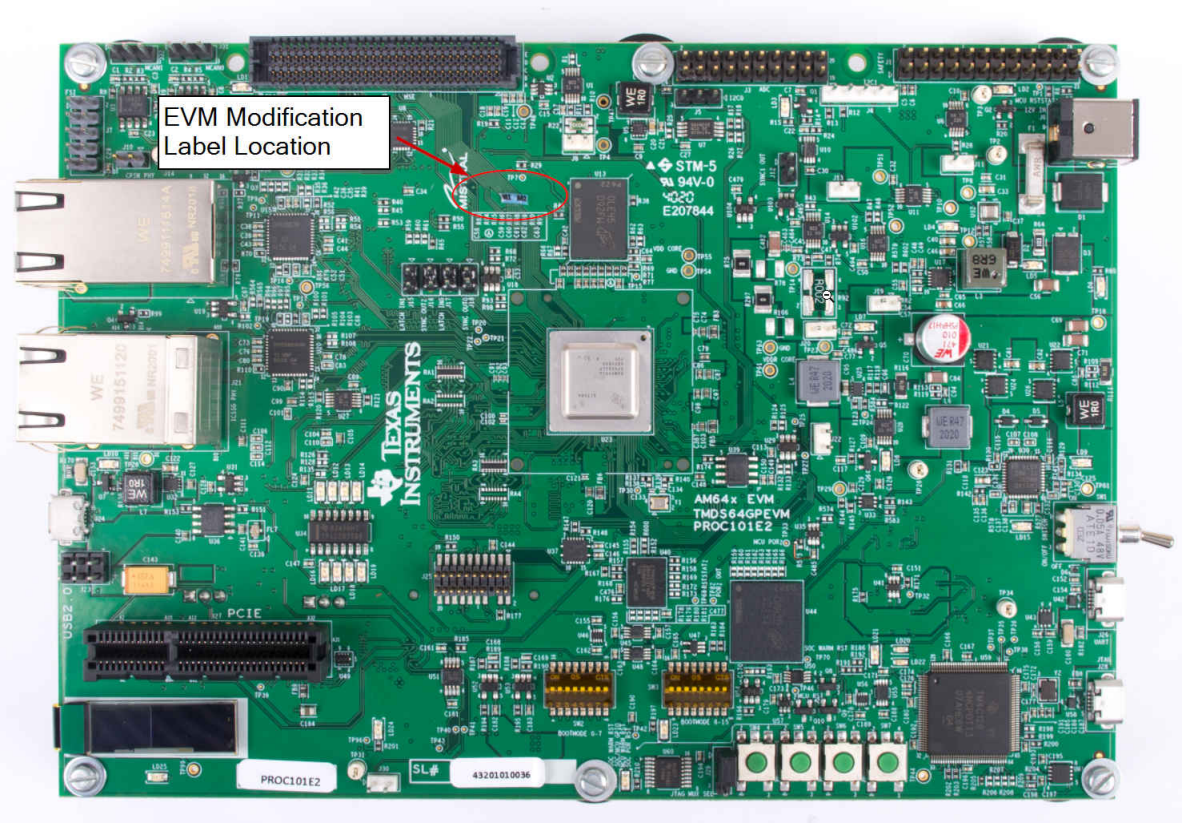


Figure 4-1. AM64x/AM243x GP EVM Modification Label Location

4.1 Issue 1 - Embedded XDS110 Connection to AM64x Target in CCS

Applicable EVM Revisions: E2

Issue Description: On some EVM, the embedded XDS110 (U59) has been shown to fail initial target connection to AM64x target in CCS after first EVM and XDS110 power cycle. No problem exists when using an attached, external emulator over the CTI20 header (J25).

This failure mode can be encountered by following the steps below:

1. XDS110 USB is attached between host PC and XDS110 USB port (J28).
2. EVM power is enabled and the AM64x is brought up in *no-boot* mode.
3. In CCS, an initial CCS target connection to the M3 DMSC core is then attempted.

4. CCS will error out with the below dialog complaining of a DAP connection error to the target core.
   a. Hitting retry results in the same error message

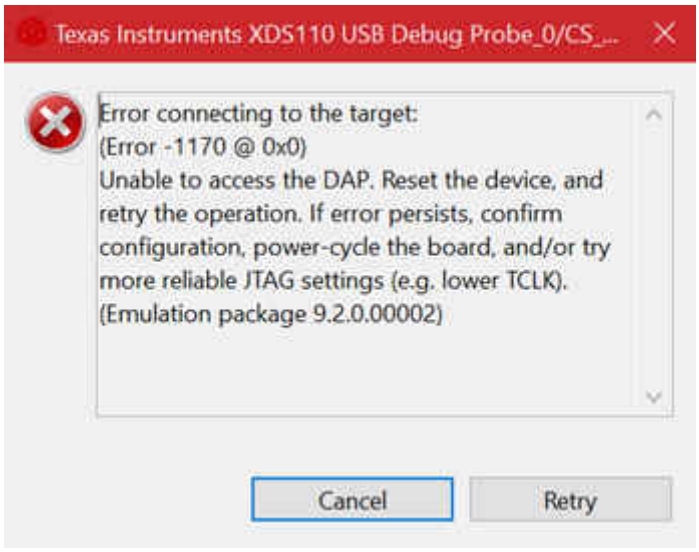


Figure 4-2. XDS110 CCS Connection Error Dialog

Workaround 1: After the connection issue is encountered, users can unplug the USB host connection to the XDS110 emulator through USB port (J28) and then plugin the USB cable again. This power cycles the XDS110 and will clear up the connection error.

Workaround 2: After the connection issue is encountered, users can toggle TRSTSN through the XDS110 debug command-line utility *xds110reset* found in the CCS XDS110 utility directory.

In the Windows OS installation, for a default installation of CCS version 10.11, this tool is found in the directory C:\ti\ccs1011\ccs\ccs_base\common\uscif\xds110>

This command can be executed on the Windows command prompt/terminal when the embedded XDS110 is powered on and connected to the host PC. A similar tool is available under the Linux OS install of CCS.

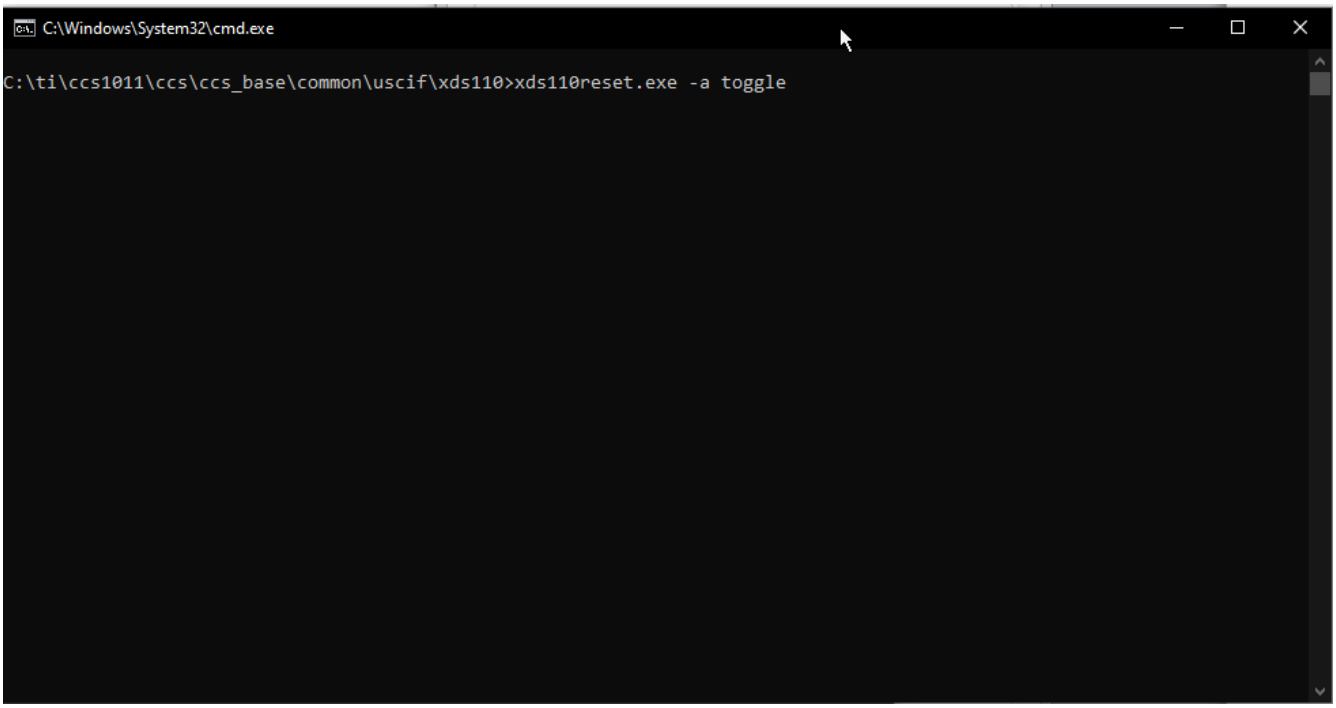


Figure 4-3. XDS110 debug reset utility command-line function

4.2 Issue 2 - MDIO Ethernet PHY Communications

Applicable EVM Revisions: E2

Issue Description: On some EVM, U78 MDIO MUX path has been shown to result in intermittent MDIO PHY communication between the AM64x SoC and CPSW and ICSSG Ethernet PHY.

Workaround: Modifications number 4 and 5 are applied to the assembly. These modifications result in the HSE header losing access to the *HSE_PRG0_PRU1_GPO18* and *HSE_PRG0_PRU1_GPO19* signals.

Modification 4 description:

- R370, 2.2kΩ resistor installed

Modification 5 description:

- All components located on the bottom of the PCB assembly layer
- Remove U78
- Short U78.2 to U78.4
- Short U78.8 to U78.6

4.3 Issue 3 - DC Barrel Jack Warning when Hot-Plugging

Applicable EVM Revisions: E2, A

Issue Description: Many cost-saving plug designs do not guarantee a secure, ground-first connection when attempting to hot-plug the J6 DC Barrel Jack connector. This could lead to intermittent brown-out type conditions that may result in damage to the board.

Solution: Hot plugging the power supply is never recommended at the connector end. The “Power On/Off Procedures” outlined in the “Getting Started” section of the document should be followed when applying or removing power from the board. Furthermore, ensure you are using the recommended part number for your EVM Revision as outlined in the Power Supply section of Section 3.1

5 References

- *AM64x Sitara™ Processors Data Manual*
- *AM64x Processors Silicon Revision 1.0 Texas Instruments Families of Products Technical Reference Manual*

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2021) to Revision D (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	3
• Updates made in Section 3.1	6
• Update was made in Section 3.4.3	13
• Updates were made in Section 3.4.4.1	18

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