

Migration Between TMS320F28002x, TMS320F280015x and TMS320F280013x Guide



ABSTRACT

This migration guide describes the hardware and software differences to be aware of when moving between F28002x, F280015x and F280013x C2000™ MCUs. This document shows the block diagram between the three MCUs as a visual representation of which blocks are similar or different. It also highlights the features that are unique between the three devices for all available packages in a device comparison table. A PCB hardware section has been added to aid in migration between packages that are in common between the devices. All three devices have the 64-pin PM and 48-pin PT/PHP packages in common. F28002x and F280015x have an additional 80-pin PN package in common, and F280013x and F280015x have an additional 32-pin RHB package in common. The digital general-purpose input/output (GPIO) and analog multiplex comparison tables show pin functionality between the three MCUs. This is a good reference for hardware design and signal routing when considering a move between the three devices. Lastly, like the F28002x device, the F280015x and F280013x software support is only in EABI format.

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1 Feature Differences Between F28002x, F280015x and F280013x

F280015x and F280013x are a subset of F28002x. The three devices have two packages in common: 48-pin and 64-pin. F28002x and F280015x have an additional 80-pin package in common. F280015x and F280013x have an additional 32-pin package in common. It is possible to migrate between F280013x, F280015x and F28002x with the caveats in this document taken into account.

Note

This comparison guide focuses on the super-set devices: F280025, F2800157 and F2800137. Other part numbers in these product families have reduced feature support. For details specific to part numbers, see the device-specific data sheet.

1.1 F28002x, F280015x and F280013x Feature Comparison

An overlaid block diagram of F28002x, F280015x and F280013x is shown in [Figure 1-1](#) while feature comparison of the superset part numbers for the F28002x, F280015x and F280013x devices is shown in [Table 1-1](#).

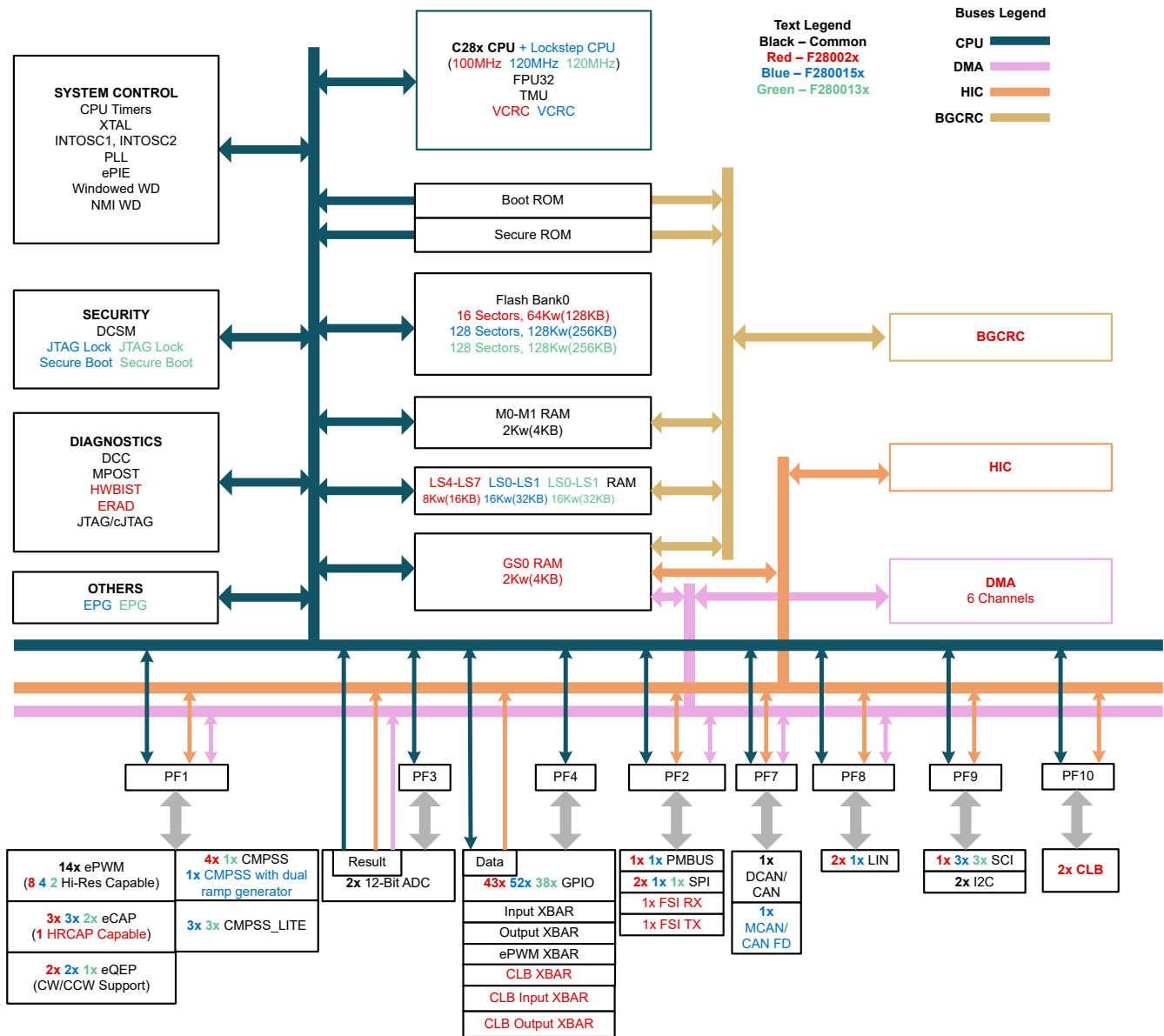


Figure 1-1. F28002x, F280015x and F280013x Overlaid Functional Block Diagram

1.1.1 F28002x, F280013x and F280015x Superset Device Comparison
Table 1-1. F28002x, F280013x and F280015x Superset Device Comparison

Feature		F28002x			F280015x								F280013x								
		ALL			F2800157, F2800155, F2800153				F2800156, F2800154, F2800152				F2800137, F2800135, F2800133				F2800132				
		80 PN	64 PM	48 PT	80 PN	64 PM	48 PHP	32 RHB	80 PN	64 PM	48 PHP	32 RHB	64 VPM	64 PM	48 PT	48 RGZ	32 RHB	48 PT	48 RGZ	32 RHB	
Processor and Accelerators																					
C28x	Frequency (MHz)	100			120																
	FPU				Yes																
	Fast Integer Division	Yes			-																
	VCRC				Yes								-								
	TMU				Yes																
	NLPID	Yes			-																
	Lockstep Compare Module (LCM)	-			Yes								-								
6-Channel DMA – Type 0		Yes			-																
External interrupts					5																
Memory																					
Flash		128KB (64Kw)			256KB (128Kw) - 157, 156 128KB (64Kw) - 155, 154 64KB (32Kw) - 153, 152								256KB (128Kw) - 137 128KB (64Kw) - 135, 135V 64KB (32Kw) - 133, 132								
RAM		24KB (12Kw)			36KB (18Kw)																
ECC		FLASH, Mx, LSx			FLASH, Mx																
Parity		GSx, ROM			LSx, ROM																
Code security for on-chip flash and RAM					Yes																
System																					
Configurable Logic Block (CLB)		2 Tiles			-																
Embedded Pattern Generator (EPG)		-			Yes																
Motor Control Libraries in ROM		Yes			-																
32-bit CPU timers					3																
Background CRC (BGCRC)		Yes			-																
Secure Boot		-			Yes																
JTAG Lock		-			Yes																
HWBIST		Yes			-																
Nonmaskable Interrupt Watchdog (NMIWD) timers					1																
Watchdog timers					1																

Table 1-1. F28002x, F280013x and F280015x Superset Device Comparison (continued)

Feature	F28002x			F280015x								F280013x								
	ALL			F2800157, F2800155, F2800153				F2800156, F2800154, F2800152				F2800137, F2800135, F2800133				F2800132				
	80 PN	64 PM	48 PT	80 PN	64 PM	48 PHP	32 RHB	80 PN	64 PM	48 PHP	32 RHB	64 VPM	64 PM	48 PT	48 RGZ	32 RHB	48 PT	48 RGZ	32 RHB	
Crystal oscillator/External clock input	1																			
0-pin internal oscillator	2																			
INTOSC with ExtR Support	-			Yes																
Pins and Power Supply																				
Internal 3.3v to 1.2v Voltage Regulator	VREG LDO	Yes																		
GPIO Pins	GPIO	39	26	14	37	22	15	9	37	22	15	9	22	23	13	16	10	13	16	10
	AGPIO (analog with digital inputs and outputs)	-			11	11	8	5	11	11	8	5	11	11	8	8	5	8	8	5
	JTAG and Oscillator GPIO	4 (2 from cJTAG and 2 from X1/X2)																		
	Total GPIO	43	30	18	52	37	27	18	52	37	27	18	37	38	25	28	19	25	28	19
	AIO (analog with digital inputs)	16	16	14	10	10	9	6	10	10	9	6	10	10	9	9	6	9	9	6
	Total GPIO and AIO	59	46	32	62	47	36	24	62	47	36	24	47	48	34	37	25	34	37	25
Analog Peripherals																				
ADC 12-bit	Number of ADCs	2																		
	Conversion-time (ns) / MSPS (AIO pins)	290 ns / 3.45 MSPS			250 ns / 4.00 MSPS				290 ns / 3.45 MSPS				250 ns / 4.00 MSPS				290 ns / 3.45 MSPS			
	Conversion-time (ns) / MSPS (AGPIO pins)	-			266 ns / 3.75 MSPS				300 ns / 3.33 MSPS				266 ns / 3.75 MSPS				300 ns / 3.33 MSPS			
ADC channels (single-ended)	16	16	14	21	17	11	21	17	11	21	17	11	21	21	17	17	11	17	17	11
Temperature sensor	1																			
CMPSS (each CMPSS has two comparators)	4 (with two internal dynamic DACs and single ramp generator)			1 (with two internal dynamic DACs and dual ramp generators)				-				1 (with two internal dynamic DACs and single ramp generator)								
CMPSS DAC Buffered Output (CMPx_DACL)	-			1 (mutually exclusive with using CMPSS for compare)				-				1 (mutually exclusive with using CMPSS for compare)								
CMPSS_LITE (each CMPSS_LITE has two comparators)	-			3 (with two internal static DAC)																
Control Peripherals																				
eCAP/HRCAP modules - Type 2	3 (1 with HRCAP capability)			3 (0 with HRCAP capability)								2 (0 with HRCAP capability)								

Table 1-1. F28002x, F280013x and F280015x Superset Device Comparison (continued)

Feature	F28002x			F280015x								F280013x								
	ALL			F2800157, F2800155, F2800153				F2800156, F2800154, F2800152				F2800137, F2800135, F2800133				F2800132				
	80 PN	64 PM	48 PT	80 PN	64 PM	48 PHP	32 RHB	80 PN	64 PM	48 PHP	32 RHB	64 VPM	64 PM	48 PT	48 RGZ	32 RHB	48 PT	48 RGZ	32 RHB	
ePWM/HRPWM channels – Type 4	14 (8 with HRPWM)			14 (4 with HRPWM)				14 (0 with HRPWM)				14 (2 with HRPWM)				6 (2 with HRPWM)				
eQEP modules - Type 2	2								1											
Communication Peripherals																				
CAN (DCAN) – Type 0	1											-								
MCAN (CAN FD) – Type 2	-			1								-								
FSI	1 (1 RX and 1 TX) – Type 1			-																
I2C – Type 1	2																			
LIN – Type 1	2			1								-								
HIC – Type 1	1			-																
PMBus – Type 0	1								-											
SCI – Type 0	1			3																
SPI – Type 2	2			1																
Package Options, Temperature, and Qualification																				
S: -40°C to 125°C (TJ)	Yes					No		Yes			No				Yes					
Q: -40°C to 125°C (TA) (AEC Q100 qualification)	Yes											No								

2 PCB Hardware Changes

The F28002x, F280015x and F280013x devices have two packages in common: 64-Pin PM and 48-Pin PT. The F28002x and F280015x devices have an additional 80-Pin PN package in common. The following sections describe the pin migration in detail.

Note

Overall compatibility depends on more than just the pins. Review all of the changes in this document during the migration process.

2.1 PCB Hardware Changes for the 80-Pin PN, 64-Pin PM and 48-Pin PT or PHP Packages

This section describes the F280013x, F280015x and F28002x differences that exist between the 80-Pin PN, 64-Pin PM and 48-Pin PT or PHP packages.

Table 2-1. Packages Available by Device

Package	F28002x	F280015x	F280013x
80 PN (QFP)	Yes	Yes	-
64 PM/VPM (QFP)	Yes	Yes	Yes
48 PT (QFP)	Yes	-	Yes
48 PHP (QFP with PowerPAD™)	-	Yes	-
48 RGZ (QFN)	-	-	Yes
32 RHB (QFN)	-	Yes	Yes

80-Pin PN: The Q and non-Q variant have the same pinout for both F28002x and F280015x devices. [Figure 2-1](#) outline the differences.

64-Pin PM/VPM: The Q and non-Q variant have the same pinout for all three devices. [Figure 2-2](#) outline the differences.

48-Pin PT or PHP: The Q and non-Q variant have the same pinout for all three devices. However the 48-Pin PHP package on F280015x has the addition of a PowerPAD™. Care must be taken when considering the board layout between these three devices due to this PowerPAD™. [Figure 2-3](#) outlines the differences.

48-Pin RGZ: This package is only available on the F280013x, and so has no cross-compatibility with the other devices.

32-Pin RHB: F280015x and F280013x devices have this package in common with the same pinout for the two devices. [Figure 2-4](#) outlines the differences.

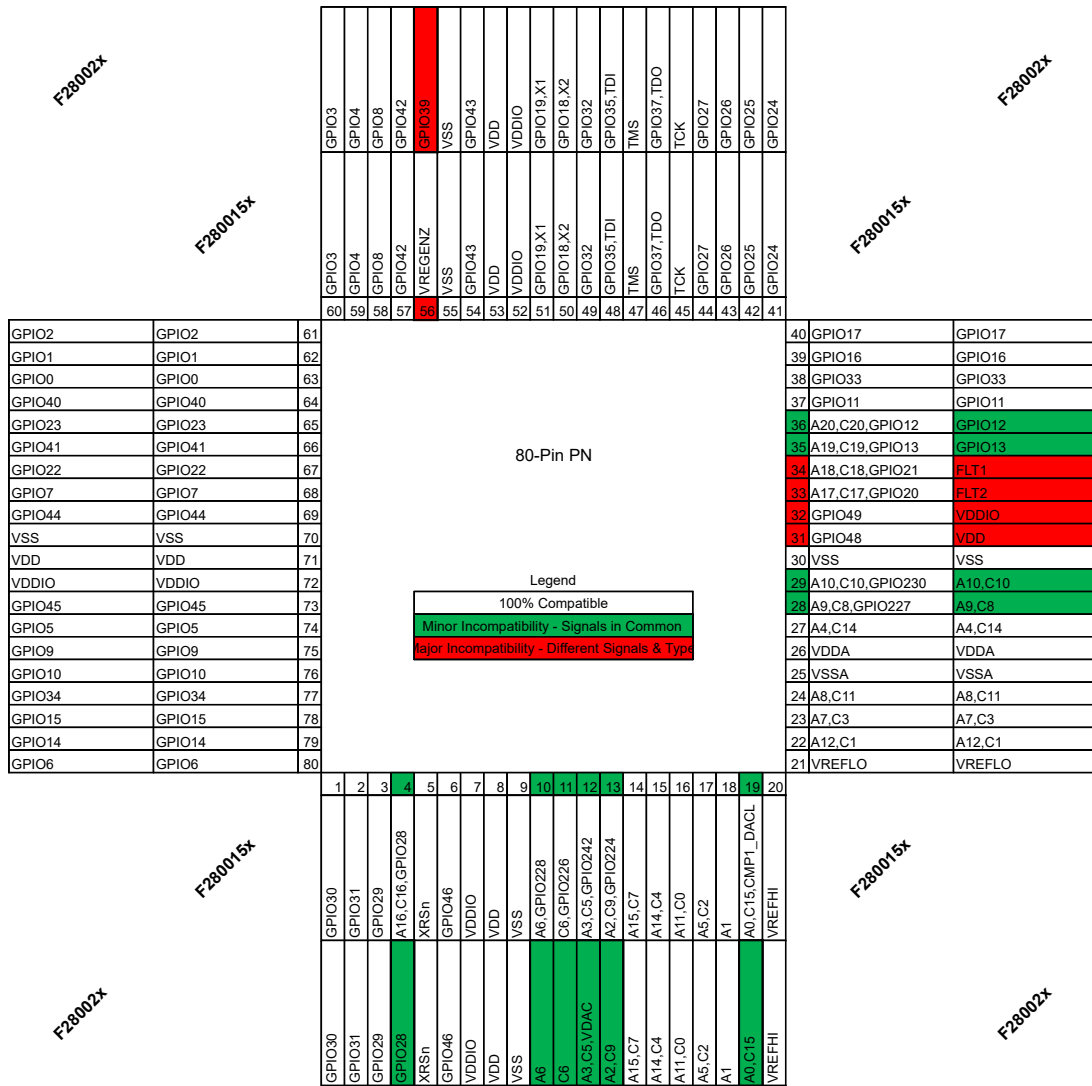


Figure 2-1. 80-Pin PN F280015x and F28002x Pin-Overlay

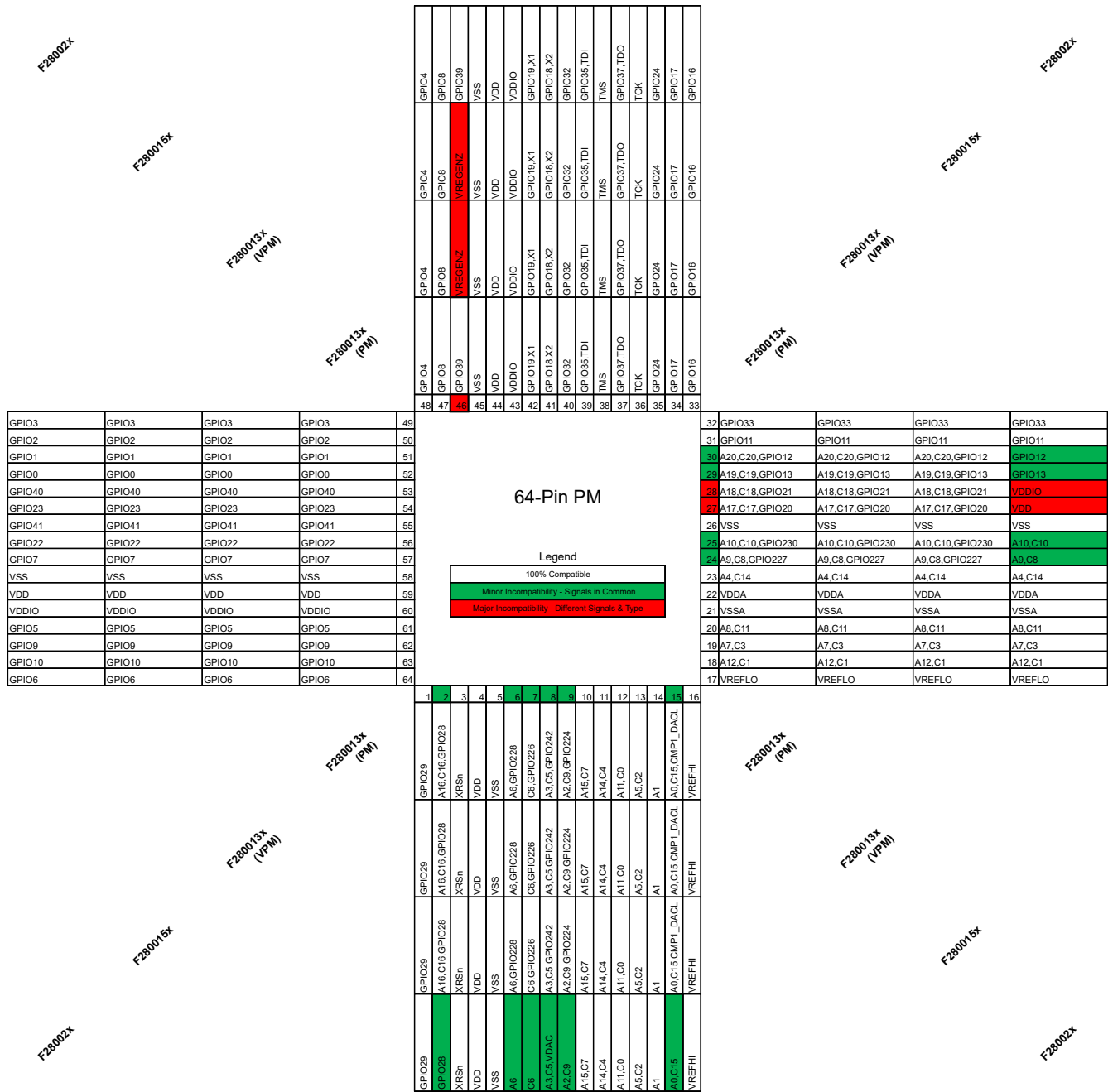
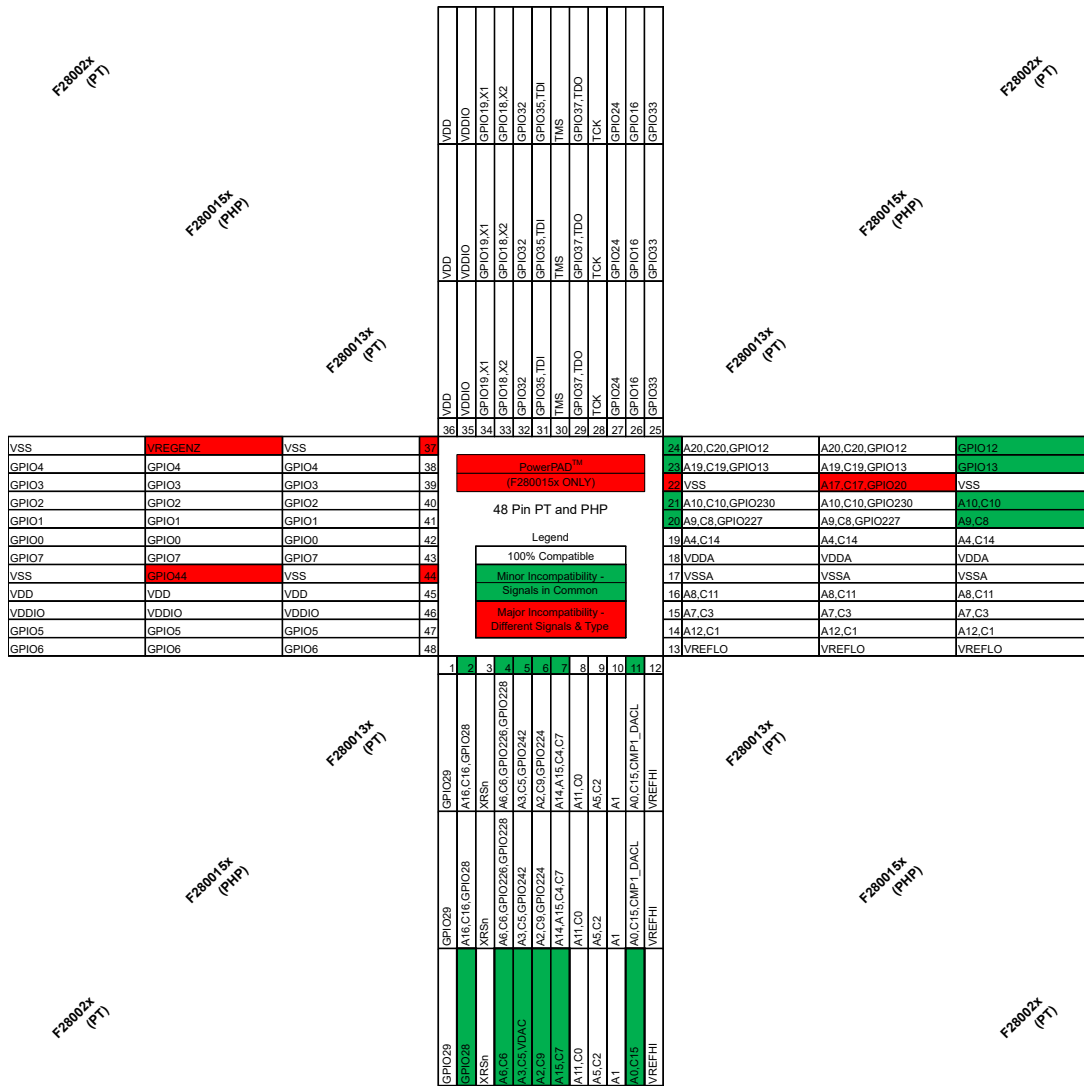


Figure 2-2. 64-Pin PM F280013x, F280015x and F28002x Pin-Overlay



Note

F280015x 48-pin PHP package has a PowerPAD™ integrated for thermal performance. This must be accounted for in design when migrating between the three 48-pin devices.

Figure 2-3. 48-Pin PT or PHP F280013x (PT), F280015x (PHP with PowerPAD™) and F28002x (PT) Pin-Overlay

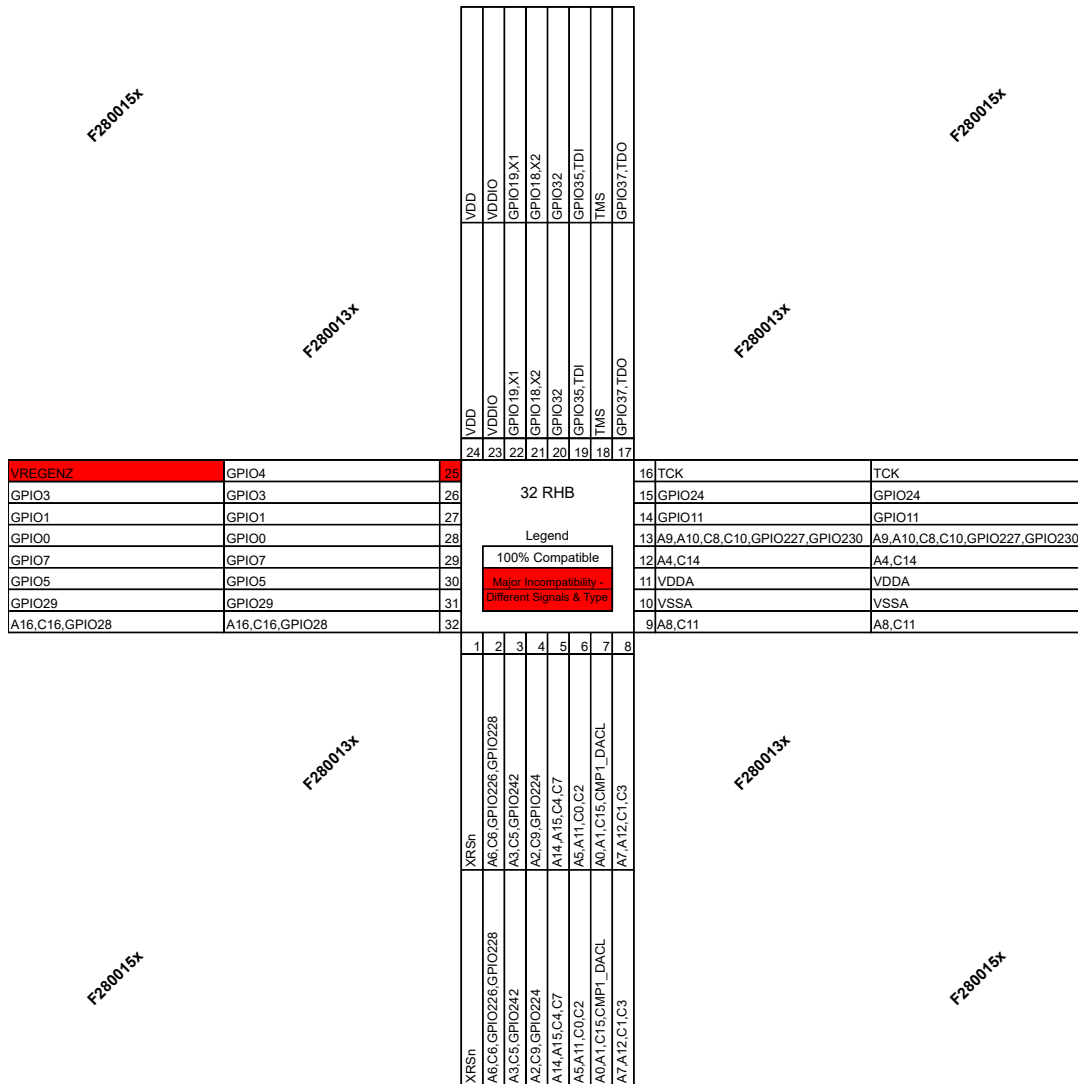


Figure 2-4. 32-Pin RHB F280013x and F280015x Overlay

2.2 New and Existing PCB Migration

This section covers migration between F28002x, F280013x, and F280015x for new and existing PCBs using 80-Pin PN, 64-Pin PM and 48-Pin PT or PHP packages.

Table 2-2. PCB Migration Incompatibilities

Pin No				Pin Name				Action
80 PN	64 PM/ VPM	48 PT/ PHP	32 RHB	F28002x	F280015x	F280013x (64 VPM)	F280013x	For Compatibility
Minor Incompatibility - Signals in Common ⁽¹⁾								
4	2	2	-	GPIO28		A16, C16	GPIO28	Use GPIO28
10	6	4	-	A6		A6	GPIO228	Use A6
11	7		-	C6		C6	GPIO226	Use C6
12	8	5	-	A3, C5, VDAC		A3, C5	GPIO242	Use A3 or C5
13	9	6	-	A2, C9		A2, C9	GPIO224	Use A2 or C9
-	-	7	-	A15, C7		A14, A15, C4, C7		Use A15 or C7
19	15	11	-	A0, C15		A0, C15	CMP1_DACL	Use A0 or C15
28	24	20	-	A9, C8		A9, C8	GPIO227	Use A9 or C8
29	25	21	-	A10, C10		A10, C10	GPIO230	Use A10 or C10
35	29	23	-	GPIO13		A19, C19	GPIO13	Use GPIO13
36	30	24	-	GPIO12		A20, C20	GPIO12	Use GPIO12
Major Incompatibility - Different Signals and Types								
-	-	PAD	-	-	PAD	-	-	The 48-pin F280015x has a PowerPAD™ while the 48-pin F28002x and F280013x do not. The PowerPAD™ must be accounted for in board layout when considering migrating between devices.
-	27	22	-	VDD		A17, C17	GPIO20	If using a F280013x/15x device in a F28002x board, the VDD pin can be used as a GPIO or you can follow the unused pins practice for GPIOs found in the device-specific data sheet. If using F28002x in a F280013x/15x board, the GPIO pin is now a VDD pin and must be tied to VDD.
31	-	-	-	VDD	GPIO48	-	-	If using a F280015x device in a F28002x board, the VDD pin can be used as a GPIO or you can follow the unused pins practice for GPIOs found in the device-specific data sheet. If using F28002x in a F280015x board, the GPIO pin is now a VDD pin and must be tied to VDD.
-	28	-	-	VDDIO		A18, C18	GPIO21	If using a F280013x/15x device in a F28002x board, the VDDIO pin can be used as a GPIO or you can follow the unused pins practice for GPIOs found in the device-specific data sheet. If using F28002x in a F280013x/15x board, the GPIO pin is now a VDDIO pin and must be tied to VDDIO.
32	-	-	-	VDDIO	GPIO49	-	-	If using a F280015x device in a F28002x board, the VDDIO pin can be used as a GPIO or you can follow the unused pins practice for GPIOs found in the device-specific data sheet. If using F28002x in a F280015x board, the GPIO pin is now a VDDIO pin and must be tied to VDDIO.

Table 2-2. PCB Migration Incompatibilities (continued)

Pin No				Pin Name				Action
80 PN	64 PM/VPM	48 PT/PHP	32 RHB	F28002x	F280015x	F280013x (64 VPM)	F280013x	For Compatibility
33	-	-	-	FLT2	A17, C17, GPIO20			<p>If using a F280013x/15x device in a F28002x board, the FLT pin can be used as a GPIO or you can follow the unused pins practice for GPIOs found in the device-specific data sheet.</p> <p>If using F28002x in a F280013x/15x board, the GPIO pin is now a FLT pin and must be left unconnected.</p>
34	-	-	-	FLT1	A18, C18, GPIO21			
56	46	-	-	GPIO39	VREGENZ	VREGENZ	GPIO39	<p>F28002x and F280013x (except for 64 VPM package) do not have a VREGENZ pin, as the internal VREG is always enabled.</p> <p>If using a VREGENZ device in a F28002x/13x board, tie the GPIO to VDDIO to use an external supply or tie the GPIO to VSS to use the internal VREG.</p> <p>If using a F28002x/13x device in a board for a device with VREGENZ, the VREGENZ pin can be used as a GPIO or you can follow the unused pins practice for GPIOs found in the device-specific data sheet.</p> <p>For additional information on external and internal supplies, see the device-specific data sheet.</p>
-	-	-	25	-		GPIO4		
-	-	37	-	VSS	VREGENZ		VSS	<p>F28002x and F280013x (except for 64 VPM package) do not have a VREGENZ pin, as the internal VREG is always enabled.</p> <p>If using a VREGENZ device in a F28002x/13x board, tie the VSS pin trace (now VREGENZ) to VDDIO to use an external supply or keep the VSS pin tied to VSS (no change) to use the internal VREG.</p> <p>If using a F28002x/13x device in a board for a device with VREGENZ, the VREGENZ pin trace (now VSS) should be tied to VSS.</p> <p>For additional information on external and internal supplies, see device-specific data sheet.</p>
-	-	44	-	VSS	GPIO44		VSS	<p>F280015x has a PowerPAD™ while F28002x and F280013x do not. VSS pins get replaced with other functions for F280015x. The PowerPAD™ must be accounted for in board layout when considering migrating between 48-pin devices.</p> <p>If using F280015x in a F28002x/13x board, the VSS pin can be used as a GPIO or you can follow the unused pins practice for GPIOs found in the device-specific data sheet.</p> <p>If using F28002x/13x in a F280015x board, the GPIO pin has been replaced by VSS so that pin should be tied to VSS.</p>

(1) Channel to use selected in software

3 Feature Differences for System Consideration

The differences and similarities that exist when moving between the F280013x, F280015x and F28002x devices is explored in this section.

3.1 New Features in F280013x and F280015x

This section outlines features that only exist in the F280013x and F280015x devices. For details on each of these new features, see the [TMS320F280013x Microcontrollers Technical Reference Manual](#) and [TMS320F280015x Microcontrollers Technical Reference Manual](#).

3.1.1 Secure Boot/JTAG Lock

The F280013x and F280015x devices support secure booting and also have the capability to lock the JTAG to avoid debug access thereby enhancing security. Secure Boot and JTAG Lock were first introduced in F2838x.

3.1.2 Embedded Pattern Generator (EPG)

The EPG on F280013x and F280015x is an interface module that can be used to generate waveforms and clocks for other modules on the device. This can be useful for communication module diagnostics.

3.1.3 Lockstep Compare Module (LCM)

This feature is only available on F280015x. The Lockstep Compare Module (LCM) provides the device with the ability to detect permanent and transient faults in the CPU and PIE. For more details on the LCM implementation, see [TMS320F280015x Microcontrollers Technical Reference Manual \(SPRUIY4\)](#).

3.1.4 INTOSC External Precision Resistor (ExtR)

To improve the accuracy of INTOSC2, an external resistor (ExtR) mode can be used. This mode allows for a highly accurate external resistor to be added to the board and connected to the ExtR-capable pin.

3.2 Communication Module Changes

Communication module changes between the F28002x, F280015x and F280013x devices affect the number of modules. Some of the communication module have been removed from F280013x or F280015x device, and some modules are added to the F280015x device. Details are available in [Table 3-1](#).

Table 3-1. Communication Module Instances

Module	Category	F28002x	F280015x	F280013x
CAN	Number	1 - CANA		
MCAN	Number	Not present	1 - MCANA	Not present
SCI	Number	1 - SCIA	3 - SCIA, SCIB, SCIC	
LIN	Number	2 - LINA, LINB	1 - LINA	Not present
SPI	Number	2 - SPIA, SPIB	1 - SPIA	
I2C	Number	2 - I2CA, I2CB		
PMBUS	Number	1 - PMBUSA		Not present
FSI	Number	1 - FSIA	Not present	
HIC	Number	1 - HICA	Not present	

3.3 Control Module Changes

There are minimal changes in the control modules between the F28002x, F280015x and F280013x devices. [Table 3-2](#) shows the module instances differences that should be considered when migrating applications between F28002x, F280015x and F280013x.

Table 3-2. Control Module Differences

Module	Category	F28002x	F280015x	F280013x	Notes
eQEP	Number	2 - EQEP1, EQEP2		1 - EQEP1	
eCAP	Number	3 - ECAP1..3		2 - ECAP1..2	
HRCAP	Number	1 - HRCAP3	Not present		
ePWM	Number	7 - EPWM1..7			Blanking window improvements on F280013x/15x
	Registers	-	DCACTL.EVT1LATSEL		DCAEVT1 Latched Signal Select
		-	DCACTL.EVT1LATCLRSEL		DCAEVT1 Latched Clear Source Select
		-	DCACTL.EVT1LAT		Indicates the status of DCAEVT1LAT signal
		-	DCACTL.EVT2LATSEL		DCAEVT2 Latched Signal Select
		-	DCACTL.EVT2LATCLRSEL		DCAEVT2 Latched Clear Source Select
		-	DCACTL.EVT2LAT		Indicates the status of DCAEVT2LAT signal
		-	DCBCTL.EVT1LATSEL		DCBEVT1 Latched Signal Select
		-	DCBCTL.EVT1LATCLRSEL		DCBEVT1 Latched Clear Source Select
		-	DCBCTL.EVT1LAT		Indicates the status of DCBEVT1LAT signal
		-	DCBCTL.EVT2LATSEL		DCBEVT2 Latched Signal Select
		-	DCBCTL.EVT2LATCLRSEL		DCBEVT2 Latched Clear Source Select
		-	DCBCTL.EVT2LAT		Indicates the status of DCBEVT2LAT signal
	DCFCCTL.PULSESEL	DCFCCTL.PULSESEL		Blank Pulse Mix added as an option for F280013x/15x	
HRPWM	Number	4 - HRPWM1..4		2 - HRPWM1..2	

3.4 Analog Module Differences

This section outlines the analog differences between F280013x, F280015x and F28002x. The GPDAC is not present on the F28002x and the analog mux table is remapped.

Table 3-3. Analog Module Differences

Category	F28002x	F2800157, F2800155, F2800153	F2800156, F2800154, F2800152	F2800137, F2800135, F2800135V, F2800133	F2800132	Notes
ADC ⁽¹⁾						
Number	2 (ADCA, ADCC)					
AIO (analog with digital inputs)	75 ns	75 ns	80 ns	75 ns	80 ns	
AGPIO (analog with digital inputs and outputs)	-	91.6 ns	90 ns	91.6 ns	90 ns	
Minimum Sample window duration (With 50 Ω or less Rs)						
Typical ADCCLK Frequency	50 MHz	60 MHz	50 MHz	60 MHz	50 MHz	
Typical SYSCLK Frequency	100 MHz	120 MHz	100 MHz	120 MHz	100 MHz	
ADCSOCxCTL.CHSEL	4 bits (select chan 0 to 15)		5 bits (select chan 0 to 19)			
CMPSS ⁽¹⁾						
Number (each CMPSS has two comparators)	4 (CMPSS1 to CMPSS4) (with two internal dynamic DACs and single ramp generator)	1 (CMPSS1) (with two internal dynamic DACs and dual ramp generators)	-	1 (CMPSS1) (with two internal dynamic DACs and single ramp generator)		
CMPSS DAC Buffered Output	-	1 (mutually exclusive with using CMPSS for compare)	-	1 (mutually exclusive with using CMPSS for compare)		

Table 3-3. Analog Module Differences (continued)

Category	F28002x	F2800157, F2800155, F2800153	F2800156, F2800154, F2800152	F2800137, F2800135, F2800135V, F2800133	F2800132	Notes	
Registers	CTRIPxFILCLKCTL.CLKPRESCALE[9..0]	CTRIPxFILCLKCTL.CLKPRESCALE[15..0]				CMPSS filter prescaling size increased on F280013x	
	COMPDACCTL	COMPDACHCTL				Register name change	
	-	COMPDACHCTL2			-	Added register to support ramp generator cross trigger configuration.	
	COMPDACCTL.Reserved[13]	COMPDACHCTL.RAMPDIR[13]	COMPDACHCTL.Reserved[13]			Added bit to support direction selection for ramp generator in F280015x.	
	RAMPMAXREFA	RAMPHREFA				Register name change	
	RAMMAXREFS	RAMPHREFS				Register name change	
	REMPDECVALA	RAMPHSTEPVALA				Register name change	
	REMPDECVALS	RAMPHSTEPVALS				Register name change	
	RAMPSTS	RAMPHSTS				Register name change	
	RAMPDLYA	RAMPHDLYA				Register name change	
	RAMPDLYS	RAMPHDLYS				Register name change	
	CTRIPLFILCTL	CTRIPLFILCTL - Field Changes		CTRIPLFILCTL - Field Changes			All three devices have additions and changes to fields within this register. For more details, see the device-specific TRMs.
	CTRIPLFILCLKCTL	CTRIPLFILCLKCTL - Field Changes				F280015x and F280013x have increased prescaler range	
	CTRIPHFILCTL	CTRIPHFILCTL - Field Changes		CTRIPHFILCTL - Field Changes			All three devices have additions and changes to fields within this register. For more details, see the device-specific TRMs.
	CTRIPHFILCLKCTL	CTRIPHFILCLKCTL - Field Changes				F280015x and F280013x have increased prescaler range	
	-	COMPDACTL			-	Register and functionality added to support dual ramp generators	
	-	RAMPLREFA			-	Register and functionality added to support dual ramp generators	
	-	RAMPLREFS			-	Register and functionality added to support dual ramp generators	
	-	RAMPLSTEPVALA			-	Register and functionality added to support dual ramp generators	
	-	RAMPLSTEPVALS			-	Register and functionality added to support dual ramp generators	
	-	RAMPLSTS			-	Register and functionality added to support dual ramp generators	
	-	RAMPLDLYA			-	Register and functionality added to support dual ramp generators	
	-	RAMPLDLYS			-	Register and functionality added to support dual ramp generators	
-	CTRIPLFILCLKCTL2			-	Register and functionality added to support digital filtering. For more details, see the device-specific TRMs.		
-	CTRIPHFILCLKCTL2			-	Register and functionality added to support digital filtering. For more details, see the device-specific TRMs.		
Other	CMPx_HP has 5 mux input options	CMPx_HP has 6 mux input options					
CMPSS_LITE ⁽¹⁾							
Number (each CMPSS_LITE has two comparators)	-	3 (CMPSS_LITE2, CMPSS_LITE3, CMPSS_LITE4) (with two internal static DAC)					

Table 3-3. Analog Module Differences (continued)

Category	F28002x	F2800157, F2800155, F2800153	F2800156, F2800154, F2800152	F2800137, F2800135, F2800135V, F2800133	F2800132	Notes
Registers	-	COMPDACHCTL.RAMPDIR[13]		COMPDACHCTL.Reserved[13]		Added bit to support direction selection for ramp generator in F280015x.
	-	CTRIPFILCTL - Field Changes		CTRIPFILCTL - Field Changes		F280013x and F280015x devices have additions and changes to fields within this register. For more details, see the device-specific TRMs.
	-	CTRIPHFILCTL - Field Changes		CTRIPHFILCTL - Field Changes		F280013x and F280015x devices have additions and changes to fields within this register. For more details, see the device-specific TRMs.
	-	COMPDACTL		-		Register and functionality added to support dual ramp generators
	-	CTRIPFILCLKCTL2		-		Register and functionality added to support digital filtering. For more details, see the device-specific TRMs.
	-	CTRIPHFILCLKCTL2		-		Register and functionality added to support digital filtering. For more details, see the device-specific TRMs.
Temp Sensor						
Number	1 - (in ADCC ch 12)					

- (1) In porting software from F28002x to F280013x or F280015x (or the other way around), care must be taken to ensure that the correct ADC channels are used because of a difference in channel assignment, see Analog Multiplexing Changes

3.4.1 CMPSS Module Variants

F280013x and F280015x devices contain two different variants of the CMPSS module: CMPSS (full module) and the CMPSS_LITE (reduced functionality and performance). The differences in features between the two variants are summarized in [Table 3-4](#)

Table 3-4. CMPSS and CMPSS_LITE Feature Comparison

Feature	CMPSS	CMPSS_LITE
High and low comparators	Yes	Yes
Dual 12-bit reference DACs	Yes	Yes
DAC ramp generation	Yes	No
Low DAC output on external pin	Yes (Some instances)	No
Digital filters	Yes	Yes
Performance	Full Performance (See CMPSS electrical characteristics in data manual)	Some Reduced Performance (See CMPSS electrical characteristics in data manual)

3.5 Other Device Changes

This section describes feature differences between F28002x, F280015x and F280013x that were not covered in the previous sections, as such the changes identified below must be considered when migrating applications between devices.

3.5.1 PIE Channel Mapping

Pie channel mapping between F28002x and F280015x or F280013x is different due to peripheral module changes between these devices. [Table 3-6](#) summarizes the common and unique pie channel assignments on these three devices.

Table 3-5. PIE Channel Legend

Color	Description
	PIE channel applicable for all three devices
	PIE channel applicable for F280013x and F280015x only
	PIE channel applicable for F280015x only
	PIE channel applicable for F280015x and F28002x only
	PIE channel applicable for F28002x only

Table 3-6. PIE Channel Mapping Comparison

	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT1.y	ADCA1	ADCC1	ADCC1	XINT1	XINT2	SYS_ERR	TIMER0	WAKE / WDOG	-	-	-	-	-	-	-	-
INT2.y	EPWM1_TZ	EPWM2_TZ	EPWM3_TZ	EPWM4_TZ	EPWM5_TZ	EPWM6_TZ	EPWM7_TZ	-	-	-	-	-	-	-	-	-
INT3.y	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	EPWM7	-	-	-	-	-	-	-	-	-
INT4.y	ECAP1	ECAP2	ECAP3	-	-	-	-	-	-	-	ECAP3 INT2	-	-	-	-	-
INT5.y	EQEP1	EQEP2	-	-	CLB1	CLB2	-	-	-	-	-	-	-	-	-	-
INT6.y	SPIA_RX	SPIA_TX	SPIB_RX	SPIB_TX	LINA_0	LINA_1	DCC0	-	-	-	-	-	-	-	-	-
INT7.y	DMA_CH1	DMA_CH2	DMA_CH3	DMA_CH4	DMA_CH5	DMA_CH6	PMBUSA	-	-	-	FSITX_INT1	FSITX_INT2	FSIRX_INT1	FSIRX_INT2	-	DCC0
INT8.y	I2CA	I2CA_FIFO	I2CB	I2CB_FIFO	SCIC_RX	SCIC_TX	-	-	LINA_0	LINA_1	LINB_0	LINB_1	PMBUSA	-	-	DCC1
INT9.y	SCIA_RX	SCIA_TX	SCIB_RX	SCIB_TX	CANA_0	CANA_1	MCANSS_0	MCANSS_1	-	-	-	-	BGCRC	-	-	HICA
INT10.y	ADCA_EVT	ADCA2	ADCA3	ADCA4	ADCC_EVT	ADCC2	ADCC3	ADCC4	ADCC_EVT	ADCC2	ADCC3	ADCC4	-	-	-	-
INT11.y	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INT12.y	XINT3	XINT4	XINT5	MPOST	FMC/FLSS_INT	VCRC	MCANSS_WAKE_AND_TS_PLS	MCANSS_ECC_CORR_PLS	-	-	RAM_CORRECTABLE_ERROR	FLASH_CORRECTABLE_ERROR	RAM_ACCESS_VIOLATION	-	-	-
							FPU_OVER_FLOW	FPU_UNDER_FLOW								

3.5.2 Bootrom

For bootrom similarities and differences between F28002x, F280015x and F280013x see [Table 3-7](#) and [Table 3-8](#).

Table 3-7. Bootloaders and GPIO Assignment Comparison

Bootloader	Option	BOOTDEFx	F28002x	F280015x	F280013x
Parallel	0	0x00	D0-D7=GPIO0 to GPIO7; DSP=GPIO16; Host=GPIO29	D0-D7=GPIO(0,1,3,4,5,7,28,29); DSP=GPIO224; Host=GPIO242	
	1	0x20	D0-D7=GPIO0 to GPIO7; DSP=GPIO16; Host=GPIO11	D0-D7=GPIO0 to GPIO7; DSP=GPIO12; Host=GPIO13	
	2	0x40	n/a	D0-D7=GPIO0 to GPIO7; DSP=GPIO16; Host=GPIO29	
SCIA	0	0x01	TX=GPIO29; RX=GPIO28		
	1	0x21	TX=GPIO16; RX=GPIO17	TX=GPIO1; RX=GPIO0	
	2	0x41	TX=GPIO8; RX=GPIO9		
	3	0x61	TX=GPIO2; RX=GPIO3	TX=GPIO7; RX=GPIO3	
	4	0x81	TX=GPIO16; RX=GPIO3		
CAN	0	0x02	TX=GPIO4; RX=GPIO5	TX=GPIO7; RX=GPIO5	TX=GPIO4; RX=GPIO5
	1	0x22	TX=GPIO32; RX=GPIO33		
	2	0x42	TX=GPIO2; RX=GPIO3		
	3	0x62	n/a	TX=GPIO13; RX=GPIO12	
SPI	0	0x06	SIMO=GPIO2; SOMI=GPIO1; CLK=GPIO3; STE=GPIO5	SIMO=GPIO7; SOMI=GPIO1; CLK=GPIO3; STE=GPIO5	
	1	0x26	SIMO=GPIO16; SOMI=GPIO1; CLK=GPIO3; STE=GPIO0		
	2	0x46	SIMO=GPIO8; SOMI=GPIO10; CLK=GPIO9; STE=GPIO11		
	3	0x66	SIMO=GPIO8; SOMI=GPIO17; CLK=GPIO9; STE=GPIO11	SIMO=GPIO16; SOMI=GPIO13; CLK=GPIO12; STE=GPIO29	
I2C	0	0x07	SDA=GPIO32; SCL=GPIO33	SDA=GPIO0; SCL=GPIO1	
	1	0x27	SDA=GPIO0; SCL=GPIO1	SDA=GPIO32; SCL=GPIO33	
	2	0x47	SDA=GPIO10; SCL=GPIO8	SDA=GPIO5; SCL=GPIO4	

Table 3-7. Bootloaders and GPIO Assignment Comparison (continued)

Bootloader	Option	BOOTDEFx	F28002x	F280015x	F280013x
MCAN	0	0x08	n/a	TX=GPIO4; RX=GPIO5	n/a
	1	0x28	n/a	TX=GPIO1; RX=GPIO0	n/a
	2	0x48	n/a	TX=GPIO13; RX=GPIO12	n/a
	3 (DEBUG- Send Test)	0x88	n/a	TX=GPIO4; RX=GPIO5	n/a
	4 (DEBUG- Send Test)	0xA8	n/a	TX=GPIO1; RX=GPIO0	n/a
	5 (DEBUG- Send Test)	0x68	n/a	TX=GPIO13; RX=GPIO12	n/a

Table 3-8. Boot Modes Comparison

Boot Mode	Option	BOOTDEFx	F28002x	F280015x	F280013x
Flash	0	0x03	Entry=0x00080000; Bank/Sector=0/0	Entry=0x00080000; Bank/Sector=0/0	
	1	0x23	Entry=0x00084000; Bank/Sector=0/4	Entry=0x00088000; Bank/Sector=0/32	
	2	0x43	Entry=0x00088000; Bank/Sector=0/8	Entry=0x0008FFF0; Bank/Sector=0/63	
	3	0x63	Entry=0x0008EFF0; Bank/Sector=0/14	Entry=0x00090000; Bank/Sector=0/64	
	4	0x83	-	Entry=0x00098000; Bank/Sector=0/96	
	5	0xA3	-	Entry=0x0009FFF0; Bank/Sector=0/127	
Secure Flash	0	0x0A	-	Entry=0x00080000; Bank/Sector=0/0	
	1	0x2A	-	Entry=0x00088000; Bank/Sector=0/32	
	2	0x4A	-	Entry=0x0008FFF0; Bank/Sector=0/63	
	3	0x6A	-	Entry=0x00090000; Bank/Sector=0/64	
	4	0x8A	-	Entry=0x00098000; Bank/Sector=0/96	
Wait	0	0x04	Watchdog enabled		
	1	0x24	Watchdog disabled		
RAM	0	0x05	Entry=0x00000000		

3.5.3 CLB and Motor Control Libraries

F280013x device does not have CLB block hence user can not use any CLB related function on this device.

3.5.4 AGPIO

F280013x and F280015x devices have 11 AGPIO channels that support both GPIO and analog functionality on a single pin. AGPIO functionality is not available on F28002x. There is a performance impact to ADC channels that share a pin with GPIO, which is described in [Table 3-3](#).

3.5.4.1 AGPIO Filter

In order to help reduce noise for the analog portion of AGPIO pins, a configurable filter is available. This filter can be enabled and configured in two banks. For more details on the two groups of AGPIO filters and configuration options available, see the AGPIO and ANALOG_SUBSYS_REGS sections of each device-specific TRM.

3.5.4.2 Digital Inputs and Outputs on ADC Pins (AGPIOs)

Some GPIOs on this device are multiplexed with analog pins. These are also referred to as AGPIOs. Unlike AIOs, AGPIOs have full input and output capability.

By default the AGPIOs are not connected and have to be configured. [Table 3-9](#) shows how to configure the AGPIOs.

Table 3-9. AGPIO Configuration

AGPIOTRLA.GPIOy (Default = 0)	GPAXMSEL.GPIOy (Default = 1)	Pin Connected To:	
		ADC	GPIOy
0	0	-	Yes
0	1	- ⁽¹⁾	- ⁽¹⁾
1	0	-	Yes
1	1	Yes	-

(1) By default there are no signals connected to AGPIO pins. One of the other rows in the table must be chosen for pin functionality.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AGPIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AGPIOs if adjacent channels are being used for analog functions.

3.6 Power Management

The F28002x and F280013x devices have similar options for power, with F280015x and F280013x-64VPM having an additional power option. F28002x and F280013x devices only support single-rail (3.3 V) with the internal LDO VREG providing the 1.2 V rail. F280015x and F280013x-64VPM have an additional option to supply the 1.2V rail externally, but can still be supplied internally as in the other two devices. This section describes the power management differences and similarities between the three devices.

3.6.1 LDO/VREG

F28002x and F280013x (for non 64VPM packages) support only internal VREG and have no VREGENZ pin. The VREGENZ pin is replaced with different functions.

F280015x and 64VPM F280013x have a VREGENZ pin, allowing support of both internal VREG and external source.

3.6.2 POR/BOR

There are no functional changes for the POR and BOR.

3.6.3 Power Consumption

There is not a significant difference in power consumption between F280013x, F280015x and F28002x if a similar system operating frequency is chosen, the same number of peripherals are being utilized, and internal VREG is being used for all three devices. However, since the F280015x and F280013x (F280013x-64VPM package only) devices have the option to supply VREG externally, they have the capability to be more power efficient.

One additional consideration is that F280015x and F280013x have a maximum frequency of 120 MHz. This increases the power requirements when compared to F28002x, whose maximum frequency is 100 MHz.

3.7 Memory Module Changes

RAM and FLASH memories in F28002x device have similarities to and differences from F280015x and F280013x devices. [Table 3-10](#) summarizes the memory features including error-checking and security assignment.

Table 3-10. RAM and FLASH memory changes

Memory		F28002x			F280015x and F280013x		
		Size	Parity/ ECC	Secured	Size	Parity/ ECC	Secured
RAM	Dedicated(M0,M1)	4KB	ECC	No	4KB	ECC	No
	Local Shared(LS0-LS7)	16KB	DCSM- controlled	Yes	32KB	Parity	DCSM- controlled
	Global Shared(GS0-GS3)	4KB (GS0)	Parity	No	-	-	-
	Message	-	-	-	-	-	-
	Total RAM	24KB			36KB		
FLASH	Per Bank	128KB(1 bank)	ECC	DCSM- controlled	256KB(1 bank)	ECC	DCSM- controlled
	Total FLASH	128KB			256KB		

3.8 GPIO Multiplexing Changes

Table 3-12 outlines the differences and similarities that exist in the GPIO mux between F28002x, F280015x and F280013x.

Table 3-11. PIE Channel Legend

Color	Description
	Mux function applicable for all four devices
	Mux function applicable for F280013x and F280015x only
	Mux function applicable for F280015x only
	Mux function applicable for F280015x and F28002x only
	Mux function applicable for F28002x only

Table 3-12. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	EPWM1_A	CANA_RX	OUTPUTXB AR7	SCIA_RX	I2CA_SDA	SPIA_STE	FSIRXA_CLK	MCAN_RX	CLB_OUTPUTX BAR8	EQEP1_INDEX		EPWM3_A HIC_BASESEL1	
GPIO1	EPWM1_B			SCIA_TX	I2CA_SCL	SPIA_SOMI	EQEP1_STROB E	MCAN_TX	CLB_OUTPUTX BAR7	HIC_A2	FSITXA_TDM_ D1	EPWM3_B HIC_D10	
GPIO2	EPWM2_A			OUTPUTXBAR1	PMBUSA_SDA	SPIA_SIMO	SCIA_TX	FSIRXA_D1	I2CB_SDA	HIC_A1	CANA_TX	EPWM4_A HIC_D9	
GPIO3	EPWM2_B	OUTPUTXBAR2		OUTPUTXBAR2	PMBUSA_SCL	SPIA_CLK	SCIA_RX	FSIRXA_D0	I2CB_SCL	HIC_NOE	CANA_RX	EPWM4_B HIC_D4	
GPIO4	EPWM3_A	I2CA_SCL	MCAN_TX	OUTPUTXBAR3	CANA_TX	SPIB_CLK	EQEP2_STROB E	FSIRXA_CLK	CLB_OUTPUTX BAR6	HIC_BASESEL2	SPIA_SOMI	EPWM1_A HIC_NWE	
GPIO5	EPWM3_B	I2CA_SDA	OUTPUTXBAR3	MCAN_RX	CANA_RX	SPIA_STE	FSITXA_D1	CLB_OUTPUTX BAR5	SCIA_RX	HIC_A7	HIC_D4	EPWM1_B HIC_D15	
GPIO6	EPWM4_A	OUTPUTXBAR4	SYNCOUT	EQEP1_A		SPIB_SOMI	FSITXA_D0		FSITXA_D1	HIC_NBE1	CLB_OUTPUTX BAR8	EPWM2_A HIC_D14	
GPIO7	EPWM4_B	EPWM2_A	OUTPUTXBAR5	EQEP1_B		SPIA_SIMO SPIB_SIMO	FSITXA_CLK	CLB_OUTPUTX BAR2	SCIA_TX	HIC_A6	CANA_TX	EPWM2_B HIC_D14	
GPIO8	EPWM5_A		ADCSOAO	EQEP1_STROB E	SCIA_TX	SPIA_SIMO	I2CA_SCL	FSITXA_D1	CLB_OUTPUTX BAR5	HIC_A0	FSITXA_TDM_ CLK	HIC_D8	
GPIO9	EPWM5_B	SCIB_TX	OUTPUTXBAR6	EQEP1_INDEX	SCIA_RX	SPIA_CLK		FSITXA_D0	LINB_RX	HIC_BASESEL0	I2CB_SCL	HIC_NRDY	
GPIO10	EPWM6_A		ADCSOCBO	EQEP1_A	SCIB_TX	SPIA_SOMI	I2CA_SDA	FSITXA_CLK	LINB_TX	HIC_NWE	FSITXA_TDM_ D0		
GPIO11	EPWM6_B	CANA_RX	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_STE	FSIRXA_D1	LINB_RX	EQEP2_A	SPIA_SIMO	HIC_D6	HIC_NBE0	
GPIO12	EPWM7_A		MCAN_RX	EQEP1_STROB E	SCIB_TX	PMBUSA_CTL	FSIRXA_D0	LINB_TX	SPIA_CLK	CANA_RX	HIC_D13	HIC_INT	
GPIO13	EPWM7_B		MCAN_TX	EQEP1_INDEX	SCIB_RX	PMBUSA_ALER T	FSIRXA_CLK	LINB_RX	SPIA_SOMI	CANA_TX	HIC_D11	HIC_D5	
GPIO14		SCIB_TX		I2CB_SDA	OUTPUTXBAR3	PMBUSA_SDA	SPIB_CLK	EQEP2_A	LINB_TX	EPWM3_A	CLB_OUTPUTX BAR7	HIC_D15	
GPIO15		SCIB_RX		I2CB_SCL	OUTPUTXBAR4	PMBUSA_SCL	SPIB_STE	EQEP2_B	LINB_RX	EPWM3_B	CLB_OUTPUTX BAR6	HIC_D12	

Table 3-12. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO16	SPIA_SIMO		OUTPUTXBAR7	EPWM5_A	SCIA_TX		EQEP1_STROBE	PMBUSA_SCL	XCLKOUT	EQEP2_B	SPIB_SOMI	HIC_D1	
GPIO17	SPIA_SOMI		OUTPUTXBAR8	EPWM5_B	SCIA_RX		EQEP1_INDEX	PMBUSA_SDA	CANA_TX		EPWM6_A	HIC_D2	
GPIO18_X2	SPIA_CLK	SCIB_TX	CANA_RX	EPWM6_A	I2CA_SCL		EQEP2_A	PMBUSA_CTL	XCLKOUT	LINB_TX	FSITXA_TDM_CLK	HIC_INT	X2
GPIO19_X1	SPIA_STE	SCIB_RX	CANA_TX	EPWM6_B	I2CA_SDA		EQEP2_B	PMBUSA_ALERT	CLB_OUTPUTXBAR1	LINB_RX	FSITXA_TDM_D0	HIC_NBE0	X1
GPIO20	EQEP1_A				SPIA_SIMO		MCAN_TX		I2CA_SCL			SCIC_TX	
GPIO21	EQEP1_B		CANA_RX		SPIA_SOMI		MCAN_RX		I2CA_SDA			SCIC_RX	
GPIO22	EQEP1_STROBE		SCIB_TX		SPIB_CLK		SCIC_TX	CLB_OUTPUTXBAR1	LINB_TX	HIC_A5	EPWM4_A	HIC_D13	
							LINA_TX						
GPIO23	EQEP1_INDEX		SCIB_RX		SPIB_STE		SCIC_RX		LINB_RX	HIC_A3	EPWM4_B	HIC_D11	
							LINA_RX						
GPIO24	OUTPUTXBAR1	EQEP2_A	SPIA_STE	EPWM8_A	SPIB_SIMO		LINB_TX	PMBUSA_SCL	SCIA_TX	ERRORSTS		HIC_D3	
GPIO25	OUTPUTXBAR2	EQEP2_B		EQEP1_A	SPIB_SOMI		FSITXA_D1	PMBUSA_SDA	SCIA_RX		HIC_BASESEL0		
GPIO26	OUTPUTXBAR3	EQEP2_INDEX		OUTPUTXBAR3	SPIB_CLK		FSITXA_D0	PMBUSA_CTL	I2CA_SDA		HIC_D0	HIC_A1	
GPIO27	OUTPUTXBAR4	EQEP2_STROBE		OUTPUTXBAR4	SPIB_STE		FSITXA_CLK	PMBUSA_ALERT	I2CA_SCL		HIC_D1	HIC_A4	
GPIO28	SCIA_RX		EPWM7_A	OUTPUTXBAR5	EQEP1_A		EQEP2_STROBE	SCIC_TX	SPIB_CLK	ERRORSTS	I2CB_SDA	HIC_NOE	
								LINA_TX					
GPIO29	SCIA_TX		EPWM7_B	OUTPUTXBAR6	EQEP1_B		EQEP2_INDEX	SCIC_RX	SPIB_STE	ERRORSTS	I2CB_SCL	HIC_NCS	AUXCLKIN
								LINA_RX					
GPIO30	CANA_RX		SPIB_SIMO	OUTPUTXBAR7	EQEP1_STROBE		FSIRXA_CLK	MCAN_RX	EPWM1_A		HIC_D8		
GPIO31	CANA_TX		SPIB_SOMI	OUTPUTXBAR8	EQEP1_INDEX		FSIRXA_D1	MCAN_TX	EPWM1_B		HIC_D10		
GPIO32	I2CA_SDA	EQEP1_INDEX	SPIA_CLK	EPWM4_B	SCIC_TX		FSIRXA_D0	CANA_TX	PMBUSA_SDA	ADCSOCBO		HIC_INT	
			SPIB_CLK		LINA_TX								
GPIO33	I2CA_SCL		SPIB_STE	OUTPUTXBAR4	SCIC_RX		FSIRXA_CLK	CANA_RX	EQEP2_B	ADCSOCAO		HIC_D0	
					LINA_RX								
GPIO34	OUTPUTXBAR1				PMBUSA_SDA					HIC_NBE1	I2CB_SDA	HIC_D9	
GPIO35	SCIA_RX	SPIA_SOMI	I2CA_SDA	CANA_RX	PMBUSA_SCL	SCIC_RX	EQEP1_A	PMBUSA_CTL	EPWM5_B		HIC_NWE	TDI	
						LINA_RX							
GPIO37	OUTPUTXBAR2	SPIA_STE	I2CA_SCL	SCIA_TX	CANA_TX	SCIC_TX	EQEP1_B	PMBUSA_ALERT	EPWM5_A		HIC_NRDY	TDO	
						LINA_TX							
GPIO39					MCAN_RX	FSIRXA_CLK	EQEP2_INDEX		CLB_OUTPUTXBAR2	SYNCOUT	EQEP1_INDEX	HIC_D7	
GPIO40	SPIB_SIMO			EPWM2_B	PMBUSA_SDA	FSIRXA_D0	SCIB_TX	EQEP1_A	LINB_TX		HIC_NBE1	HIC_D5	
GPIO41	EPWM7_A			EPWM2_A	PMBUSA_SCL	FSIRXA_D1	SCIB_RX	EQEP1_B	LINB_RX	HIC_A4	SPIB_SOMI	HIC_D12	
GPIO42		LINA_RX	OUTPUTXBAR5	PMBUSA_CTL	I2CA_SDA	SCIC_RX		EQEP1_STROBE	CLB_OUTPUTXBAR3		HIC_D2	HIC_A6	
GPIO43			OUTPUTXBAR6	PMBUSA_ALERT	I2CA_SCL	SCIC_TX	PMBUSA_ALERT	EQEP1_INDEX	CLB_OUTPUTXBAR4		HIC_D3	HIC_A7	
GPIO44			OUTPUTXBAR7	EQEP1_A	PMBUSA_SDA	FSITXA_CLK	PMBUSA_CTL	CLB_OUTPUTXBAR3		HIC_D7		HIC_D5	

Table 3-12. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO45			OUTPUTXBAR8			FSITXA_D0	PMBUSA_ALERT	CLB_OUTPUTXBAR4				HIC_D6	
GPIO46			LINA_TX	MCAN_TX		FSITXA_D1	PMBUSA_SDA					HIC_NWE	
GPIO48			CANA_TX	MCAN_TX	SCIA_TX		PMBUSA_SDA						
GPIO49			CANA_RX	MCAN_RX	SCIA_RX		LINA_RX						
GPIO224	AIO224			OUTPUTXBAR3	SPIA_SIMO		EPWM1_A	CANA_TX	EQEP1_A		SCIC_TX	HIC_A3	
AIO225												HIC_NWE	
GPIO226	AIO226		LINA_RX	EPWM6_A	SPIA_CLK		EPWM1_B		EQEP1_STROBE		SCIC_RX	HIC_A1	
GPIO227	AIO227	I2CB_SCL		EPWM3_A	OUTPUTXBAR1	EPWM2_B						HIC_NBE0	
GPIO228	AIO228			ADCSOCAO	CANA_TX	SPIA_SOMI		EPWM2_B	EQEP1_B			HIC_A0	
GPIO230	AIO230	I2CB_SDA		EPWM3_B	CANA_RX	EPWM2_A	I2CA_SDA	PMBUSA_SCL				HIC_BASESEL2	
AIO231												HIC_BASESEL1	
AIO232												HIC_BASESEL0	
AIO233												HIC_A4	
AIO237												HIC_A6	
AIO238												HIC_NCS	
AIO239												HIC_A5	
AIO241												HIC_NBE1	
GPIO242	AIO242			OUTPUTXBAR2	SPIA_STE		EPWM4_A	CANA_RX	EQEP1_INDEX			HIC_A2	
AIO244												HIC_A7	
AIO245												HIC_NOE	

3.9 Analog Multiplexing Changes

Table 3-14 outlines the differences and similarities that exist in the analog mux between F280013x, F280015x and F28002x for the 80-Pin PN, 64-Pin PM, and 48-Pin PT/PHP packages. The legend for the table is Table 3-13.

Table 3-13. Mux Legend

Color	Description
	Mux function common for all three devices
	Mux function applicable only for F28002x only
	Mux function applicable only for F280013x and F280015x only

Table 3-14. F28002x, F280015x and F280013x 64-Pin PM and 48-Pin PT/PHP Analog Mux Table Differences

(F28002x Pin Name)	Package Pin				ADC		Comparator Subsystem (MUX)				AIO Input
	80 PN	64 PM	48 PT	48 PHP	A	C	High Positive	High Negative	Low Positive	Low Negative	
VREFHI	20	16	12	12							
VREFLO	21	17	13	13	A13	C13					
Analog Group 1							CMP1				
(A6) A6/GPIO228	10	6	4	4	A6	-	CMP1 (HPMXSEL=2)		CMP1 (LPMXSEL=2)		AIO228 GPIO228
(A2/C9) A2/C9/GPIO224	13	9	6	6	A2	C9	CMP1 (HPMXSEL=0)		CMP1 (LPMXSEL=0)		AIO224 GPIO224
(A15/C7) A15/C7	14	10	7	7	A15	C7	CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP1 (LNMXSEL=0)	AIO233
(A11/C0) A11/C0	16	12	8	8	A11	C0	CMP1 (HPMXSEL=1)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=1)	CMP1 (LNMXSEL=1)	AIO237
(A1) A1	18	14	10	10	A1	-	CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		AIO232
Analog Group 2							CMP2				
(A10/C10) A10/C10/GPIO230	29	25	21	21	A10	C10	CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP2 (LNMXSEL=0)	AIO230 GPIO230
Analog Group 3							CMP3				
(C6) C6/GPIO226	11	7	4	4	-	C6	CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		AIO226 GPIO226
(A3/C5/VDAC) A3/C5/GPIO242	12	8	5	5	A3	C5	CMP3 (HPMXSEL=3) CMP3 (HPMXSEL=5)	CMP3 (HNMXSEL=0)	CMP3 (LPMXSEL=3) CMP3 (LPMXSEL=5)	CMP3 (LNMXSEL=0)	AIO242 GPIO242

Table 3-14. F28002x, F280015x and F280013x 64-Pin PM and 48-Pin PT/PHP Analog Mux Table Differences (continued)

(F28002x Pin Name) F280015x and F280013x Pin Name	Package Pin				ADC		Comparator Subsystem (MUX)				AIO Input
	80 PN	64 PM	48 PT	48 PHP	A	C	High Positive	High Negative	Low Positive	Low Negative	
(A14/C4) A14/C4	15	11	7	-	A14	C4	CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO239
(A5/C2) A5/C2	17	13	9	9	A5	C2	CMP3 (HPMXSEL=1) CMP2 (HPMXSEL=5)	CMP3 (HNMXSEL=1)	CMP3 (LPMXSEL=1) CMP2 (LPMXSEL=5)	CMP3 (LNMXSEL=1)	AIO244
(A0/C15) A0/C15	19	15	11	11	A0	C15	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO231
Analog Group 4							CMP4				
(A7/C3) A7/C3	23	19	15	15	A7	C3	CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	AIO245
Combined Analog Group 2/4							CMP2/4				
(A12/C1) A12/C1	22	18	14	14	A12	C1	CMP2 (HPMXSEL=1) CMP4 (HPMXSEL=2)	CMP2 (HNMXSEL=1)	CMP2 (LPMXSEL=1) CMP4 (LPMXSEL=2)	CMP2 (LNMXSEL=1)	AIO238
(A8/C11) A8/C11	24	20	16	16	A8	C11	CMP2 (HPMXSEL=4) CMP4 (HPMXSEL=4)		CMP2 (LPMXSEL=4) CMP4 (LPMXSEL=4)		AIO241
(A4/C14) A4/C14	27	23	19	19	A4	C14	CMP2 (HPMXSEL=0) CMP4 (HPMXSEL=3)	CMP4 (HNMXSEL=0)	CMP2 (LPMXSEL=0) CMP4 (LPMXSEL=3)	CMP4 (LNMXSEL=0)	AIO225
(A9/C8) A9/C8/GPIO227	28	24	20	20	A9	C8	CMP2 (HPMXSEL=2) CMP4 (HPMXSEL=0)		CMP2 (LPMXSEL=2) CMP4 (LPMXSEL=0)		AIO227 GPIO227
Other Analog											
A16/C16/GPIO28	4	2	2	2	A16	C16					GPIO28
A17/C17/GPIO20	33	27	-	22	A17	C17					GPIO20
A18/C18/GPIO21	34	28	-	-	A18	C18					GPIO21
A19/C19/GPIO13	35	29	23	23	A19	C19					GPIO13
A20/C20/GPIO12	36	30	24	24	A20	C20					GPIO12
TempSensor	-	-	-	-	-	C12					-

4 Application Code Migration From F28002x to F280015x or F280013x

The following section describes code changes when migrating from F28002x to either F280015x or F280013x. Software examples for the new features in F280015x and F280103x are also discussed in this section.

4.1 C2000Ware Header Files

Header files for F280013x, F280015x and F28002x devices are available in C2000Ware under the device_support sub directory.

4.2 Linker Command Files

Linker command files for F280013x, F280015x and F28002x devices are available in C2000Ware under the device_support sub directory. F28002x, F280015x and F280013x have to be compiled to the Embedded Application Binary Interface (EABI) format. Section names would also need to conform to the EABI standard.

4.3 C2000Ware Examples

C2000Ware has examples specific for F280013x, F280015x and F28002x devices.

5 Specific Use Cases Related to F280015x and F280013x New Features

This section outlines the new examples in C2000Ware for the F280015x and F280013x devices to support the new features on F280015x and F280013x that do not exist on F28002x/F28004x.

5.1 EPG

C2000Ware has examples that demonstrate the functionality of the EPG module.

6 EABI Support

F28002x, F280015x and F280013x devices use the Embedded Application Binary Interface (EABI) format for the binary executable output. All F28002x, F280015x and F280013x libraries supplied by TI will be released as EABI. Future F280015x and F280013x libraries created by customers should be generated and compiled as EABI format as well.

6.1 Flash API

F28002x, F280015x and F280013x all have one Flash bank. Compared to the F28002x Flash API library (Flash_API_F28002x_FPU32.lib), the F280013x and F280015x Flash API is enhanced to return an error when an invalid address is provided for erase, blank-check, program and verify functions. Also, the F280013x and F280015x Flash API is enhanced to return an error when an invalid programming mode is provided for program operation. Fapi_getLibraryInfo() in FlashAPI_F280013x_FPU32.lib and FlashAPI_F280015x_FPU32.lib returns the Flash API minor version as TBD (F28002x Flash API returns 57 as the API minor version). F28002x, F280015x and F280013x Flash API libraries are compiled for EABI format. Note that F28002x, F280015x and F280013x have the same Bank0 memory map but different sector sizes. F280013x and F280015x have small sector size to provide better granularity. These features are summarized in [Table 6-1](#).

Table 6-1. Flash API Differences

Feature	F28002x	F280015x	F280013x
Library Name	FlashAPI_F28002x_FPU32.lib	FlashAPI_F280015x_FPU32.lib	FlashAPI_F280013x_FPU32.lib
Library Executable Output	EABI		
Erase, Blank-check, Program and Verify	Operation on one bank		
Flash Wait States	4 (100MHz)	2 (120MHz)	
FlashAPI Major Version	1	2	
FlashAPI Minor Version	57	0	

7 References

- Texas Instruments: [TMS320F28002x Microcontrollers Technical Reference Manual](#)
- Texas Instruments: [TMS320F28002x Microcontrollers Data Sheet](#)
- Texas Instruments: [TMS320F280013x Microcontrollers Technical Reference Manual](#)
- Texas Instruments: [TMS320F280013x Microcontrollers Data Sheet](#)
- Texas Instruments: [TMS320F280015x Microcontrollers Technical Reference Manual](#)
- Texas Instruments: [TMS320F280015x Microcontrollers Data Sheet](#)
- Texas Instruments: [TMS320F2838x Microcontrollers Technical Reference Manual](#)

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