User's Guide

AM69 Processor Starter Kit User's Guide

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1 Introduction

1.1 Inside the Box

The SK-AM69 Processor Starter Kit includes:

- AM69 Starter Kit EVM
- Micro-SD Card
- USB Cable (Type-A to Micro-B) for serial terminal/logging
- Paper Card with Start-up Link/Support Information

The EVM is powered from a Type-C power supply, but the power supply is *not included*. For more information on the types of supplies recommended with the EVM, see Table 2-1.

The EVMs orderable part number is: SK-AM69

1.2 Key Features and Interfaces

- Processor
  - Texas Instruments AM69 Super-Set device
- Optimized Power Management Solution
  - Dynamic Voltage Scaling
  - Multiple Clock and Power Domains
- Memory
  - 4x 8GByte LPDDR4 DRAM (2133 MHz)
  - 512 Mb Non-Volatile Flash, Octal-SPI NOR
  - 32GB eMMC, version 5.1 compliant
  - Multimedia Card (MMC)/Secure Digital Card (Micro SD) Cage, UHS-I
- USB
  - USB3.1 (Gen1) Hub to 3x Type A (Host)
  - USB3.1 (Gen1) Type C (DFP modes)
  - USB2.0 Micro B (for Quad UART-over-USB Transceiver)
- Display
  - VESA Display Port (v1.4), supports 4K UHD with MST support
  - DVI (v1.0) via HDMI Type A, supports 1080p
- Wired Network
  - Gigabit Ethernet (RJ45 Connector)
  - 4x CAN-FD Headers (1x3)
- Camera Interfaces
  - 2x 22-Pin Flex Cable Interface (CSI-4L)
  - 2x 40-pin High Speed Connector (dual CSI-4L, I2C, GPIO, and so forth)
- Expansion/Add-on
  - M.2 Key M Interface (PCIe/Gen3 x 2 Lane)
  - M.2 Key E Interface (PCIe/Gen3 x 1 Lane)
  - Standard x8 PCIe Interface (Gen3 x 4 Lane)
  - 60-pin ENET expansion header SGMII Interface
  - 40-pin Header (2x20) (I2C, SPI, UART, I2S, GPIO, PWM, and so forth)
  - Fan Header (12 V)
- User Control/Indication
  - Pushbuttons (Reset, Power/User Defined)
  - LEDs (Power, User Defined, Serial Port)
  - User Configuration (Boot Mode)
  - On board Emulator Support (XDS110) with optional external support (20-pin Header)
- REACH and RoHS Compliant
- EMI/EMC Radiation Compliant

1.3 Thermal Compliance

There is elevated heat on the processor/heatsink, use caution particularly at elevated ambient temperatures!

Although the processor/heatsink is not a burn hazard, caution should be used when handling the SK due to increased heat in the area of the heatsink.

	Caution	Caution Hot surface. Contact may cause burns. Do not touch!

1.4 Electrostatic Discharge (ESD) Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity-controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory condition and the applied standard will be as per ENC IEC 61326-1:2021.

2 User Interfaces

Figure 2-1 and Figure 2-2 identify the key user interfaces on the AM69 Processor SK (top and bottom view).

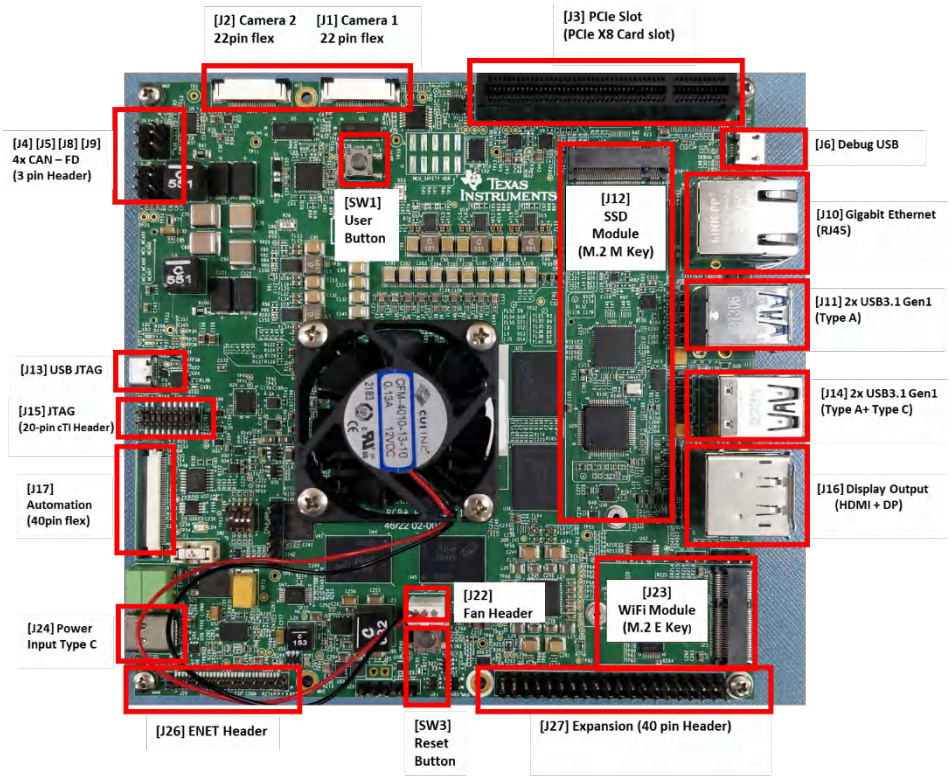

Figure 2-1. User Interfaces (Top)

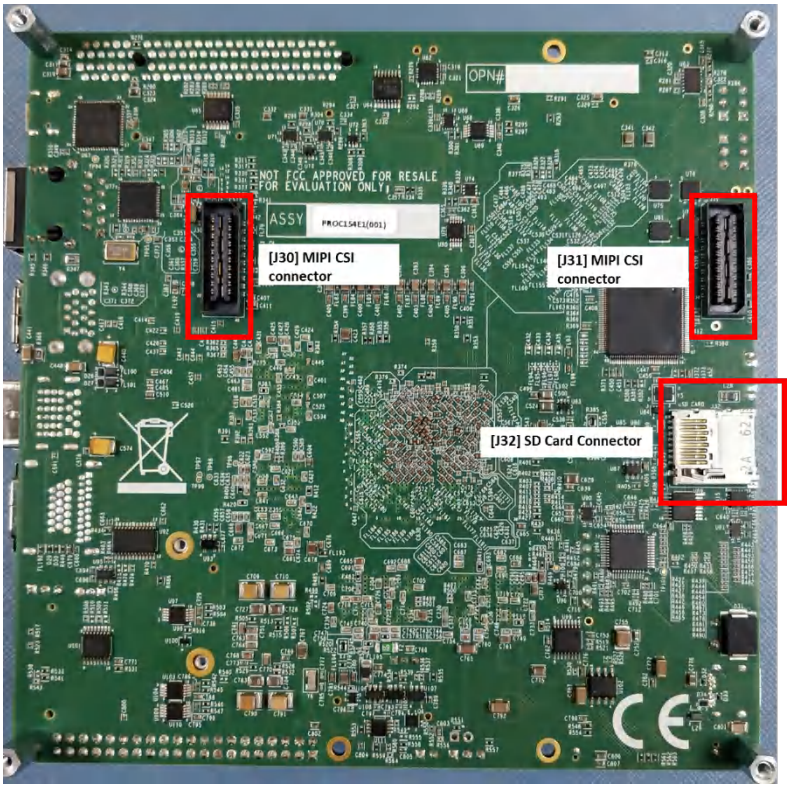

Figure 2-2. User Interfaces (Bottom)

2.1 Power Input

A power supply is not included with the SK and must be purchased separately.

External Power Supply or Power Accessory Requirements:

- Nominal Output Voltage: 5-20VDC
- Maximum Output Current: 5000 mA
- Efficiency Level V

Note

TI recommends using an external power supply or power accessory that complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE, and so forth.

2.1.1 Power Input [J24] With LED for Status [LD4]

The dedicated power input connector is a USB Type C connector [J24] with Power Delivery 3.0 support. The input can accept wide range of input voltages (5 V to 20 V). The exact power required for the SK is largely dependent on the application and the connected peripherals. The recommended supplies are listed in Table 2-1. These supplies are 20 V Type C supplies capable of supplying up to 100W of power (20VDC at 5A). The minimum supply required is 60W supply (20VDC at 3A). However, a 60W supply may limit available processing with processor as well as limit some of the available peripherals. USB and PCIe peripherals can require significant power and this is a reason higher wattage supply is recommended.

There are many USB Type C power supply manufactures and models available in the market, and it is not possible to test the SK with every combination.

Table 2-1 lists a few recommended supplies the SK has tested.

Table 2-1. Recommended External Power Supply

Manufacturer	Part #/Model #	Description	Ordering Information
Dell	450-AJWU	Dell USB-C 90 W AC Adapter	https://www.dell.com/en-in/work/shop/dell-usb-c-90-w-ac-adapter-with-1-meter-power-cord-india/apd/450-ajwu/pc-accessories
Asus	AC100-00(A20-100P1A)	ROG 100W USB-C Adapter	https://rog.asus.com/power-protection-gadgets/chargers-and-adapters/rog-100w-usb-c-adapter-model/spec/
GlobTek, Inc.	TR9CZ3000USBCG2R6BF2	AC/DC DESKTOP ADAPTER 5V-20V 60W	1939-1794-ND [Digikey part#]
Qualtek	QADC-65-20-08CB	AC/DC DESKTOP ADAPTER 20V 65W	Q1251-ND [Digikey part#]

2.1.2 Power Budget Considerations

The exact power required for the SK is largely dependent on the application, usage of the on-board peripherals, and power needs of add-on devices. Table 2-2 shows the designs power allocations. (Again, the input supply must be capable of supplying the power needs for your application.)

Table 2-2. Power Supply Allocation

Function	Power	Description
Processor Core	Up to 50W	Processor, Memory
On-board Peripherals	Up to 3W	SD card, Ethernet, Logic, and so forth
USB Port(s)	Up to 19W	USB Hub Type A Ports (2.8A at 5V) Type C Port (1.5A at 5V)
Camera Ports	Up to 2W	Cam Ports (0.5A at 3.3V)
Expansion Interface(s)	Up to 40W	M.2 Type E (1A at 3.3V) M.2 Type M (3A at 3.3V) PCIe Card Slot (2A at 12V, 3A at 3.3V) 40p Expansion(2A at 3.3V,1.5A at 5V)
Display(s)	Up to 3W	HDMI Transceiver HDMI Panel(55mA at 5V) DP Panel (0.5A at 3.3V)

2.2 User Inputs

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.2.1 Board Configuration Settings [SW2]

Dip Switch [SW2] is used to configure different options available on the SK, including processor boot mode.

Table 2-3. Processor Bootmode Settings [SW2 Switch 1-3]

Processor Boot Source	SW2.1	SW2.2	SW2.3
MicroSD Card [J32]	OFF	OFF	OFF
Non-Volatile Flash (xSPI)	OFF	OFF	ON
eMMC	ON	ON	OFF
Reserved	OFF	ON	ON
UART (for Flashing)	ON	OFF	ON
No Boot (JTAG/Emulator)	ON	OFF	OFF

Table 2-3. Processor Bootmode Settings [SW2 Switch 1-3] (continued)

Processor Boot Source	SW2.1	SW2.2	SW2.3
Ethernet[J10]	OFF	ON	OFF

2.2.2 Reset Pushbutton [SW3]

When pressed [SW3], the SK is issued a Power-On (Cold) Reset, and is held in reset until the button is released.

If the pushbutton is held longer than 5 seconds, the system will power down. The system can be restarted by either pressing the User Pushbutton [SW1] or by cycling power to the board.

2.2.3 User Pushbutton [SW1] With User LED Indication [LD5]

The pushbutton [SW1] can be used for several different functions.

Function 1: System Wake from Shutdown. After software-initiated power down (using WKUP_GPIO0_69), pressing pushbutton [SW1] will re-enable and boot the SK.

Function 2: Power Management Enable. The pushbutton [SW1] is connected with Power Management IC (nPWRON/ENABLE), and used for enabling the SOC supplies

Function 3: User Defined Input/Interrupt. The pushbutton [SW1] is connected with the processor (WKUP_GPIO0_82), and can be programmed for variety of user input/interrupt needs.

A red LED [LD5] is available as user indicator, and is controlled via the processor (WKUP_GPIO0_55).

2.3 Standard Interfaces

The EVM provides industry standard interfaces/connectors to connect a wide variety of peripherals. As these interfaces are standard, specific pin information is not provided in this document.

2.3.1 UART-Over-USB [J6] With LED for Status [LD1]

Four UART ports of the processor are interfaced with UART-over-USB transceiver. When the EVM's USB micro-B connector (J6) is connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Port(s) which can be used with any terminal emulation application. Virtual Com Port drivers for the transceiver (CP2108-B02-GM) can be obtained fromhttps://www.silabs.com/developers/usb-touart-bridge-vcp-drivers.

Once installed, the Host-PC will create four Virtual Com Ports. Depending on the other Host-PC resources available - the Virtual COM Ports not be located at COM1-4. However, they will remain in the same numerical order.

Table 2-4. UART to COM Port Mapping

AM69 UART	Host-PC COM Port
WKUP_UART0	COM 1
MCU_UART0	COM 2
UART8	COM 3
UART2	COM 4

The circuit is powered through BUS power, therefore the COM connection is not lost when the EVM power is removed. An LED [LD1] is used to indicate an active COM connection with Host-PC.

2.3.2 Gigabit Ethernet [J10] With Integrated LEDs for Status

A wired Ethernet network is supported on the base board via RJ45 cable interface [J10], and is compatible with IEEE 802.3 10BASETe,100BASE-TX, and 1000BASE-T specifications. The connector includes status indicators for link and activity.

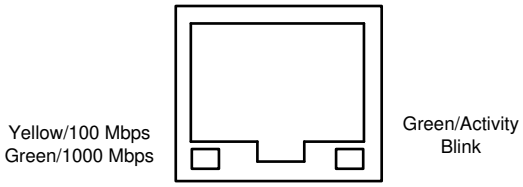

Figure 2-3. RJ45 LED Indicators [J10]

Power-Over-Ethernet (PoE) is not supported.

2.3.3 On-Board JTAG/Emulator [J13] with optional External Interface [J15]

The EVM supports an integrated XDS110 emulator for loading and debugging software. The EVM's USB micro-B connector [J13] is connected to a Host-PC using supplied USB cable (Type-A to Micro-B). The computer can use Texas Instruments Code Composer Studio (CCS) to establish a connection with the processor and download/debug software on the various processor core(s). The circuit is powered through BUS power. LEDs [LD12] [LD3] are used to indicate an active connection with Host-PC/processor.

Optionally – an external JTAG emulation/debugger can connect using a dedicated emulation connector [J15]. The connector is aligned with the Texas Instrument 20-pin CTI header standard (2x20, 1.27mm pitch), and is compatible with Texas Instruments modules (XDS110, XDS200, XDS560v2) and 3rd party modules.

Table 2-5. Expansion Header Pin Definition [J15]

Pin #	Pin Name	Description	Dir
1	TMS	Test Mode Select	Input
2	TRSTn	Test Reset	Input
3	TDI	Test Data Input	Input
4	TDIS	Target Disconnect	Output
5	Vref	Target Voltage Detect, 3.3V	Output
6	<No pin>	No pin/Key	
7	TDO	Test Data Output	Output
8	GND	Ground	
9	RTCK	Test Clock Return	Output
10	GND	Ground	
11	TCK	Test Clock	Input
12	GND	Ground	
13	EMU0	Emulation Pin 0	Bi-Dir
14	EMU1	Emulation Pin 1	Bi-Dir
15	RESETz	Target Reset	Input
16	GND	Ground	
17		Open	
18		Open	
19		Open	
20	GND	Ground	

Note

In the DIR column, output is to the JTAG module, input is from the JTAG module. Bi-Dir signals can be configured as either input or output.

2.3.4 USB3.1 Gen1 Interfaces [J11] [J14]

The EVM supports three USB3.1 Gen1 Type A ports [J11][J14], which operate in Host mode. The combined VBUS output for these ports is limited to 2.8A.

Also supported is one USB3.1 Gen1 Type C interface [J14], which can function as a DFP. The VBUS output for this port is limited to 1.5A. The EVM cannot be powered from this port.

2.3.5 Stacked DisplayPort and HDMI Type A [J16]

The EVM supports DisplayPort panel via standard DP cable interface [J16]. The interface supports resolutions to 4K UHD (3840x2160) including MST (Mutli-Stream Transport) for supporting multiple panels. A second display interface is supported via HDMI connector [J13], and supports resolutions up to 1080p (1920x1080). The interface is DVI, and therefore does not support the integrated audio. Both DisplayPort and HDMI interfaces can be used simultaneously.

2.3.6 PCIe Connector [J3] for PCIe Card Modules

The EVM supports a PCIe card slot for supporting full size PCIe cards. The slot accepts up to 8-Lane cards, but only 4-Lanes are supported. This expansion interface is used for a wide variety of peripherals, and supports the following interfaces: PCIe (4x) and I2C.

2.3.7 M.2 Key M Connector [J12] for SSD Modules

The EVM supports a Mini-PCIe M.2, Key M slot (2280) for expansion modules [J12]. This expansion interface is primarily used for Solid State Drives (SSD), and supports the following interfaces: PCIe (2x) and I2C.

2.3.8 M.2 Key E Connector [J23] for Wi-Fi Networking Modules

The EVM supports a Mini-PCIe M.2, Key E slot (2230) for expansion modules [J23]. This expansion interface is primarily used for BT/Wi-Fi modules, and supports the following interfaces: PCI Express (PCIe) (1x) and inter-integrated circuit (I2C).

Note

An example optional add-on Wireless Network module for this interface is the Intel M.2 Type E Wi-Fi/ 9260NGW.

2.3.9 MicroSD Card Cage [J32]

The EVM supports a micro-SD card cage. It supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a PUSH-PUSH connector, meaning you push to insert the card and push again to remove the card.

A MicroSD Card is included with the EVM.

2.4 Expansion Interfaces

The EVM supports expansion interfaces that have non-standard/custom pinouts. Each of those interfaces are introduced and specific pin information is provided.

2.4.1 Heatsink [ACC] With [J22] Fan Header

The heatsink supports cooling of the device at ambient temperatures which will be mounted on the processor. If your environment or use case requires additional cooling, a fan can be added to the Heatsink.

The fan connector is a 3-pin header (TE CONNECTIVITY, Part number 440054-3).

Table 2-6. Fan Header Pin Definition [J22]

Pin #	Pin Name	Description	Direction
1	<open>	Unconnected	N/A
2	12V	Main 12V supply	Output
3	GND	Ground	

2.4.2 CAN-FD Connector(s) [J4] [J5] [J8] [J9]

The EVM supports four (4x) CAN Bus interfaces.

Table 2-7. CAN-FD Interface Assignment

Connector Ref	Processor Resource
J4	MCU_CAN1
J5	CAN6
J8	MCU_CAN0
J6	CAN7

Each Controller Area Network (CAN) Bus interface is supported on a 3-pin, 2.54 mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards, and supports CAN and optimized CAN-FD performance up to 8 Mbps. Each includes CAN Bus end-point termination. If the SK is included in a network with more than two nodes, the termination my need to be adjusted.

Table 2-8. CAN-FD Header Pin Definition [J4][J5][J8][J9]

Pin #	Pin Name	Description	Direction
1	CAN-H	High-Level CAN Bus Line	Bi-Dir
2	GND	Ground	
3	CAN-L	Low-Level CAN Bus Line	Bi-Dir

2.4.3 Expansion Header [J27]

The EVM includes a 40-pin (2x20, 2.54mm pitch) expansion interface [J27]. The expansion connector supports variety of interfaces including: I2C, serial peripheral interface (SPI), I2S with Audio clock, UART, pulse width modulator (PWM), and GPIO. All signals on the interfaces are 3.3 V levels.

Table 2-9. Expansion Header Pin Definition [J27]

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
1	Power	Power,3.3 V	Output
2	Power	Power,5.0 V	Output
3	I2C_SDA	MCU I2CBus #0, Data (G34)	Bi-Dir
4	Power	Power,5.0 V	Output
5	I2C_SCL	MCU I2CBus #0, Clock (M35)	Bi-Dir
6	GND	Ground	
7	GP_CLK/GPIO	REFCLK0/WKUP_GPIO0_66 (N34)	Bi-Dir
8	UART_TXD	UART#5 Transmit (AG36)	Output
9	GND	Ground	
10	UART_RXD	UART#5 Receive (AJ33)	Input
11	GPIO	GPIO0_42 (AF34)	Bi-Dir
12	I2S_SCLK	McASP#1 ACLKX (AC34)	Bi-Dir
13	GPIO	GPIO0#36 (AC35)	Bi-Dir
14	GND	Ground	
15	GPIO	WKUP_GPIO0_49 (M33)	Bi-Dir
16	GPIO	GPIO0#3 (AF33)	Bi-Dir
17	Power	Power,3.3V	Output
18	GPIO	AUDIO_EXT_REFCLK0(AJ34)	Bi-Dir
19	SPI_MOSI	MCU SPI#1 Data 0 (J34)	Bi-Dir
20	GND	Ground	
21	SPI_MISO	MCU SPI#1 Data 1 (J35)	Bi-Dir
22	GPIO	WKUP_GPIO0_67 (M34)	Bi-Dir

Table 2-9. Expansion Header Pin Definition [J27] (continued)

Pin #	Pin Name	Description (TDA4VM Pin #)	Dir
23	SPI_SCLK	MCU SPI#1 Clock (H38)	Bi-Dir
24	SPI_CS0	MCU SPI #1 Chip Select 0 (J36)	Bi-Dir
25	GND	Ground	
26	SPI_CS1	MCU SPI #1 Chip Select 2 (K37)	Bi-Dir
27	ID_SDA	WKUP I2C #0 Data (N35)	Bi-Dir
28	ID_SCL	WKUP I2C #0 Clock (N33)	Bi-Dir
29	GPIO	WKUP_GPIO0_56 (M37)	Bi-Dir
30	GND	Ground	
31	GPIO	WKUP_GPIO0_57(M36)	Bi-Dir
32	PWM0	PWM3_A (AE35)	Output
33	PWM1	PWM0_A (AM37)	Output
34	GND	Ground	
35	I2S_FS	McASP #1 AFSX (AD33)	Bi-Dir
36	GPIO	GPIO0_41 (AJ36)	Bi-Dir
37	GPIO	GPIO0_27 (AJ37)	Bi-Dir
38	I2S_DIN	McASP #1 AXR0 (AD38)	Bi-Dir
39	GND	Ground	
40	I2S_DOUT	McASP #1 AXR4 (AL34)	Bi-Dir

2.4.4 Camera Interface, 22-Pin Flex Connectors [J1] [J2]

The EVM supports two (2) 22-pin flex (0.5mm pitch) connectors [J1][J2] for interfacing with camera modules. Each camera interface provides MIPI CSI-2interface (4Lane), Clock/Control signals, and power (3.3 V) to the camera.

To enable camera modules with same addressing to be used simultaneously, I2C mux is used to select each camera. The voltage level for Clock/Control signals is selectable between 1.8 V/3.3 V.

Table 2-10. Camera 0 Flex Pin Definition [J1]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI0_D0_N	CSIPort 0 Data Lane 0	Input
3	CSI0_D0_P	CSIPort 0 Data Lane 0	Input
4	GND	Ground	
5	CSI0_D1_N	CSIPort 0 Data Lane 1	Input
6	CSI0_D1_P	CSIPort 0 Data Lane 1	Input
7	GND	Ground	
8	CSI0_CLK_N	CSIPort 0 CLK	Input
9	CSI0_CLK_P	CSIPort 0 CLK	Input
10	GND	Ground	
11	CSI0_D2_N	CSIPort 0 Data Lane 2	Input
12	CSI0_D2_P	CSIPort 0 Data Lane 2	Input
13	GND	Ground	
14	CSI0_D3_N	CSIPort 0 Data Lane 3	Input
15	CSI0_D3_P	CSIPort 0 Data Lane 3	Input
16	GND	Ground	
17	CAM0_PWDN	Pwr-Dwn(IO expander)	Output
18	CAM0_AUX	AUX (WKUP_GPIO0_88)	Bi-Dir
19	GND	Ground	
20	I2C_SCL	I2C Clock #1, Mux 0	Output

Table 2-10. Camera 0 Flex Pin Definition [J1] (continued)

Pin #	Pin Name	Description	Dir
21	I2C_SDA	I2C Data # 1, Mux 0	Bi-Dir
22	Power	Power, 3.3V	Output

Table 2-11. Camera 1 Flex Pin Definition [J29]

Pin #	Pin Name	Description	Dir
1	GND	Ground	Output
2	CSI1_D0_N	CSIPort 1 Data Lane 0	Input
3	CSI1_D0_P	CSIPort 1 Data Lane 0	Input
4	GND	Ground	
5	CSI1_D1_N	CSIPort 1 Data Lane 1	Input
6	CSI1_D1_P	CSIPort 1 Data Lane 1	Input
7	GND	Ground	
8	CSI1_CLK_N	CSIPort 1 CLK	Input
9	CSI1_CLK_P	CSIPort 1 CLK	Input
10	GND	Ground	
11	CSI1_D2_N	CSIPort 1 Data Lane 2	Input
12	CSI1_D2_P	CSIPort 1 Data Lane 2	Input
13	GND	Ground	
14	CSI1_D3_N	CSIPort 1 Data Lane 3	Input
15	CSI1_D3_P	CSIPort 1 Data Lane 3	Input
16	GND	Ground	
17	CAM1_PWDN	Pwr-Dwn(IO expander)	Output
18	CAM1_AUX	AUX (WKUP_GPIO0_70)	Bi-Dir
19	GND	Ground	
20	I2C_SCL	I2C Clock #1, Mux 1	Output
21	I2C_SDA	I2C Data # 1, Mux 1	Bi-Dir
22	Power	Power, 3.3V	Output

2.4.5 Camera Interface, 40-Pin High Speed [J31] [J30]

The EVM includes a 40-pin (2x20, 2.54 mm pitch) high speed camera interface [J31][J30]. Each expansion connector [J31][J30] supports two CSI-2 (4 Lanes each), power, and control signals (I2C, GPIO, and so forth). All control signals are configurable for 3.3 V or 1.8 V voltage levels.

Table 2-12. Camera IO Voltage Control

I2C IO Expander (P0)	Camera IO Level
Low or ‘0’	1.8V (Default)
High or ‘1’	3.3V

Table 2-13. 40-Pin High-Speed Camera Expansion Pin Definition [J31]

Pin #	Pin Name	Description (Processor Pin #)	Dir
1	Power		Output
2	I2C_SCL	I2CBus #1, Clock (AE34)	Bi-Dir
3	Power		Output
4	I2C_SDA	I2CBus #1, Data (AL33)	Bi-Dir
5	CSI0_CLK_P	CSIPort 0 Clock	Input
6	GPIO/PWMA	WKUP_GPIO0_32(C31)	Bi-Dir
7	CSI0_CLK_N	CSIPort 0 Clock	Input
8	GPIO/PWMB	WKUP_GPIO0_36 (G31)	Bi-Dir
9	CSI0_D0_P	CSIPort 0 Data Lane 0	Input

Table 2-13. 40-Pin High-Speed Camera Expansion Pin Definition [J31] (continued)

Pin #	Pin Name	Description (Processor Pin #)	Dir
10	REFCLK	MCU CLKOUT0(M38)	Bi-Dir
11	CSI0_D0_N	CSI Port 0 Data Lane 0	Input
12	GND	Ground	
13	CSI0_D1_P	CSI Port 0 Data Lane 1	Input
14	RESETz	FROM IO EXPANDER	Output
15	CSI0_D1_N	CSI Port 0 Data Lane 1	Input
16	GND	Ground	
17	CSI0_D2_P	CSI Port 0 Data Lane 2	Input
18	GPIO	WKUP_GPIO0_37 (F33)	Bi-Dir
19	CSI0_D2_N	CSI Port 0 Data Lane 2	Input
20	GPIO	WKUP_GPIO0_38 (G32)	Bi-Dir
21	CSI0_D3_P	CSI Port 0 Data Lane 3	Input
22	GPIO	WKUP_GPIO0_35 (D31)	Bi-Dir
23	CSI0_D3_N	CSI Port 0 Data Lane 3	Input
24	GND	Ground	
25	CSI1_CLK_P	CSI Port 1 Clock	Input
26	CSI1_D3_P	CSI Port 1 Data Lane 3	Input
27	CSI1_CLK_N	CSI Port 1 Clock	Input
28	CSI1_D3_N	CSI Port 1 Data Lane 3	Input
29	CSI1_D0_P	CSI Port 1 Data Lane 0	Input
30	Power	Power, 3.3V	Output
31	CSI1_D0_N	CSI Port 1 Data Lane 0	Input
32	Power	Power, 3.3V	Output
33	CSI1_D1_P	CSI Port 1 Data Lane 1	Input
34	Power	Power, 3.3V	Output
35	CSI1_D1_N	CSI Port 1 Data Lane 1	Input
36	Power	Power, 3.3V	Output
37	CSI1_D2_P	CSI Port 1 Data Lane 2	Input
38	Power	Power, IO Level (1.8 or 3.3V)	Output
39	CSI1_D2_N	CSI Port 1 Data Lane 2	Input
40	Power	Power, IO Level (1.8 or 3.3V)	Output

Table 2-14. 40-Pin High-Speed Camera Expansion Pin Definition [J30]

Pin #	Pin Name	Description (Processor Pin #)	Dir
1	Power		Output
2	I2C_SCL	I2CBus #1, Clock (AE34)	Bi-Dir
3	Power		Output
4	I2C_SDA	I2CBus #1, Data (B34)	Bi-Dir
5	CSI2_CLK_P	CSIPort 0 Clock	Input
6	GPIO/PWMA	WKUP_GPIO0_29(C31)	Bi-Dir
7	CSI2_CLK_N	CSIPort 0 Clock	Input
8	GPIO/PWMB	WKUP_GPIO0_31 (F32)	Bi-Dir
9	CSI2_D0_P	CSIPort 0 Data Lane 0	Input
10	REFCLK	MCU CLKOUT0(M38)	Bi-Dir
11	CSI2_D0_N	CSI Port 0 Data Lane 0	Input
12	GND	Ground	
13	CSI2_D1_P	CSI Port 0 Data Lane 1	Input

Table 2-14. 40-Pin High-Speed Camera Expansion Pin Definition [J30] (continued)

Pin #	Pin Name	Description (Processor Pin #)	Dir
14	RESETz	FROM IO EXPANDER	Output
15	CSI2_D1_N	CSI Port 0 Data Lane 1	Input
16	GND	Ground	
17	CSI2_D2_P	CSI Port 0 Data Lane 2	Input
18	GPIO	WKUP_GPIO0_33 (F31)	Bi-Dir
19	CSI2_D2_N	CSI Port 0 Data Lane 2	Input
20	GPIO	WKUP_GPIO0_34 (E35)	Bi-Dir
21	CSI2_D3_P	CSI Port 0 Data Lane 3	Input
22	GPIO	WKUP_GPIO0_39 (G33)	Bi-Dir
23	CSI2_D3_N	CSI Port 0 Data Lane 3	Input
24	GND	Ground	
25	<open>		N/A
26	<open>		N/A
27	<open>		N/A
28	<open>		N/A
29	<open>		N/A
30	Power	Power, 3.3V	Output
31	<open>		N/A
32	Power	Power, 3.3V	Output
33	<open>		N/A
34	Power	Power, 3.3V	Output
35	<open>		N/A
36	Power	Power, 3.3V	Output
37	<open>		N/A
38	Power	Power, IO Level (1.8 or 3.3V)	Output
39	<open>		N/A
40	Power	Power, IO Level (1.8 or 3.3V)	Output

2.4.6 Automation and Control Connector [J17]

The EVM supports an interface to allow for automated control of the system, including functions like on/off, reset, and boot mode settings.

Table 2-15. Test Automation Interface Pin Definition [J25]

Pin	Pin Name	Description (Processor Pin #)	Dir
1	Power	Power,3.3 V	Output
2	Power	Power,3.3 V	Output
3	Power	Power,3.3 V	Output
4-6	<open>		N/A
7	GND	Ground	
8-15	<open>		N/A
16	GND	Ground	
17-24	<open>		N/A
25	GND	Ground	
26	POWERDOWNz	SK Power Down	Input
27	PORz	SK Power-On/Cold Reset	Input
28	RESETz	SK Warm Reset	Input
29	<open>		N/A
30	INT1z	MCU_ADC1_AIN0 (Y38)	Input

Table 2-15. Test Automation Interface Pin Definition [J25] (continued)

Pin	Pin Name	Description (Processor Pin #)	Dir
31	INT2z	MCU_ADC1_AIN1 (Y34)	Bi-Dir
32	BOOTMODE_CNTL#	NA	N/A
33	BOOTMODE_RSTz	Bootmode Buffer Reset	Input
34	GND	Ground	
35	<open>		N/A
36	I2C_SCL	I2C Bus #0, Clock (AN36)	Bi-Dir
37	BOOTMODE_SCL	Bootmode Buffer I2C Clock	Input
38	I2C_SDA	I2C Bus #0, Data (AP37)	Bi-Dir
39	BOOTMODE_SDA	Bootmode Buffer I2C Data	Bi-Dir
40-42	GND	Ground	

3 Circuit Details

This sections provides additional details on the EVM design and processor connections.

3.1 Top Level Diagram

Figure 3-1 shows the functional block diagram of the EVM.

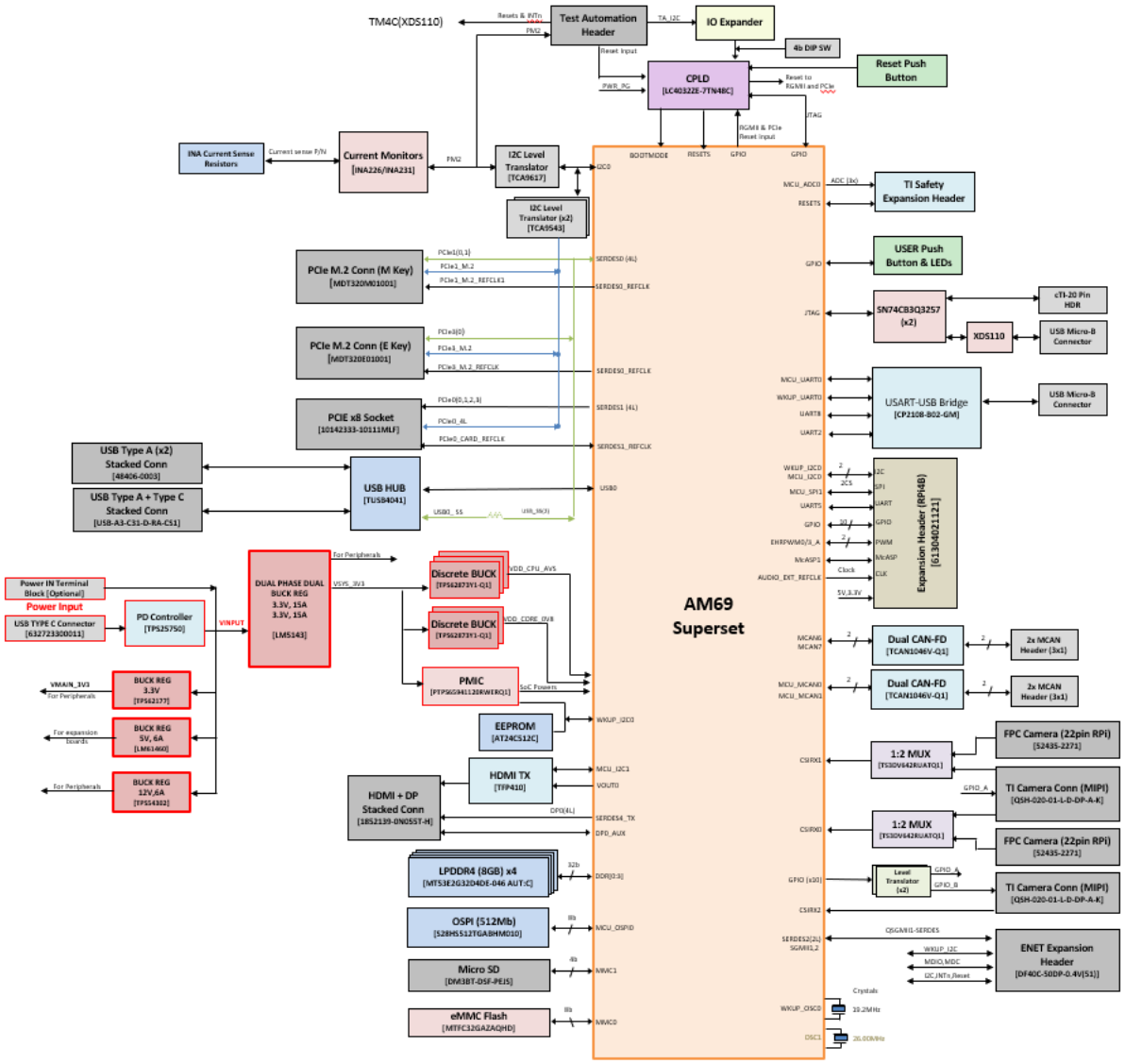

Figure 3-1. SK-AM69 Functional Block Diagram

3.2 Interface Mapping

The processor Interface Mapping table is provided in Table 3-1.

Table 3-1. Interface Mapping Table

Connected Peripheral	Processor Resources	Components / Part Numbers
Memory, LPDDR4 DRAM	DDR0, DDR1, DDR2, DDR3	Micron MT53E2G32D4DE-046 AUT:C
Memory, eMMC Flash	MMC0	Micron MTFC32GAZAQHD-IT
Memory, xSPI NOR Flash	MCU_OSPI0	CypressS28HS512TGABHM010
Micro-SDCard Cage	MMC1	
EEPROM, Board Identification	WKUP_I2C0	MicrochipTech AT24C512C
Wired Ethernet	MCU_RGMII1, MCU_MDIO	Texas Instruments DP83867E
USB Type C + CC Controller	USB0(SERDES0)	Texas Instruments TUSB321
USB Type A (3x)	USB0(SERDES0)	Texas Instruments TUSB8041
HDMI	DPI0, MCU_I2C1	Texas Instruments TFP410
Display Port	DP0 (SERDES4)	
PCIe – M.2 Socket (E-Key 2230)	PCIe3 (SERDES0), I2C0	
PCIe– M.2 Socket (M-Key 2280)	PCIe1 (SERDES0), I2C0	
PCIe– Standard x8 Socket	PCIe0 (SERDES1), I2C0	
ENET Expansion Connector	SGMII2 (SERDES2), I2C0, WKUP_I2C0	
CSIRx Interface	CSI0,CSI1, CSI2, I2C1	
UART Terminal (UART-to-USB)	WKUP_UART0, MCU_UART0, UART8, UART2	Silicon Labs CP2108
CAN (4x)	MCU_MCAN0, MCU_MCAN1, MCAN6, MCAN7	Texas Instruments TCAN1046V
Expansion Header (40-pin)	McASP1, MCU_SPI1, UART5, MCU_I2C0, WKUP_I2C0	
Expansion Header (10-pin)	MCU_ADC0, RESETs	
Test Automation Header	I2C0	

3.3 I2C Address Mapping

Table 3-2 provides the complete I2C address mapping details on the EVM.

Table 3-2. I2C Mapping Table

Interface Name	Processor Resources		Components / Part Numbers
	I2C Port	Address	
Power Management IC	WKUP_I2C0	0x48, 0x49, 0x4A & 0x4B	Texas Instruments TPS6594133
Buck Regulator	WKUP_I2C0	0x40	Texas Instruments TPS62873
Buck Regulator	WKUP_I2C0	0x43	Texas Instruments TPS62873
EEPROM, Board Id	WKUP_I2C0	0x51	MicrochipTech AT24C512C
ENET Expansion Connector	WKUP_I2C0	Add-on	
Expansion Header (40p)	WKUP_I2C0	Add-on	
Expansion Header (40p)	MCU_I2C0	Add-on	
Current Monitor IC	I2C0	0x40, 0x41, 0x45, 0x46, 0x4D, 0x4F	Texas Instruments INA226
Test Automation Header	I2C0	Add-on	
PCIe M.2 Key E/M	I2C0	Add-on	
PCIe x8 Socket	I2C0	Add-on	
Input PD Controller	I2C0	0x20	Texas Instruments TPS25750
IO expander	I2C0	0x21	Texas Instruments TCA6416
Level Shifters	I2C0	0x71, 0x72	Texas Instruments TCA9543
ENET Expansion Connector	I2C0	Add-on	

Table 3-2. I2C Mapping Table (continued)

Interface Name	Processor Resources		Components / Part Numbers
	I2C Port	Address	
HDMI DDC	MCU_I2C1	Add-on	
Camera Expansion	I2C1	0x21	Texas Instruments TCA9543A
Bootmode IO expander	I2C1	0x70	Texas Instruments TCA6408
CSI FPC Conn	I2C1	Add-on	

3.4 GPIO Mapping

The General Purpose IOs of processor are segmented into two major groups as WKUP/MCU and MAIN, and are used interchangeably for this design. Table 3-3 describes the IO mapping to the EVM peripherals and provides the default settings.

Table 3-3. GPIO Mapping Table

Processor Pin Name	GPIO	Function	Dir/Level	Remarks
MCU_OSPI0_CSn1	WKUP_GPIO0_28	Enable for eFUSE Programming Supply	Output	0'– Disabled (Default) '1'– Enabled
MCU_OSPI0_CSn2	WKUP_GPIO0_29	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI2 Expansion Board Specific (Pin 6)
MCU_OSPI1_CLK	WKUP_GPIO0_31	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI2 Expansion Board Specific (Pin 8)
MCU_OSPI1_LBCLKO	WKUP_GPIO0_32	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI0/1 Expansion Board Specific (Pin 6)
MCU_OSPI1_DQS	WKUP_GPIO0_33	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI2 Expansion Board Specific (Pin 18)
MCU_OSPI1_D0	WKUP_GPIO0_34	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI2 Expansion Board Specific (Pin 20)
MCU_OSPI1_D1	WKUP_GPIO0_35	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI0/1 Expansion Board Specific (Pin 22)
MCU_OSPI1_D2	WKUP_GPIO0_36	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI0/1 Expansion Board Specific (Pin 8)
MCU_OSPI1_D3	WKUP_GPIO0_37	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI0/1 Expansion Board Specific (Pin 18)
MCU_OSPI1_CSn0	WKUP_GPIO0_38	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI0/1 Expansion Board Specific (Pin 20)
MCU_OSPI1_CSn1	WKUP_GPIO0_39	GPIO signal for CSI EXPANSION Connector	Bi-Dir	CSI2 Expansion Board Specific (Pin 22)
MCU_SPI0_CLK	WKUP_GPIO0_54	MUX Select	Output	'0' – A to B1 port selected '1' – A to B2 port selected
MCU_SPI0_D0	WKUP_GPIO0_55	User LED	Output	'0' – LED [LD5] is OFF (default) '1' – LED [LD5] is ON
MCU_SPI0_D1	WKUP_GPIO0_69	System Power Down	Output	'0' - Normal Operation (default) '1' - System Power Down/Off
MCU_SPI0_CS0	WKUP_GPIO0_70	Camera #1 Flex Signal (GPIO)	Bi-Dir	Camera Specific (Pin 18)

Table 3-3. GPIO Mapping Table (continued)

Processor Pin Name	GPIO	Function	Dir/Level	Remarks
WKUP_GPIO0_10	WKUP_GPIO0_10	HDMI Monitor Enable	Output	'0' – Power Down '1' – Normal Operation (default)
WKUP_GPIO0_14	WKUP_GPIO0_14	HDMI Transceiver Enable	Output	'0' - Power Down (default) '1' - Normal Operation
WKUP_GPIO0_49	WKUP_GPIO0_49	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 15)
PMIC_POWER_EN1	WKUP_GPIO0_88	Camera #0 Flex Signal (GPIO)	Bi-Dir	Camera Specific (Pin 18)
WKUP_GPIO0_56	WKUP_GPIO0_56	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 29)
WKUP_GPIO0_57	WKUP_GPIO0_57	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 31)
MCU_ADC1_AIN0	WKUP_GPIO0_79	Test Automation Interrupt #1	Input	'0' - To Be Defined by User '1' - To Be Defined by User (default)
MCU_ADC1_AIN1	WKUP_GPIO0_80	Test Automation Interrupt #2	Input	'0' - To Be Defined by User '1' - To Be Defined by User (default)
MCU_ADC1_AIN2	WKUP_GPIO0_81	Ethernet PHY Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Request (default)
MCU_ADC1_AIN3	WKUP_GPIO0_82	SW1 Pushbutton	Input	'0' – SW1 is Pressed '1' – SW1 is NOT Pressed (default)
MCU_ADC1_AIN4	WKUP_GPIO0_83	Power Management IC Interrupt	Input	'0'– Active Interrupt Request '1'– No Interrupt Request (default)
MCU_ADC1_AIN5	WKUP_GPIO0_84	ENET Expansion Header Interrupt	Input	
MCU_ADC1_AIN6	WKUP_GPIO0_85	GPIO Expander Interrupt	Input	
WKUP_GPIO0_66	WKUP_GPIO0_66	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 7)
WKUP_GPIO0_67	WKUP_GPIO0_67	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 22)
EXTINTn	GPIO0_0	HDMI Monitor Detect	Input	Active High Signal '0' – No Monitor Detected (default) '1' – Monitor Detected
MCAN13_TX	GPIO0_3	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 16)
MCAN13_RX	GPIO0_4	Display Port Monitor Enable	Output	'0' – Monitor is Disabled (default) '1' – Monitor is Enabled
MCAN1_TX	GPIO0_27	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 37)
MCASP0_AXR8	GPIO0_36	40 pin Expansion Header (GPIO)	Bi-Dir	Expansion Board Specific (Pin 13)

Table 3-3. GPIO Mapping Table (continued)

Processor Pin Name	GPIO	Function	Dir/Level	Remarks
ECAP0_IN_APWM_OUT	GPIO0_49	SD Card IO Voltage Selection	Output	'0' – SD Card IO Voltage is 1.8V '1' – SD Card IO Voltage is 3.3 V (default)

3.5 I2C GPIO Expander Mapping

The EVM uses I2C-based IO expanders for some peripheral control. Table 3-4 explains the functionality of the pins.

Table 3-4. IO Expander Mapping Table

IO EXP PORT NO	Net name	Function	Dir/ Level	Remarks
I2C Bus: I2C1, Addr: 0x21 (TCA6408A)				
P0	CSI_VIO_SEL	CSI I2C/GPIO Voltage Selection	Output	'0' – 1.8 V IO (default) '1' – 3.3 V IO
P1	CSI_MUX_SEL_2	CSI Expansion Interface Selection	Output	CSI I2C MUX select '0' – Camera/Flex Selected (default) '1' – 40-pin Camera Expansion Selected
P2	CSI2_RSTz	CSI Expansion Interface Reset		
P3	IO_EXP_CAM0_GPIO1	Camera #0 Flex Signal (GPIO)	Bi-Dir	Camera Specific (Pin 17)
P4	IO_EXP_CAM1_GPIO1	Camera #1 Flex Signal (GPIO)	Bi-Dir	Camera Specific (Pin 17)
I2C Bus: I2C0, Addr: 0x21 (TCA6416A)				
P00	BOARDID_EEPROM_WP	EEPROM Write Protect	Output	'0' – EEPROM is NOT Write Protected (default) '1' – EEPROM is Write Protected
P01	CAN_STB	CAN Standby signal	Output	'0' – Normal Mode '1' – Standby Mode (default)
P02	GPIO_uSD_PWR_EN	SD Card Power Enable	Output	'0' – SD Card Power Disabled '1' – SD Card Power Enable (default)
P03	IO_EXP_MCU_RGMII_RST#	Ethernet PHY Reset	Output	'0' – Ethernet is Reset '1' – Ethernet is NOT Reset (default)
P04	IO_EXP_PCIe0_4L_PERST#			
P05	IO_EXP_PCIe1_M.2_RTSz	M.2 Key M Interface Signal (RSTz)	Output	RSTz, See M.2 Key M Specification for more details. (Default = '0')
P06	IO_EXP_PCIe3_M.2_RTSz	M.2 Key E Interface Signal (RSTz)	Output	RSTz, See M.2 Key M Specification for more details. (Default = '0')
P07	PM_INA_BUS_EN	Test Automation I2C translator	Output	

Table 3-4. IO Expander Mapping Table (continued)

IO EXP PORT NO	Net name	Function	Dir/ Level	Remarks
P10	ENET1_EXP_PWRDN	Enable signal for PM2 I2C lines	Output	
P11	EXP1_ENET_RSTz	Power Down Signal for Enet Expansion Header	Output	
P12	ENET1_I2CMUX_SEL	Reset Signal for Enet Expansion Header	Output	
P13	PCIe0_CLKREQ#	I2C mux select Signal for Enet Expansion Header	Input	
P14	PCIe1_M.2_CLKREQ#	PCIe Card Clock request Signal	Input	
P15	PCIe3_M2_CLKREQ#	PCIe M Key Clock request Signal	Input	
P16	PCIe0_PRSNT2#_1	PCIe E Key Clock request Signal	Input	
P17	PCIe0_PRSNT2#_2	Reset Signal for PCIe card Slot	Input	

3.6 Identification EEPROM

The SK-AM69 board identified and revision information are stored in an on-board EEPROM. The first 259 bytes of memory are pre-programmed with SK identification information. The format of that data is provided in Table 3-5. The remaining 32509 bytes are available for data or code storage.

The SK EEPROM is accessible from WKUP I2C0 port of processor at address 0x51.

Table 3-5. Board ID memory Header Information

Field Name	Offset / Size	Value	Comments
MAGIC	0000/ 4B	0xEE3355AA	Header Identifier
M_TYPE	0004/1B	0x1	Fixed length and variable position board ID header
M_LENGTH	0005/2B	0x37	Size of payload
B_TYPE	0007/1B	0x10	Payload type
B_LENGTH	0008/2B	0x2E	Offset to next header
B_NAME	000A/16B	AM69-SK	Name of the board
DESIGN_REV	001A/2B	E1	Revision number of the design
PROC_NBR	001C/4B	154	PROC number
VARIANT	0020/2B	1	Design variant number
PCB_REV	0022/2B	E1	Revision number of the PCB
SCHBOM_REV	0024/2B	0	Revision number of the schematic
SWR_REV	0026/2B	1	First software release number
VENDORID	0028/2B	1	
BUILD_WK	002A/2B		Week of the year of production
BUILD_YR	002C/2B		Year of production
BOARDID	002E/6B	0	
SERIAL_NBR	0034/4B		Incrementing board number
DDR_INFO	TYPE	1	
	Length	2	Offset to next header
	DDRcontrol	2	DDR Control Word
MAC_ADDR	TYPE	1	Payload type
	Length	2	Size of payload
	MAC control	2	MAC header control word
	MAC_adrs	192	

Table 3-5. Board ID memory Header Information (continued)

Field Name	Offset / Size	Value	Comments
END_LIST	TYPE	1	End Marker

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2023	*	Initial Release

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