EVM User's Guide: SK-AM62P-LP

AM62P SK Evaluation Module

Description

The SK-AM62P-LP starter kit (SK) evaluation module (EVM) is built around our AM62P display processor, which includes scalable Arm® Cortex®-A53 performance and embedded features, such as: triple high-definition display support, high-performance 3D-GPU, 4K video acceleration, and extensive peripherals. SK-AM62A-LP is an excellent choice for those looking to develop automotive and industrial applications, including automotive digital instrumentation, automotive displays, industrial HMI, and more.

SK-AM62P-LP includes multiple display connectors that enable supporting up to three screens, a mobile industry processor interface (MIPI®) CSI-2 camera connector, an M.2 connector for WiFi® and Bluetooth® modules, two Gigabit Ethernet ports, UART to USB circuit for debug output, and two temperature sensors for monitoring SoC and LPDDR4 thermal monitoring.

Get Started

1. Order the EVM at SK-AM62P-LP.
2. Download the EVM design files.
3. Download the software from SK-AM62P-LP.
4. Read this EVM User's Guide.

Features

- USB-C powered standalone mode of operation
- Power optimized PMIC based power management
- Onboard XDS110 JTAG interface with USB connectivity for code development and debugging
- Onboard 32 GB eMMC memory and 512 Mb OSPI NOR Flash
- 40 pin FPC connector for OLDI interface
- 22 pin FPC connector for DSI interface
- Onboard HDMI™ connector to interface with external display
- 2x RGMII RJ45 connectors
- 2x USB 2.0 on type A and type C connectors
- Test automation interface through XDS110
- Expansion connectors to access the low speed interfaces
- MCU connector to access MCU interfaces
- GPMC connector for external GPMC NAND interface
- M.2 connector for Wi-Fi/BT module

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1 Evaluation Module Overview

1.1 Introduction

The starter kit allows the user to experience high resolution display features through HDMI (over DPI), dual port LVDS and MIPI DSI, as well as industrial communication designs using serial, Ethernet, USB, and other interfaces. The SK EVM can communicate with other processors or systems, and act as a communication gateway. In addition, the SK EVM can directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network. The embedded emulation logic allows for emulation and debugging using standard development tools, such as Code Composer Studio™ from TI.

This technical user's guide describes the hardware architecture of the AM62P SK EVM, a low-cost, low-power Starter Kit built around the TI's AM62P System-on-Chip (SOC). The AM62P SOC comprises of a Quad-Core 64-bit Arm® Cortex® - A53 microprocessor, and a dual-core Arm® Cortex®-R5F MCU with deep learning accelerator.

1.2 Kit Contents

- SK-AM62P-LP EVM
- EVM user guide pamphlet
- EVM disclaimer and standard terms

1.3 Device Information

Furthermore, the SK-AM62P-LP supports Linux® and Android development with a feature-rich software development kit (SDK). On-chip emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio integrated development environment (IDE) (CCSTUDIO) as well as an intuitive out-of-box user's guide to quickly start design evaluation.

1.4 Specification

The figure below shows the functional block diagram of the AM62P SK EVM.

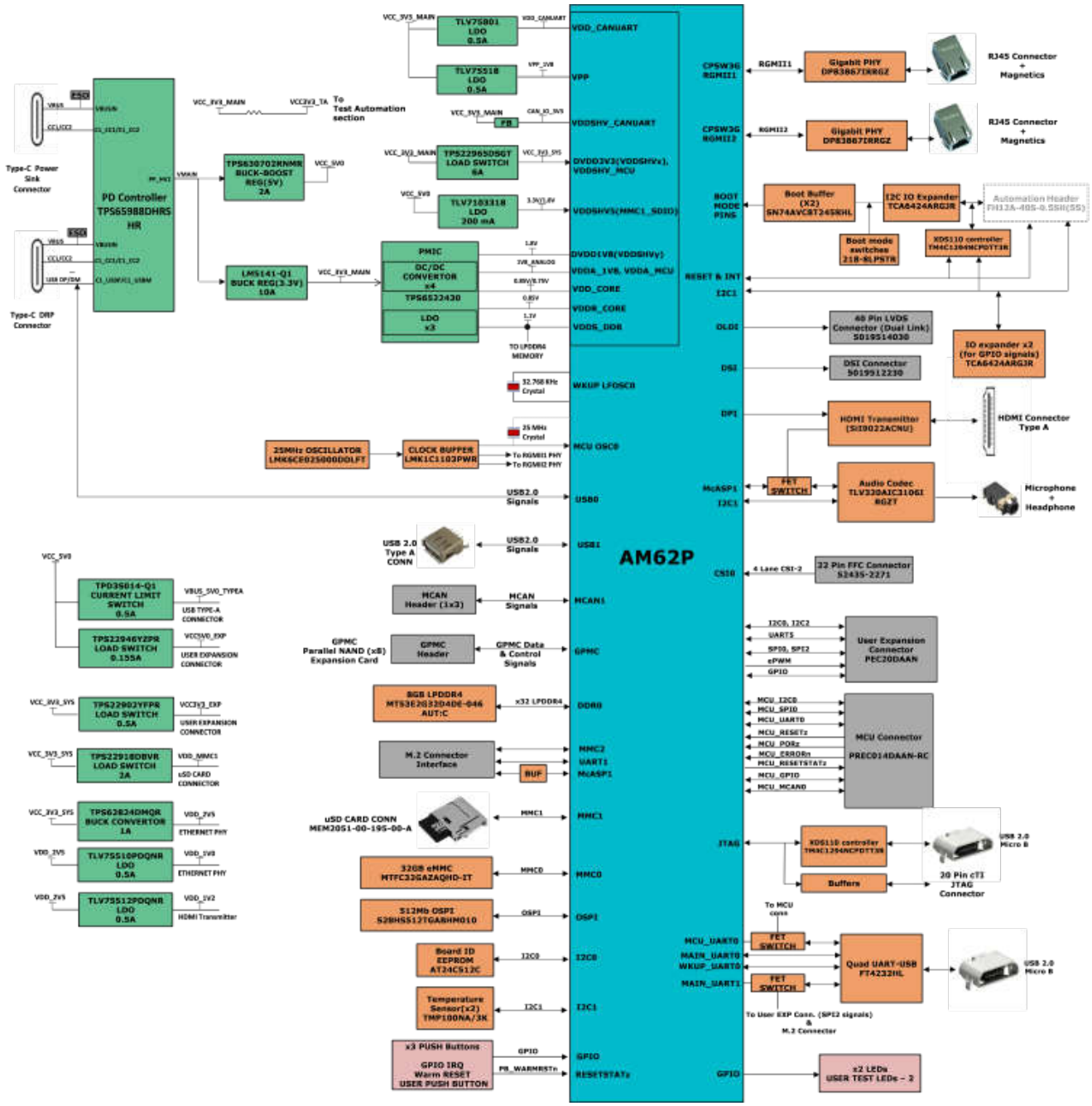

Figure 1-1. Functional Block Diagram of AM62P SK EVM

2 Hardware

2.1 Additional Images

This section shows the EVM pictures and location of various blocks on the board.

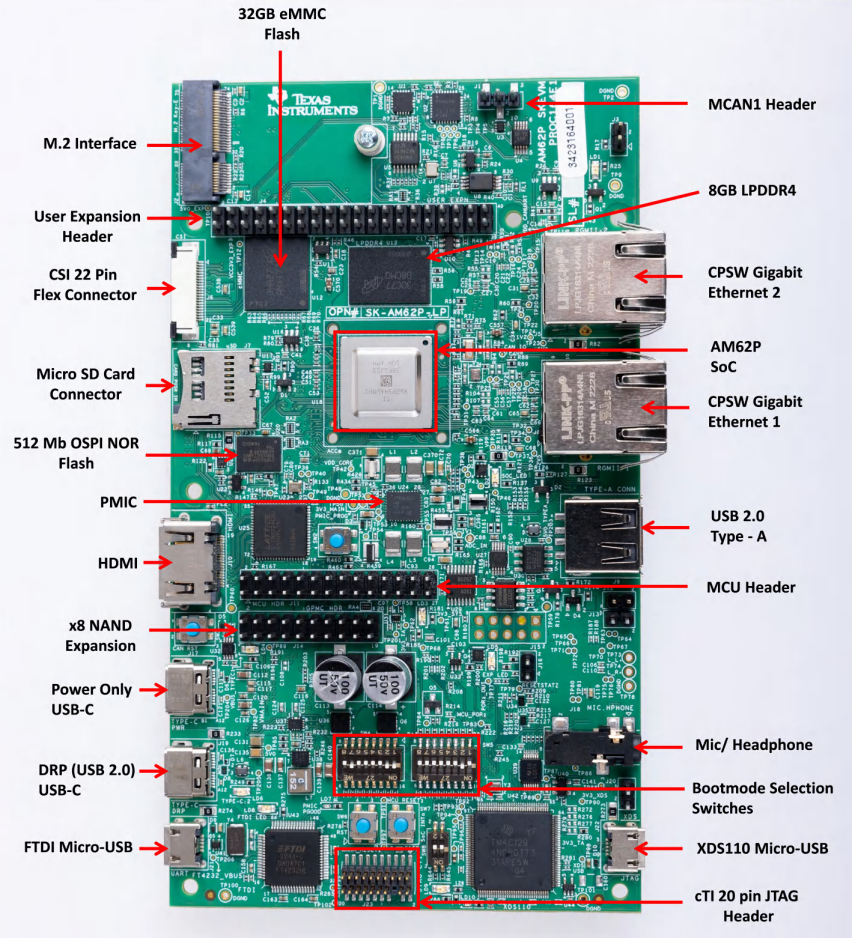

Figure 2-1. EVM Top Side

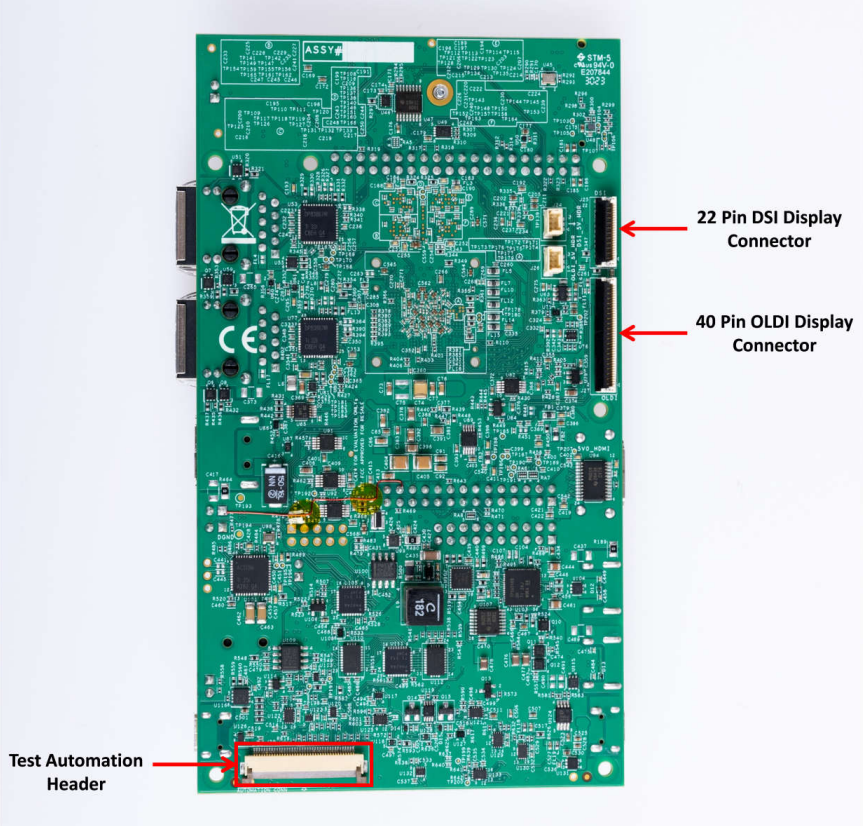

Figure 2-2. EVM Bottom Side

2.2 Key Features

The AM62P SK EVM is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for the Texas Instrument's AM62P System-on-Chip (SoC).

The following sections discuss the key features of the SK EVM.

2.2.1 Processor

- AM62P SoC, 17 mm x 17 mm, 466-pinBGA.

2.2.2 Power Supply

- Two USB Type-C ports (5 V-15 V input range).
- Optimized power designs with PMIC, discrete regulators and LDOs for the processor and peripherals.

2.2.3 Memory

- 8GB LPDDR4 supporting data rate up to 3200 Mb/s per pin.
- Micro SD Card slot with UHS-1 support.
- 512 Mbit Octal SPI NOR Flash memory.
- 512Kbit Inter-Integrated Circuit (I2C) board ID EEPROM.
- 32GB eMMC Flash.

2.2.4 JTAG/Emulator

- XDS110 On-Board Emulator.
- Supports 20-pin JTAG connection from external emulator.

2.2.5 Supported Interfaces and Peripherals

- 1x USB2.0 Type C Interface, support DFP and UFP modes (Data) and DRP mode (Power).
- 1x USB2.0 Host Interfaces, Type A.
- 1x HDMI Interface.
- Audio Line In and MIC + Headphone out.
- M.2 Key E interface support for both Wi-Fi and Bluetooth modules.
- 2x Gigabit Ethernet port supporting 10/100/1000 Mbps data rate on RJ45 connector.
- Quad port UART to USB circuit over microB USB connector.
- User test LEDs.
- INA devices for SoC power monitoring.
- 2x Temperature Sensors near SoC and LPDDR4 for thermal monitoring.

2.2.6 Expansion Connectors/Headers

- CSI Camera connector
- DSI Display connector
- LVDS Display connector
- User Expansion connector
- MCU header
- GPMC NAND (x8) header
- MCAN1 header

2.3 Interface Mapping

Table 2-1. Interface Mapping

Interface Name	Port on SoC	Device Part Number
Memory – LPDDR4	DDR0	MT53E2G32D4DE-046 AUT:C
Memory – OSPI	OSPI0	S28HS512TGABHM010
Memory – Micro SD socket	MMC1	MEM2051-00-195-00-A
Memory – eMMC	MMC0	MTFC32GAZAQHD-IT
Memory – Board ID EEPROM	SoC_I2C0	AT24C512C-MAHM-T
Ethernet 1 – RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2 – RGMII	SoC_RGMII2	DP83867IRRGZ
GPIO port expander 1	SoC_I2C1	TCA6424ARGJR
User expansion connector – 2x20 HDR	SPI0, SPI2, UART5, SoC_I2C0, SoC_I2C2, McASP1 and GPIOs	PEC20DAAN
MCU header – 2x14 HDR	MCU MCU_UART0, MCU_MCAN0, MCU_SPI0, MCU_I2C0 and MCU GPIOs	PREC014DAAN-RC
GPMC NAND (x8) HDR	G GPMC	PREC010DAAN-RC
USB– 2.0 Type C	USB0	2012670005
USB– 2.0 Type A	USB1	629104151021
CSI interface	CSI0-RX	52435-2271
DSI interface	DSI0-TX	5019512230
OLDI interface	OLDI	5019514030
MCAN1 interface	MCAN1	TSM-103-02-T-SV
HDMI	VOUT0, McASP1and SoC_I2C1	SiI9022ACNU + TPD12S016PWR + DC04S019JA1R600
Audio codec	McASP1 and SoC_I2C1	TLV320AIC3106IRGZT+ SJ-43514-SM
GPIO port expander 2	SoC_I2C1	TCA6424ARGJR
UART terminal (UART-to-USB)	SoC_UAR SoC_UART[1:0], WKUP_UART0 and MCU_UART0	FT4232HL + 629105150521
Test automation header	SoC_I2C1	FH12A-40S-0.5SH
Temperature sensors	SoC_I2C1	TMP100NA/3K

Table 2-1. Interface Mapping (continued)

Interface Name	Port on SoC	Device Part Number
Current monitors	SoC_I2C1	INA228AIDGSR
Connectivity– M.2 Key E	MMC2, McASP1 and SoC_UART1	2199119-4

2.4 Power ON/OFF Procedure

Power to the EVM is provided through an external power supply with PD capability to either of the two USB Type-C Ports.

Note

The maximum length of the I/O cables shall not exceed 3 meters.

2.4.1 Power ON Procedure

1. Place the SK EVM boot switch selectors (SW4, SW5) into selected boot mode. Example boot-mode for SD card is shown below.
2. Connect your boot media (if applicable).
3. Attach the PD capable USB Type-C® cable to the SK EVM Type-C (J17 or J19) connector.
4. Connect the other end of the USB Type-C cable to the source, either AC Power Adapter, or USB Type C source device (such as a laptop computer).
5. Visually inspect that either LD4 or LD6 LED is illuminated.
6. XDS110 JTAG and UART debug console outputs are routed to micro-USB ports J22 and J21, respectively.

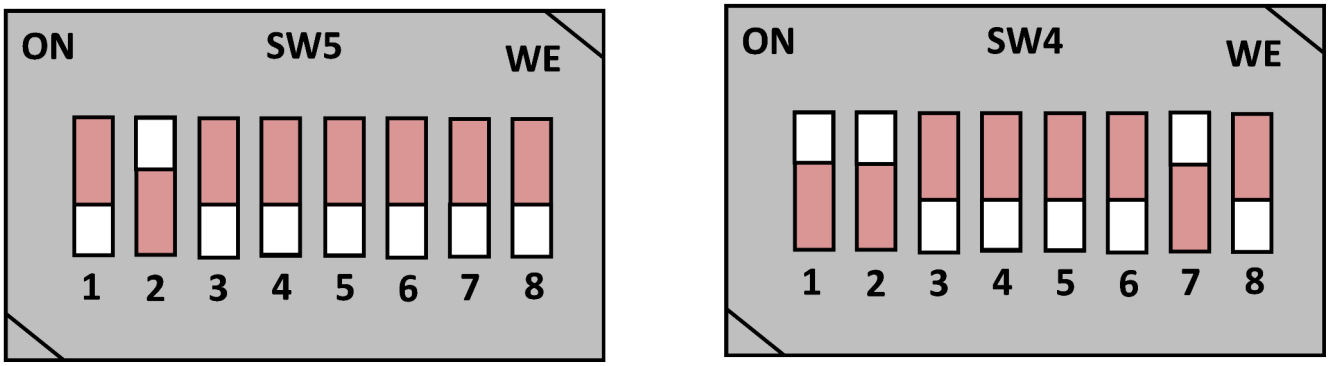

Figure 2-3. Example Boot Mode (MMCSD Boot)

2.4.2 Power OFF Procedure

1. Disconnect AC power from AC/DC converter.
2. Remove the USB Type-C cable from the SK EVM.

2.4.3 Test Points

Test points for each power output on the board are mentioned in Table 2-2.

Table 2-2. Test Points

SL. No.	Power Supply	Test Point	Voltage
1	VCC5V0_EXP	TP10	5
2	VDD_CANUART	TP11	0.85
3	VCC3V3_EXP	TP12	3.3
4	VDD_1V0	TP23	1
5	VDD_1V2	TP24	1.2
6	VDDSHV_SDIO	TP33	3.3/1.8
7	VPP_1V8	TP35	1.8
8	VDD_2V5	TP36	2.5
9	VDD_CORE	TP42	0.85/0.75
10	VDDR_CORE	TP43	0.85
11	VCC1V8_SYS	TP54	1.8
12	VDDA_1V8	TP55	1.8
13	VDD_LPDDR4	TP56	1.1
14	VCC_3V3_SYS	TP61	3.3
15	VCC_3V3_MAIN	TP68	3.3
16	VMAIN	TP82	12
17	VCC_5V0	TP85	5
18	VCC3V3_XDS	TP90	3.3
19	XDS_USB_VBUS	TP98	5
20	VCC3V3_TA	TP201	3.3
21	VBUS_5V0_TYPEA	TP203	5
22	VBUS_TYPEC1	TP204	12
23	VBUS_TYPEC2	TP205	12
24	FT4232_USB_VBUS	TP206	5
25	LDO_3V3	U30.8	3.3
26	VCC_3V3_FT4232	C153.2	3.3
27	VDD_MMC1_SD	TP202	3.3
28	VCC_5V0_HDMICONN	TP207	5

2.5 Clocking

The clock architecture of AM62P SK EVM is shown below.

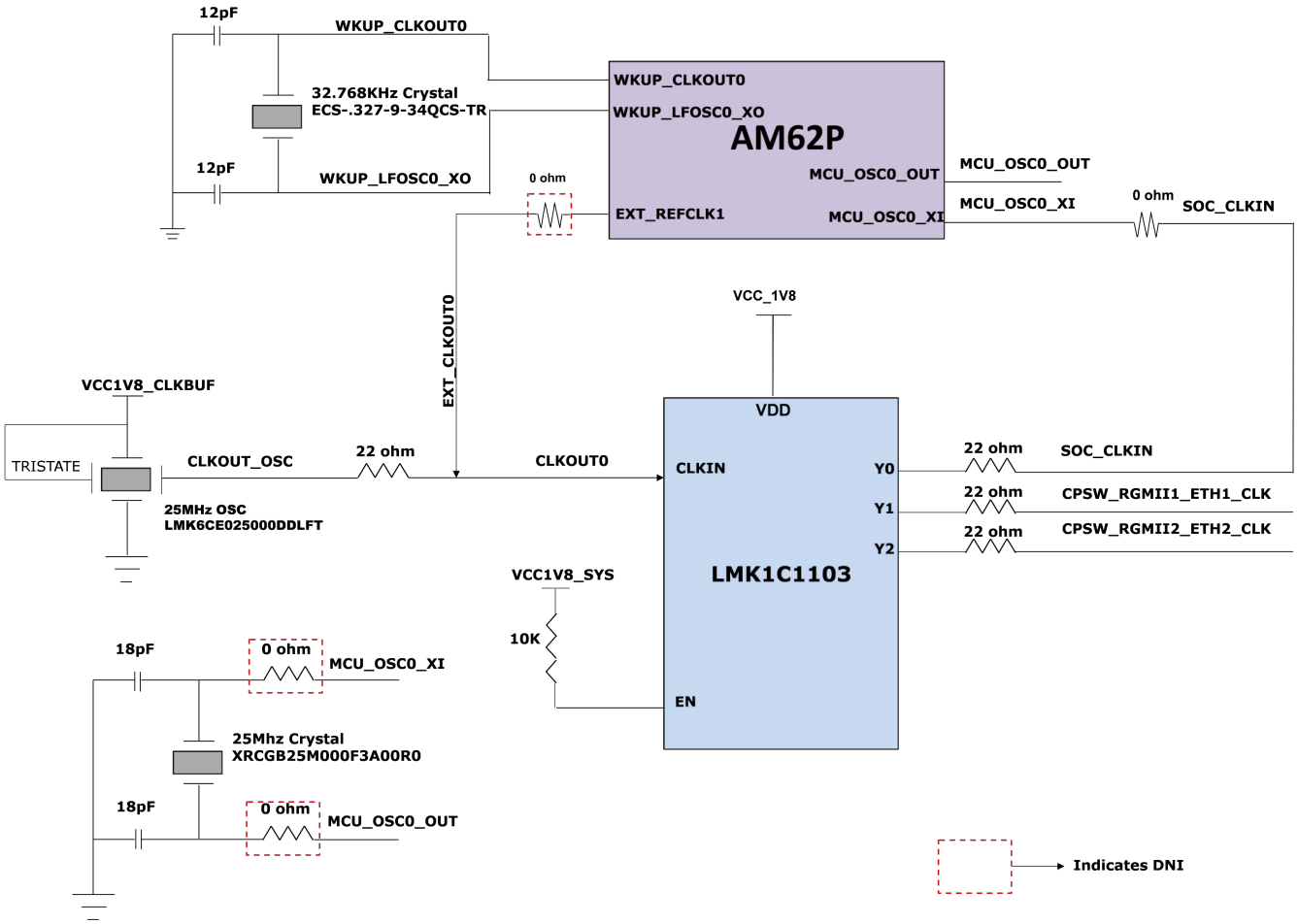

Figure 2-4. Clock Architecture

A clock buffer of part number LMK1C1103PWR is used to drive the 25 MHz clock to the SOC and the two Ethernet PHYs. LMK1C1103PWR is a 1:3 LVCMOS clock buffer, which takes the 25 MHz crystal/LVCMOS reference input and provides three 25 MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SOC or a 25 MHz oscillator, the selection of which is made using a set of resistors. By default, an oscillator is used as an input to the clock buffer on the AM62P SK EVM. Outputs Y1 and Y2 of the clock buffer are used as reference clock inputs for the two Gigabit Ethernet PHYs.

There is one external crystal (32.768 KHz) attached to the AM62P SOC to provide clock to the WKUP domain.

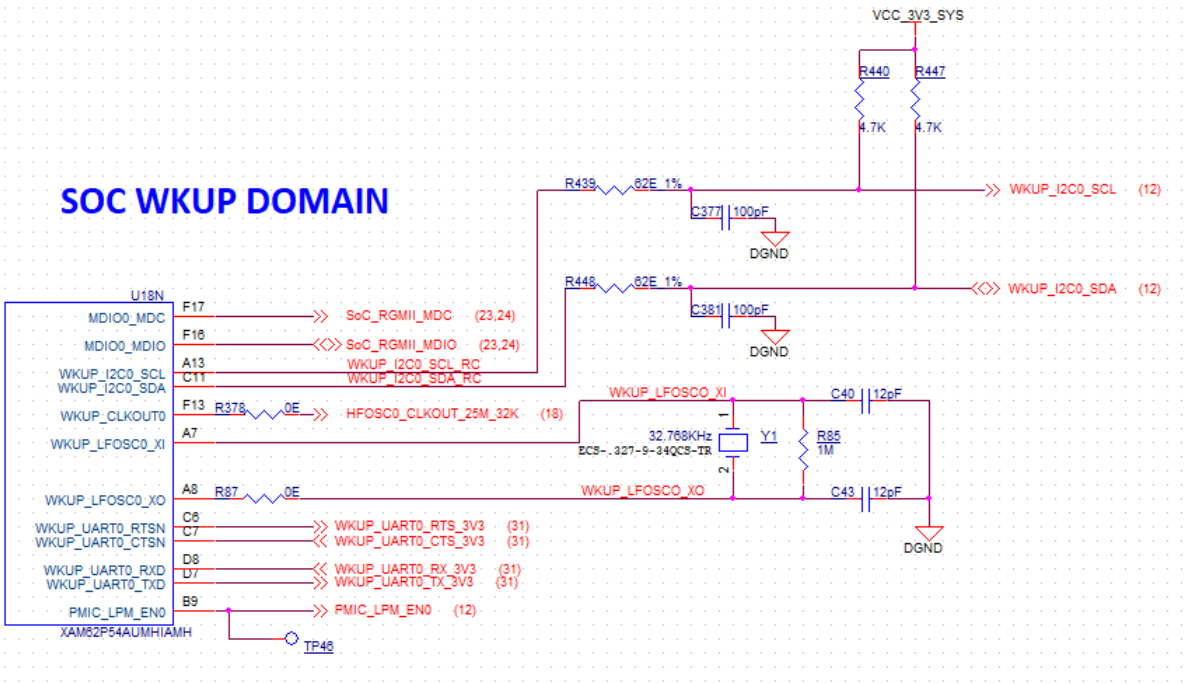

Figure 2-5. SoC WKUP Domain Clock

2.5.1 Peripheral Ref Clock

Clock inputs required for peripherals such as XDS110, FT4232, M.2 Interface, HDMI Framer and Audio Codec are generated locally using separate crystals or oscillators. Crystals or Oscillators used to provide the reference clocks to the EVM peripherals are shown in below table.

Table 2-3. Clock Table

Peripheral	Mfr. Part #	Description	Frequency
XDS110 emulator (Y3)	XRCGB16M000FXN01R0	CRY 16.000MHz 8 pF SMD	16.000 MHz
FT4232 Bridge (Y4)	445I23D12M00000	CRY 12.000MHz 18 pF SMD	12.000 MHz
M.2 Interface (U45)	ECS-327MVATX-2-CN-TR	OSC 32.768KHz CMOS SMD	32.768 KHz
Audio Codec (U98)	LMK6CE012288CDLFT	OSC 12.288MHz CMOS SMD	12.288 MHz
HDMI Framer (U23)	LMK6CE012288CDLFT	OSC 12.288MHz CMOS SMD	12.288 MHz

The clock required by the HDMI Transmitter can be provided by either the on-board oscillator or the AUDIO_EXT_REFCLK1 of the SOC, which can be selected through a resistor mux. The EXT_REFCLK1 of the SOC is used to provide clock to the User Expansion Connector on the SK EVM. The 32.768 KHz clock to the M.2 module is provided by default from WKUP_CLKOUT0 ball of AM62P SOC.

2.6 Reset

The Reset Architecture of AM62P SK EVM is shown below. The SOC has the following resets.

- RESETSTATz is the Main domain warm reset status output.
- PORz_OUT is the Main domain power ON reset status output.
- RESET_REQz is the Main domain warm reset input.
- MCU_PORz is the MCU domain power ON/Cold Reset input.
- MCU_RESETz is the MCU domain warm reset input.
- MCU_RESETSTATz is the MCU domain warm reset status output.

Upon power on reset, all peripheral devices connected to the main domain get reset by RESETSTATz.

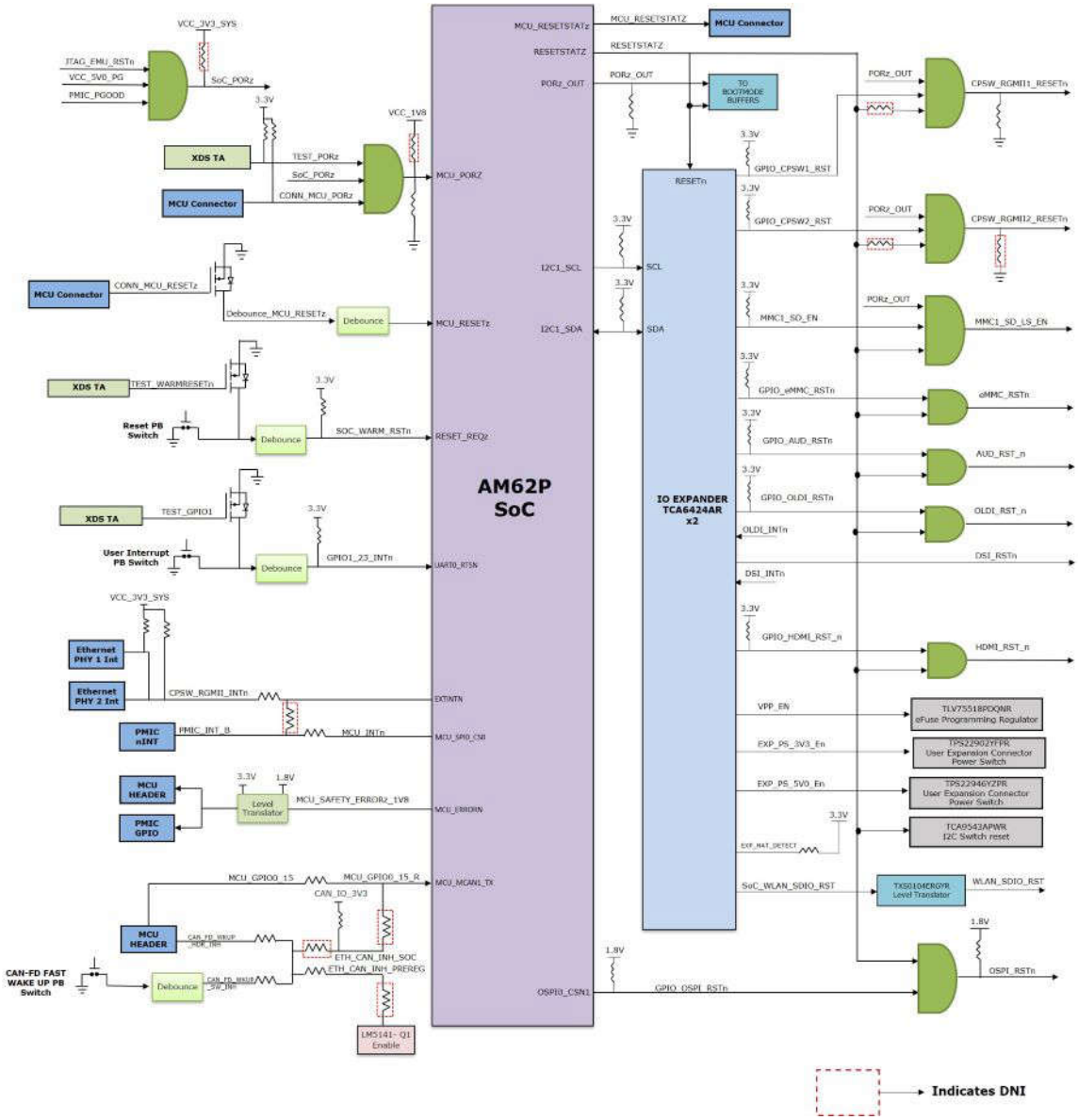

Figure 2-6. Reset Architecture

2.7 CSI Interface

The CSI-2 signals from the AM62P SOC are terminated to a 22 pin FFC connector 52435-2271 to interface with commercially available of the shelf CSI-2 standard Camera Card/Modules. All four CSI RX lanes are pinned out on the SK EVM along with SOC_I2C2 instance and a couple of GPIO's from the I2C1 controlled GPIO Port Expander.

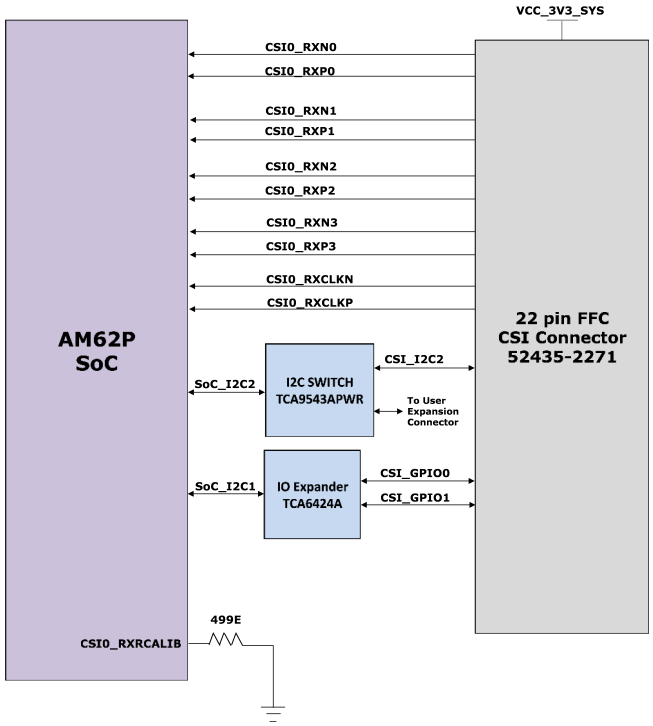

Figure 2-7. CSI Interface

Table 2-4. CSI Camera Connector (J6) Pin-Out

Pin No	Pin Description
1	DGND
2	CSI0_RXN0
3	CSI0_RXP0
4	DGND
5	CSI0_RXN1
6	CSI0_RXP1
7	DGND
8	CSI0_RXCLKN
9	CSI0_RXCLKP
10	DGND
11	CSI0_RXN2
12	CSI0_RXP2
13	DGND
14	CSI0_RXN3
15	CSI0_RXP3
16	DGND
17	CSI_GPIO0
18	CSI_GPIO1
19	DGND

Table 2-4. CSI Camera Connector (J6) Pin-Out (continued)

Pin No	Pin Description
20	CSI_I2C2_SCL
21	CSI_I2C2_SDA
22	VCC_3V3_SYS

2.8 OLDI Interface

The OLDI0 Display interface of the AM62P SOC is connected to a 40 pin LVDS display connector (J27) Mfr Part# 5019514030 from Molex. The AM62P SK EVM supports dual channel 8-bit LVDS output with resolutions up to 3840x1080p. Apart from the dual channel LVDS signals, the 40-pin connector is provided with a 3.3V supply with sourcing capability until 500 mA, I2C0 for any pre-initializations and two GPIO's for handling interrupt and reset to the interfacing display.

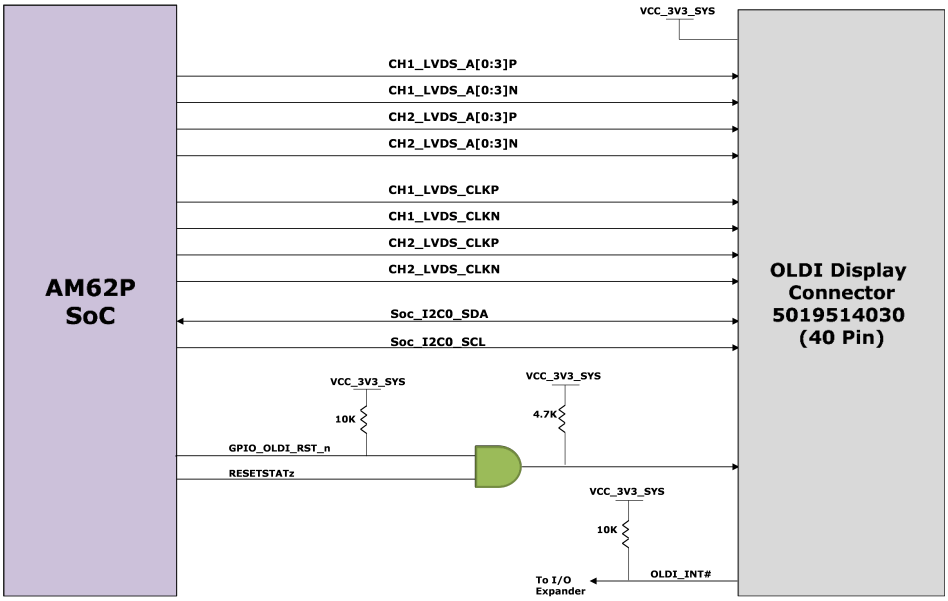

Figure 2-8. OLDI Interface

Table 2-5. OLDI Display Connector (J27) Pinout

Pin No.	Signal	Pin No.	Signal
1	DGND	21	CH1_LVDS_A2N
2	CH2_LVDS_A3P	22	DGND
3	CH2_LVDS_A3N	23	CH1_LVDS_CLKP
4	DGND	24	CH1_LVDS_CLKN
5	CH2_LVDS_A2P	25	DGND
6	CH2_LVDS_A2N	26	CH1_LVDS_A1P
7	DGND	27	CH1_LVDS_A1N
8	CH2_LVDS_CLKP	28	DGND
9	CH2_LVDS_CLKN	29	CH1_LVDS_A0P
10	DGND	30	CH1_LVDS_A0N
11	CH2_LVDS_A1P	31	DGND
12	CH2_LVDS_A1N	32	OLDI_INT#
13	DGND	33	OLDI_RESETN
14	CH2_LVDS_A0P	34	DGND
15	CH2_LVDS_A0N	35	DGND
16	DGND	36	NC
17	CH1_LVDS_A3P	37	NC
18	CH1_LVDS_A3N	38	SOC_I2C0_SDA
19	DGND	39	SOC_I2C0_SCL
20	CH1_LVDS_A2P	40	VCC_3V3_SYS_CONN

2.9 DSI Interface

The DSI Display interface of the AM62P SOC is connected to a 22-pin display connector (J25) Mfr Part# 5019512230 from Molex. The AM62P SK EVM supports 4 DSI-TX lanes for high-speed video link and low power command link with resolutions up to 3840x1080p. Apart from these four lanes, the 22-pin connector is provided with a 3.3V supply with sourcing capability until 500 mA, I2C0 for any pre-initializations and two GPIO's for handling interrupt and reset to the interfacing display.

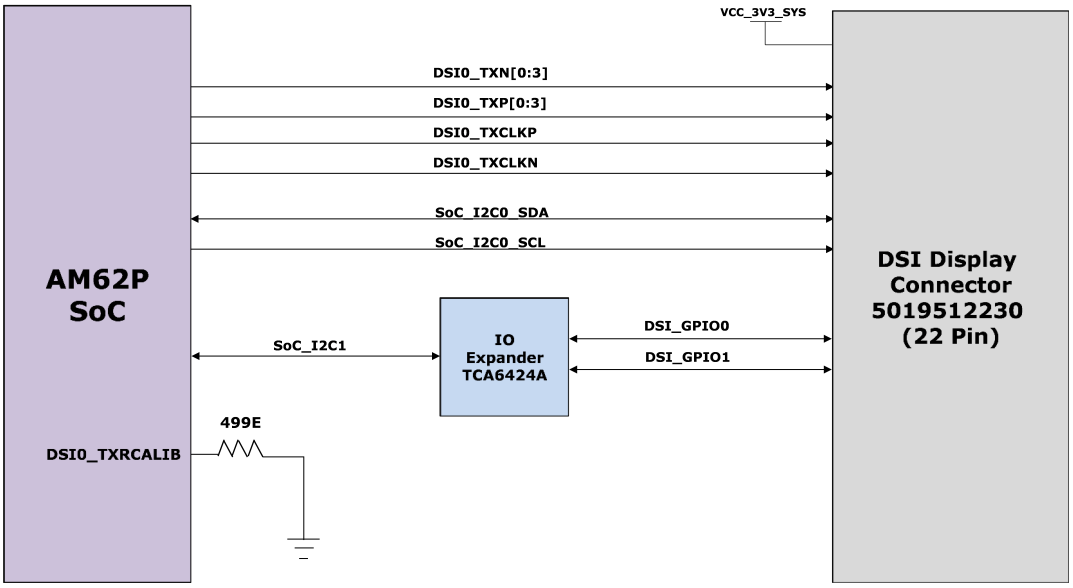

Figure 2-9. DSI Interface

Table 2-6. DSI Display Connector (J25) Pinout

Pin No.	Signal
1	VCC_3V3_SYS
2	SOC_I2C0_SDA
3	SOC_I2C0_SCL
4	DGND
5	DSI_INTN#
6	DSI_RESETN
7	DGND
8	DSI_TX3_P
9	DSI_TX3_N
10	DGND
11	DSI_TX2_P
12	DSI_TX2_N
13	DGND
14	DSI_TXCLK_P
15	DSI_TXCLK_N
16	DGND
17	DSI_TX1_P
18	DSI_TX1_N
19	DGND
20	DSI_TX0_P
21	DSI_TX0_N
22	DGND

2.10 Audio Codec Interface

AM62P SK EVM houses TI's TLV320AIC3106 Stereo Audio Codec to interface with AM62P via McASP1 group of signals.

TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single ended or fully differential configurations. The record path of the TLV320AIC3106 contains integrated microphone bias, digitally controlled stereo microphone preamplifier and Automatic gain control (AGC) with mix/Mux capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8 kHz to 96 kHz.

1x Standard 3.5mm TRRS Audio Jack connector (J18) Mfr. Part# SJ-43514 is provided for MIC IN and Headphone output. Audio Codec's Line inputs are terminated to test points. The codec can be configured over I2C with device address set to 0x1B.

The Controller Clock input, MCLK to the Audio Codec is provided through a 12.288MHz Oscillator. Audio serial data bus bit clock (BCLK) & Audio serial data bus input and output (DIN & DOUT) are connected to SOC's MCASP1 instance through a Mux/Demux. An AND output of RESETSTATz and a GPIO sourced via IO expander is used to reset the Audio codec.

The TLV320AIC3106 is powered by an analog supply of 3.3 V, a digital core supply of 1.8 V, and a digital I/O supply of 3.3 V.

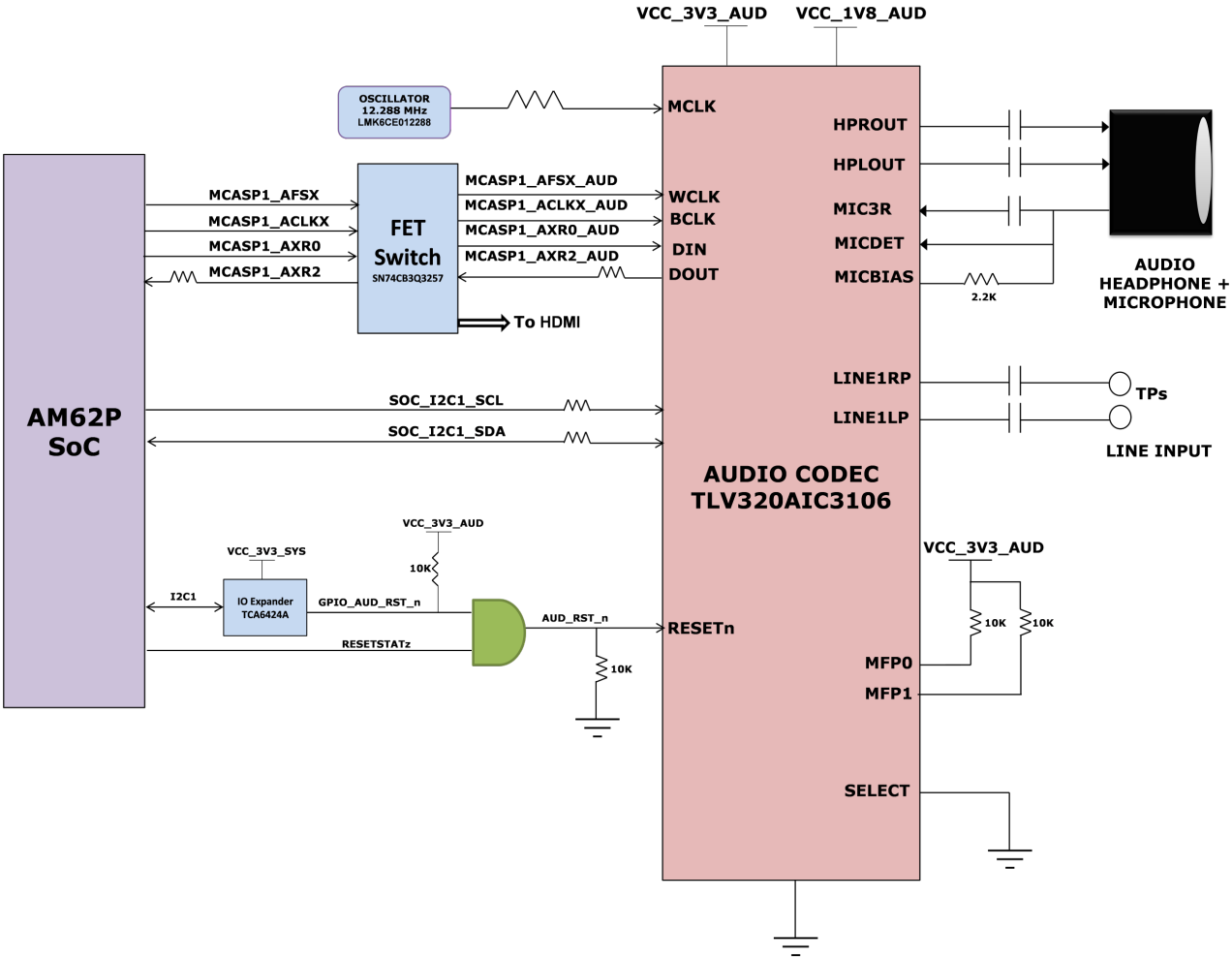

Figure 2-10. Audio Codec Interface

2.11 HDMI Display Interface

The DSS (Display Sub-System) from AM62P SOC is used on the SK EVM to provide HDMI Interface through a standard Type-A Connector. The SK EVM features a SiI9022A HDMI Transmitter from Lattice semiconductor to convert the 24bit Parallel RGB DSS output stream as well as McASP1 signals to a HDMI-compliant digital audio and video signal.

To use SiI9022A, the SOC needs to set up the device. This is done via the I2C1 interface between the SOC and the SiI9022A. SoC_I2C1 instance connected to the HDMI Transmitter accesses the compatible mode registers, the TPI registers, and the CPI registers. Audio Data is sent from the SOC to HDMI transmitter through the McASP1 instance. HDMI_I2C Bus accesses the EDID and HDCP data on an attached sink device.

TMDS Differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through HDMI ESD device Mfr Part# TPD12S016PWR which also acts as a load switch to limit current supplied to the HDMI connector from onboard 5 V supply.

The HDMI Framer is powered using 3.3V Board I/O Supply and 1.2V for the AVCC & DVCC supply by a dedicated LDO Mfr Part# TLV75512PDQNR.

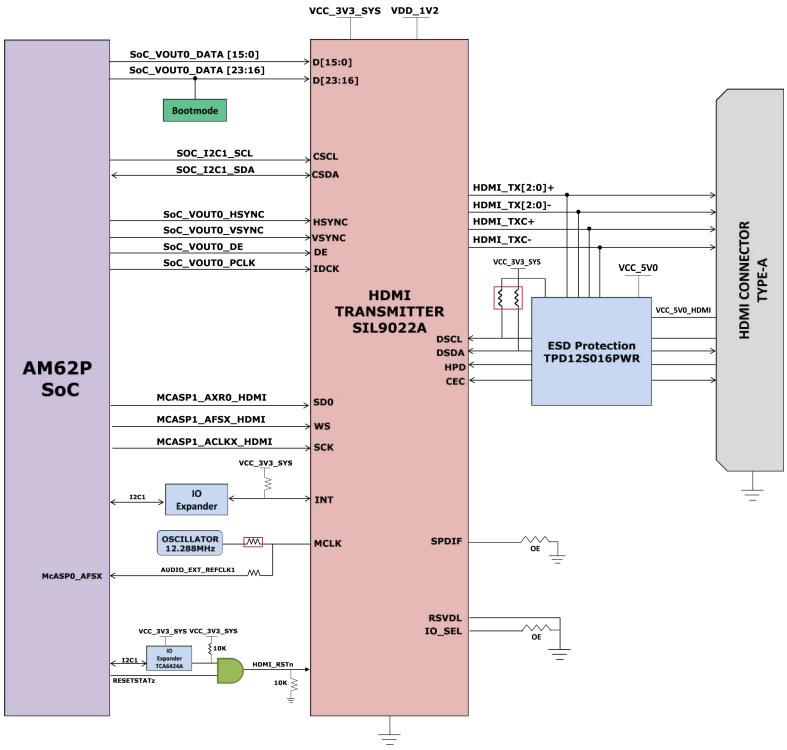

Figure 2-11. HDMI Interface

2.12 JTAG Interface

AM62P SK EVM includes XDS110 class on board emulation. The connection for this emulator uses a standard USB 2.0 micro-B connector and the circuit acts as a Bus powered USB device. The VBUS power from the connector is used to power the emulation circuit such that connection to the emulator is not lost when the power to the SKEVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the SK EVM.

Optionally, JTAG Interface on SK EVM is also provided through a 20 Pin Standard JTAG cTI Header J23. This allows the user to connect an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAGsignals of cTI header from rest of the SK EVM. The output of the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to the AM62P JTAG Interface. If a connection to the cTI 20 Pin JTAG connector is sensed using an auto presence detect circuit, the mux routes the 20 pin signals from the cTI connector to the AM62P SoC in place of the on-board emulation circuit.

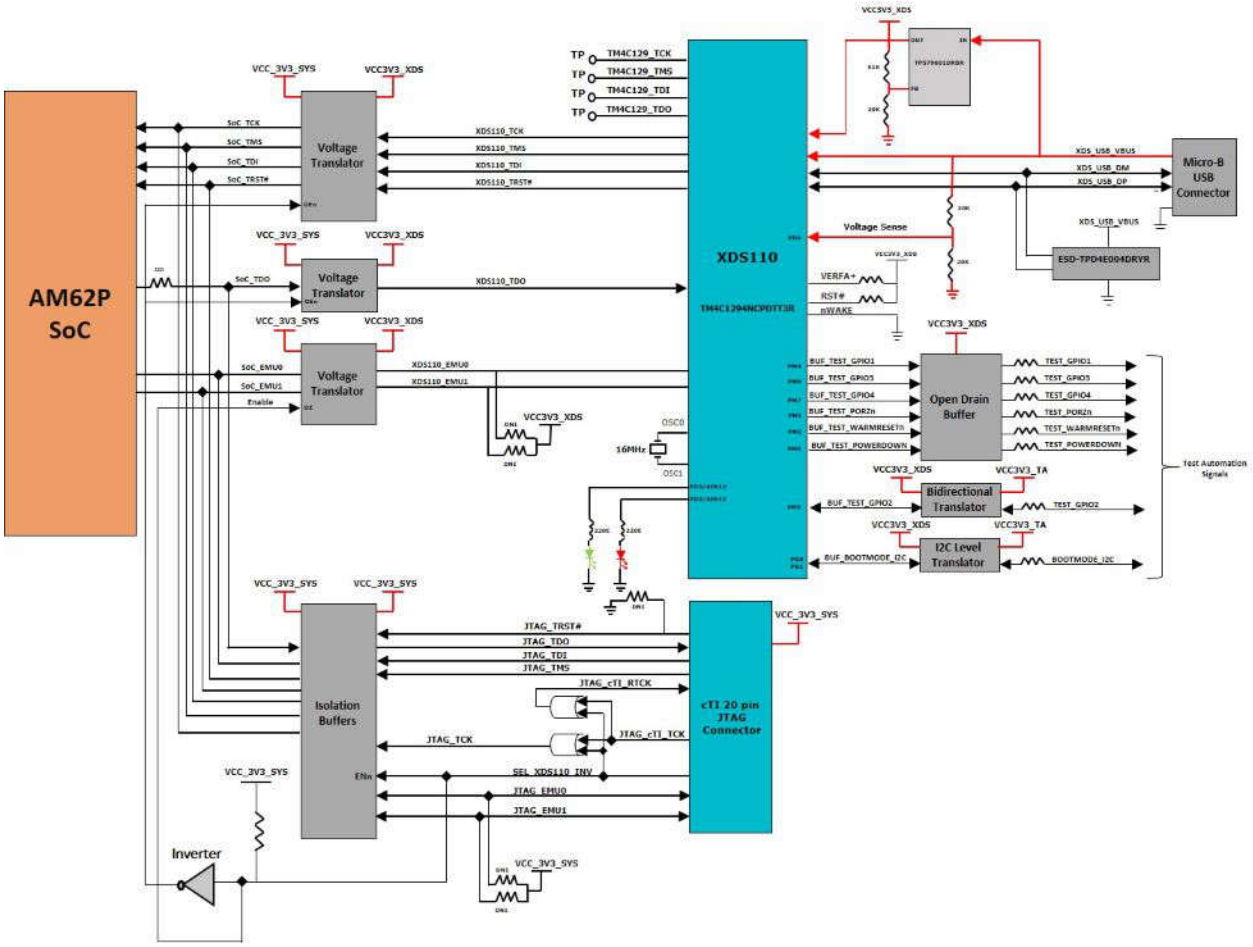

Figure 2-12. JTAG Interface

The pin-outs of the cTI 20 pin JTAG connector are given in the table below. A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15-kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8-kV contact discharge and ±12- kV air-gap discharge.

Table 2-7. JTAG Connector (J23) Pinout

Pin No.	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC_3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

2.13 Test Automation Header

AM62P SK EVM has an optional 40-pin test automation header (FH12A-40S-0.5SH) to allow any external controller to manipulate some basic operations like Power Down, POR, Warm Reset, and Boot Mode control.

The Test Automation Circuit is powered by the 3.3V supply generated by an Always On regulator Mfr. Part# LM5141QRGETQ1. The SOC's I2C1 instance is connected to the test automation header. Another I2C instance (BOOTMODE_I2C) from the Test Automation Header is connected to the 24-bit I2C boot mode IO Expander of Mfr. Part# TCA6424ARGJR to allow control of the boot modes for the AM62P SOC.

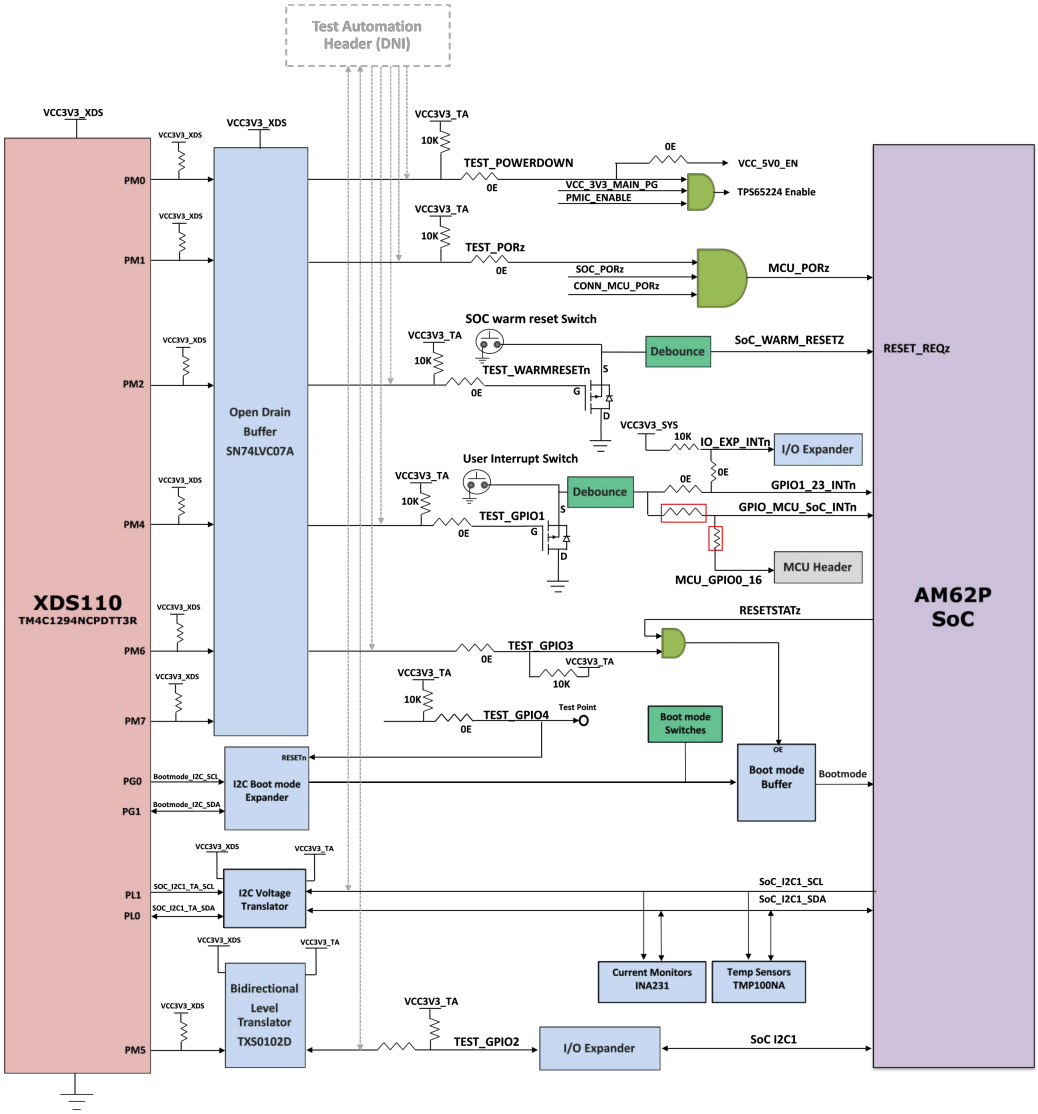

Figure 2-13. Test Automation Interface

The test automation has voltage translation circuits so that the controller is isolated from the I/O voltages used by the AM62P. Boot mode for the AM62P can be user controlled by either using DIP Switches or the test automation header through the I2C I/O Expander. Boot Mode Buffers are used to isolate the Boot Mode controls driven through DIP Switches or I2C I/O Expander. The boot mode can also be set using two 8-bit DIP switches on the board, which connects a pull-up resistor to the output of a buffer when the switch is set to the ON position and to a weaker pull-down resistor when set to OFF position. The outputs of the buffer are connected to the boot mode pins on the AM62P SOC and the output is only enabled when the boot mode is needed during a reset cycle.

When boot mode is to be set through Test Automation header, the required switch values are set at the I2C I/O expander output, which overwrites the DIP switch values to give the desired boot values to the SOC. The pins used for boot mode also have other functions which are automatically isolated by disabling the boot mode buffer during normal operation.

The power down signal from the Test automation header instructs the SK EVM to power down all the rails except for dedicated power supplies on the board. Similarly, PORZn signal provides a hard reset to the SOC and WARM_RESETn for a warm reset to the SOC.

Table 2-8. Test Automation Connector (J29) Pinout

Pin no.	Signal	IO Direction	Pin no.	Signal	IO Direction
1	VCC3V3_TA	Power	21	NC	NA
2	VCC3V3_TA	Power	22	NC	NA
3	VCC3V3_TA	Power	23	NC	NA
4	NC	NA	24	NC	NA
5	NC	NA	25	DGND	Power
6	NC	NA	26	TEST_POWERDOWN	Input
7	DGND	Power	27	TEST_PORZn	Input
8	NC	NA	28	TEST_WARMRESETn	Input
9	NC	NA	29	NC	NA
10	NC	NA	30	TEST_GPIO1	Input
11	NC	NA	31	TEST_GPIO2	Bidirectional
12	NC	NA	32	TEST_GPIO3	Input
13	NC	NA	33	TEST_GPIO4	Input
14	NC	NA	34	DGND	Power
15	NC	NA	35	NC	NA
16	DGND	Power	36	SoC_I2C1_TA_SCL	Bidirectional
17	NC	NA	37	BOOTMODE_I2C_SCL	Bidirectional
18	NC	NA	38	SoC_I2C1_TA_SDA	Bidirectional
19	NC	NA	39	BOOTMODE_I2C_SDA	Bidirectional
20	NC	NA	40	DGND	Power

2.14 UART Interface

The four UART ports of the SOC (MCU UART0, WKUP UART0, SOC UART0 and SOC UART1) are interfaced with an FTDI Bridge FT4232HL for UART-to-USB functionality and then terminated on a USB micro-B connector (J21) on board. When the AM62P SK EVM is connected to a host using USB cable, the computer can establish a Virtual COM Port which can be used with any terminal emulation application. Since FT4232HL device is bus powered the connection to the COM port is not be lost when the SK EVM power is removed.

Table 2-9. UART Port Interface

UART PORT	USB to UART Bridge	USB Connector	COM Port
SOC_UART0	FT4232HL	J21	COM1
SOC_UART1			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in ‘Single chip USB to four channel UART’ mode using the configuration file from an external SPI EEPROM connected. The EEPROM (93LC46B) supports 1 Mbit/s clockrate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

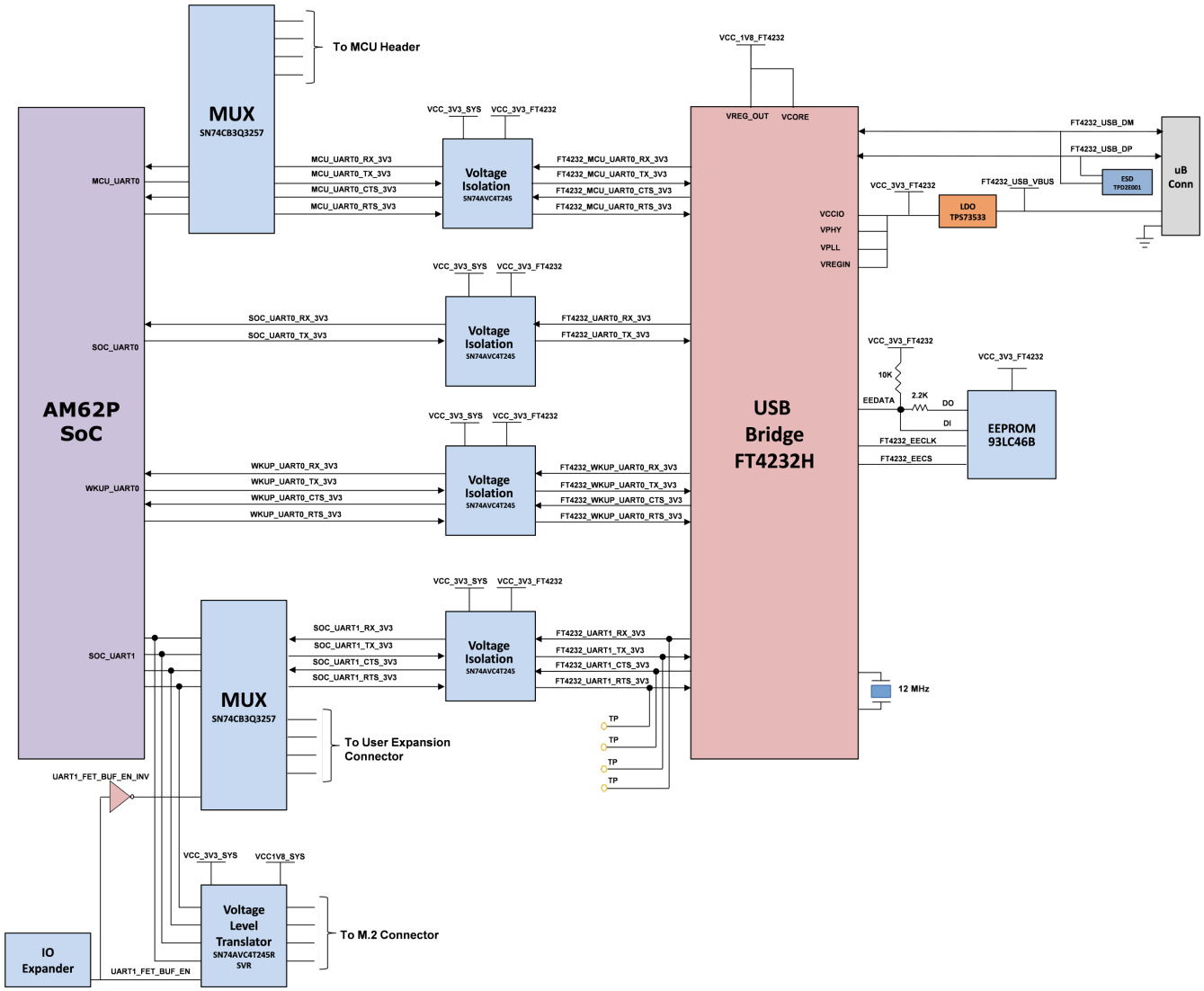

Figure 2-14. UART Interface

2.15 USB Interface

2.15.1 USB 2.0 Type A Interface

USB2.0 data lines DP and DM from Type A connector J9 are connected to the USB1 interface of the AM62P SOC to provide USB high-speed/full-speed communication. USB1_VBUS to the SOC is provided through a resistor divider network to support (5 V-30 V) VBUS operation. USB1_DRVVBUS from SOC controls the enable pin of a 500 mA current limited load switch Mfr Part# TPS2051BDto allow on board 5 V supply to power the VBUS. This load switch has an over current indication pin connected to I2C based GPIO expander on the SK EVM.

A common mode choke of Mfr Part# DLW21SZ900HQ2B is provided on USB Data lines for EMI/ EMC reduction along with ESD protection Mfr Part# TPD4S012DRYR to suppress any transient voltages.

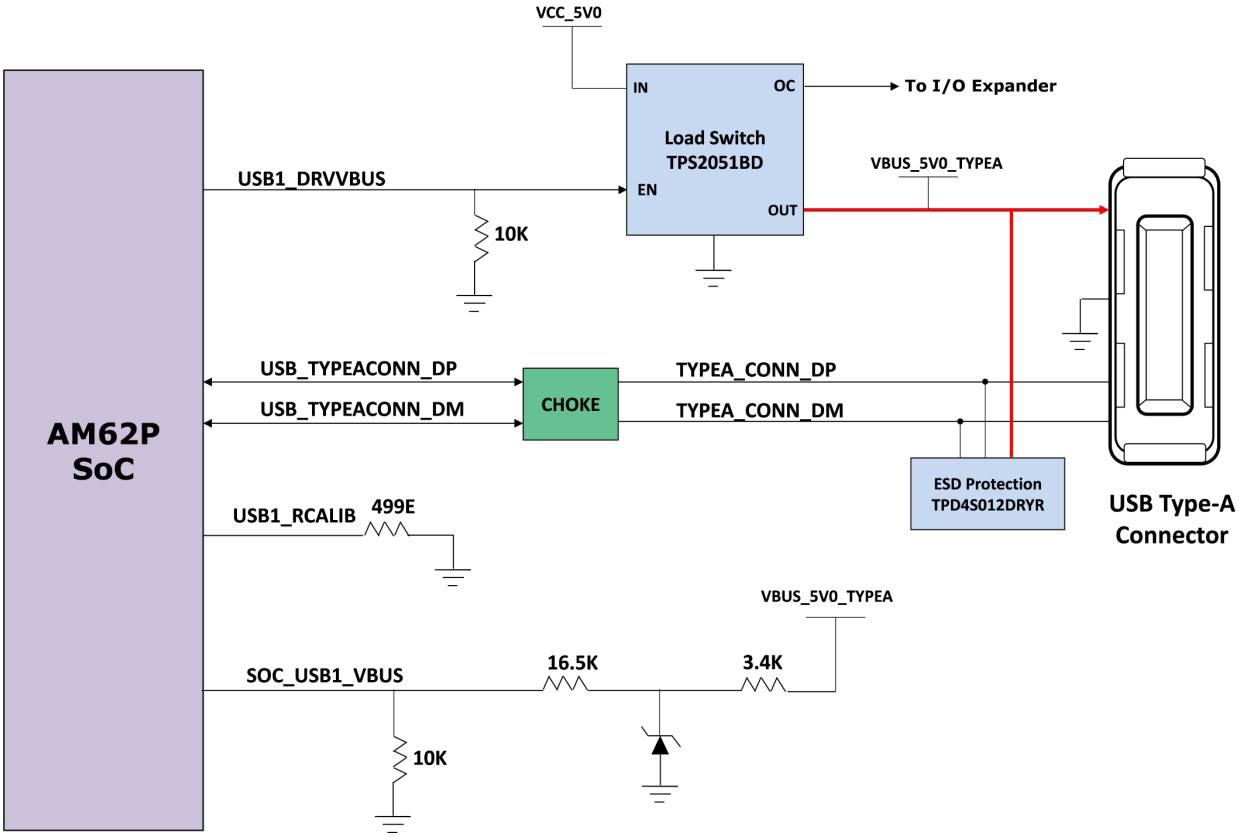

Figure 2-15. USB 2.0 Type A Interface

2.15.2 USB 2.0 Type C Interface

On SK EVM, USB 2.0 Interface is offered through USB Type-C Connector J19 Mfr part# 2012670005 which supports data rate up to 480Mbps. J19 can be used for data communication and as a power connector sourcing supply to the SK EVM. J19 is configured as DRP port using PD controller TPS65988DHRSHR IC. So, J19 can act as either a host or device. The role of the port depends on the type of device getting connected on the connector and the ability to either sink or source. When the port is acting as DFP, DFP can source up to 5 V @ 500 mA.

USB 2.0 data lines DP and DM from J19 are provided with a choke and an ESD protection device. USB0_VBUS to the SOC is provided through a resistor divider network to support (5V-30V) VBUS operation.

A common mode choke of Mfr Part# DLW21SZ900HQ2B is provided on USB data lines for EMI/ EMC reduction. ESD protection devices of part number ESD122DMXR is included to dissipate any ESD strikes on USB2.0 DP/DM signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J19 to dissipate ESD strikes.

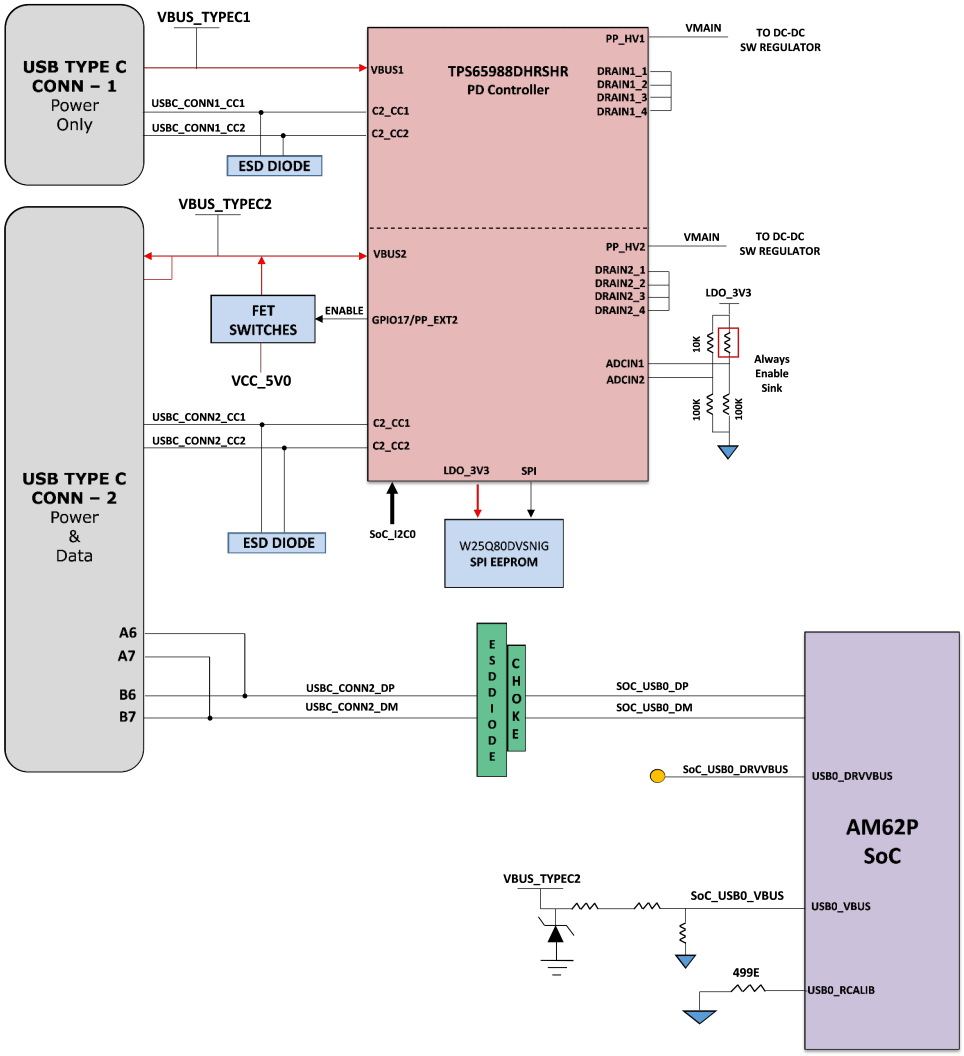

Figure 2-16. USB 2.0 Type C Interface

2.16 Memory Interfaces

2.16.1 LPDDR4 Interface

AM62P SK EVM houses Micron's (MT53E2G32D4DE-046 AUT:C) dual Rank dual Die 8GB, 32-bit wide LPDDR4 memory supporting data rates up to 3200 Mb/s per pin. The LPDDR4 memory is placed routed to the DDR0 group of SOC to support point to point communication.

The LPDDR4 memory requires 1.8V for the core supply, thus reducing power demand. The I/O's are supplied from a 1.1V supply output from the PMIC. LPDDR4 reset (active low) controlled by the AM62P SOC is pulled down to set the default active state. The provision for mounting a pull up resistor is also provided.

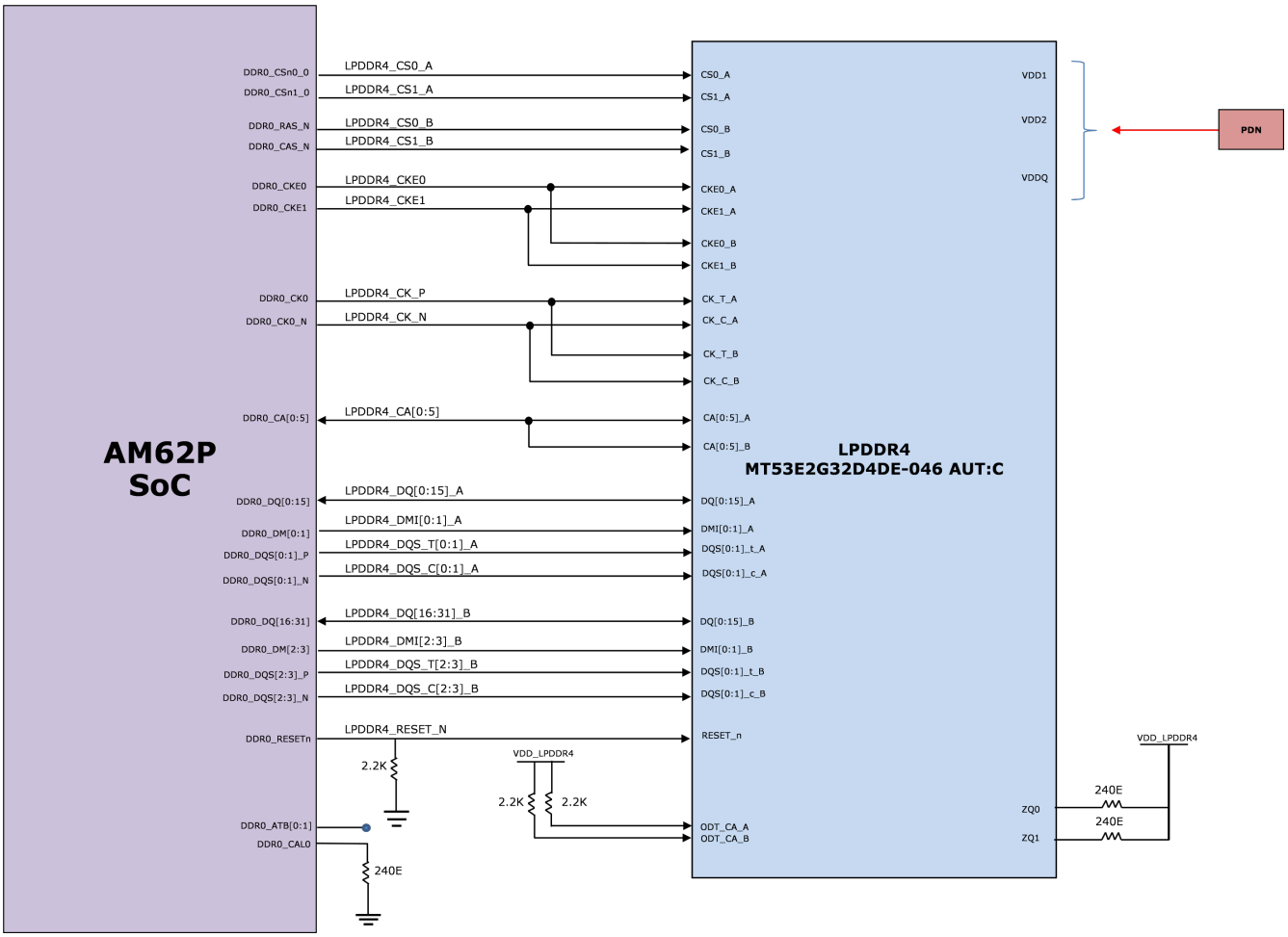

Figure 2-17. LPDDR4 Interface

2.16.2 OSPI Interface

AM62P SK EVM board features a 512Mb OSPI memory device from Cypress Part# S28HS512TGABHM010 connected to the OSPI0 interface of the AM62P SOC. The OSPI memory supports single and double data rates with memory speeds up to 200MBps SDR and 400MBps DDR (200 MHz clock speed).

OSPI & QSPI implementation: 0 ohm resistors are provided for DATA[7:0], DQS, INT# and CLK signals. External pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0 ohm series resistors provided for pins OSPI_DQ[4:7] can be removed if a QSPI Flash is to be mounted.

Reset: The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the AM62P with the signal GPIO_OSPI_RSTn from the SOC GPIO. A pull-up resistor is provided on GPIO_OSPI_RSTn to set the default active state.

Power: Both VCC and VCCQ pins of the OSPI Flash memory is supplied through an on board 1.8V system power. The OSPI I/O group is powered by the VDDSHV1 domain of SOC sourced from the same 1.8V system power.

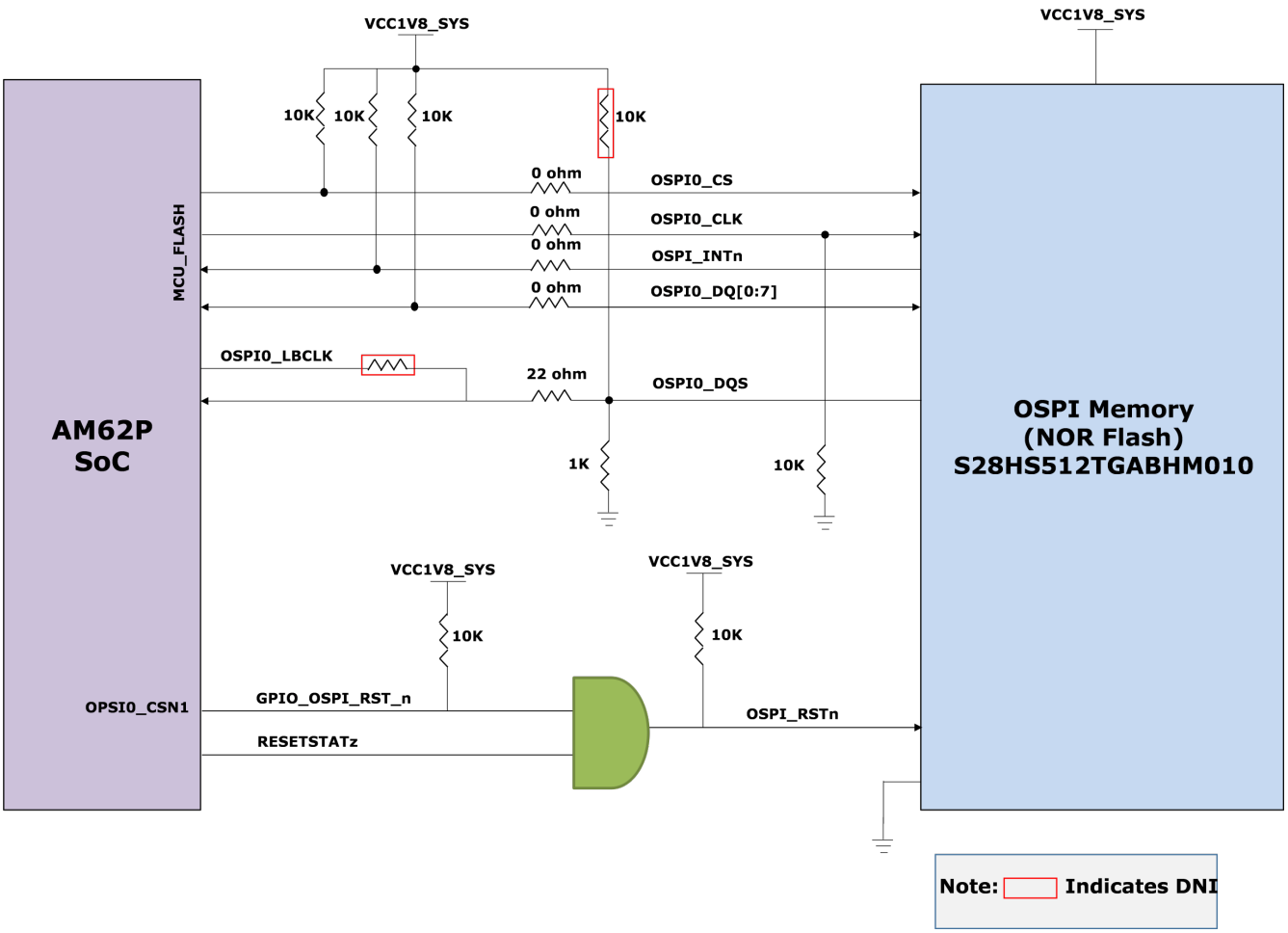

Figure 2-18. OPSI Interface

2.16.3 MMC Interfaces

AM62P SOC features three MMC ports (MMC0, MMC1 and MMC2). MMC0 is connected to eMMC, MMC1 is interfaced with a Micro SD Card connector and MMC2 is terminated to a M.2 Key E expansion connector for Wi-Fi and BT Module Interface.

2.16.3.1 MMC0 - eMMC Interface

The SK EVM board contains 32GB of eMMC flash memory from Micron Part# MTFC32GAZAQHD-IT connected to the MMC0 port of AM62P SOC.

The data bus from the flash memory is connected to the 8 data bits of the MMC0 interface supporting HS400 double data rates up to 200 MHz. The Micron eMMC is a communication and mass data storage device that includes a Multimedia Card (MMC) interface and a NAND Flash component. Option to mount external pull up resistors are provided on DAT[7:1] to prevent bus floating and series resistor is provided for CLK signal close to SOC pad to match the characteristic impedance.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0 I/O's of the SOC are powered by VDDS_MMC0 supplied from an fixed 1.8V supply.

eMMC device requires active low reset from host. By default, the RST_n signal is temporarily disabled in the device. The host must set ECSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use. The External Reset is provided by ANDing RESETSTATz from SOC and a GPIO from IO Expander. A pull up is provided on GPIO pin to set the default active state.

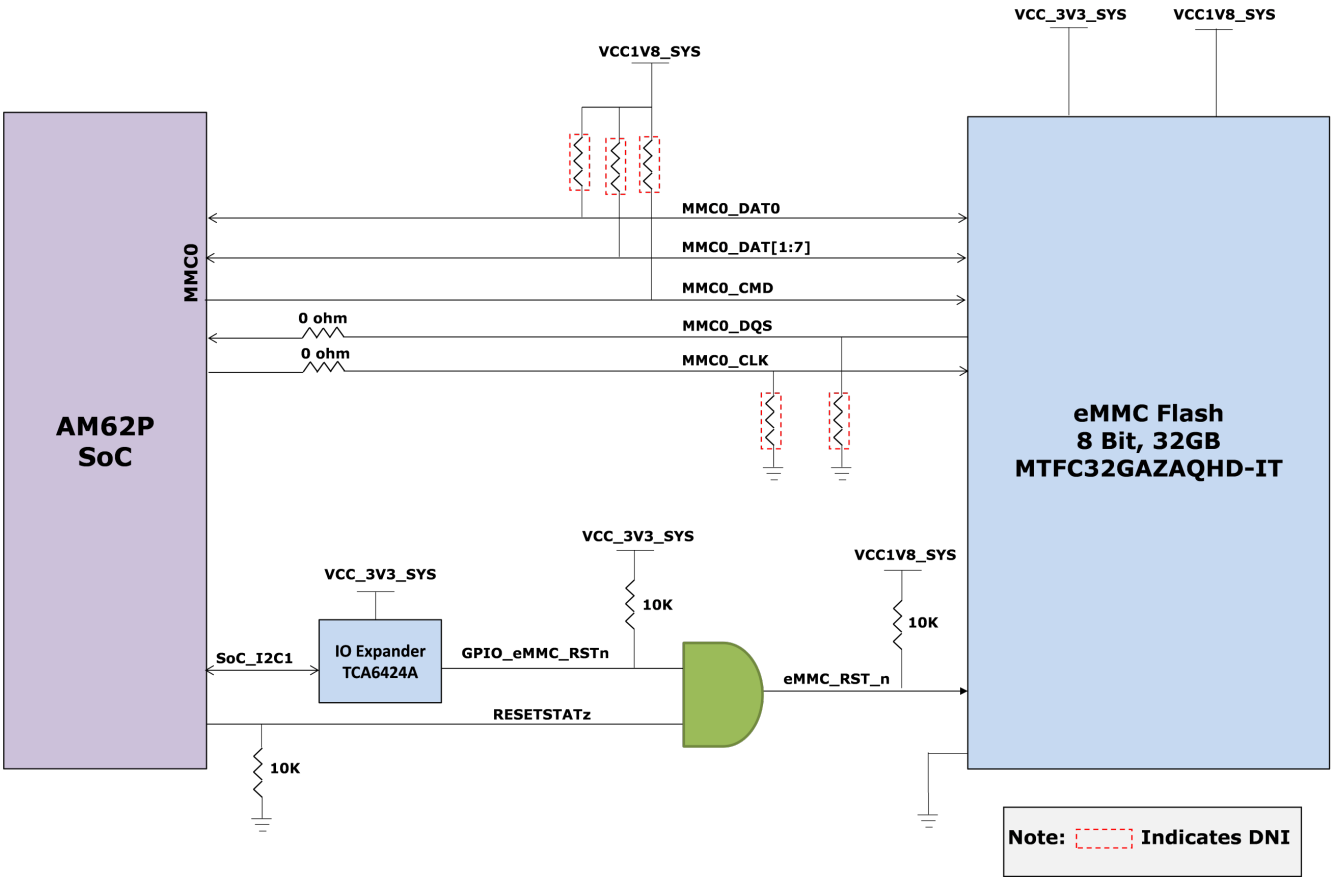

Figure 2-19. eMMC Interface

2.16.3.2 MMC1 - Micro SD Interface

The SK EVM provides a micro SD card socket of Mfr. Part# MEM2051-00-195-00-A connected to the MMC1 port of AM62P SOC. This supports UHS1 operation including I/O operations at both 1.8V and 3.3V. The Micro SD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SOC attempts to find the fastest speed that the card and controller can support and then have a transition to 1.8V through a VSEL_SD_SOC signal from the SOC.

TheSD Card connector power is provided using a load switch of Mfr. Part # TPS22918DBVR, which is controlled by ANDing the output of RESETSTATz, PORz_OUT and a GPIO from IO Expander.

An ESD protection device of part number TPD6E001RSE is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ± 8-kV contact discharge and ± 15kV air-gap discharge.

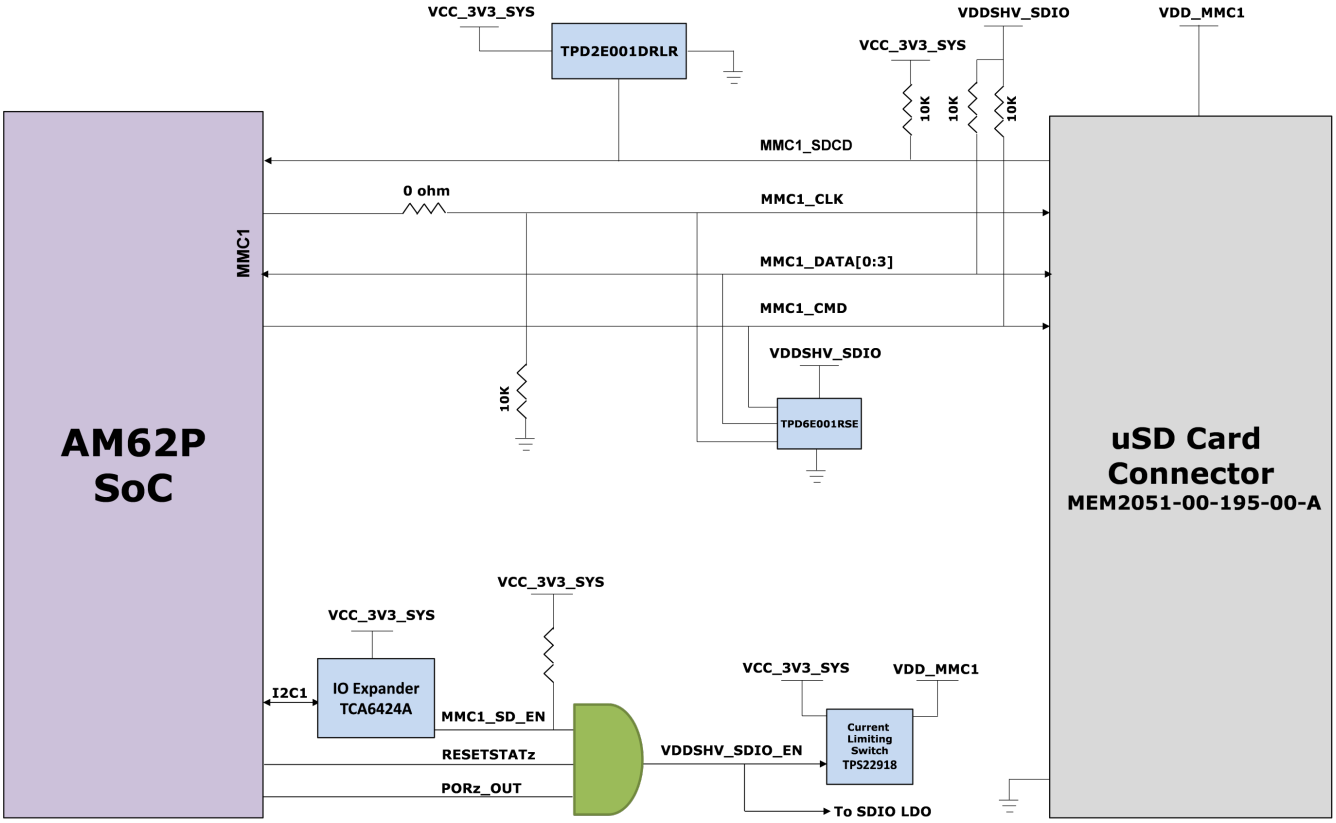

Figure 2-20. uSD Interface

2.16.3.3 MMC2 - M.2 Key E Interface

AM62P SK EVM has a M.2 Key E expansion for connecting WiFi/BT modules to MMC2, UART2 and McASP1 interface through buffers. This can be used to interface with a Wi-Fi, dual-band, 2.4 and 5-GHz module with antennas supporting Industrial temperature grade. The M.2 is provided with 4-bit I/O's of the MMC2 interface supporting IEEE standard 802.11a/b/g/n data. The M.2 connector can be interfaced with modules that can offer high throughput and extended range along with Wi-Fi and Bluetooth coexistence for a power-optimized design.

The M.2 Connector is provided with a 3.3 V on board power supply to meet the power supply requirements of the interfacing modules. The MMC2 interface of the SOC is powered by the VDDSHV6 power domain, which is connected to 1.8V IO supply.

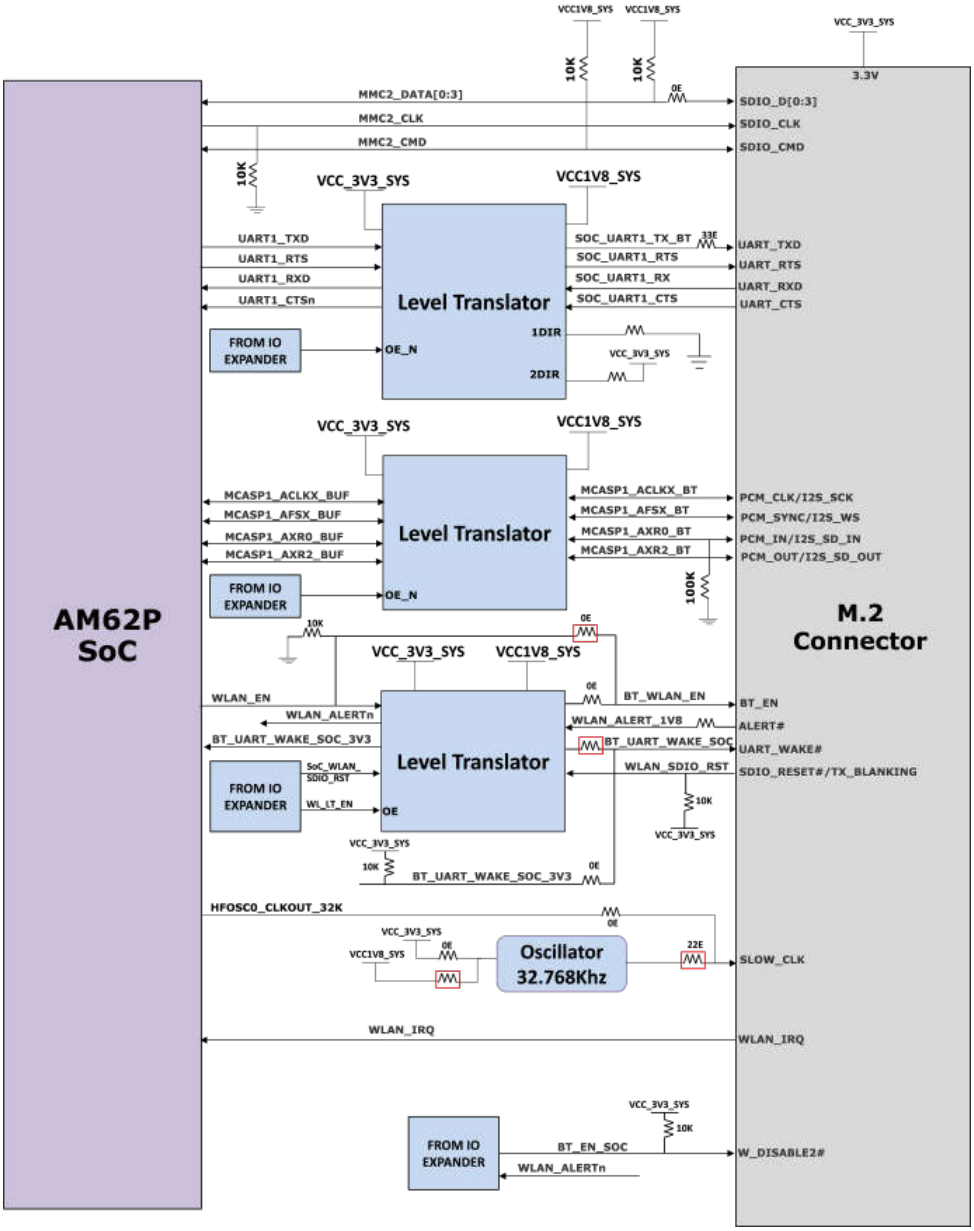

Figure 2-21. M.2 Interface

2.16.4 Board ID EEPROM

AM62P SK- EVM can be identified remotely from the version and serial number data stored on the onboard EEPROM.

Board ID memory AT24C512C-MAHM-T from Microchip is interfaced to the I2C0 port of the SOC and is configured to respond to address 0x51 programmed with the header description. I2C address of the EEPROM can be modified by driving the A0 pin to high and A1, A2 pins to LOW. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

Note

Header J3 must be shorted with a jumper to perform a write operation.

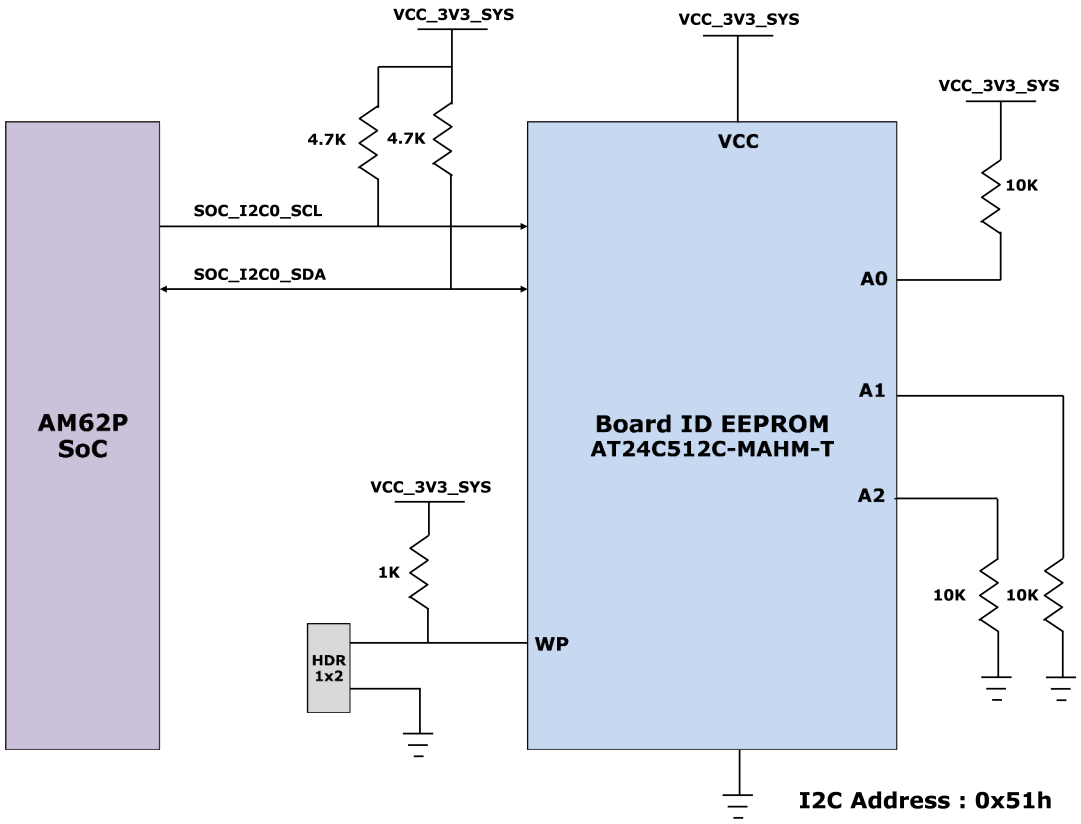

Figure 2-22. Board ID EEPROM Interface

2.17 Ethernet Interface

The AM62P SK EVM offers two Ethernet Ports of 1 Gigabit Speed for external Communication. Two channels of RGMII Gigabit Ethernet CPSW Ports from AM62P SoC are connected to separate Gigabit Ethernet PHY Transceivers DP83867, which are finally terminated on two RJ45 connectors with integrated magnetics.

The 48pin version of the PHY DP83867 is configured to advertise 1Gb operation with the Tx & Rx clock skew set to accommodate the internal delay inside the AM62P. CPSW_RGMII1 and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

Two Single port RJ45 Connectors Mfr Part# LPJG16314A4NL from Link-PP are used on the board for Ethernet 10/100/1000 Mbps Connectivity. RJ45 Connectors have integrated magnetics and LEDs for indicating 1000BASE-T link as well as receive or transmit Activity.

I/O supply to the Ethernet PHY is set 3.3V IO level.

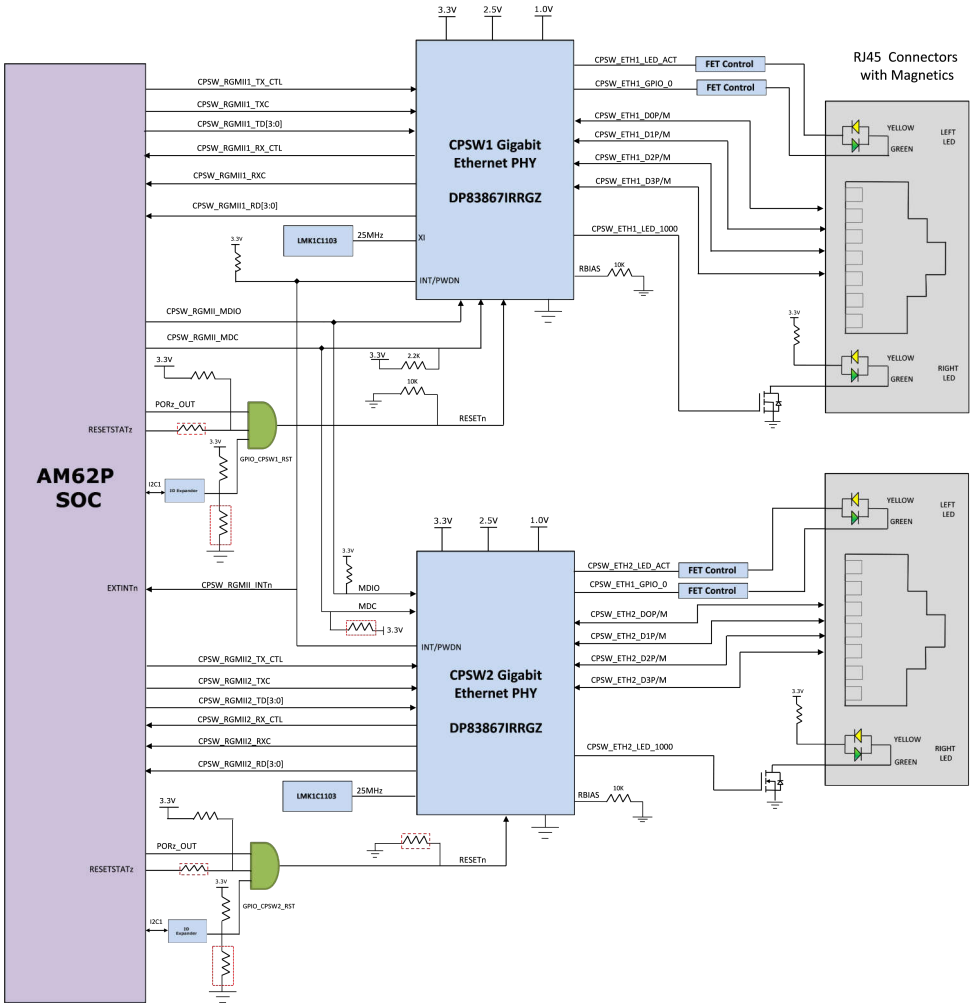

Figure 2-23. Ethernet Interface

2.17.1 CPSW Ethernet PHY Strapping

The default configuration of the DP83867 is determined using several resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes. The AM62P SK EVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltage ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

Mode1 - 0 V to 0.3V

Mode 2 – 0.462V to 0.6303V

Mode3 – 0.7425V to 0.9372V

Mode4 – 2.2902V to 2.9304V

Footprint for both pull-up and pull-down is provided on all the strapping pins except LED_0. LED_0 is for mirror enable, which is set to mode 1 by default, Mode 4 is not applicable, and Mode 2 and Mode 3 option is not desired.

2.17.2 CPSW Ethernet PHY1 Default Configuration

PHY ADDR: 00000

Auto_neg: Enabled

ANG_SEL: 10/100/1000

RGMII TXCLK skew: 0 ns

RGMII RXCLK skew: 2 ns

2.17.3 CPSW Ethernet PHY2 Default Configuration

PHY ADDR: 00001

Auto_neg: Enabled

ANG_SEL: 10/100/1000

RGMII TXCLK skew: 0 ns

RGMII RXCLK skew: 2 ns

2.18 GPIO Port Expander

The I/O Expanders used in the AM62P SK EVM are 24-Bit I2C based I/O Expander which is used for daughter cards plug-in detection and for generating resets and enable signals to various peripheral devices connected onboard. The SoC_I2C1 bus of the AM62P SOC is used to interface with the I/O Expanders. The I2C device addresses of the I/O Expanders are 0x21 and 0x23. See below tables for the list of signals being controlled by the expanders.

Table 2-10. IO Expander 1 Signal Details

Pin No.	Signal	Direction	Purpose
P00	OLDI_INT#	INPUT	Interrupt from OLDI display
P01	x8_NAND_DETECT	INPUT	x8 NAND Card Presence Detect
P02	UART1_FET_SEL	OUTPUT	UART1 FET selection
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_EN	OUTPUT	SOC eFuse Voltage (VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	UART1_FET_BUF_EN	OUTPUT	SOC UART1 Mux Select
P07	EXP_HAT_DETECT	INPUT	EXP CONN HAT Board Detection
P10	DSI_GPIO0	BIDIRECTIONAL	DSI Display GPIO0
P11	DSI_GPIO1	BIDIRECTIONAL	DSI Display GPIO1
P12	OLDI_EDID	INPUT	OLDI to HDMI Card Device ID interrupt
P13	BT_UART_WAKE_SOC_3V3	INPUT	BT UART WKUP Signal
P14	USB_TYPEA_OC_INDICATION	INPUT	USB Type A overcurrent indicator
P15	CSI_GPIO0	BIDIRECTIONAL	CSI Camera GPIO1
P16	CSI_GPIO1	BIDIRECTIONAL	CSI Camera GPIO2
P17	WLAN_ALERTn	INPUT	M.2 Module WLAN Alert Input
P20	HDMI_INTN	INPUT	HDMI Interrupt
P21	TEST_GPIO2	BIDIRECTIONAL	TEST GPIO2 from Test Automation Connector
P22	MCASP1_FET_EN	OUTPUT	MCASP1 Enable and Direction Control
P23	MCASP1_BUF_BT_EN	OUTPUT	
P24	MCASP1_FET_SEL	OUTPUT	
P25	DSI_EDID	INPUT	DSI to HDMI Card Device ID interrupt
P26	PD_I2C_IRQ	INPUT	Interrupt Request from PD Controller
P27	IO_EXP_TEST_LED	OUTPUT	User Test LED 2

Table 2-11. IO Expander 2 Signal Details

Pin No.	Signal	Direction	Device
P00	BT_EN_SOC	OUTPUT	M.2 module Bluetooth LDO Enable
P01	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5 V power switch enable
P10	WL_LT_EN	OUTPUT	M.2 interface level translator enable
P20	SoC_I2C2_MCAN_SEL	OUTPUT	SoC I2C2 & MCAN MUX selection
P21	GPIO_HDMI_RSTn	OUTPUT	HDMI transmitter reset control GPIO
P22	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 reset control GPIO
P23	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 reset control GPIO
P24	GPIO_OLDI_RSTn	OUTPUT	OLDI display reset control GPIO
P25	GPIO_AUD_RSTn	OUTPUT	Audio codec reset control GPIO
P26	GPIO_eMMC_RSTn	OUTPUT	eMMC Reset control GPIO
P27	SOC_WLAN_SDIO_RST	OUTPUT	M.2 Module WLAN/SDIO Reset

2.19 GPIO Mapping

Table 2-12 describes the detailed GPIO mapping of AM62P SOC with AM62P SK EVM peripherals.

Table 2-12. GPIO Mapping

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAINON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	MCU Interrupt	MCU_INTn	INTERRUPT	MCU_GPIO0_0	MCU_SPI0_CS0	INPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
9	PMIC Interrupt	PMIC_INTn	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
11	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
12	User test LED control signal	SOC_GPIO1_49	ENABLE	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	User Interrupt									
15	Low power mode enable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
16	SD Card I/O Voltage Selection	VSEL_SD_SOC	SELECTION	GPIO0_31	GPMC0_CLK	OUTPUT	NA	NA	VDDSHV2	SoC_DVDD3V3
IO EXPANDER – 01										
1	Interrupt from OLDI display	OLDI_INT#	INTERRUPT	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	x8 NAND Card Presence Detect	x8_NAND_DETECT	DETECTION	IO EXPANDER-P01		INPUT	HIGH	LOW		VCC_3V3_SYS
3	UART1 FET selection control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	-		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS

Table 2-12. GPIO Mapping (continued)

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAINON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
9	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
10	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
11	OLDI to HDMI Card Device ID interrupt	OLDI_EDID	INTERRUPT	IO EXPANDER-P12		INPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	USB Type A overcurrent indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		BIDIRECTIONAL	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22	DSI to HDMI Card Device ID interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
2	EXP CONN 5 V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P01		OUTPUT	LOW	HIGH		VCC_3V3_SYS
3	M.2 Interface Level Translator Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SoC I2C2 & MCAN MUX Selection	SoC_I2C2_MCAN_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	HIGH	-		VCC_3V3_SYS
5	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_SYS
6	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
7	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_SYS

Table 2-12. GPIO Mapping (continued)

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAINON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
8	OLDI display Reset control GPIO	GPIO_OLDI_RSTn	RESET	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS

2.20 Power

2.20.1 Power Requirement

AM62P SK EVM can be powered through either of the two USB Type C Connectors,

- Connector1 (J17) - Power role – SINK, No Data role
- Connector2 (J19) - Power role – DRP, Data role – USB 2.0 DFP or UFP

The AM62P SK EVM supports voltage input ranges of 5 V - 15 V and 3 A of current. A USB PD controller Mfr. Part# TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port, and can act as DFP only when the board is being powered by Connector 1. When both the connectors are connected to external power supply, the port with highest PD power contract are selected to power the board.

Table 2-13. Type C Port Power Roles

J17 (UFP)	J19 (DRP)	Board Power	Remarks
Plugged in	NC	ON - J17	J17 are UFP and only sinks power & J19 can act as DFP if a peripheral is connected.
NC	Plugged in	ON - J19	J19 is UFP and can only sink power.
Plugged in	Plugged in	ON- J17 or J19	Board is powered by the port with highest PD power contract.

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so SPI EEPROM can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J15. Once the EEPROM is programmed the PD obtains the configuration files via SPI communication. Upon loading the configuration file, the PD negotiates with the source to obtain the necessary power requirement.

Note

The EEPROM is pre-programmed with the configuration file for the operation of the PD controller.

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the SK EVM board. An external power supply (Type-C output) can be used to power the EVM but is not included as part of the SK EVM kit.

The external power supply requirements (Type-C) are:

Table 2-14. Recommended External Power Supply

DigiKeyPart#	Manufacturer	Manufacturer Part #
1939-1794-ND	GlobTek, Inc.	TR9CZ3000USBCG2R6BF2
Q1251-ND	Qualtek	QADC-65-20-08CB

Note

Minimum voltage: 5 VDC, Recommended minimum current: 3000 mA, Maximum voltage: 15VDC, Maximum current: 5000 mA. Since SK-AM62P-LP implements USB PD for power, the device can negotiate to the highest voltage and current combination supported by both the device and power adapter. Therefore, if the power supply exceeds the maximum voltage and current requirements listed above, then the power supply is acceptable as long as the power adapter is compliant with the USB-C PD specification.

2.20.2 Power Input

Both Type-C Connectors (VBUS and CC lines) are connected to a Dual PD controller Mfr Part# TPS65988. The TPS65988 is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5 V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 pin of the PD controller along with a resistor option to also enable using USB0 DRVVBUS from AM62P SOC.

TPS65988 PD controller can provide an output of 3 A (15 V max) through CC negotiation. The VBUS pins from both the Type C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN which is supplied to on board Buck-Boost and Buck regulators to generate fixed 5 V and 3.3V supply for the SK EVM.

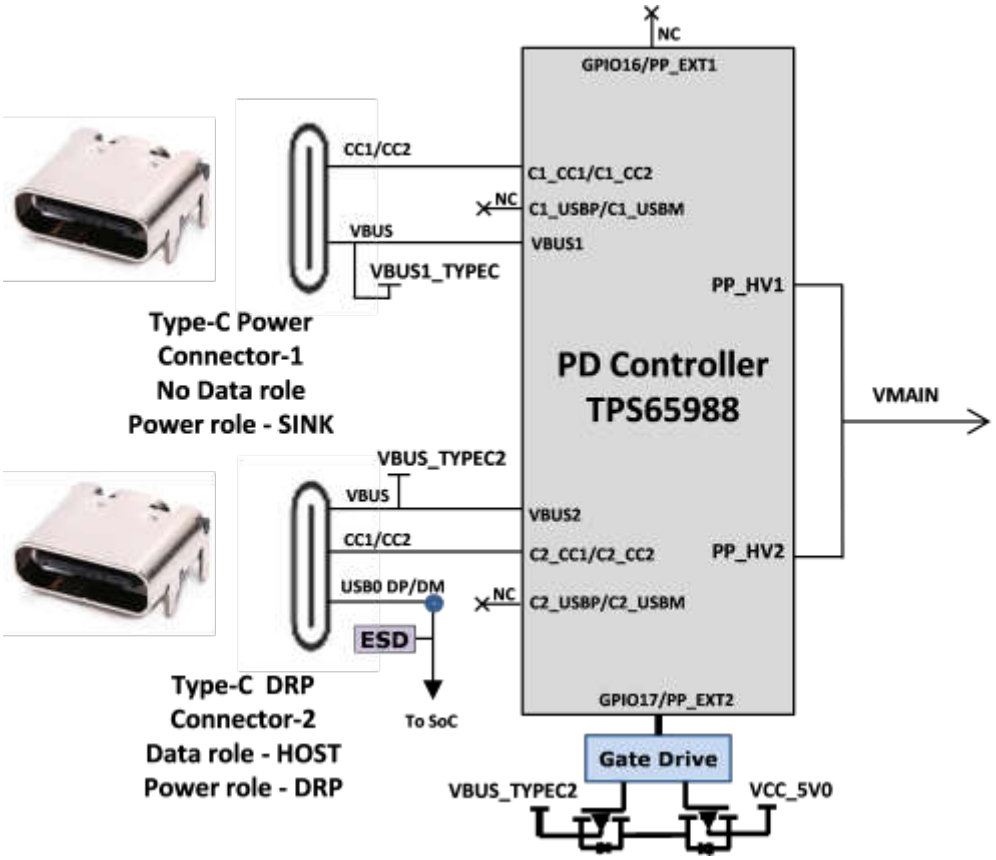

Figure 2-24. Power Input

2.20.3 Power Supply

AM62P SK EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SOC and other components/peripherals on the board with the necessary voltage and the power required.

The figure below figure shows the various discrete regulators, PMIC and LDOs used to source power rails for each peripheral on AM62P SK EVM.

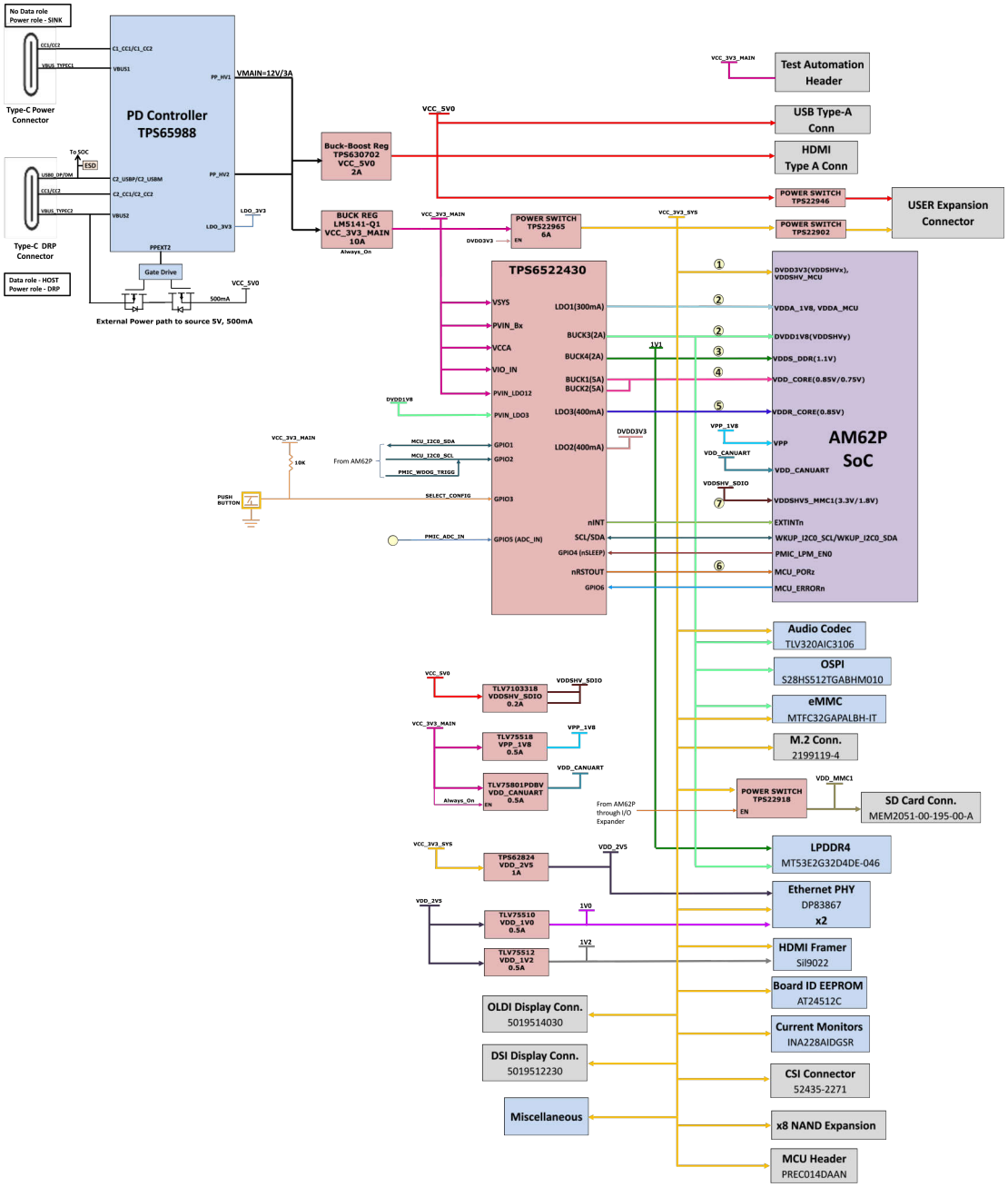

Figure 2-25. Power Architecture

The following sections describe the power distribution network topology that supplies the SK EVM board, supporting components and reference voltages.

The AM62P SK EVM includes a power design based on discrete power supply components. The initial stage of the power supply is VBUS voltage from either of the two USB Type C connectors J17 and J19. USB Type-C Dual PD controller of Mfr. Part# TPS65988DHRSHR is used for negotiation of the required power to the system.

Buck-Boost controller TPS630702RNMR and Buck converter LM5141-Q1 are used for the generation of 5 V and 3.3V respectively and the input to the regulators is the PD output, VMAIN. These 3.3V and 5 V are the primary voltages for the AM62P SK EVM board power resources. The 3.3V supply generated from the Buck regulator LM5141-Q1 is the input supply to the PMIC, various SOC regulators and LDOs. The 5 V supply generated from the Buck Boost regulator TPS630702RNMR is used for powering the onboard peripherals.

Discrete regulators and LDOs used on board are:

- TPS62824DMQR– To generate VDD_2V5 rail for Ethernet PHYs
- TLV75510PDQNR– To generate VDD_1V0 for Ethernet PHYs
- TLV75512PDQNR– To generate VDD_1V2 for HDMI Framer
- PTPS6522430RAHRQ1 (PMIC) – To generate various SOC and Peripheral supplies
- TLV75801PDBVT LDO - VDD_CANUART power of SOC
- TPS79601LDO - XDS110 On board emulator
- TPS73533LDO - FT4232 UART to USB Bridge
- TLV7103318 LDO - To generate VDDSHV5_MMC1 (SD interface) supply for SOC
- TLV75518 LDO - e-Fuse programming of SOC

Additionally,GPIO (TEST_POWERDOWN) is connected to the ENABLE pin of PMIC to control ON/OFF of the SK EVM via XDS110/Test automation. GPIO also disables the VCC_5V0 output of TPS630702RNMR from which several other power supplies are derived.

2.20.4 Power Sequencing

The figure below shows the Power Up sequence of the AM62P SOC power supplies.

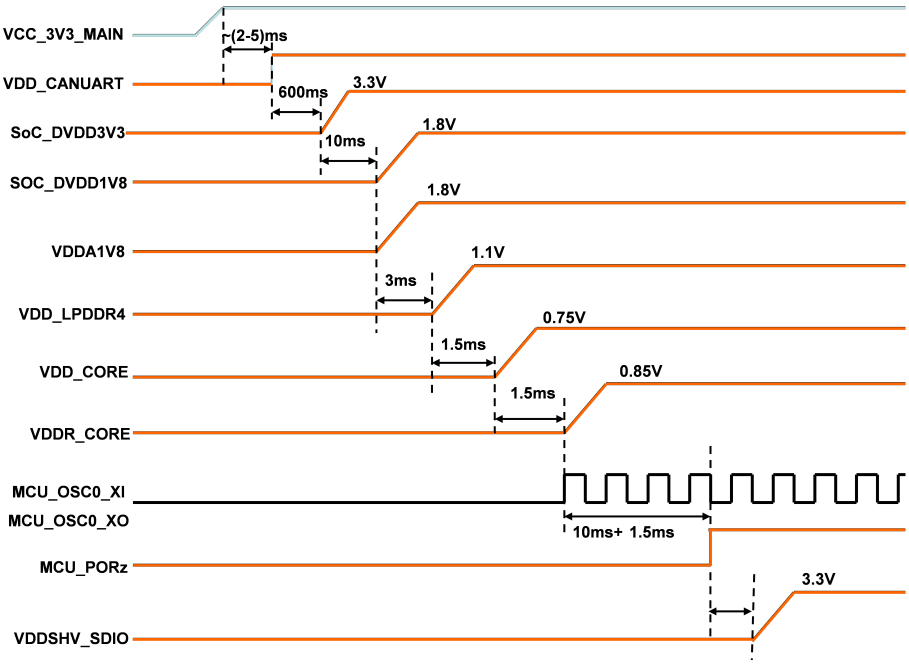

Figure 2-26. Power Sequence

2.20.5 AM62P SoC Power

The core voltage of the AM62P SOC can be 0.75 V or 0.85 V based on the PMIC Configuration and on the power optimization requirement. By default, the PMIC is configured to supply VDD_CORE at 0.85V, however the PMIC can be changed to 0.75V by removing R157. Current monitors are provided on all the SOC Power rails.

The SOC has different I/O groups. Each I/O group is powered by specific power supplies as listed in Table 2-15.

Table 2-15. SoC Power Supplies

SL. No.	Power Supply	SoC Supply Rail	IO Power Group	Voltage
1	VDD_CORE	VDD_CORE	CORE	0.75/0.85
		VDDA_CORE_CSI_DSI	CSI & DSI	
		VDDA_CORE_DSI_CLK	DSI	
		VDDA_DDR_PLL0	DDR PLL	
		VDDA_CORE_USB	USB	
2	VDD_CANUART (Always ON)	VDD_CANUART	CANUART	0.75/0.85
3	VDDR_CORE	VDDR_CORE	CORE	0.85
		VDD_MMC0	MMC0	
		VDDS_DLL_MMC0	MMC0	
4	VDDA_1V8	VDDA_1P8_CSI_DSI	CSI & DSI	1.8
		VDDA_1P8_OLDI0	OLDI	
		VDDA_MCU	MCU	
		VDDS_OSC0	OSC0	
		VDDA_PLL[0:4]	PLL	
		VDDA_TEMP[0:2]	TEMP	
		VDDA_1P8_USB	USB	
5	VDD_LPDDR4	VDDS_DDR	DDR0	1.1
		VDDS_DDR_C		
6	CAN_IO_3V3 (Always ON)	VDDSHV_CANUART	CANUART	3.3
7	VPP_1V8	VPP_1V8		1.8
8	SOC_VDDSHV5_SDIO	VDDSHV5	MMC1	3.3/1.8
9	SOC_DVDD1V8	VDDSHV1	OSPI	1.8
		VDDS_MMC0	MMC0	
		VDDSHV6	MMC2	
		VMON_1P8_SOC		
10	SOC_DVDD3V3	VDDSHV0	GENERAL	3.3
		VDDSHV2	GEMAC	
		VDDSHV3	GPMC	
		VDDSHV_MCU	MCU GENERAL	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.20.6 Current Monitoring

INA228 power monitor devices are used to monitor current and voltage of various power rails of AM62P SOC. The INA228 interfaces to the AM62P SOC through I2C interface (SoC_I2C1). Four terminal, high precision shunt resistors are provided to measure load current.

Note

The design supports current/voltage measurements using either INA228 or INA231. INA228 is only populated on the SK (Implemented via stacked PCB footprint).

Table 2-16. INA I2C Device Address

Source	Supply Net	Device Address	Value of the Shunt
VCC_CORE	VDD_CORE	0x40	1 mΩ ± 1%
VDD_CORE_0V85	VDDR_CORE	0x41	10 mΩ ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10 mΩ ± 1%

Table 2-16. INA I2C Device Address (continued)

Source	Supply Net	Device Address	Value of the Shunt
VCC1V8_SYS	SoC_DVDD1V8	0x45	10 mΩ ± 1%
VDDA1V8	VDDA_1V8	0x4D	10 mΩ ± 1%
VCC1V1	VDD_LPDDR4	0x47	1 mΩ ± 1%

2.21 EVM User Setup/Configuration

2.21.1 DIP Switches

AM62P SK EVM has two 8 position DIP Switches to set the desired SOC Boot mode.

2.21.2 Boot Modes

The boot mode for the SK EVM is defined by two banks of switches SW4 and SW5 or by the I2C buffer connected to the Test automation (XDS110 & Header). This allows for AM62P SOC Boot mode control by either the user (DIP Switch Control) or by the Test Automation.

All the bits of switch (SW4 & SW5) have a weak pull down resistor and a strong pull up resistor. Note that OFF setting provides a low logic level (‘0’) and an ON setting provide a high logic level (‘1’).

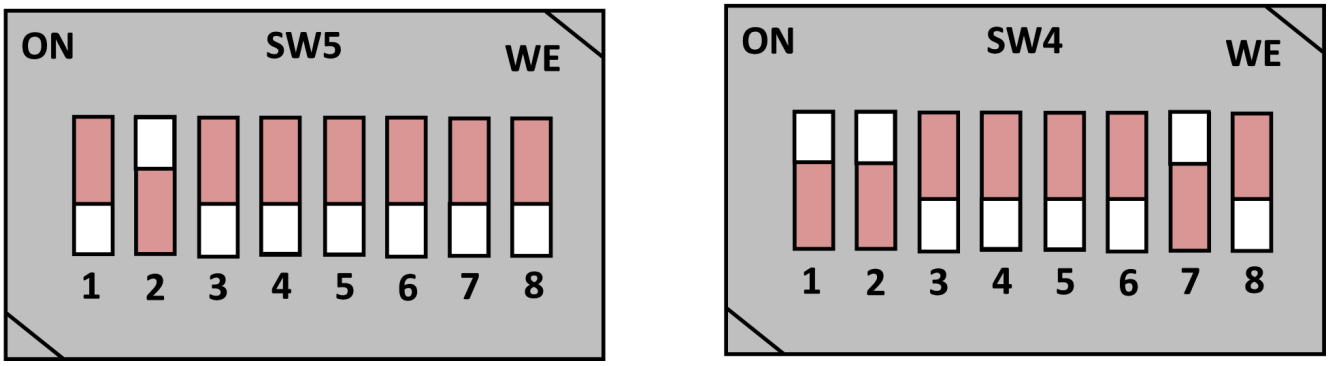

Figure 2-27. Boot Mode Switch (MMCSD Boot)

The boot mode pins of the SOC have associated alternate functions during normal operation. Hence isolation is provided using Buffer IC’s to cater for alternate pin functionality. The output of the buffer is connected to the boot mode pins on the AM62P SOC and the output is enabled only when the boot mode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C IO Expander set by the test automation circuit. If the test automation circuit controls the boot mode, then all the switches are manually set to the OFF position. The boot mode buffer is powered by an always ON power supply to make sure that the boot mode remains present even if the SOC is power cycled.

Switch SW4 and SW5 bits [15:0] are used to set the SOC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

Table 2-17. Boot Mode Pin Mapping

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Backup boot mode configuration	Backup boot mode			Primary boot mode configuration			Primary boot mode				PLL configuration		

- BOOTMODE[2:0]– Denote system clock frequency for PLL configuration.
- The below table gives the details of PLL reference clock selection.

Table 2-18. PLL Reference Clock Selection BOOTMODE[2:0]

SW4.3	SW4.2	SW4.1	PLL REF CLK (MHz)
OFF	OFF	OFF	19.2
OFF	OFF	ON	20
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	27
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

- BOOTMODE[6:3] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from primary boot device selection details.

Table 2-19. Boot Device Selection BOOTMODE[6:3]

SW4.7	SW4.6	SW4.5	SW4.4	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII
OFF	ON	OFF	ON	Ethernet RMII
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

- BOOTMODE[12:10] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.

Table 2-20. Backup Boot Mode Selection BOOTMODE[12:10]

SW5.5	SW5.4	SW5.3	Backup Boot Device Selected
OFF	OFF	OFF	None (No backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI
ON	ON	ON	I2C

- BOOTMODE[9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 2-21. Primary Boot Media Configuration BOOTMODE[9:7]

SW5.2	SW5.1	SW4.8	Boot Device
Reserved	Read Mode 2	Read Mode 1	Serial NAND
Reserved	Iclk	Csel	QSPI
Reserved	Iclk	Csel	OSPI
Reserved	Mode	Csel	SPI
Clkout	0	Link Info	Ethernet RGMII
Clkout	Clk src	0	Ethernet RMII
Bus Reset	Reserved	Addr	I2C
Reserved	Reserved	Reserved	UART
1	Reserved	Fs/raw	MMC/ SD card
Reserved	Reserved	Reserved	eMMC
Core Volt	Mode	Lane swap	USB0
Reserved	Reserved	Reserved	GPMC NAND
Reserved	Reserved	Reserved	GPMC NOR
Reserved	Reserved	Reserved	Reserved
SFPD	Read Cmd	Mode	xSPI
Reserved	ARM/Thumb	No/Dev	No boot/Dev Boot

- BOOTMODE[13] – These pins provide optional settings and are used in conjunction with the backup boot device devices. Switch SW 3.6 when ON sets 1 and sets 0 if OFF, see the device specific TRM.
- BOOT-MODE[15:14] – Reserved. Provides backup boot media configuration options.

2.21.3 User Test LEDs

The AM62P SK EVM consists of two LEDs for user defined functions.

Table 2-22 indicates the User test LEDs and the associated GPIOs used to control.

Table 2-22. User Test LEDs

SL.No.	LED	GPIO used	SCH Net Names
1	LD2	GPIO1_49	SOC_GPIO1_49
2	LD5	U105.24(P27)	IO_EXP_TEST_LED

2.22 Expansion Headers

AM62P SK EVM features three expansion Headers, a 40 pin User expansion connector, a 20 pin GPMC NAND (x8) connector and a 28 pin MCU Header.

2.22.1 User Expansion Connector

The AM62P SK EVM supports RPi expansion interface using a 40-pin User expansion connector Mfr. Part# PEC20DAAN. Three mounting holes are oriented with the connector to allow for connection of any generic HAT boards.

Following interfaces and IOs are included on to the 40 pin user expansion connector:

- 2x SPI: SPI0 with 2 CS and SPI2 with 3 CS
- 2x I2C: SoC_I2C0 and SoC_I2C2
- 1x UART: UART5
- 2x PWM: EHRPWM0_A, EHRPWM1_B
- 1x CLK: CLKOUT0
- 10x GPI0: GPIOs from main domain
- 5Vand 3.3V supply (current limited to 155 mA and 500 mA)

Each of the power supplies 5 V and 3.3V are current limited to 155 mA and 500 mA respectively. This is achieved by using two individual load switch TPS22902YFPR and TPS22946YZPR. Enable for the load switches are controllable by an I2C based GPIO port expander.

Signals routed from User Expansion connector are listed in Table 2-23.

Table 2-23. User Expansion Connector (J4)

Pin No.	SoC Ball	Net Name
1	-	VCC3V3_EXP
2	-	VCC5V0_EXP
3	U25	EXP_I2C2_SDA
4	-	VCC5V0_EXP
5	T22	EXP_I2C2_SCL
6	-	DGND
7	C25	EXP_CLKOUT0
8	F20	EXP_UART5_TXD
9	-	DGND
10	B23	EXP_UART5_RXD
11	F24	EXP_SPI2_CS1
12	G20	EXP_SPI2_CLK
13	U23	EXP_GPIO0_42
14	-	DGND
15	A23	EXP_GPIO1_22
16	AD24	EXP_GPIO0_38
17	-	VCC3V3_EXP
18	P24	EXP_GPIO0_39
19	B20	EXP_SPI0_D0
20	-	DGND
21	C21	EXP_SPI0_D1
22	L23	EXP_GPIO0_14
23	B21	EXP_SPI0_CLK
24	D20	EXP_SPI0_CS0
25	-	DGND
26	E20	EXP_SPI0_CS1
27	A24	SOC_I2C0_SDA
28	B25	SOC_I2C0_SCL
29	T24	EXP_GPIO0_36
30	R25	EXP_GPIO0_32
31	R24	EXP_GPIO0_33
32	P25	EXP_GPIO0_40/ PR0_ECAP0_IN_APWM_OUT
33	F23	EXP_EHRPWM1_B
34	-	DGND
35	G23	EXP_SPI2_CS0/EHRPWM0_A
36	E24	EXP_SPI2_CS2
37	T23	EXP_GPIO0_41
38	E25	EXP_SPI2_D1/ECAP2_IN_APWM_OUT
39	-	EXP_HAT_DETECT
40	D25	EXP_SPI2_D0

2.22.2 MCU Connector

AM62P SK EVM has a 14 x 2 standard 0.1” spaced MCU connector which includes signals connected to the MCU Domain of the SOC. The connected signals include MCU_I2C0, MCU_UART0 (with flow

control), MCU_SPI0 and MCU_MCAN0 signals. Additional control signals connected on the header includes CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3V IO supply and GND. MCU_UART0 signals from AM62P SOC are connected to both MCU Header and FT4232 Bridge through a MUX Mfr Part # SN74CB3Q3257PWR. The MCU Header does not include the Board ID memory interface. The allowed current limit is 100 mA on 3.3V rail.

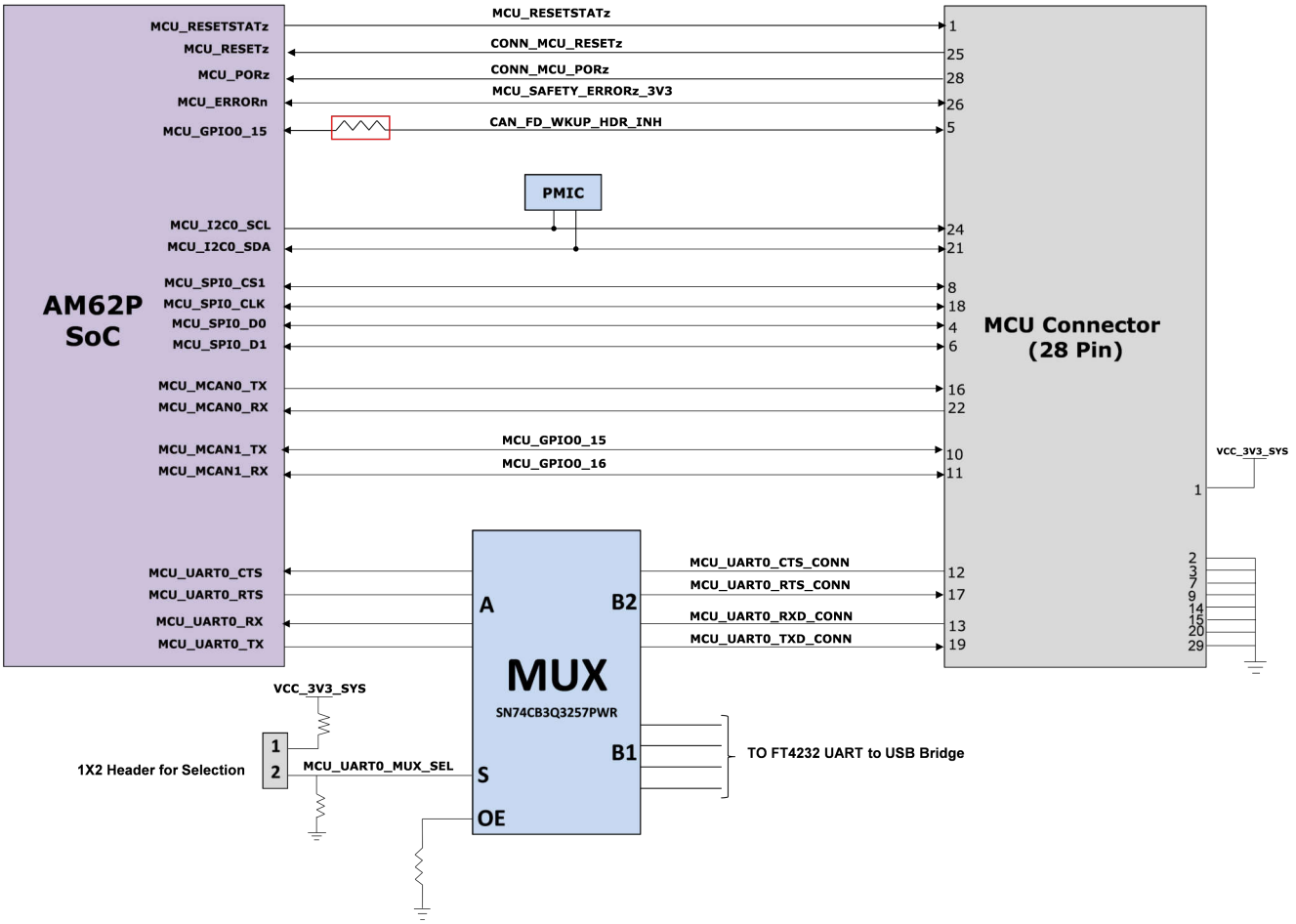

Figure 2-28. MCU Connector Interface

Table 2-24. MCU Connector (J11)

Pin No.	SoCBall No.	Net Name
1	-	VCC_3V3_SYS
2	-	DGND
3	-	DGND
4	D10	MCU_SPI0_D1
5	F8	CAN_FD_WKUP_HDR_INH
6	B11	MCU_SPI0_D0
7	-	DGND
8	E10	MCU_SPI0_CS1
9	-	DGND
10	F8	MCU_GPIO0_15
11	E7	MCU_GPIO0_16
12	B8	MCU_UART0_CTS_CONN
13	B6	MCU_UART0_RXD_CONN
14	-	DGND

Table 2-24. MCU Connector (J11) (continued)

Pin No.	SoCBall No.	Net Name
15	-	DGND
16	E8	MCU_MCAN0_TX
17	B7	MCU_UART0_RTS_CONN
18	C10	MCU_SPI0_CLK
19	C8	MCU_UART0_TXD_CONN
20	-	DGND
21	D11	MCU_I2C0_SDA
22	D6	MCU_MCAN0_RX
23	F14	MCU_RESETSTATz
24	E11	MCU_I2C0_SCL
25	F11	CONN_MCU_RESETz
26	G6	MCU_SAFETY_ERRORz_3V3
27	-	DGND
28	H6	CONN_MCU_PORz

2.22.3 GPMC NAND (x8) Connector

The AM62P SK EVM supports GPMC NAND(x8) interface using a 20-pin standard 0.1” spaced connector Mfr. Part# PREC010DAAN-RC. This connector includes GPMC_AD[0:7] signals which on power up executes prominent boot mode functions. The other control signals GPMC0_WEn, GPMC0_WAIT0 and GPMC0_BE0N_CLE can be routed to this connector by mounting RA5 and removing RA1. This connector is provided with a 3.3V supply to power any x8 NAND expansion card.

Note

User expansion connector and MCU Header can be used in conjunction with the GPMC NAND (x8) connector to expand number of control signals (for example, GPIO’s & I2C) that can be required for the operation of a NAND memory device.

Table 2-25. GPMC NAND (x8) Connector (J14)

Pin No.	SoCBall No.	Netname
1	-	VCC_3V3_SYS
2	-	DGND
3	-	x8_NAND_DETECT
4	-	NC
5	-	NC
6	-	NC
7	T25	GPMC0_WEn
8	-	NC
9	AA24	GPMC0_WAIT0
10	-	NC
11	U24	GPMC0_BE0N_CLE
12	-	NC
13	U22	GPMC0_AD0
14	U21	GPMC0_AD1
15	U20	GPMC0_AD2
16	V25	GPMC0_AD3
17	T20	GPMC0_AD4
18	T21	GPMC0_AD5
19	V24	GPMC0_AD6

Table 2-25. GPMC NAND (x8) Connector (J14) (continued)

Pin No.	SoCBall No.	Netname
20	W25	GPMC0_AD7

2.23 Interrupt

AM62P SK EVM supports two push buttons for providing reset input and a user generated interrupt to the AM62P SOC. These push buttons are placed on the Top side of the Board and are listed in Table 2-26.

Table 2-26. EVM Push Buttons

SL. No.	Push Buttons	Signal	Function
1	SW6	SoC_WARM_RESETZ	Main domain Warm Reset input
2	SW7	GPIO_MCU	Generates interrupt on GPIO1_23 (UART0_RTSn)

2.24 I2C Address Mapping

There are five AM62P I2C instances communicating with the various peripherals in the SKEVM.

- SoC_I2C0 Interface: SoC I2C[0] is connected to Board ID EEPROM, User Expansion Connector, USB PD controller, OLDI display connector and DSI display connector.
- SOC_I2C1 Interface: SoC I2C[1] is connected to Test Automation Header, Current Monitors (x6), Temperature Sensors (x2), Audio Codec, HDMI Transmitter & GPIO Port Expander (x2).
- SOC_I2C2 Interface: SoC I2C[2] is connected to the User Expansion Connector and CSI Camera connector.
- MCU_I2C0 Interface: MCU I2C[0] is connected to the MCU Header & PMIC.
- WKUP_I2C0 Interface: WKUP I2C[0] is only connected to the PMIC.

The image below depicts the I2C tree, and the below table provides the complete I2C address mapping details present on the AM62P SK EVM.

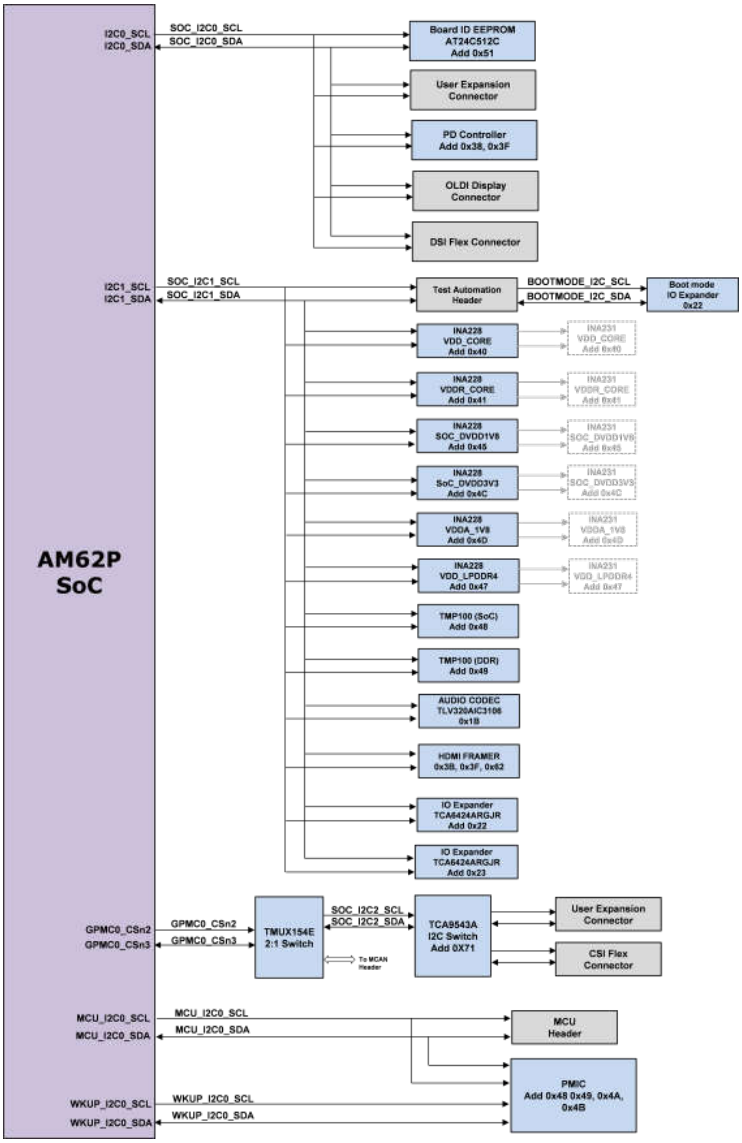

Figure 2-29. I2C Interface

Table 2-27. I2C Mapping Table

I2C Port	Device/Function	Part#	I2C Address
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x51
	User Expansion Connector	<connector interface>	
	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
	OLDI Display Connector	<connector interface>	
	DSI Display Connector	<connector interface>	
SoC_I2C1	Test Automation Header	<connector interface>	
	Current Monitors	INA228AIDGSR	0x40, 0x41, 0x4C, 0x45, 0x4D and 0x47
	Temperature Sensors	TMP100NA/3K	0x48, 0x49
	Audio Codec	TLV320AIC3106IRGZT	0x1B
	HDMI Transmitter	Sil9022ACNU	0x3B, 0x3F, 0x62
	GPIO Port Expander	TCA6424ARGJR	0x22, 0x23
SoC_I2C2	CSI Camera Connector	<connector interface>	
	User Expansion Connector	<connector interface>	

Table 2-27. I2C Mapping Table (continued)

I2C Port	Device/Function	Part#	I2C Address
MCU_I2C0	MCU Header	<connector interface>	
WKUP_I2C0	PMIC	PTPS6522430RAHRQ1	0x48, 0x49, 0x4A, 0x4B
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22
	Test Automation Header	<connector interface>	

3 Hardware Design Files

The hardware design files such as schematics, BOM, PCB Layout, Assembly Files and Gerber files are available in the link below.

Design Files

4 Compliance Information

4.1 Compliance and Certifications

EMC, EMI and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). TI recommends this product be used in an ESD controlled environment. This can include a temperature or a humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

5 Additional Information

5.1 Known Hardware or Software Issues

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched have modification labels attached to the EVM assembly.

Table 5-1. AM62P SK EVM Known Issues and Modifications

Issue Number	Issue Title	Issue Description	Variants Affected
1	Watchdog reset	PMIC Watchdog reset happens around 10 seconds.	E1
2	Power down sequence	PMIC not able to complete proper power down sequence	E1

5.1.1 Issue 1 - Watchdog Reset

Applicable EVM Revisions: E1

Issue Description: Due to incorrect pull-up voltage on the PMIC watchdog disable pin (R124), the EVM is getting reset after around 10 seconds.

Fix: The pull-up voltage for R124 needs to be changed from VCC_3V3_SYS to VCC_3V3_MAIN. Change R131 pull-up voltage from VCC_1V8_SYS to VCC_3V3_SYS.

5.1.2 Issue 2 - Power Down Sequence

Applicable EVM Revisions: E1

Issue Description: Due to incorrect voltage (excessive capacitance) connection to the PMIC VSENSE pin, PMIC cannot able to complete the power down sequence before VCCA goes below threshold level.

Fix: The VSENSE pin input voltage are changed from VMAIN to dual voltage VBUS_TYPEC1 and VBUS_TYPEC2 through ORing diodes.

5.2 Trademarks

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