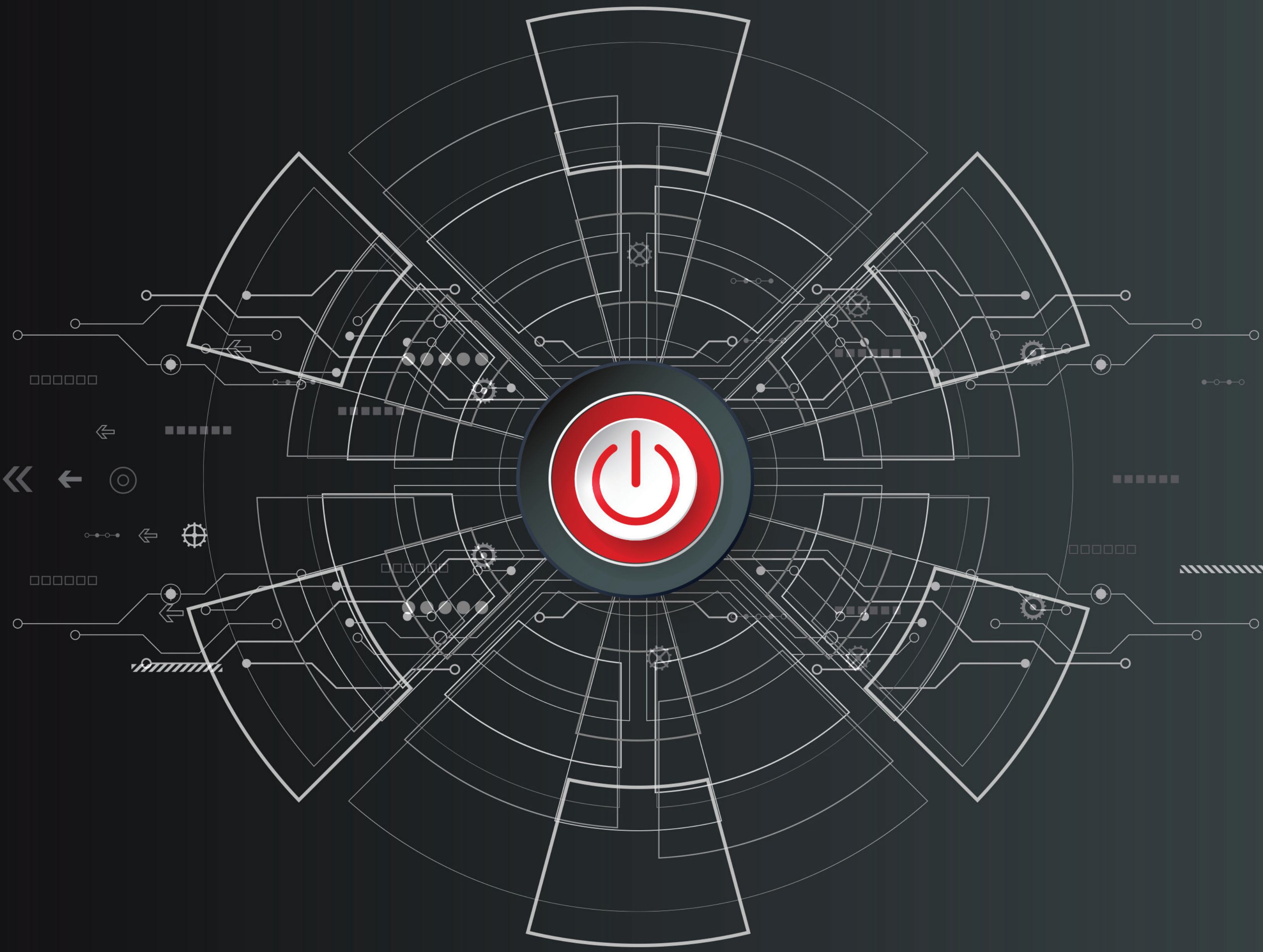


TI-PMLK

TI Power Management Lab Kit
WEBENCH® design tools exercise book

Texas Instruments

Table of Contents: WEBENCH design tools exercise book

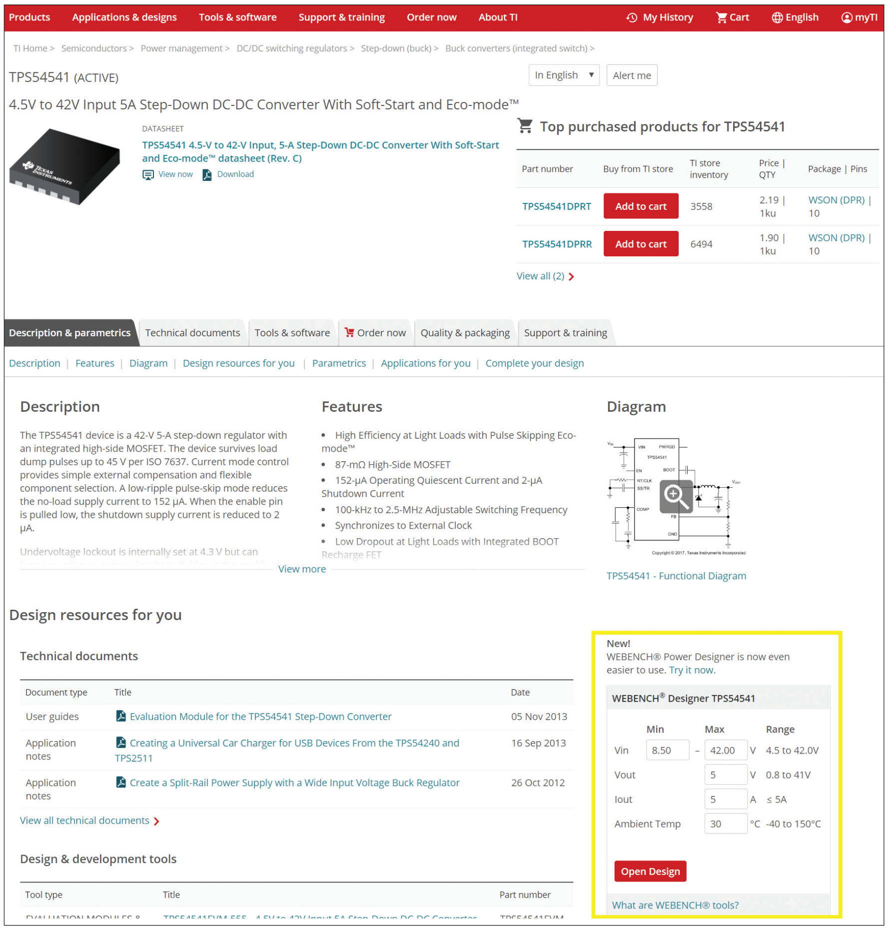
WEBENCH® Power Designer is an online design tool that helps you select, design, and compare power supply solutions that are tailored to your needs. Power Designer is both easy to use and powerful, guiding users through the process of choosing and simulating a list of possible circuit designs. Each solution is optimized based on the user's priorities and includes a full list of components and prices for comparison. Along the way, you can learn about and choose the many tradeoffs that are encountered while designing a power supply, namely the overall solution cost, footprint, and efficiency. After selecting your preferred solution, you can optimize the design further, if desired, by changing any of the components and by simulating your design to observe and validate its operation and performance. Once the user is satisfied with the finished design and has been autosaved to their my.ti.com account, it can then be printed or saved as a detailed PDF design report, shared with others, or exported for use in several different CAD tools.

This guide will help you get started using **WEBENCH Power Designer** by walking you through each step in the process and explaining the main features. The included design examples can then be used for additional practice and to get familiar with the process of sharing your designs and results with others.

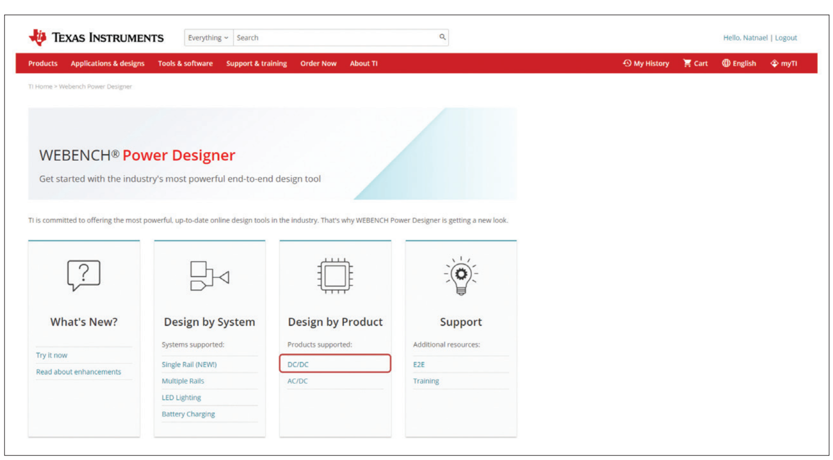
WEBENCH Getting Started

Using TI WEBENCH® Power Designer

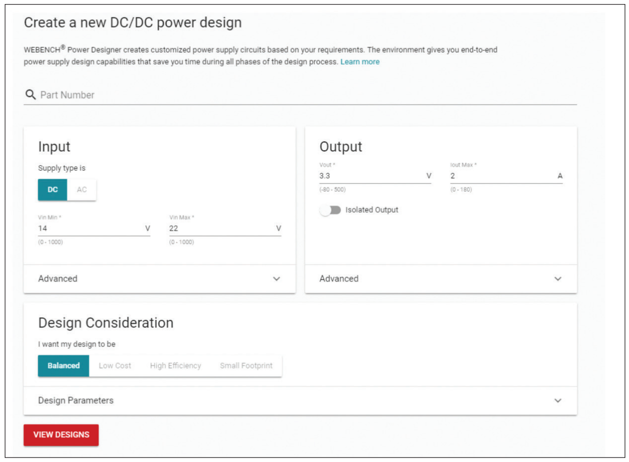
If you have already selected a specific product that you'd like to design with, **WEBENCH** can be launched from its product page on ti.com. If **WEBENCH** is available for that product, it will be shown on the right hand side of the main tab. Simply enter your requirements and click on **'Open Design'** to immediately open the recommended solution in **WEBENCH**.



If you haven't yet selected a part, go to webench.ti.com and click on the DC/DC link under the **Design by Product** tab in the WEBENCH® Power Designer page.



This will open up a new page called **'Create a new DC/DC power design'**.



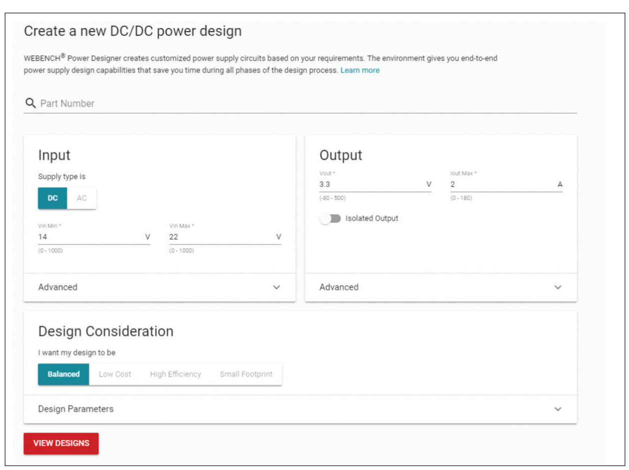
WEBENCH first presents a search bar for those that have already selected a part number that they'd like to use. If you haven't yet selected a part, then skip the search bar and begin entering your requirements:

- Input voltage range
- Output voltage
- Load current
- Additional criteria and options using the **'Advanced'** section

In the **Design Consideration** section, you can choose whether or not to optimize your power supply design towards a target attribute. A "Balanced" design will place equal importance and weighting on all three design tradeoffs: Lowest Cost, Highest Efficiency, and Smallest Footprint. If one of these aspects is more important to your design than the others, such as Lowest Cost, then select the **'Low Cost'** Design Consideration so that **WEBENCH** can optimize the design and component choices towards this aspect.

Clicking on the **'Advanced'** drop down menus will reveal additional options for further design optimization by **WEBENCH**. These are optional settings that can be ignored or modified as desired.

Once complete, click on the **'View Designs'** button to launch **WEBENCH Power Designer**.



About the Navigation bar

The **Navigation bar** now appears at the top of the new view. The **Navigation bar** allows you to quickly switch between the **CUSTOMIZE** (Schematic, BOM, Operating Values), **SIMULATE**, and **EXPORT** views.

CUSTOMIZE Tab

You will enter this view after you've selected a solution using the **'Select'** tab that you're in now. This tab can be used to view your schematic and layout, and to change components to further optimize your solution. You will also see tables and charts for key operating values and performance data for your design over its range.

SIMULATE Tab

When you've finished customizing the solution, you will click on the **'Simulate'** tab to view which electrical simulations are available to run. The following simulations are typically supported and can be launched by selecting the desired simulation and pressing the **'Start'** button:

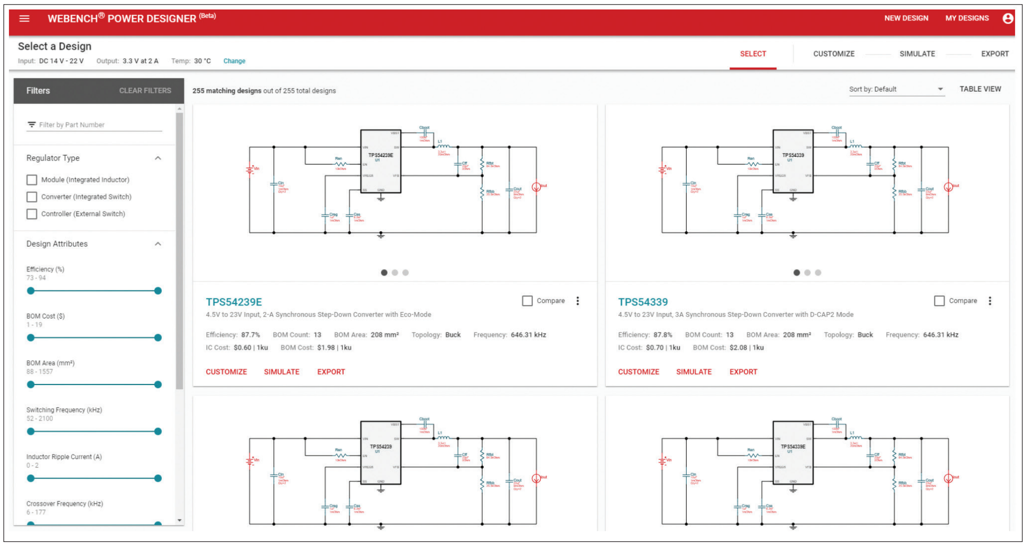
- Startup
- SteadyState
- Load transient
- Line transient
- Bode plot
- 2-Step startup

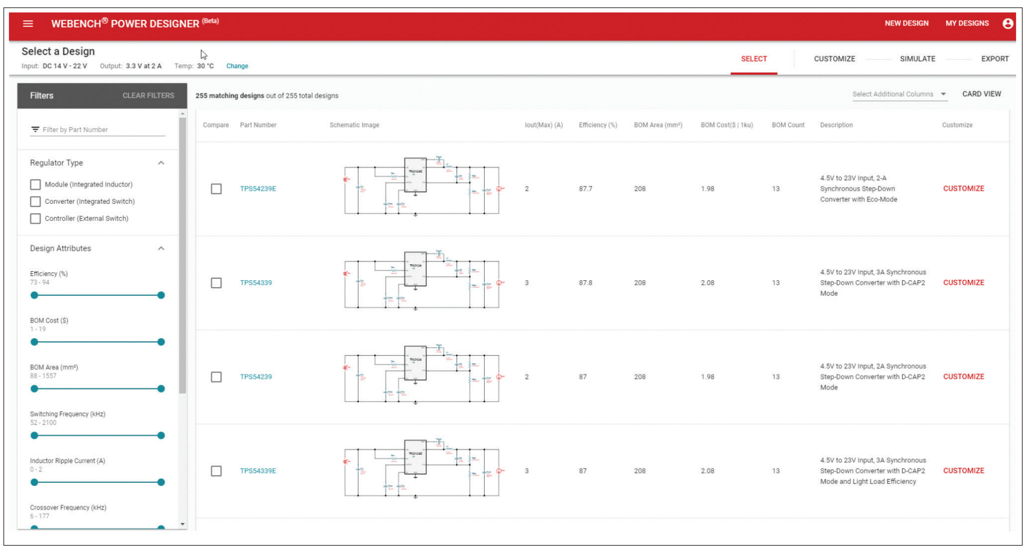
EXPORT Tab

The **Export** tab will allow you to export your designs to CAD tools such as Altium, Cadence, and more. You can also print a full design report from here to save and share with others. Lastly, you can send a link to share your complete design with your colleagues to have them review your design.

Select a solution

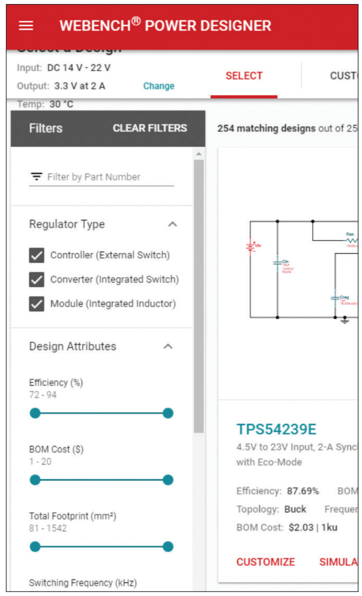
Once you've entered all of your design criteria and clicked on the **'View Designs'** button, **WEBENCH** will quickly generate a list of possible parts and solutions that satisfy your requirements and will display them with the most optimal solutions on top. **WEBENCH** also offers a card view of the solutions, which can be selected at top right under the **EXPORT** tab.



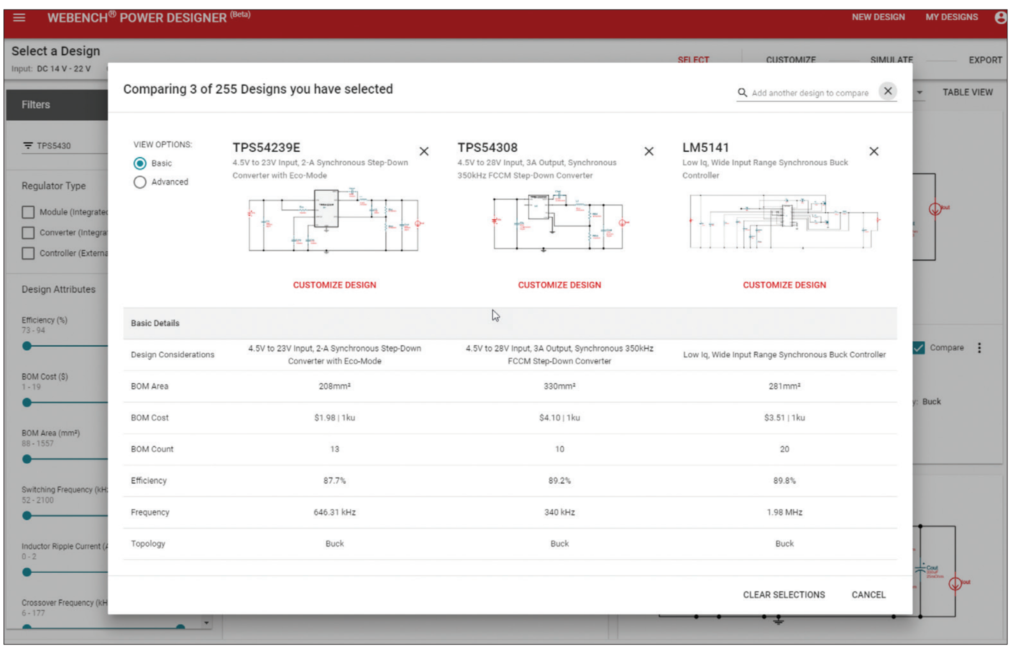


At this point, **WEBENCH** has already selected the right topologies and components to create solutions based on your design inputs. The topologies that **WEBENCH** supports include bucks (step-down), boosts (step-up), flybacks, inverting buck-boosts, 4-switch buck-boosts, SEPICs (buck/boost), Half Bridge Resonant LLCs and PFC-Boost topologies. **WEBENCH** has also calculated, selected, and priced all of the necessary external components for every solution so that you can compare solution costs, sizes, and efficiencies for complete solutions rather than just for the ICs themselves.

To help with the selection process, **WEBENCH** provides a list of additional **Filters** on the left hand side of the page. If desired, you can use these filters to eliminate solutions from the list that don’t have required features or attributes, such as **Enable pins**. This is optional and is presented as another opportunity to further optimize your list of possible solutions for cost, size, efficiency, and features.



You can also use the **Compare** checkboxes to view more detailed comparison tables for selected solutions.

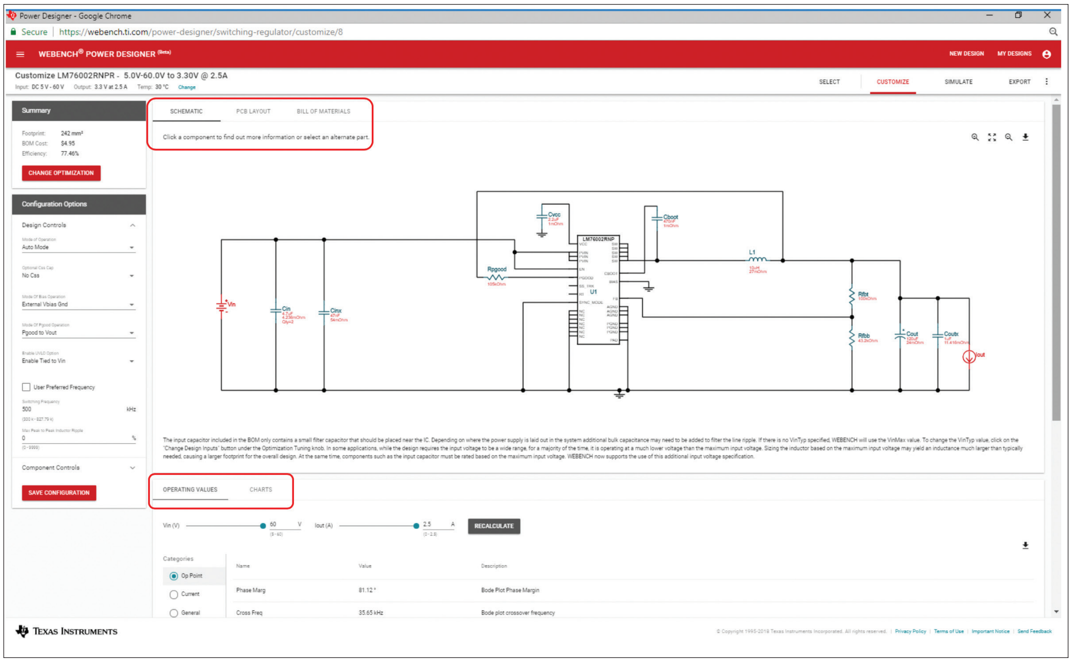


Note: If you don't see a specific part number that you'd like to see in your top recommended list, you may still be able to find it by using the **Filter by Part Number** option on the left.

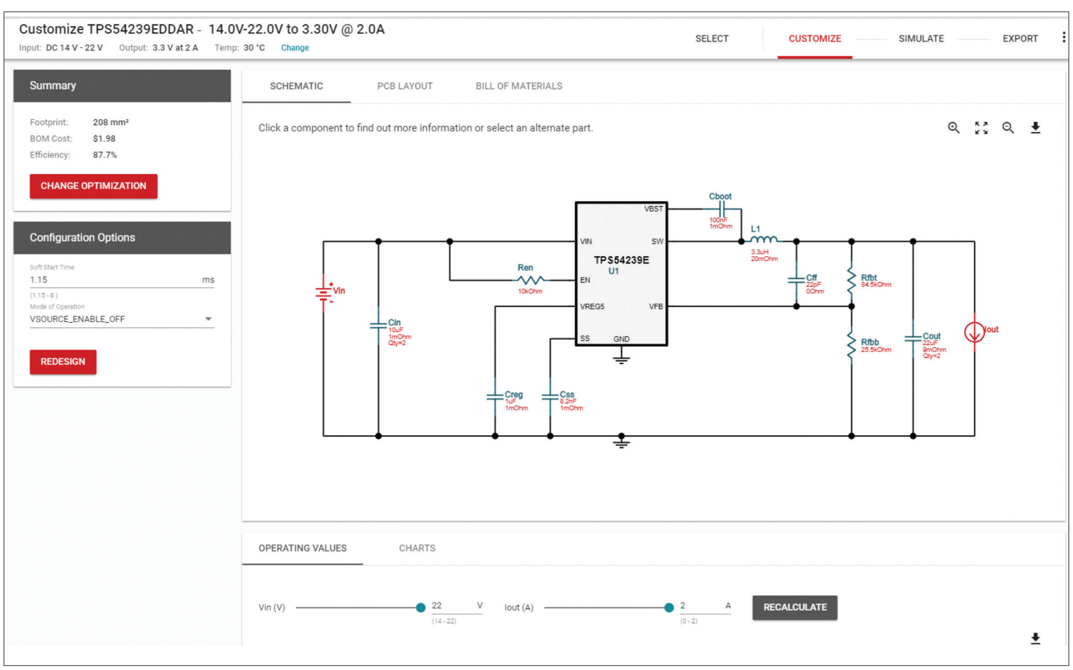
After you've finished your sorting and selection process to identify the solution that you believe will be the best fit for your needs, click on the red **'Customize'** link within that design's window to proceed. This will now open up the more detailed **'Customize'** view of your design so that you can see the **Schematic, Operating Values, Example Layout,** and **Bill of Materials**.

CUSTOMIZE TAB

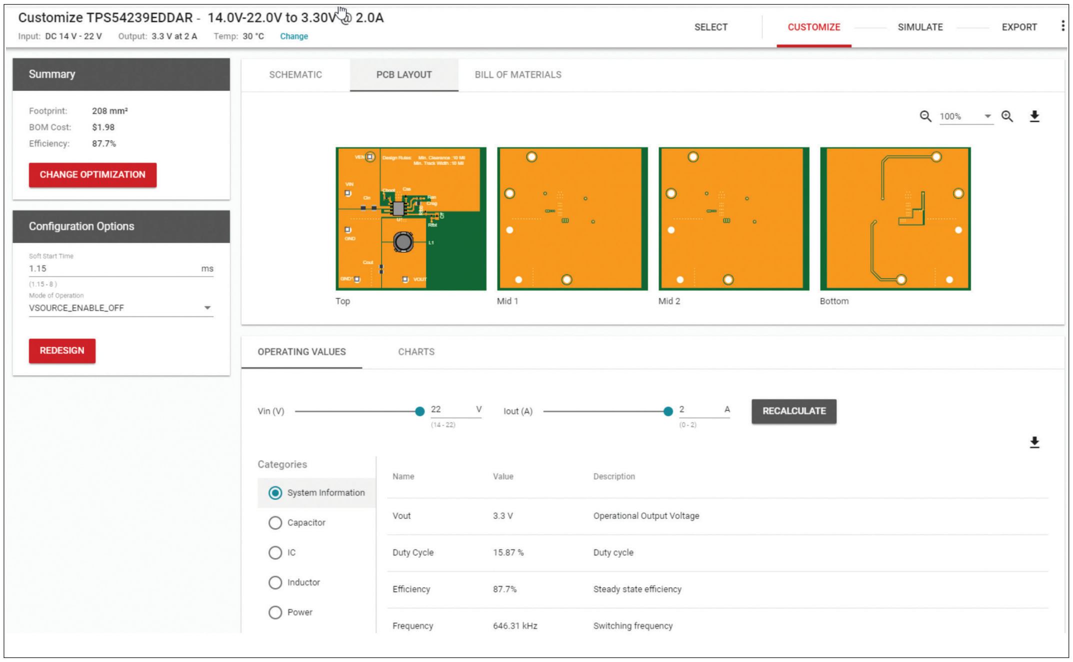
Now that you've selected a solution, you will be in the **'Customize'** view. At the top of the page you will see **SCHEMATIC**, **PCB LAYOUT**, and **BILL OF MATERIALS** tabs. In the middle of the page you will see the **Operating Values** and **Charts** tabs. The four windows for **Charts**, **Schematic, Operating Values,** and **Bill of Materials** (BOM) will be used the most within the **WEBENCH** exercises.



- **SCHEMATIC** shows the schematic drawing of the solution using the components that have been computed and selected by **WEBENCH**.



- **PCB LAYOUT** shows the printed circuit board layout, which is based on the board design of that part's **Evalution Module** (EVM).



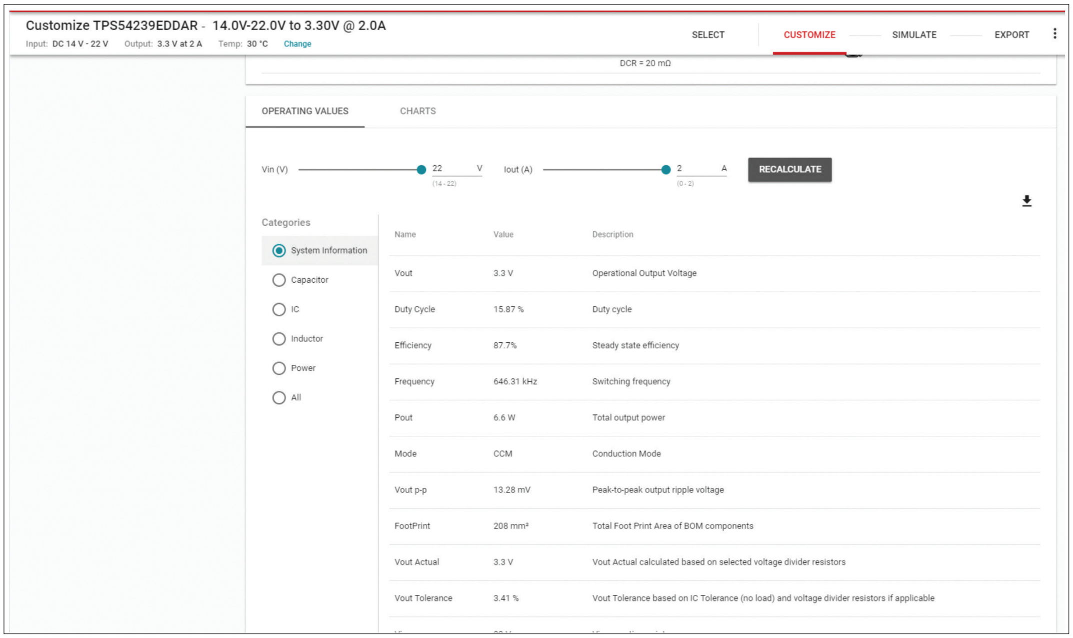
- **BILL OF MATERIALS** lists all of the components needed for the design, along with a rough price estimate for a 1kµ quantity.


SCHEMATIC PCB LAYOUT BILL OF MATERIALS

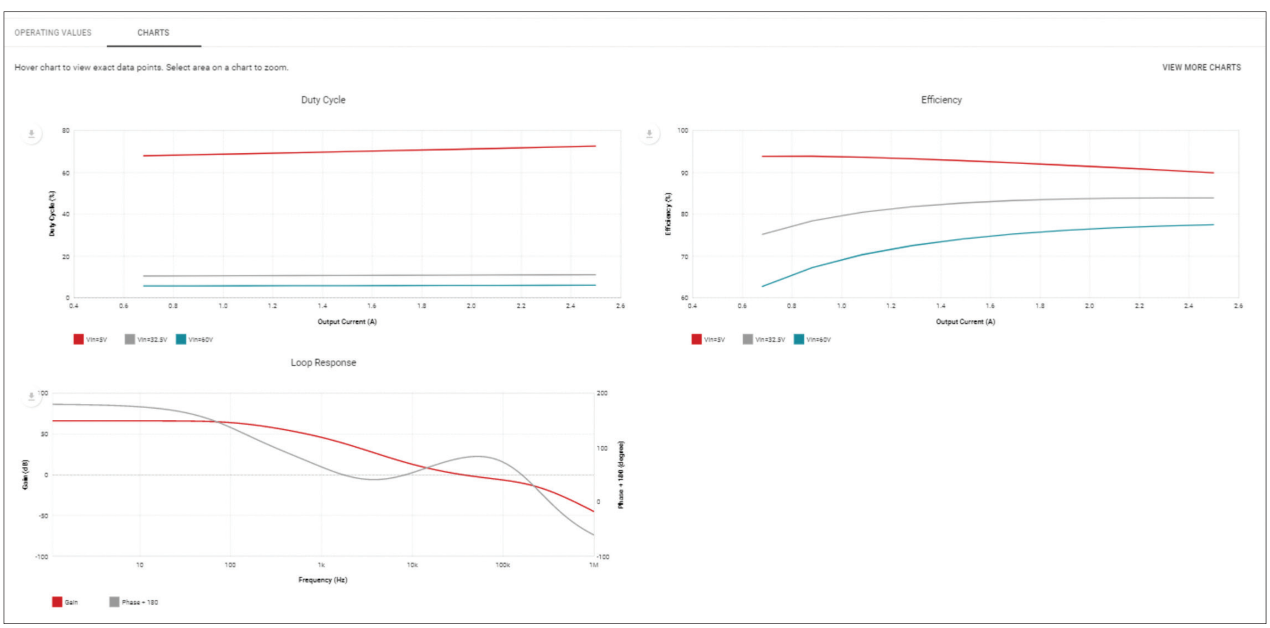
*Footprint is component footprint plus 1 mm per side.

Part	Manufacturer	Part Number	Quantity	Total Price ($)	Attribute	Total Footprint (mm²)	Top View	Edit
Rpgood	Yageo	RC0201FR-07105KL	1	0.01	Tolerance = 1.0% Resistance = 105 kΩ Power = 50 mW	2.08		SELECT ALTERNATE PART
Rfbt	Panasonic	ERJ-6ENF1003V	1	0.01	Tolerance = 1.0% Resistance = 100 kΩ Power = 125 mW	6.75		SELECT ALTERNATE PART
Rfbb	Vishay-Dale	CRCW040243K2FKED	1	0.01	Tolerance = 1.0% Resistance = 43.2 kΩ Power = 63 mW	3		SELECT ALTERNATE PART
Cboot	Taiyo Yuden	EMK212B7474KD-T	1	0.02	ESR = 1 mΩ Cap = 470 nF Total Derated Cap = 470 nF	6.75		SELECT ALTERNATE PART
Cin	TDK	CGA6M3X7S2A475K200AB	2	1.08	ESR = 4.24 mΩ Cap = 4.7 µF Total Derated Cap = 2.4 µF	29.4		SELECT ALTERNATE PART
Cinx	AVX	12061C473MAT2A	1	0.03	ESR = 54 mΩ Cap = 47 nF Total Derated Cap = 47 nF	10.92		SELECT ALTERNATE PART
Cout	Chemi-Con	APXE6R3ARA121ME61G	1	0.42	ESR = 24 mΩ Cap = 120 µF Total Derated Cap = 120 µF	53.29		SELECT ALTERNATE PART
Coutx	TDK	C1005X6S1C105K050BC	1	0.02	ESR = 11.42 mΩ Cap = 1 µF Total Derated Cap = 490 nF	3		SELECT ALTERNATE PART
Cvcc	Taiyo Yuden	EMK212BJ225KG-T	1	0.03	ESR = 1 mΩ Cap = 2.2 µF Total Derated Cap = 2.2 µF	6.75		SELECT ALTERNATE PART
L1	Coilcraft	XAL6060-103MEB	1	0.82	IDC = 7 A L = 10 µH DCR = 27 mΩ	71.56		SELECT ALTERNATE PART
U1	Texas Instruments	LM76002RNPR	1	2.50		48		

- **OPERATING VALUES:** You must scroll down to the bottom of the page to see the detailed performance metrics and calculated values for the most important components and nodes. If desired, these values can be instantly recalculated for various input voltages and output loads.



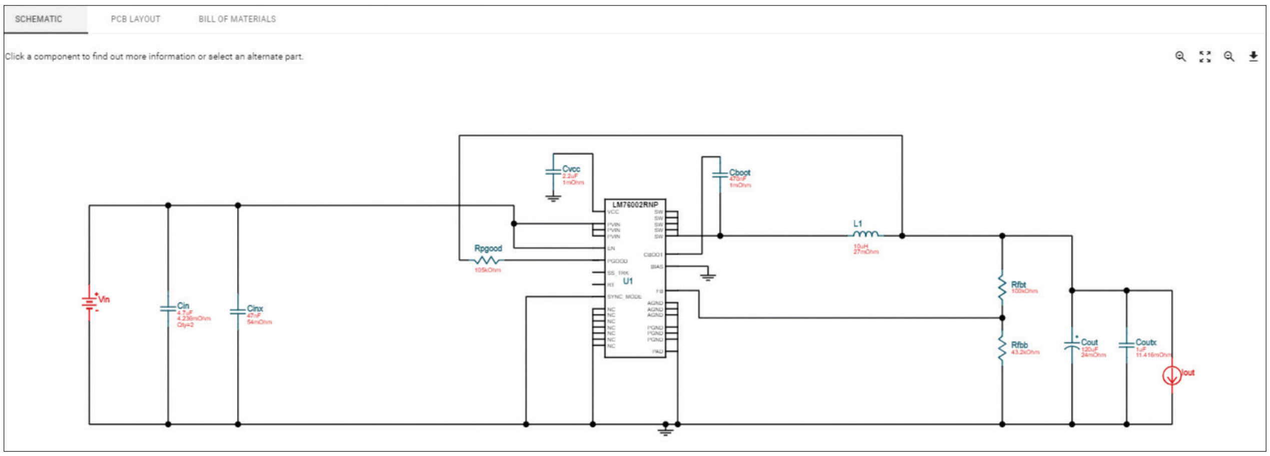
- **Charts** will display the calculation results over your full operating value range (input voltages and load currents). It is a visual representation of the value ranges displayed in the **OPERATING VALUES** tab. You can use **View Other Charts** to select which charts you would like to view.



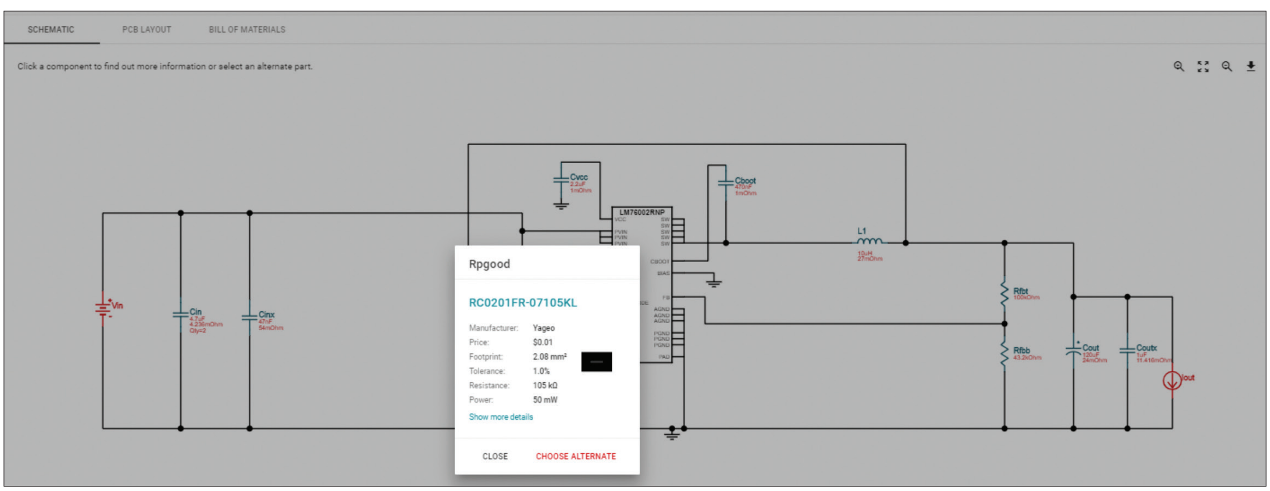
Schematic view and changing components

The **SCHEMATIC** view can be selected using the tab located under the navigation bar.

The zoom in, zoom out, and export to CAD icons are located at the top right of the schematic.



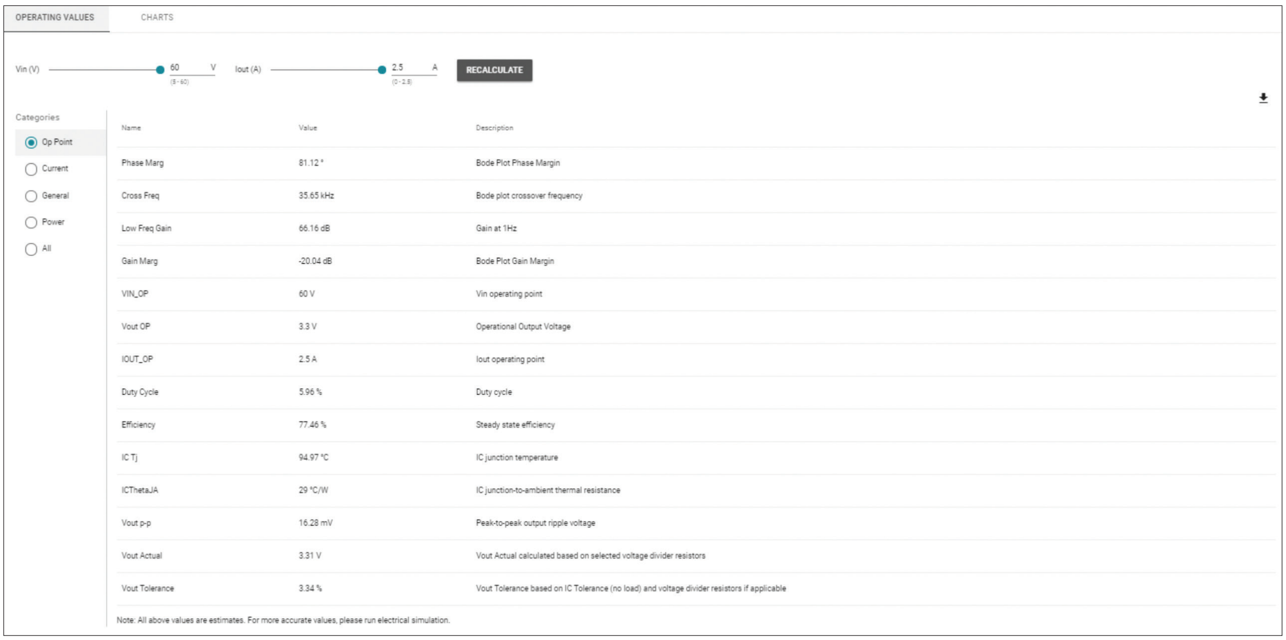
If you'd like to change a component from within the **Schematic** view rather than the **BILL OF MATERIALS** view, then click on a component to see its properties and select **'Choose Alternative'**.



OPERATING VALUES

Click the **'OPERATING VALUES'** tab in the middle of the page to view the operating values and performance data for any point in your input voltage and load current range.

You can see a list of all the operating point values in the table. Click the table header for **Name** or **Category** to sort them alphabetically or group them by category.



Name	Value	Description
Phase Marg	81.12 °	Bode Plot Phase Margin
Cross Freq	35.65 kHz	Bode plot crossover frequency
Low Freq Gain	66.16 dB	Gain at 1Hz
Gain Marg	-20.04 dB	Bode Plot Gain Margin
VIN_OP	60 V	Vin operating point
Vout OP	3.3 V	Operational Output Voltage
IOUT_OP	2.5 A	Iout operating point
Duty Cycle	5.96 %	Duty cycle
Efficiency	77.46 %	Steady state efficiency
IC Tj	94.97 °C	IC junction temperature
ICThetaJA	29 °C/W	IC junction-to-ambient thermal resistance
Vout p-p	16.28 mV	Peak-to-peak output ripple voltage
Vout Actual	3.31 V	Vout Actual calculated based on selected voltage divider resistors
Vout Tolerance	3.34 %	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable

Note: All above values are estimates. For more accurate values, please run electrical simulation.

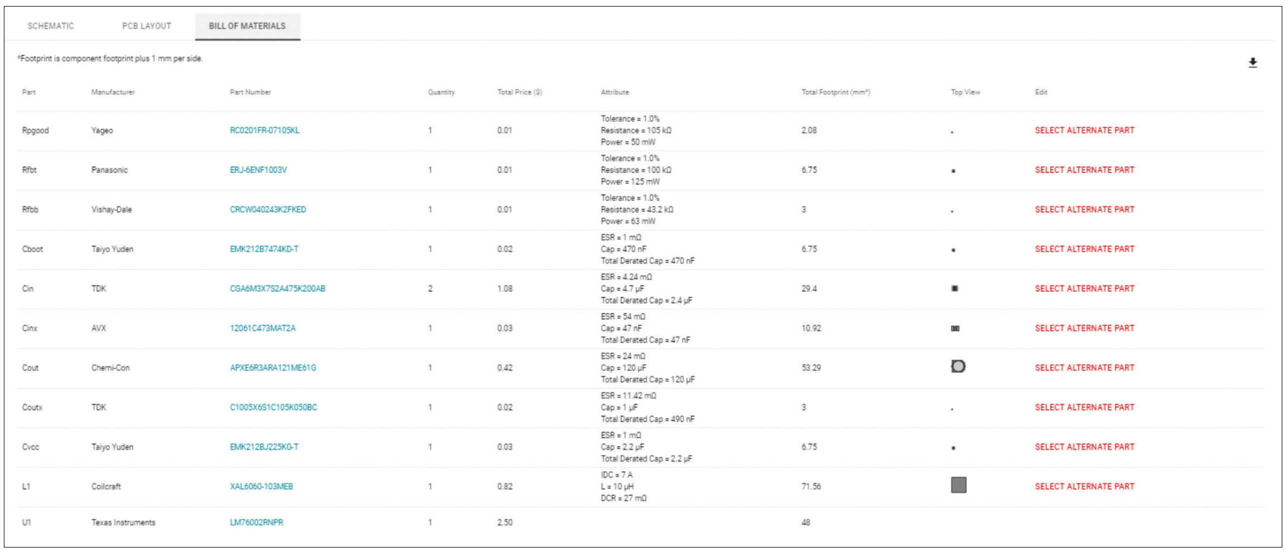
You can recalculate the values for different operating points without changing your design. Simply move the scale to new values for V_{IN} and I_{OUT} and press **RECALCULATE**.

There is a note at the bottom that reminds you that phase margin and crossover frequency are estimates from the calculations. To get a more accurate value and to get a better view of whether or not your solution is stable, you will need to use electrical simulation.

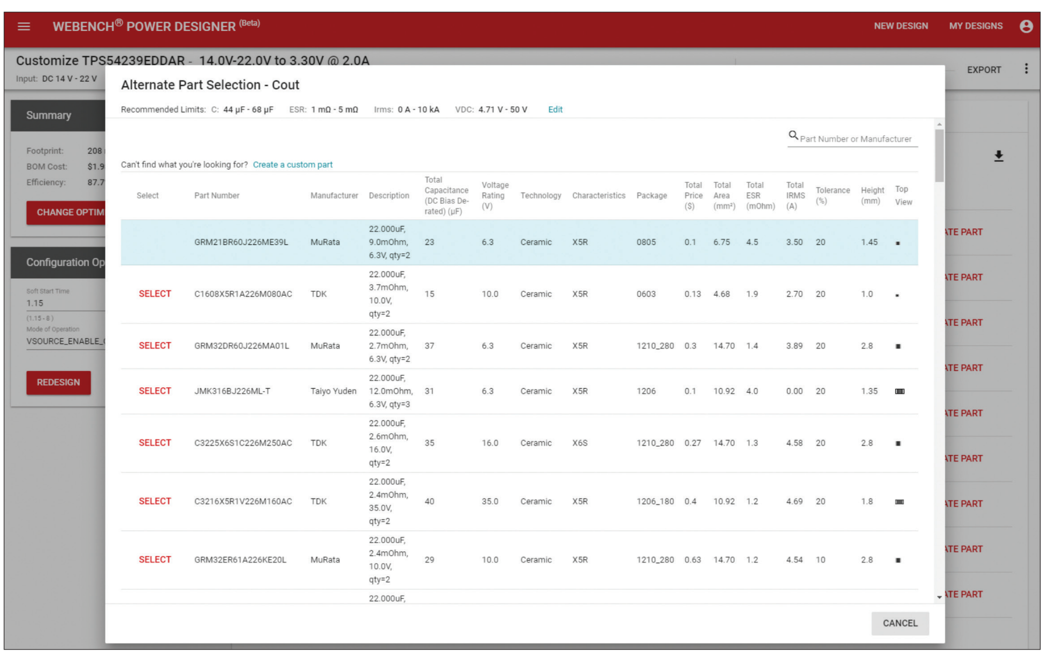
Viewing the Bill of Materials and changing components

Click the **BILL OF MATERIALS** tab located under the navigation bar to view a list of all components.

If you want to change a component, use Select **'Alternate Part'** in the last column of the **BOM** table to change to the component you would prefer.



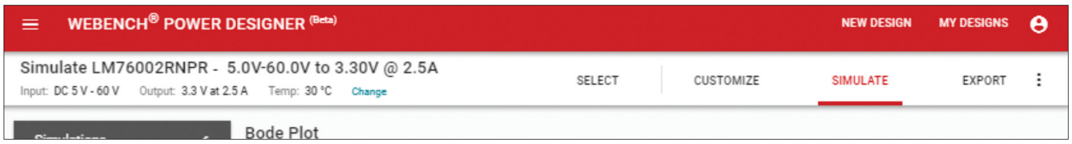
For example, once you click **'Select Alternate Part'** for C_{OUT}, you will see a window that shows alternate capacitors that can be used in the design. You can then select an **alternate capacitor** if desired.



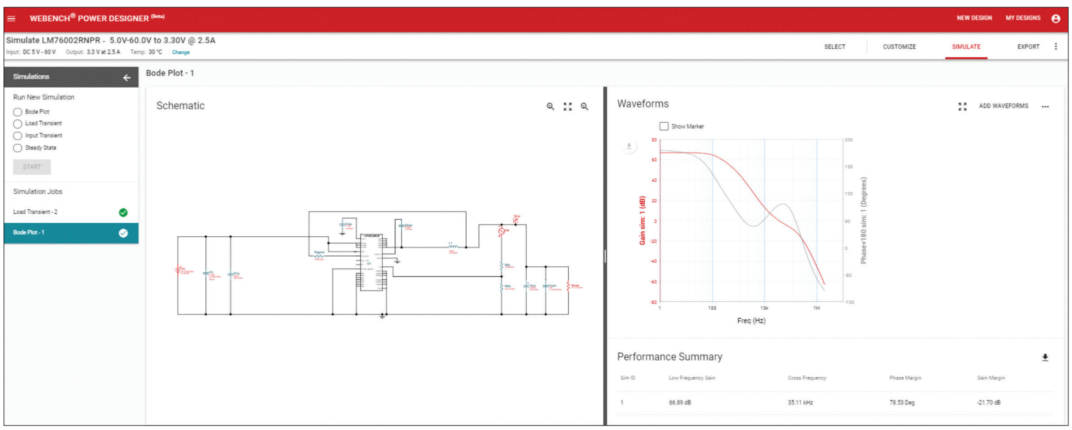
Running slectrical simulations and changing components

WEBENCH uses a **Spice** simulation engine to simulate the electrical behavior of your power supply circuit. You can simulate bode plots, steady state waveforms, input transient, load transient, and startup simulations. Through probe points on a schematic display, you can examine waveforms, change component values, and view a history of simulation results to fine-tune your design.

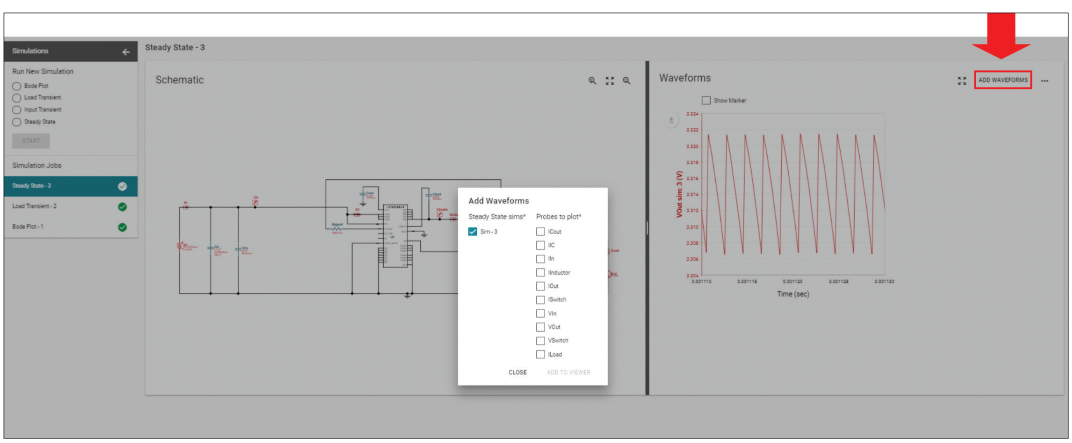
Select **'SIMULATE'** in the navigation bar at top to select a simulation type.



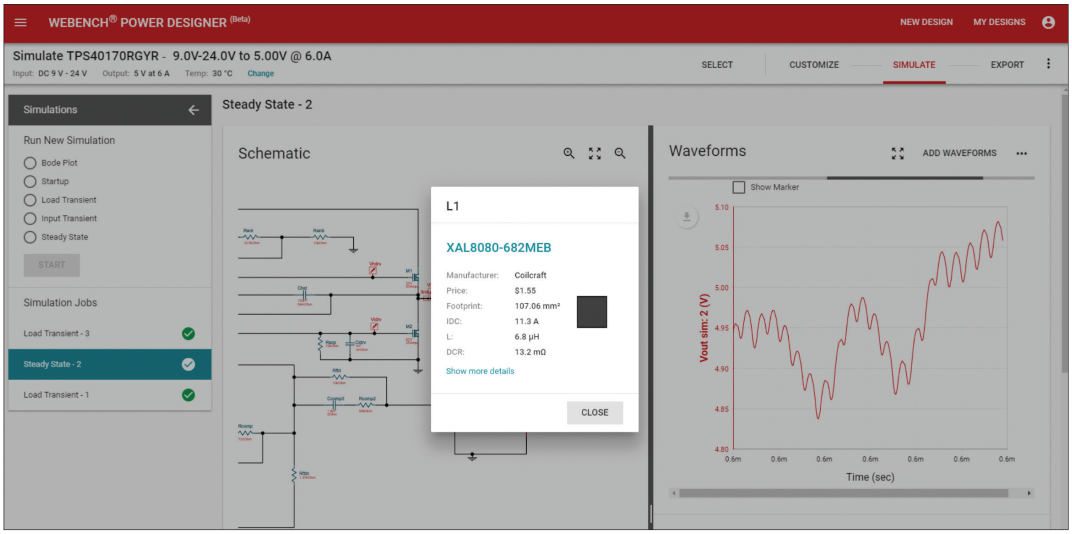
From within the **'SIMULATE'** view, and to the left of the schematic, is a selection table showing the available simulation types, along with a button to start the desired simulation.



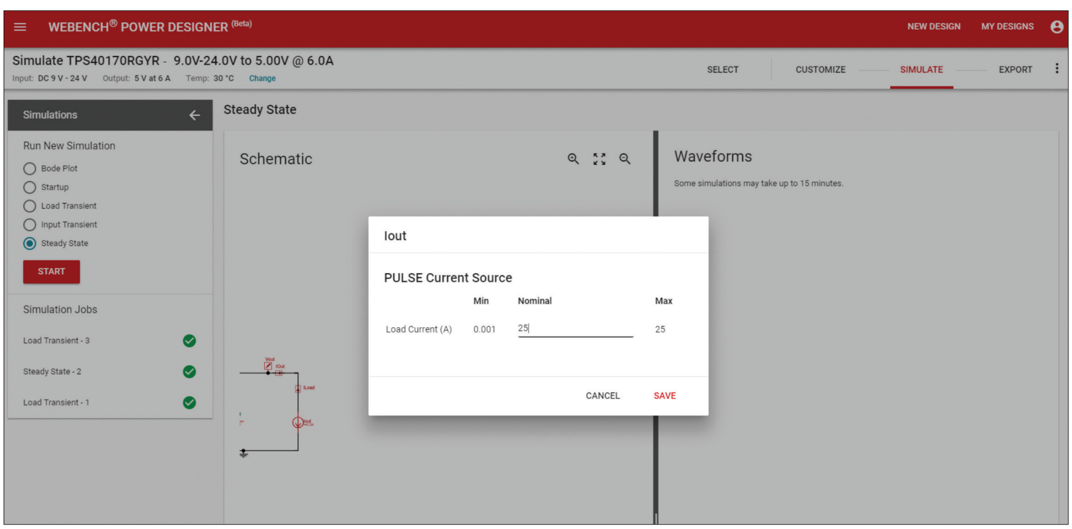
On the right, is the waveform area where you can view the simulation as it progresses. This is also where you can **Add WAVEFORMS** to view different points on the schematic.



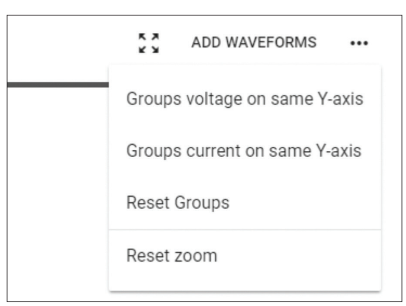
Click **'Start'** to run the simulation and select the probes of interest on the schematic that you'd like to display. Just like the **Schematic** view, you can click the schematic components to view their properties. If you'd like to change a component, select a new simulation from the simulation list and then click on the components in the schematic to select alternate parts or configure sources. Please note that if you edit the sources or components on the schematic, you must then run a new simulation to get the results from the new components.



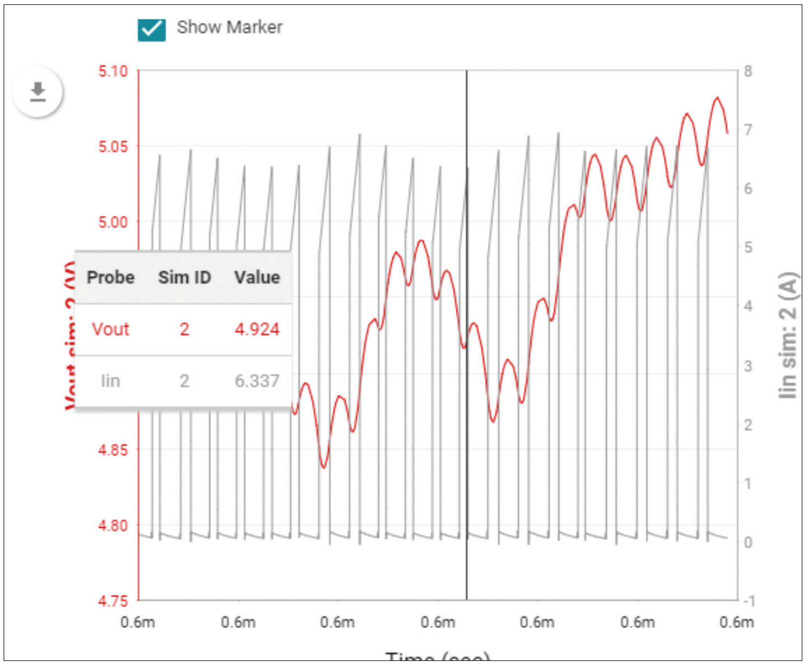
The image shows the window that appears after clicking on the I_{OUT} icon on the schematic. You can enter a new load current value in the text box and **Save Changes**, then start a new simulation to see the new results.



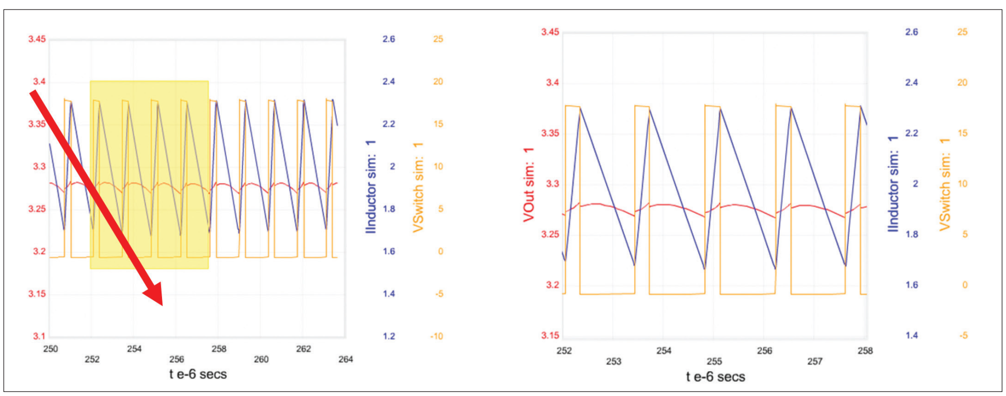
To overlay plotted WAVEFORMS, click the dotted icon next to **ADD WAVEFORMS** and group the plotted voltages so they overlay.



You can also check the **Marker** box to measure values along the WAVEFORMS.

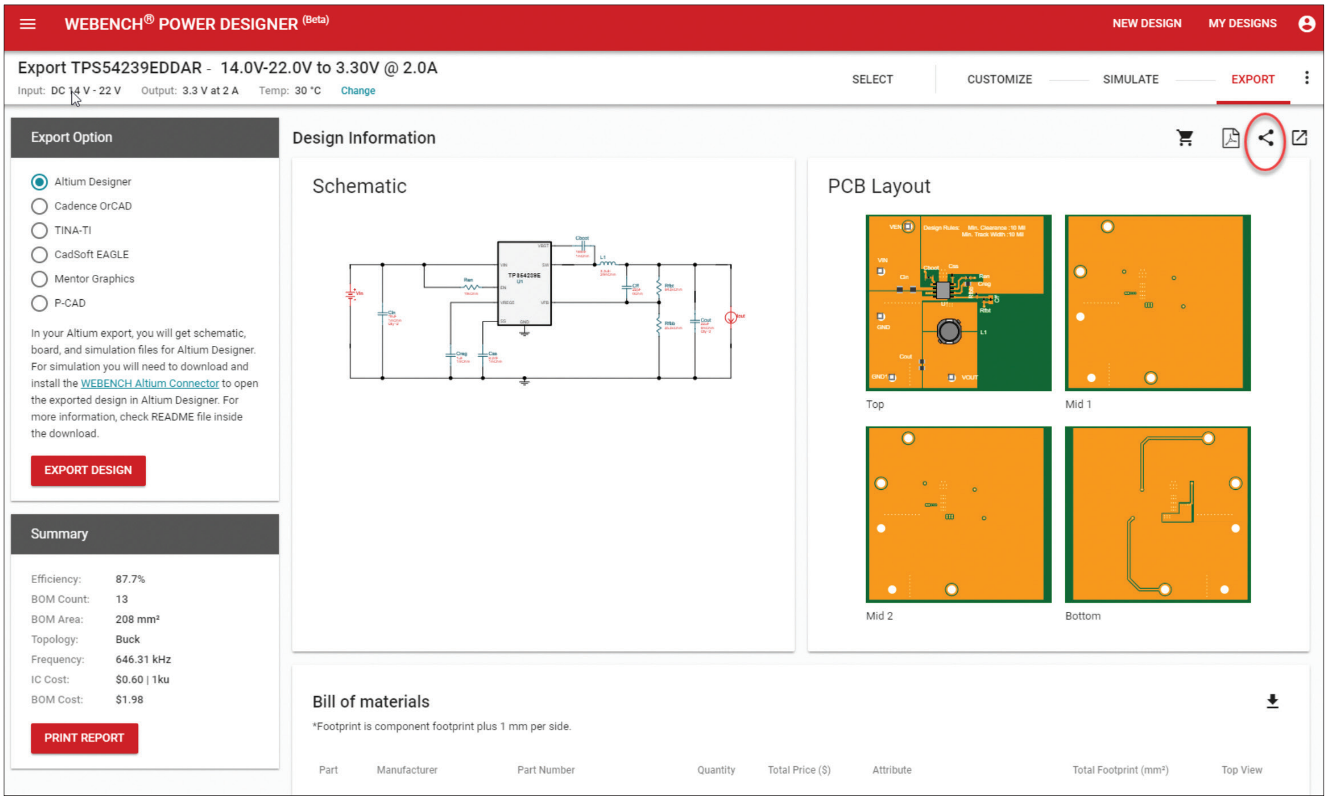


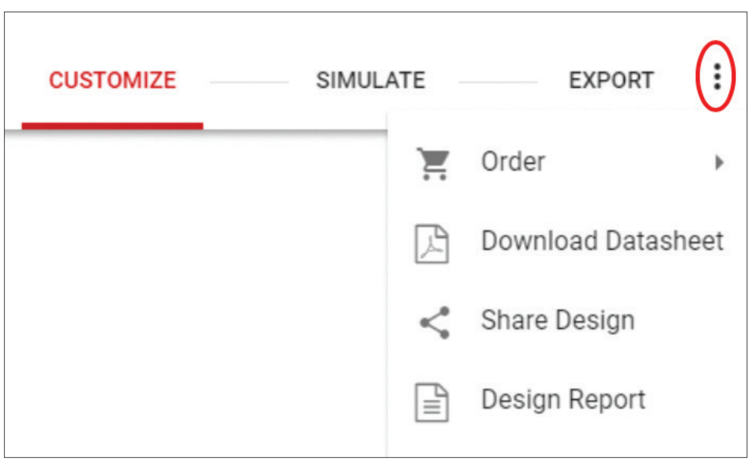
Zooming on the WAVEFORMS is achieved by selecting and dragging the pointer from the top left corner to the right corner. The opposite direction will reset zooming to full view.

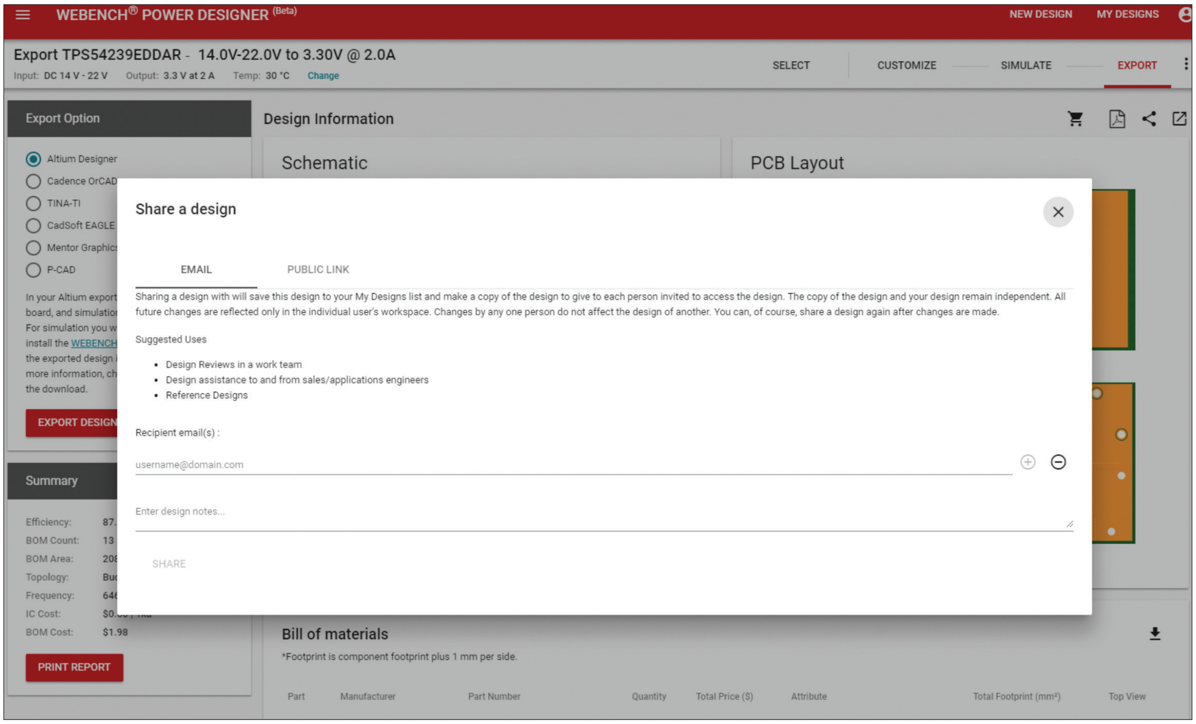


How to share a design with others

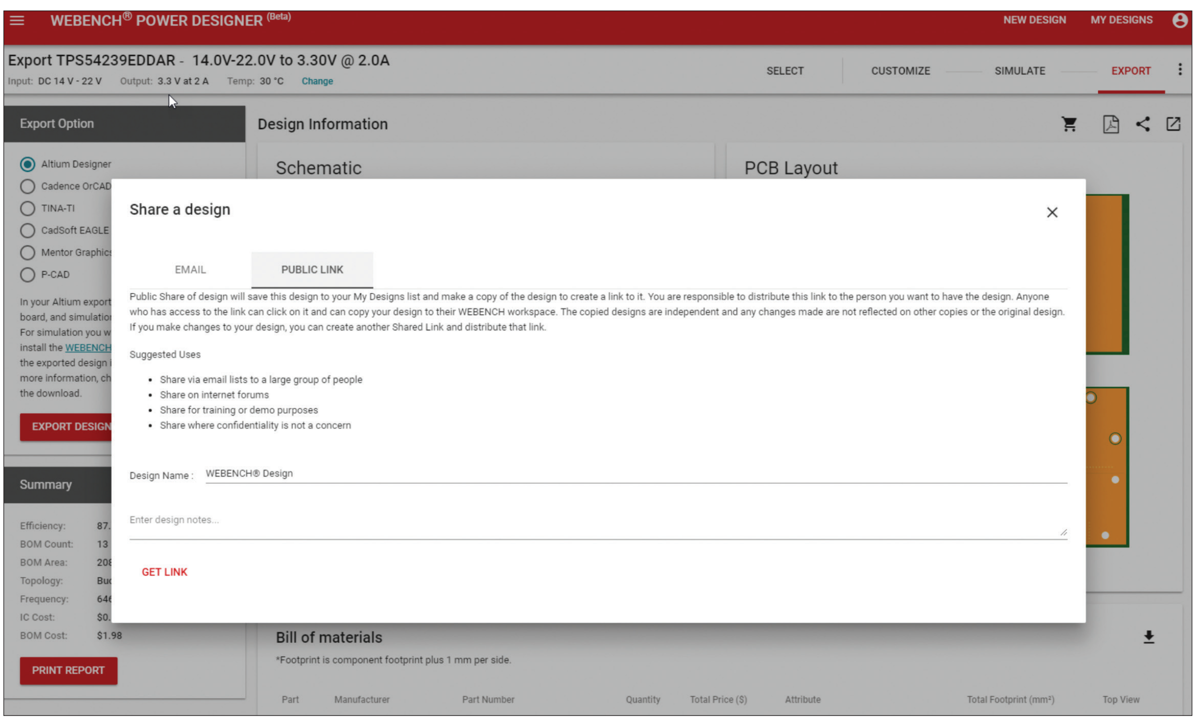
From within the **EXPORT** tab, you can share a copy of your design with others. Simply click on the share icon at the top right or navigate to the dotted icon button to the right of the **EXPORT** tab and select **'Share Design'**. Enter the recipient's email address in the text box and **WEBENCH** will send an email inviting them to open the shared design. It will create a copy of your design in their account so that their edits will not affect your original design.







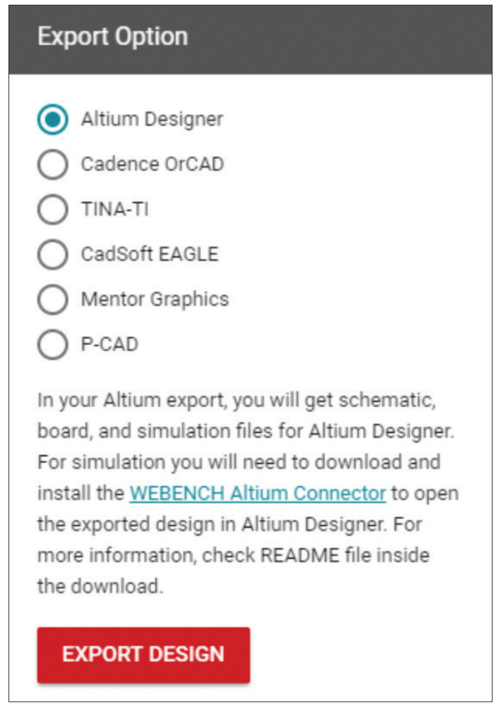
You can also create a **Public Link** to share the design with several recipients. Anyone with the shared link can create a copy of your design in their account. Simply provide a **Design Name** along with any comments and click on the **GET LINK** button to generate the link.



How to Export a design to CAD

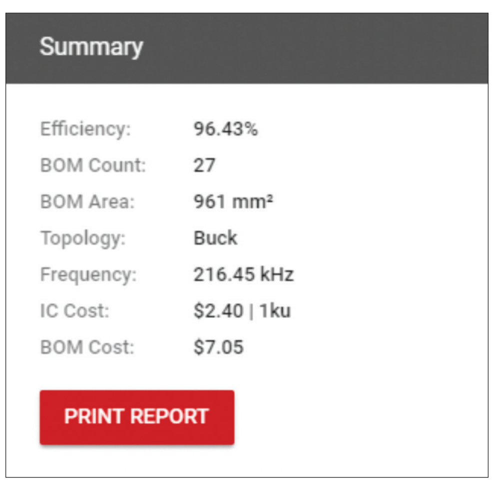
The **EXPORT** tab allows you to export your design to various CAD tools. You can select the **CAD tool** of your choice by selecting the radio button and then clicking **EXPORT DESIGN**.

This will generate a zip file. Unzip the file and follow the instructions in the readme file to open the schematic, layout and simulations in the respective tools.



How to generate PDF reports

From within the **EXPORT** tab, at the bottom left of the page is a **PRINT REPORT** section, which can be used to provide a full PDF report of all your design materials, including the schematic, BOM, operating values, layout, and simulations.



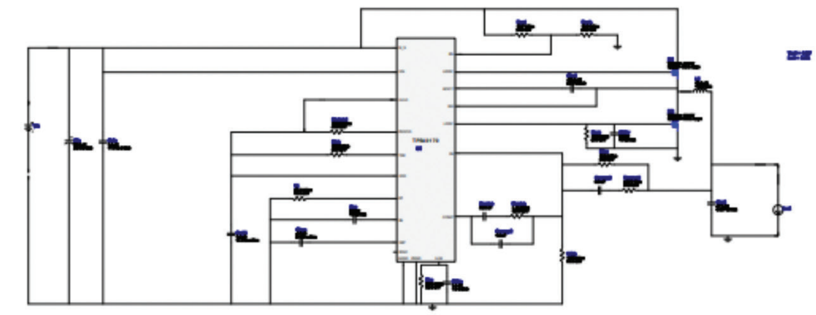
TEXAS INSTRUMENTS

WEBENCH ® Design Report

VinMin = 9.0V
VinMax = 24.0V
Vout = 5.0V
Iout = 6.0A

Device = TPS40170RGYR
Topology = Buck
Created = 2018-07-26 16:29:25.218
BOM Cost = $7.05
BOM Count = 27
Total Pd = 1.11W

Design : 17 TPS40170RGYR
TPS40170RGYR 9.0V-24.0V to 5.00V @ 6.0A



Mechanical BOM

#	WEBENCH Name	Altrium Comp Type	Part Name	FootPrint
1.	VIN	Test Point, Red, Thru Hole	TP-1502	TP-1502
2.	GND	Test Point, Red, Thru Hole	TP-1502	TP-1502
3.	GND1	Test Point, Red, Thru Hole	TP-1502	TP-1502
4.	VOUT	Test Point, Red, Thru Hole	TP-1502	TP-1502

Electrical BOM

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cbst	Kemet	C0805C104M5RACTU Series= X7R	Cap= 100.0 nF ESR= 64.0 mOhm VDC= 50.0 V IRMS= 1.64 A	1	$0.01	0805 7 mm²
Cbyp	MuRata	GRM21BC81E475KA12L Series= X6S	Cap= 4.7 uF ESR= 5.166 mOhm VDC= 25.0 V IRMS= 2.03531 A	1	$0.03	0805 7 mm²
Ccomp	TDK	CGA4J2C0G1H333J125AA Series= C0G/NP0	Cap= 33.0 nF VDC= 50.0 V IRMS= 0.0 A	1	$0.10	0805 7 mm²
Ccomp2	Samsung Electro-Mechanics	CL10C122JB8NNNC Series= C0G/NP0	Cap= 1.2 nF VDC= 50.0 V IRMS= 0.0 A	1	$0.01	0603 5 mm²
Ccomp3	TDK	C2012C0G1H392K060AA Series= C0G/NP0	Cap= 3.9 nF VDC= 50.0 V IRMS= 0.0 A	1	$0.04	0805 7 mm²
Cilim	MuRata	GRM216R71E102KA01D Series= X7R	Cap= 1.0 nF ESR= 1.0 mOhm VDC= 25.0 V IRMS= 0.0 A	1	$0.01	0805 7 mm²
Cin	Panasonic	50SVPF39M Series= SVPF	Cap= 39.0 uF ESR= 25.0 mOhm VDC= 50.0 V IRMS= 3.8 A	1	$0.78	CAPSMT_62_E12 106 mm²

TI-PMLK LDO Experiment 1

Impact of line and load conditions on dropout voltage

Using TI WEBENCH® Power Designer

LDO (TPS7A4901)

TI-PMLK LDO Experiment 1

Pre-Work

Before starting with this exercise, please refer to TI-PMLK LDO experiment book, review the sections on **Case Study** and **Theory Background**. Refer the TI-PMLK LDO board to configure design in **WEBENCH**. Login or register for your my.ti.com account to access **WEBENCH**.

Goal

The goal of this experiment is to analyze how the dropout voltage and output voltage accuracy of the LDO regulator depend on line and load conditions. **WEBENCH® Power Designer Tool** will be used to provide analysis and simulation results to compare with your **TI-PMLK** lab experiments.

Test #1:

Impact of load current and output voltage setting on dropout voltage

Calculations

- Dropout voltage of the **TPS7A4901** is measured under conditions below
- Measure V_{OUT} at 95% V_{OUT} (nominal) for V_{IN}
- Calculate dropout as $V_{DO} = V_{IN} - V_{OUT}$

Procedure

1. Click on the link to open the V_{OUT} = 5V TPS7A4901 design in WEBENCH® Power Designer.
   Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 1**.

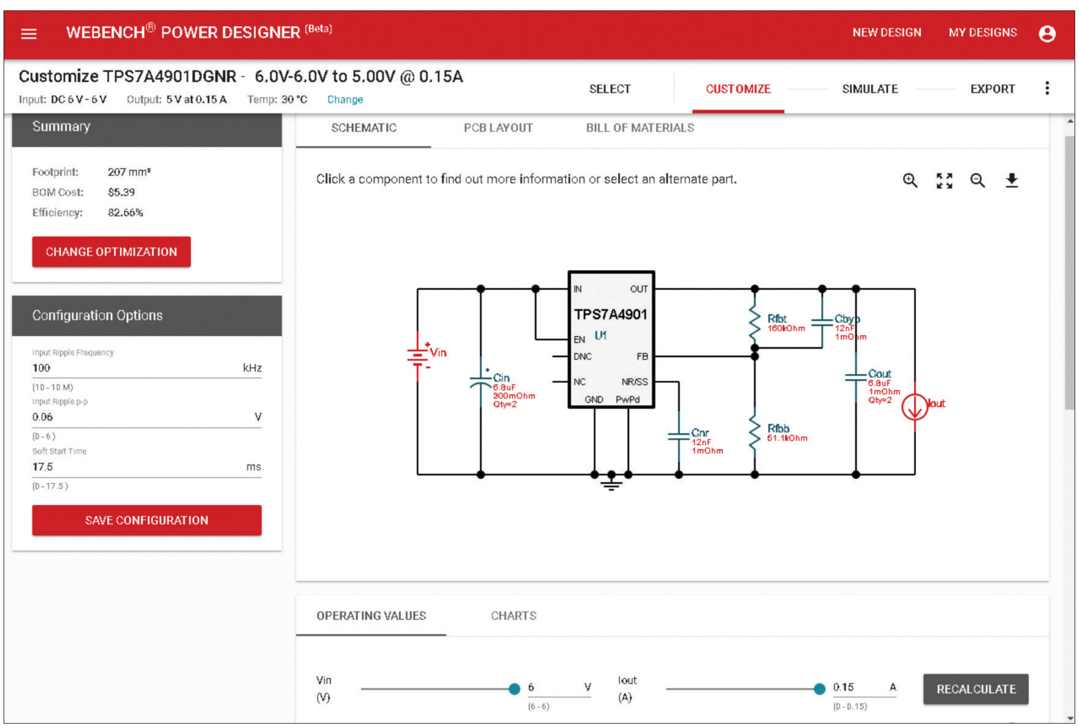


Figure 1.

2. Click the **'SIMULATE'** button to access the electrical simulation environment.

Note: R_{load} = 33.3 ohms, for the case I_{OUT} = 150mA. See **Figure 2**.

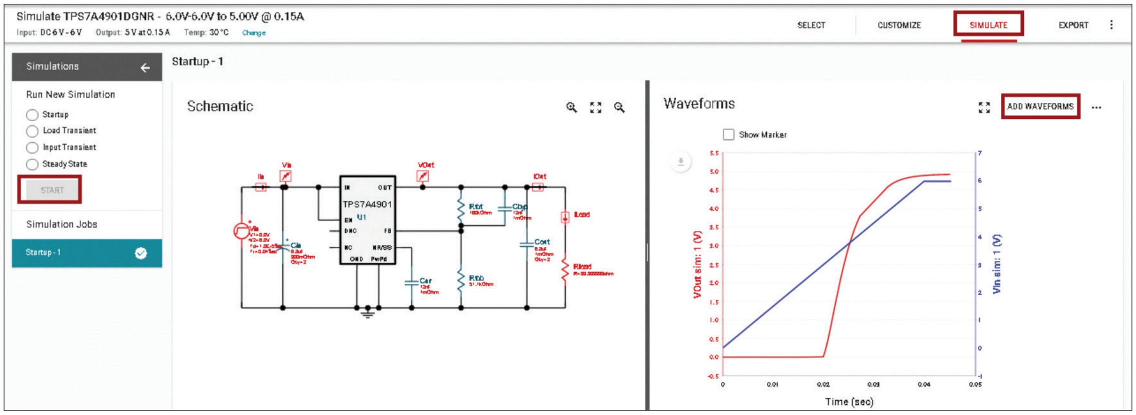


Figure 2.

3. Click the green **'START'** button after selecting the **Startup** button. A streaming **WAVEFORM control** panel will appear.

4. When the simulation is complete, WAVEFORM for V_{IN} (which is V_{IN}) and V_{OUT} (which is V_{OUT}) will appear by default. The WAVEFORMS for those two nodes will appear from the first simulation as noted by V_{OUT} sim: 1 and V_{IN} sim: 1. The next simulations will appear with the simulation number after the colon.

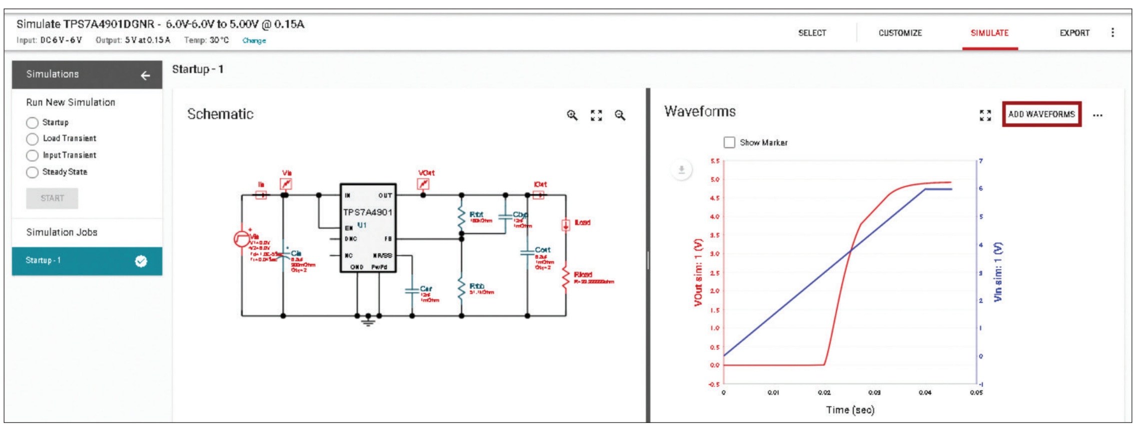


Figure 3.

5. Click on highlighted button (Step-1) in below image. The WAVEFORM Controls dropdown will appear. Click the **"Group voltage on same Y-axis"** option (Step-2) see **Figure 4**, which will force Y-axis voltage scales for V_{IN} and V_{OUT} to be the same. Then click the **'Reset Groups'** (Step-3) option to dismiss it.

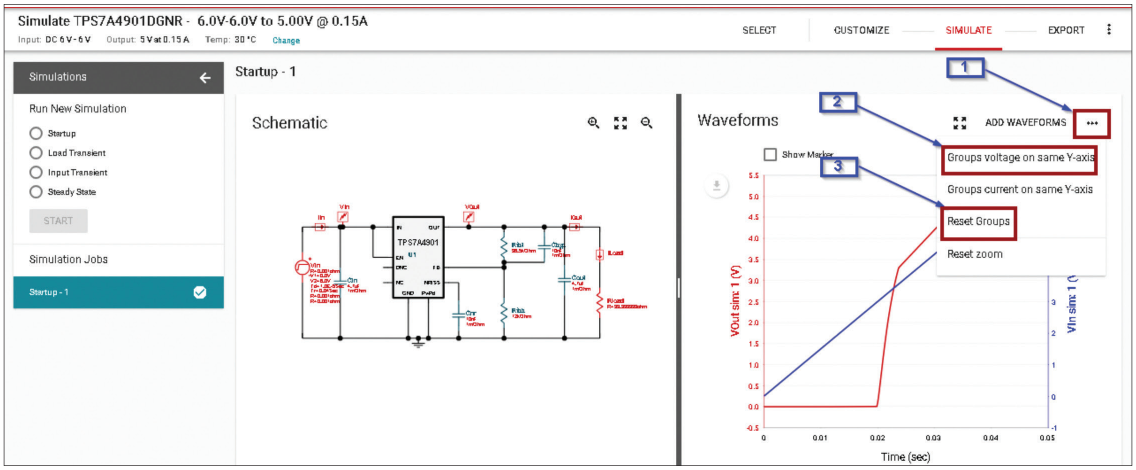


Figure 4.

6. Observe that VOut (V_{OUT}) and VIn (V_{IN}) now use the same Y-axis scale. Click the **'Show Marker'** to enable the active cursor, and position it at V_{IN} = 4.655V as close as you can (V_{IN} = 4.655V which is 95% of V_{OUTNOM} = 4.9V) see **Figure 5**. **Note:** The values of V_{IN} and V_{OUT}. Enter into **Table 1** (for I_{OUT} = 150mA, V_{OUTNOM} = 4.9V) the values for VIn (= V_{IN}), VOut (= V_{OUT}), and the calculated value for $V_{dropout}$ (=V_{IN}-V_{OUT}).

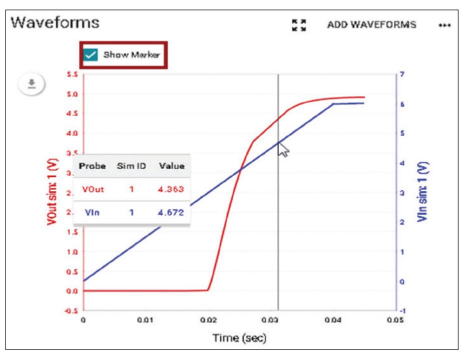


Figure 5.

V_{IN}(V) @ 95%V_{OUTNOM}	I_{OUT} (mA)					
V_{OUT}(V) @ V_{IN} V_{DROP}(mV)	**25mA**	**50mA**	**75mA**	**100mA**	**125mA**	**150mA**
V_{OUTNOM} = 4.9V						
V_{OUTNOM} = 14.9V						

Table 1: Dropout voltage at V_{OUT} = 5V & 15V vs I_{OUT} Load current.

Calculations:

7. To set up the simulation for other loads, you will need to change the **Load Resistance** used for the simulation. See **Figure 6**. From the simulation schematic after selecting the. Click on **'Startup'** button on the top left, click the **'R_{load} resistor'** component. A pop-up will appear. Click on **'Update'**. Enter the Nominal value matching your new load current, and then click **'SAVE'**.

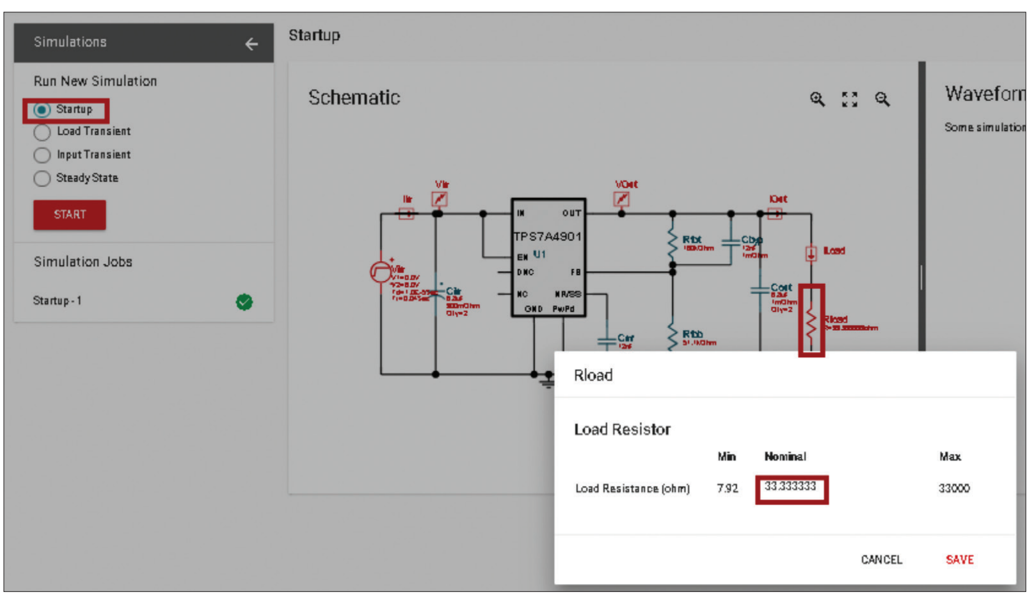


Figure 6.

For V_{OUT} = 5V:

Load	Rload
150mA	33.3 Ω
125mA	40 Ω
100mA	50 Ω
75mA	66.7 Ω
50mA	100 Ω
25mA	200 Ω

For V_{OUT} = 15V:

Load	Rload
150mA	100 Ω
125mA	120 Ω
100mA	150 Ω
75mA	200 Ω
50mA	300 Ω
25mA	600 Ω

Table 2.

Click on the **'Cancel'** to remove the window. Click on **'START'** button to run the simulation. Once the simulation completes, your previous plot of Vin and Vout will appear from the original simulation (shown in **Figure 2**) along with new V_{IN} and V_{OUT}. You will now see the plot for VIn (V_{IN}) along with the plots of VOut (V_{OUT}) for the various load simulations. Repeat **Step 5** to group the voltages, refer **Figure 4**. Repeat **Step 6** to record the new data.

8. Repeat **Steps 4-7** for the remaining load currents see **Table 2**.

9. For target V_{OUT} = 15V, you need a design with R1 = 594k (which is Rfbt in your **WEBENCH** design). Open this link to open the TPS7A4901 design set up for V_{OUT} = 15V.

10. Repeat **Steps 4-8** for target V_{OUT} = 15V and all the load currents and record your results in **Table 1**. When recording data for VOut (V_{OUT}), use marker for VIn (V_{IN}) = 14.15V which is 95% of V_{OUTNOM} (= 14.9V).

Test #2:

Impact of load current on output voltage (load regulation); and impact of input voltage setting on output voltage (line regulation)

Calculations

1. V_{OUT} Load Sensitivity (%) = $|(V_{OUTNOM} - V_{OUT})|/V_{OUTNOM}$ x 100

- Measure V_{OUT} for different loads, and then calculate load regulation.
- Load regulation is defined by the TPS7A4901 datasheet as the change in V_{OUT} over a change in I_{OUT} divided by V_{OUTNOM}:

  Load Regulation (%) = $\Delta V_{OUT}(\Delta I_{OUT})/V_{OUTNOM}$ x 100

  Calculate Load Regulation by using the change in V_{OUT} from 25mA to 150mA and compare to the datasheet typical value of 0.04%V_{OUT}.

2. V_{OUT} Line Sensitivity (%) = $|(V_{OUTNOM} - V_{OUT})|/V_{OUTNOM}$ x 100

- Measure V_{OUT} for different V_{IN}, you can then calculate line regulation.

  Line Regulation (%) = $\Delta V_{OUT}(\Delta V_{IN})/V_{OUTNOM}$ x100

  Calculate Line Regulation by using the change in V_{IN} from 6V to 21V and compare to the datasheet typical value of 0.086% V_{OUT}.

Impact of load current on output voltage (load regulation):

Procedure

1. Click on the link to open the V_{out} = 5V TPS7A4901 design in WEBENCH® Power Designer
   Note: Need to be sure that V_{IN} = 6V on design. We can leave the shared design exactly as the **TI-PMLK** board.
2. Your design will be ready within **WEBENCH Power Designer** configured for this experiment.

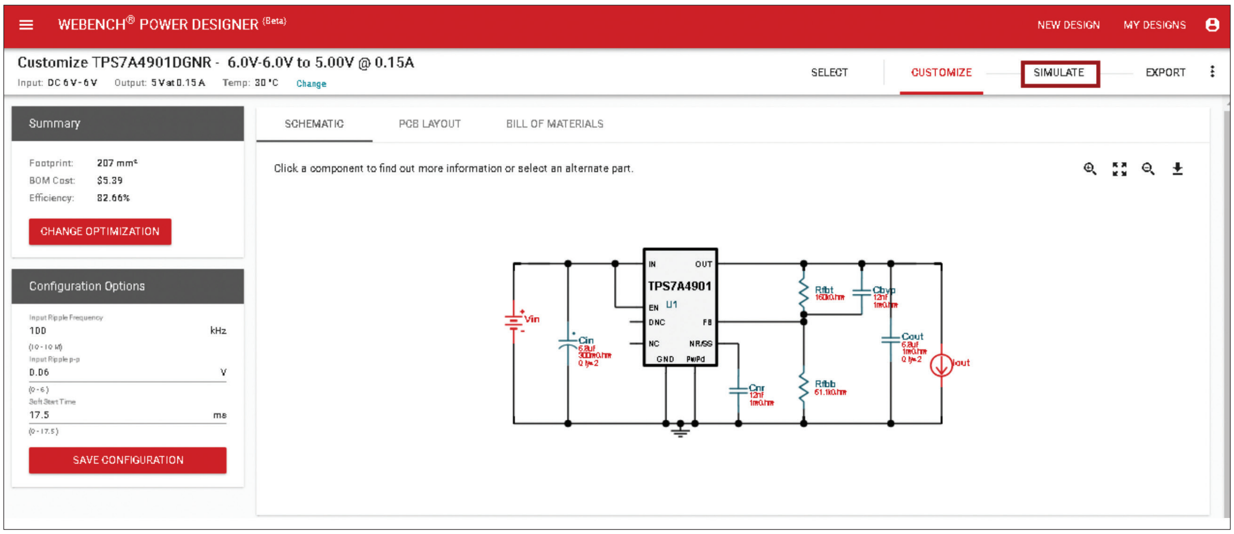


Figure 7.

3. Click the **'SIMULATE'** button (see top panel in **Figure 7**) to access the electrical simulation environment. Click the **input source symbol** to see its **Simulation Parameters** pop-up, Click on **'Update'**. Select **Rise Time** (source rise time), click **'SAVE'**. Select **V2**, enter 6 (for V_{IN} = 6V), then dismiss the pop-up.

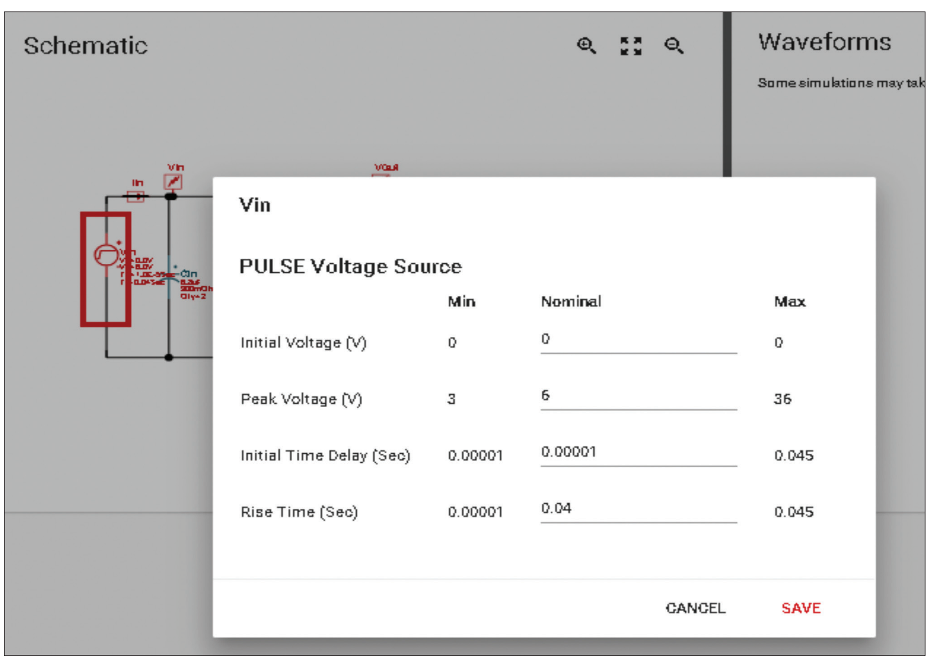


Figure 8.1.

4. **Note** that R_{load} = 33.3 ohms, for the case that I_{OUT} = 150mA

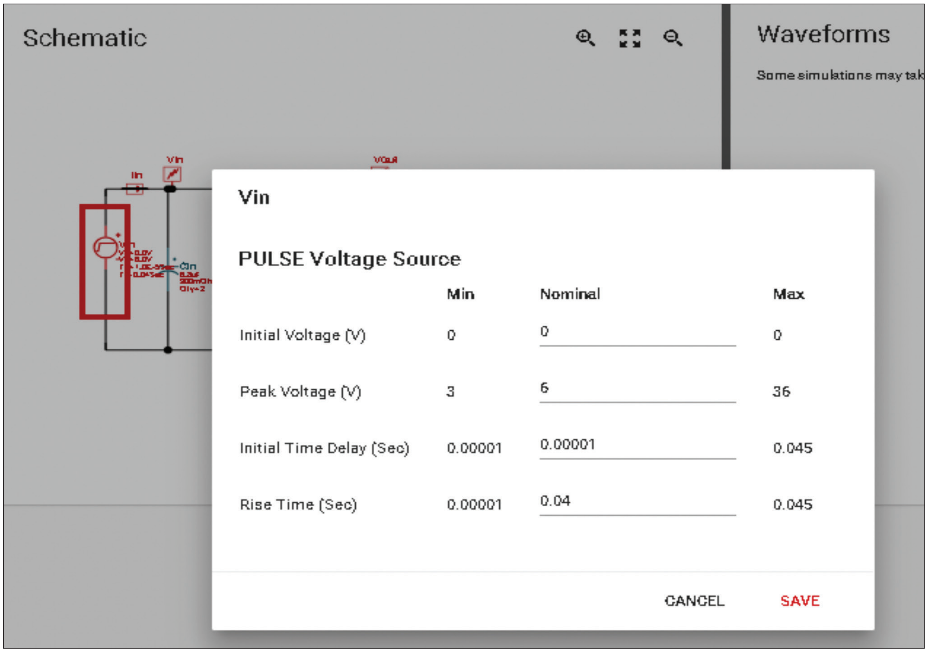


Figure 8.2.

5. Click the Red **'START'** button. A streaming **WAVEFORM control** panel will appear. When the simulation is complete, by defualt WAVEFORMS for V_{IN} (which is V_{IN}) and V_{OUT} (which is V_{OUT}) nodes will appear. Click **'Show Marker'** to obtain values for the node voltages. Center the marker in the window, at around 0.040 seconds. Enter the value (at least 3 decimal places) for VOut (V_{OUT}) in the appropriate cell of **Table 2**. (For the first case, it's for V_{IN} = 6V, I_{OUT} = 150mA). Once you record the V_{OUT} result, calculate the load sensitivity by means of formula for each value of load current (remember to take the absolute value of the difference of V_{OUTNOM} and V_{OUT}.

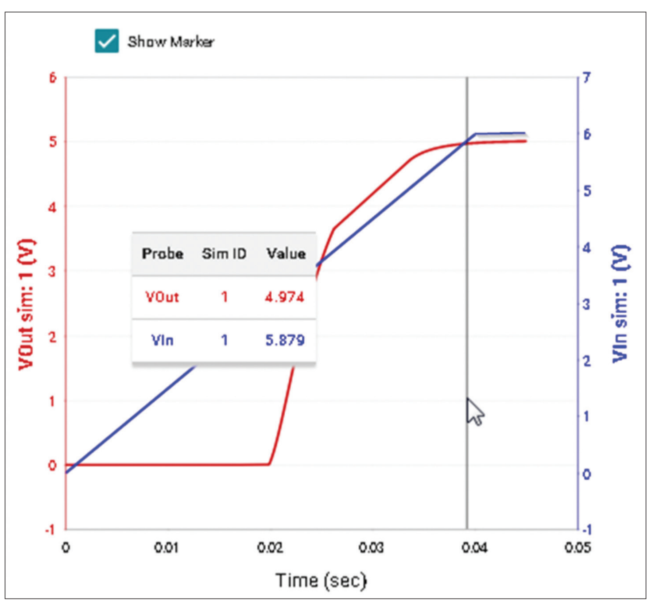


Figure 9.

6. To set up the simulation for other loads, you will need to change the load resistance used for the simulation. Click on the **'Startup'** button on the left from the simulation schematic, click on the **'R_{load} resistor'** component. A **Component Simulation Parameters** pop-up will appear. Enter the nominal value matching your new load current, then click **'SAVE'**.

   Click the **'START'** button on the left side. Once the simulation completes, your previous plot of V_{IN} and V_{OUT} will appear from the original simulation along with the new V_{IN} and V_{OUT} for the various load simulations. Repeat **Step 6** to record the new data.

For V_{OUT} = 5V:

Load	Rload
150mA	33.3 Ω
125mA	40 Ω
100mA	50 Ω
75mA	66.7 Ω
50mA	100 Ω
25mA	200 Ω

Table 2.

7. Repeat **Step 7** for V_{IN} = 6V and the remaining load current settings shown in **Table 4**.

V_{IN} = 6V	I_{OUT} (mA)					
	25mA	**50mA**	**75mA**	**100mA**	**125mA**	**150mA**
V_{OUT} (v)						
Load sensitivity (%)						

Table 4. *V_{OUT} Load Sensitivity of TPS7A4901 LDO Regulator at V_{OUT} = 5V.*

Impact of input voltage setting on output voltage (line regulation):

8. To get ready for the Line Regulation simulations, first remove the plots of the previous load regulation sims. To remove the plots, click on the plot you wish to delete and click on the **'Remove probe'** option from the dropdown. Repeat for every plot you wish to delete.

9. At this point, your design should be set up for V_{IN} = 6V and I_{OUT} = 25mA. To prepare to fill out **Table 5** for line regulation, you will change the value of Rload fixed at 200 ohms to 100 ohms to set the load current at 50mA, Click on the **'SAVE'** button on the bottom to update the value of Rload and change V_{IN} for line regulation tests. From the simulation schematic, double-click the R_{load} resistor component. A "Component Simulation Parameters" pop-up will appear. Enter the nominal value matching your new load current, and then click **'SAVE'**. Click on the **'CLOSE'** to remove the window. Hit **'START'** to run the sim for V_{IN} = 6V and I_{OUT} = 50mA.

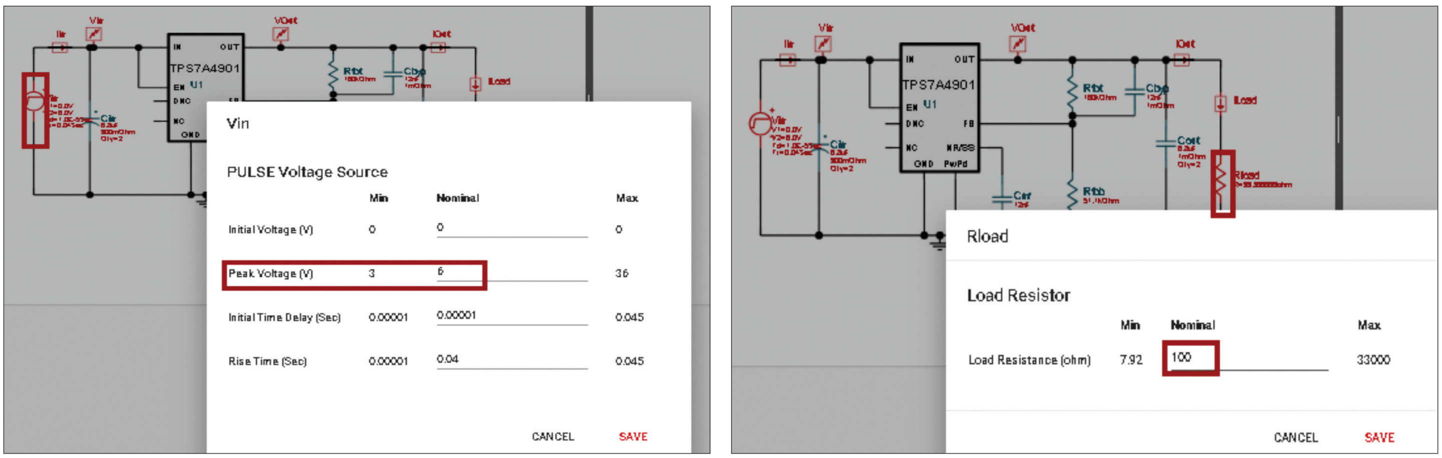


Figure 8.2.

10. Run simulation as before in **Step 5**. Note the value of VOut (V_{OUT}) as in **Step 6**.

11. Change the input voltage to the next value in **Table 5**. Repeat **Step 11** until **Table 3** is completely filled out. Once you record the V_{OUT} result, calculate the line sensitivity by means of formula for each value of input voltage

I_{OUT} = 50mA	V_{IN} (V)					
	6V	**9V**	**12V**	**15V**	**18V**	**21V**
V_{OUT} (v)						
Load sensitivity (%)						

Table 5. V_{OUT} Line Sensitivity of TPS7A4901 LDO Regulator at V_{OUT} = 5V.

Calculations:

TI-PMLK LDO Experiment 2

Impact of line and load conditions on efficiency

Using TI [WEBENCH® Power Designer]

LDO (TPS7A4901)

TI-PMLK LDO Experiment 2

Pre-Work

Before starting with this exercise, please refer to [TI-PMLK LDO experiment book](), review the sections on **Case Study** and **Theory Background**. Refer the [TI-PMLK LDO board]() to configure design in **WEBENCH**. Login or register for your [my.ti.com]() account to access **WEBENCH**.

Goal

The goal of this experiment is to analyze the correlations between the efficiency of the LDO regulator and the values of the load current and the line voltage. **WEBENCH® Power Designer Tool** will be used to provide analysis and simulation results to compare with your **TI-PMLK** lab experiments.

Test #1:

Impact of load current at a given output voltage on the efficiency at low V_{IN} values.

Calculations

Efficiency percentage is calculated per the formula below see **Theory Background Section** of the **TI-PMLK** book:

$$\eta\ \% = (V_{OUT}\, I_{OUT})/(V_{IN}\, I_{IN}) \times 100$$

where I_{IN} equals I_{OUT} OP + IC I_{ground} from the **WEBENCH** Op Values, the equation will look like this:

$$\eta\ \% = (V_{OUT}\ \text{Actual} \times I_{OUT}\ \text{OP})/(V_{IN}\ \text{OP} \times I_{IN}\ \text{Avg}) \times 100$$

where I_{IN} AVG = I_{OUT} OP + IC I_{ground}

Note: I_{IN} AVG is calculated from the two operating values (I_{OUT} OP + IC I_{ground})) because the value for I_{OUT} OP in **WEBENCH** does not have enough decimal places to show the included ground current. (You will notice I_{OUT} OP I is in 'Amps' and IC I_{ground} in 'microAmps' so be sure and remember this when adding the two numbers together).

Procedure

1. Click on the [link] to open the TPS7A4901 design in WEBENCH® Power Designer.

   Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

   Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 1**.

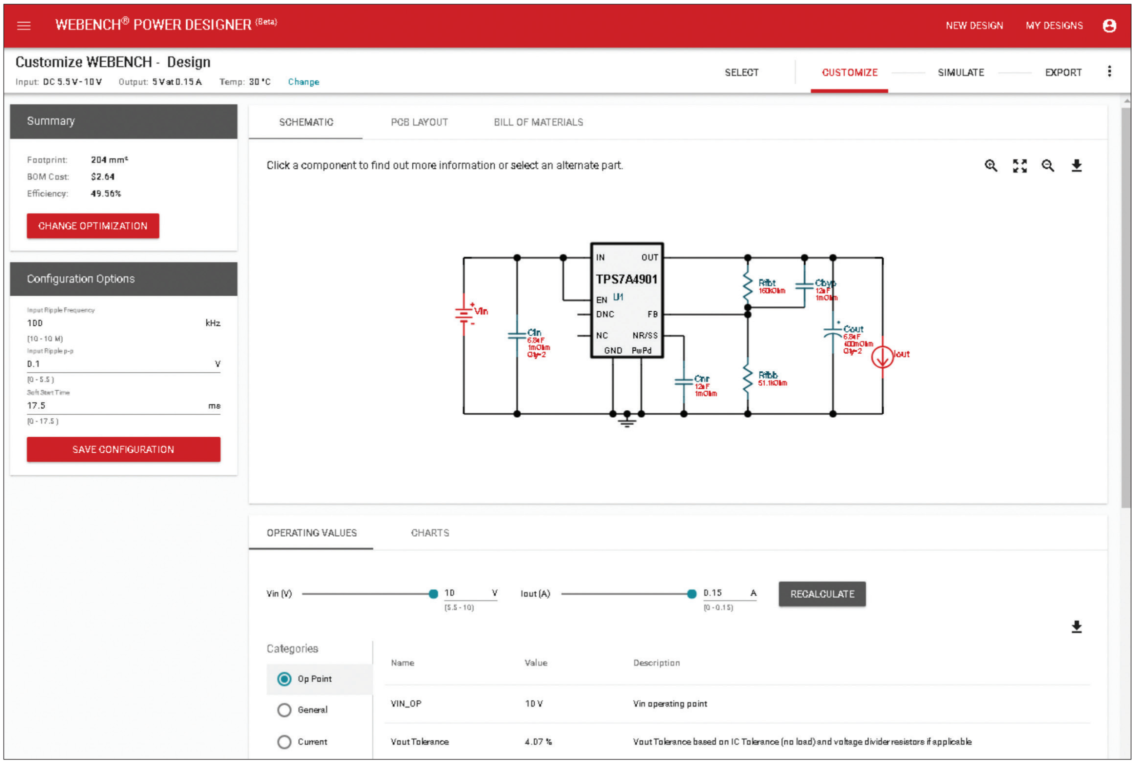


Figure 1.

2. You can click on the **'schematic'** to expand and view your **WEBENCH** design as shown in **Figure 2**.

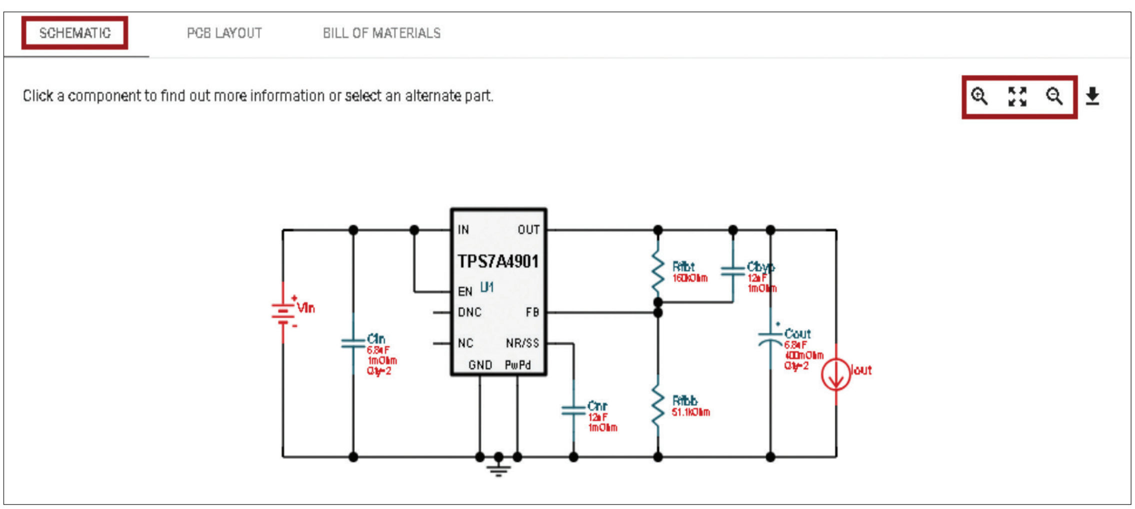


Figure 2.

3. In **WEBENCH**, select the **OPERATING VALUES** button at the bottom of the window and scroll down to view the operating values for your experiment measurements.

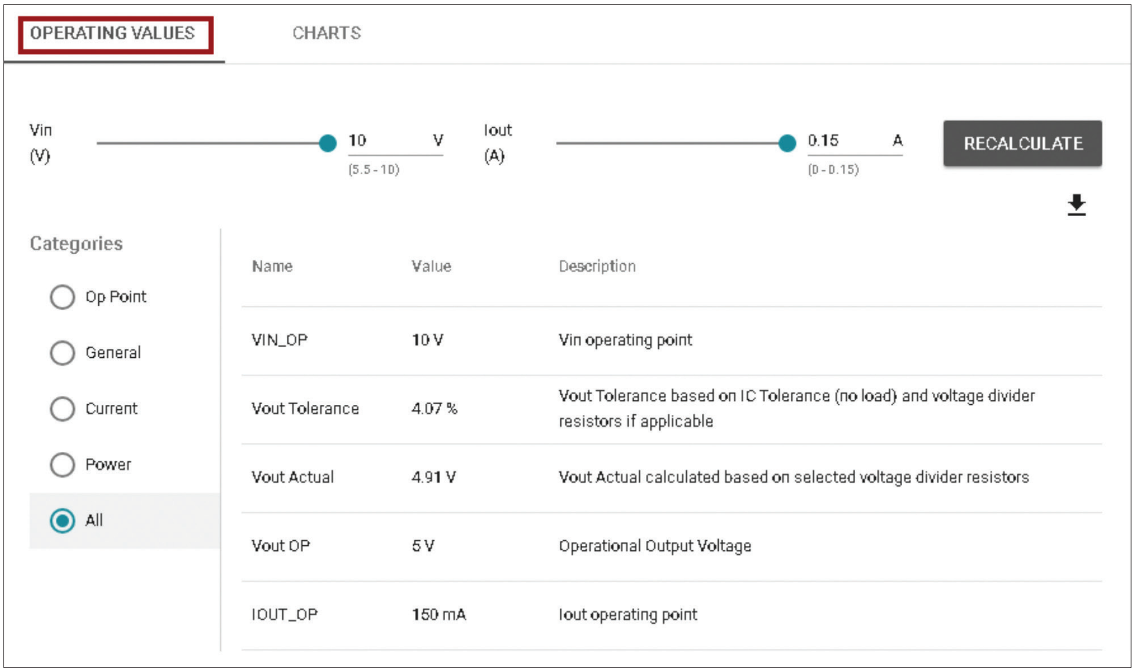


Figure 3.

4. Enter 8V for V_{IN} and 0.025 for I_{OUT} and **Recalculate**.

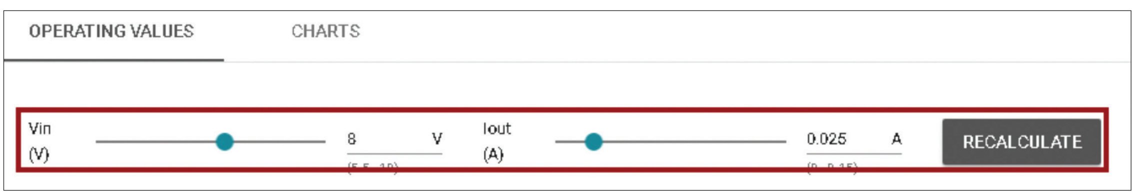


Figure 4.

5. Read the values **I_{OUT} OP, IC I_{ground}, V_{OUT} Actual, and Efficiency** from the **Operating Values table**, see **Figure 5** and enter them into **Table 1**. Calculate I_{IN} AVG from the equation and enter into **Table 1**. Then calculate efficiency from the equation using the **WEBENCH Operating value table** below and enter that into **Table 1** and compare that to the efficiency read from the **Op Vals** table. You may see a slight difference and this is due to the fact that **WEBENCH** uses V_{OUT} Op to calculate efficiency and we will use the V_{OUT} Actual voltage in our equation.

Again, efficiency is calculated as follows:

$$\eta\ \% = (V_{OUT} I_{OUT})/(V_{IN} I_{IN}) \times 100$$

To use the values from the **WEBENCH** Op Values, the equation will look like this:

$$\eta\ \% = (V_{OUT}\text{ Actual} \times I_{OUT}\text{ OP})/(V_{IN}\text{ OP} \times I_{IN}\text{ AVG}) \times 100$$

$$\text{where } I_{IN}\text{ AVG} = I_{OUT}\text{ OP} + \text{IC } I_{ground}$$

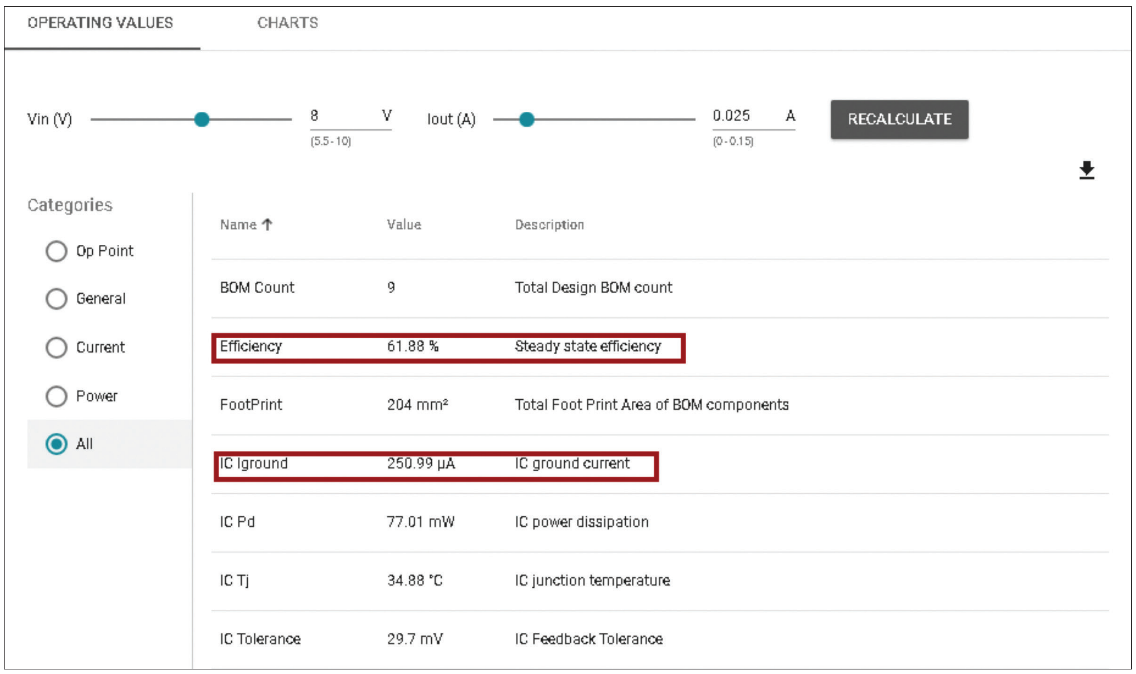


Figure 5.

6. Repeat **Step 4** for the values provided in the **Table 1**, enter the values for all combinations of input voltage and output current.

I_{OUT} OP (A) IC Iground (A) $I_{IN\ AVG}$ (A) $V_{OUT\ Actual}$ (V) η (%) from Op Vals η (%) calculated	**I_{OUT} (A)**					
	0.025	**0.050**	**0.075**	**0.100**	**0.125**	**0.150**
V_{IN} = 8V						
V_{IN} = 10V						

Table 1. *Efficiency of TPS7A4901 vs load current/input voltage for V_{OUT} = 5V.*

Calculations:

Test #2:

Impact of line voltage (higher V_{IN}) and low load currents on efficiency.

Calculations

Efficiency percentage is calculated per the formula below see ***Theory***.

Background Section of the **TI-PMLK** book:

$$\eta\ \% = (V_{OUT}I_{OUT})/(V_{IN}I_{IN}) \times 100$$

where I_{IN} equals I_{OUT} OP + IC I_{ground} from the **WEBENCH** Op Values, the equation will look like this:

$$\eta\ \% = (V_{OUT}\text{ Actual} \times I_{OUT}\text{ OP})/(V_{IN}\text{ OP} \times I_{IN}\text{ Avg}) \times 100$$

$$\text{where } I_{IN}\text{ AVG} = I_{OUT}\text{ OP} + \text{IC } I_{ground}$$

Note: I_{IN} AVG is calculated from the two operating values (I_{OUT} OP + IC I_{ground}) because the value for $I_{OUT\ OP}$ in **WEBENCH** does not have enough decimal places to show the included ground current. (You will notice $I_{OUT\ OP}$ I is in 'Amps' and IC I_{ground} in **'microAmps'** so be sure and remember this when adding the two numbers together).

Procedure

1. Click on the link to open the TPS7A4901 design in WEBENCH® Power Designer
2. Your design will be ready within **WEBENCH Power Designer** configured for this experiment.
3. You can click on the schematic to expand and view your **WEBENCH** design as shown in **Figure 2**.

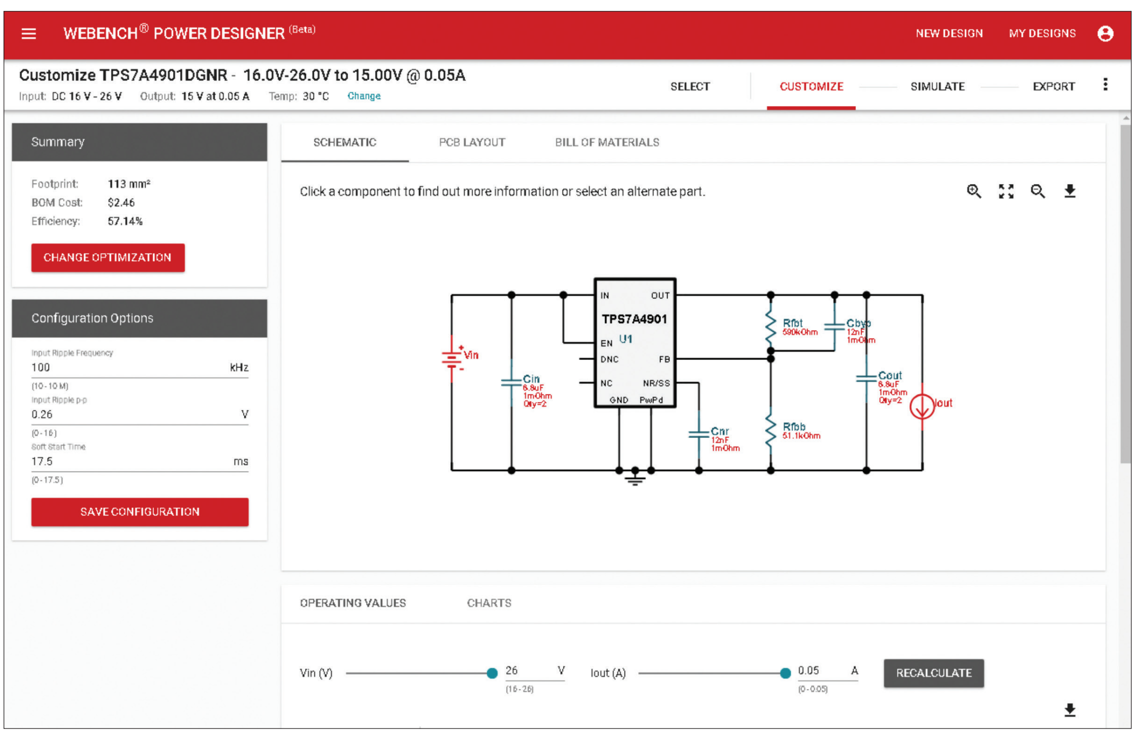


Figure 1.

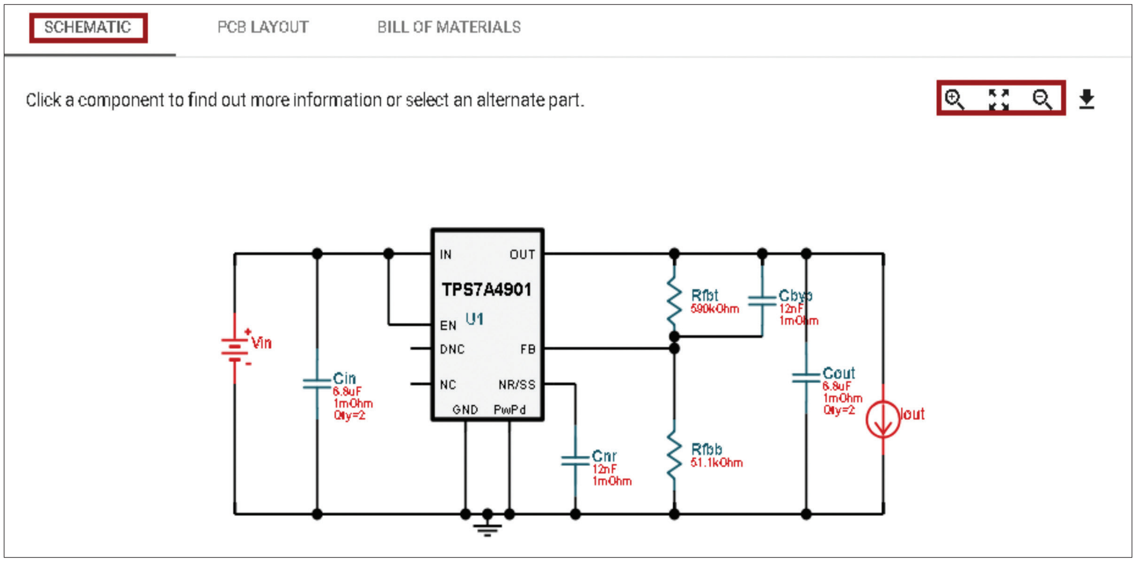


Figure 2.

4. Select the **'OPERATING VALUES'** button at the bottom of the window and scroll down to view the operating values.

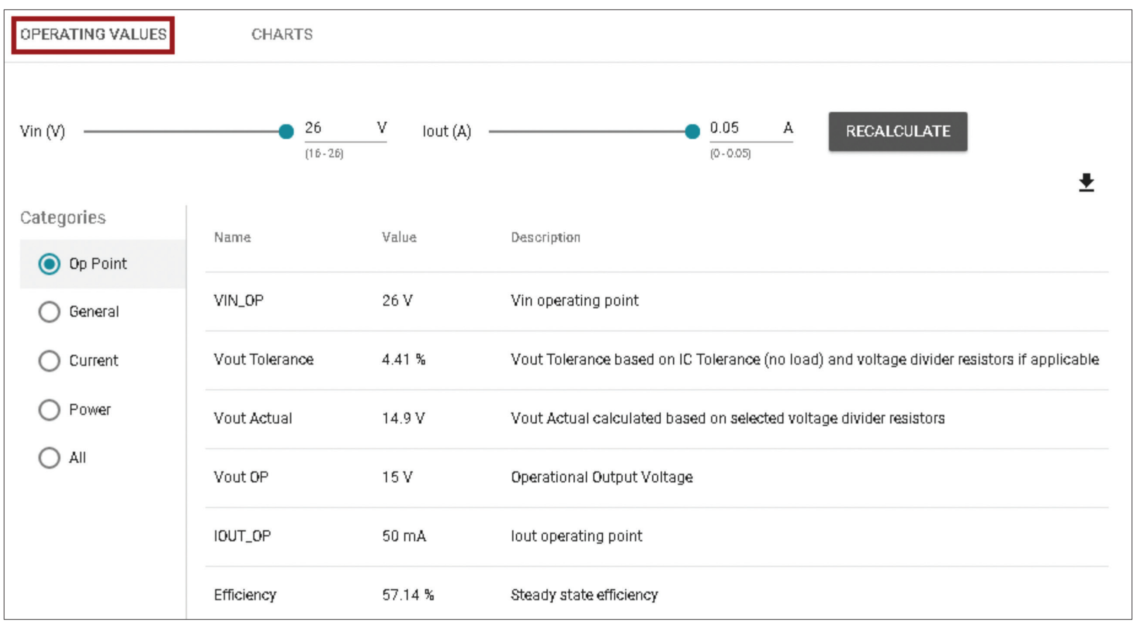


Figure 3.

5. In the **Operating Values Window** window, enter 16V for V_{IN} and 0.010A for I_{OUT} and **Recalculate**.

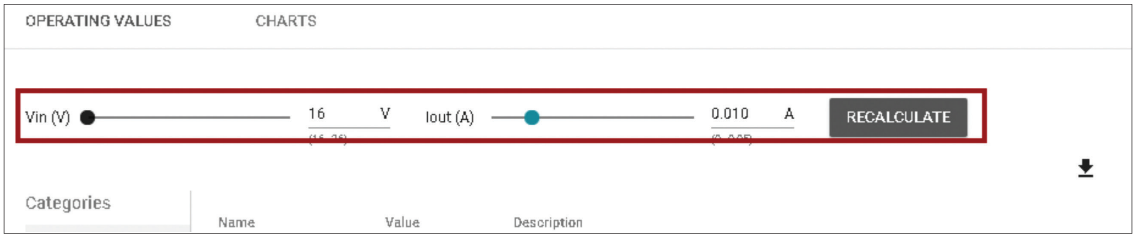


Figure 4.

6. Read the **I_{OUT} OP, IC I_{ground}, V_{OUT} Actual, Efficiency, and Total Pd** values from the **Operating Values** table and enter them into **Table 2**: Calculate I_{IN} AVG from the equation below and enter into **Table 2**. Then calculate efficiency from the equation using the **WEBENCH** Op Values and enter that into **Table 2**.

   Again, efficiency is calculated as follows:

$$\eta\ \% = (V_{OUT}\, I_{OUT})/(V_{IN}\, I_{IN}) \times 100$$

   To use the values from the **WEBENCH** Op Values, the equation will look like this:

$$\eta\ \% = (V_{OUT\ Actual} \times I_{OUT\ OP})/(V_{IN\ OP} \times I_{IN\ AVG}) \times 100$$

$$\text{where } I_{IN}\ \text{AVG} = I_{OUT}\ \text{OP} + \text{IC}\ I_{ground}$$

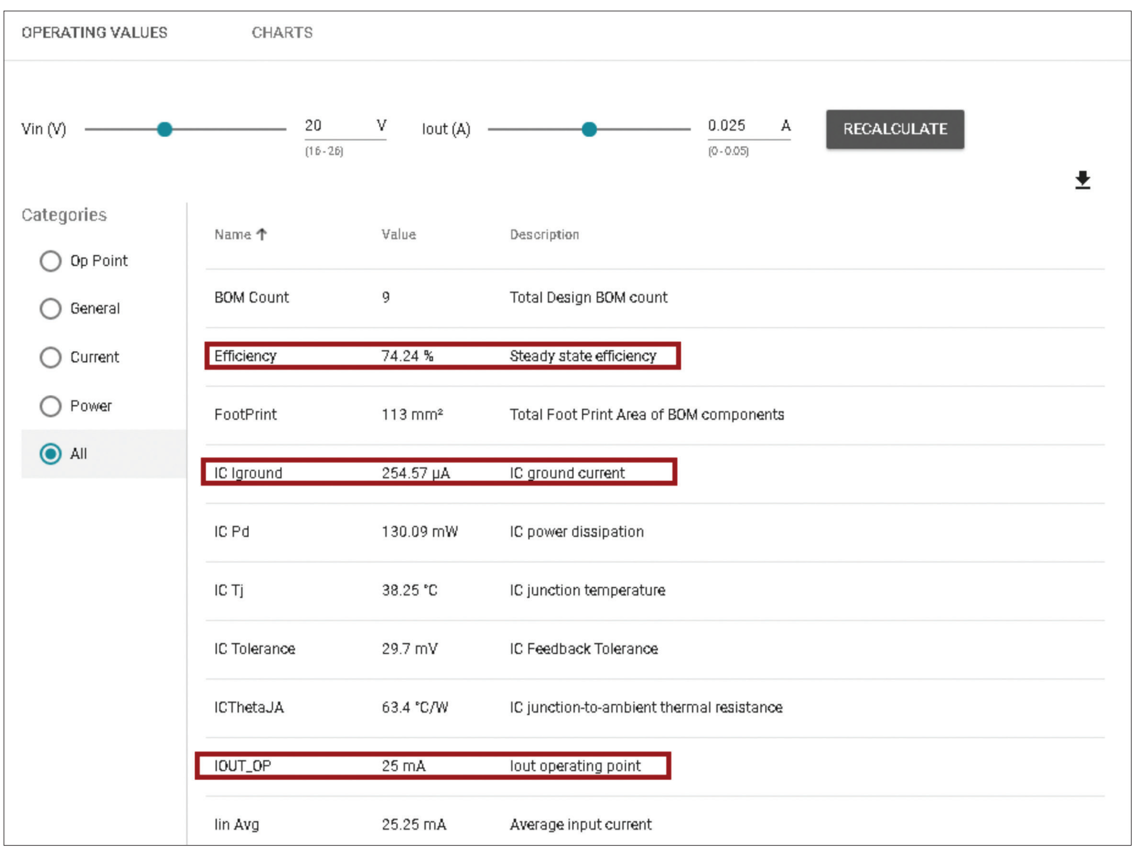


Figure 5.

7. Repeat **Step 4** and complete **Table 2**.

I_{OUT} OP (A) IC I_{ground} (A) $I_{IN\ AVG}$ (A) $V_{OUT\ Actual}$ (V) η (%) calculated P_d loss (W)	V_{IN}					
	16V	**18V**	**20V**	**22V**	**24V**	**26V**
I_{OUT} = 10mA						
I_{OUT} = 50mA						

Table 2. *Efficiency and Power Loss of TPS7A4901 at V_{OUT} = 15V.*

TI-PMLK Buck Experiment 1

Impact of operating conditions on efficency

Using TI WEBENCH® Power Designer

Buck (TPS54160)

TI-PMLK Buck Experiment 1

Pre-Work

Before starting with this exercise, please refer to TI-PMLK LDO experiment book, review the sections on **Case Study** and **Theory Background**. Refer the TI-PMLK Buck board to configure design in **WEBENCH**. Login or register for your my.ti.com account to access **WEBENCH**.

Goal

The goal of this experiment is to analyze how the efficiency of a buck regulator depends on the line and load conditions and on the switching frequency. **WEBENCH® Power Designer Tool** will be used to provide analysis and simulation results to compare with your **TI-PMLK** lab experiments.

Test #1:

Analyze variation in efficiency due to change in line voltage and load current at the switching frequency of 250kHz. Compare experimental efficiency with theoretically obtained efficiency.

Calculations

Calculate the theoretical efficiency of the converter by

$$\eta theo = P_{OUT} / (P_{OUT} + P_{loss}) \times 100,$$

$$\text{where } P_{OUT} = V_{OUT} * I_{OUT},$$

$$P_{loss} = P_{MOS,c} + P_{MOS,sw} + P_{MOS,g} + P_{diode} + P_{L,w} + P_{L,c} + P_{Cin} + P_{Cout} + P_{IC}$$

using the **Loss Formulas** given in the Theory Background section of **TI-PMLK** book.

Procedure

1. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer.
   Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 1**. Please note that the **WEBENCH** Footprint and BOM cost are displayed as NA. This is because the components in the schematic have been modified as **CUSTOM** components to match the component values and properties as the components in the **TI-PMLK** experiment board.

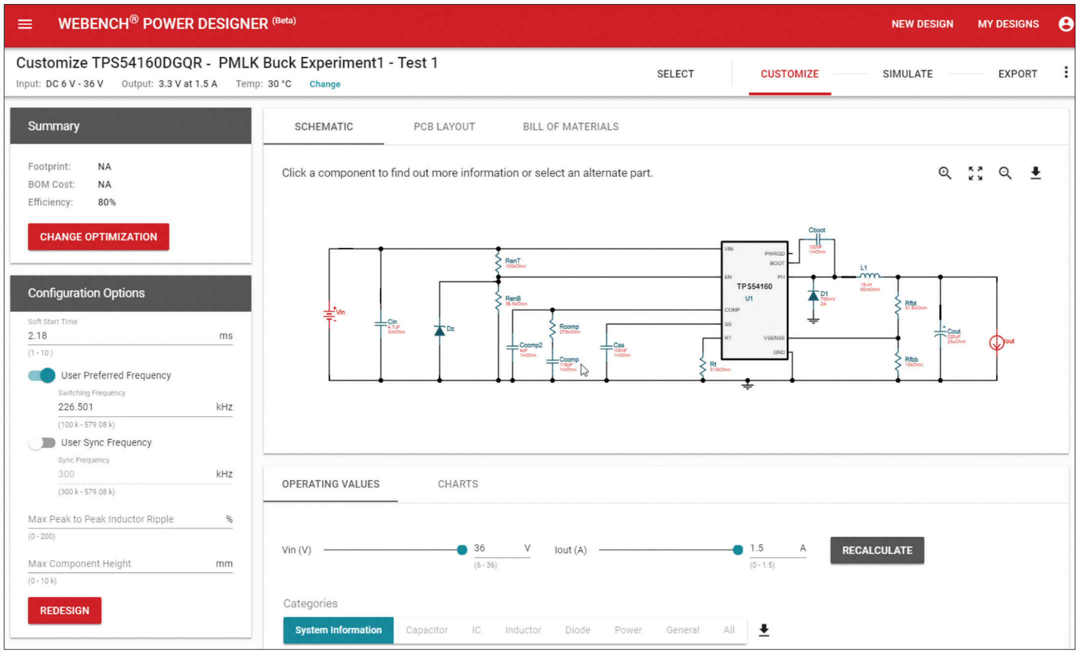


Figure 1.

Within **WEBENCH Power Designer** customize screen, you will be able to find the **'Operating Values'** tab (you can scroll to locate this).

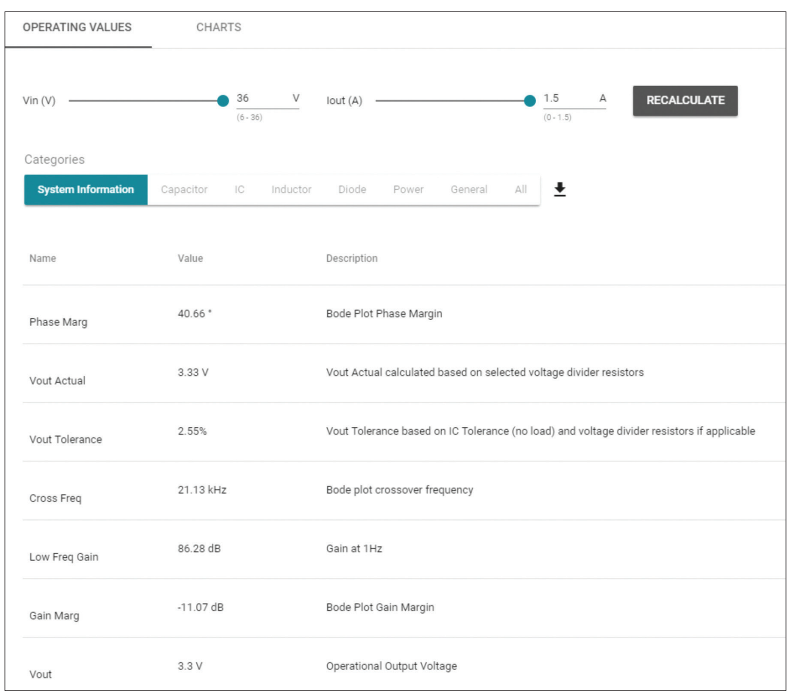


Figure 2.

Within the **'System Information'** category, you will be able to find the **Efficiency** value listed. To see the efficiency at 6V V_{IN} and 0.1A I_{OUT}, change the value using the slider or enter it in the text box at the top and then press **Recalculate**.

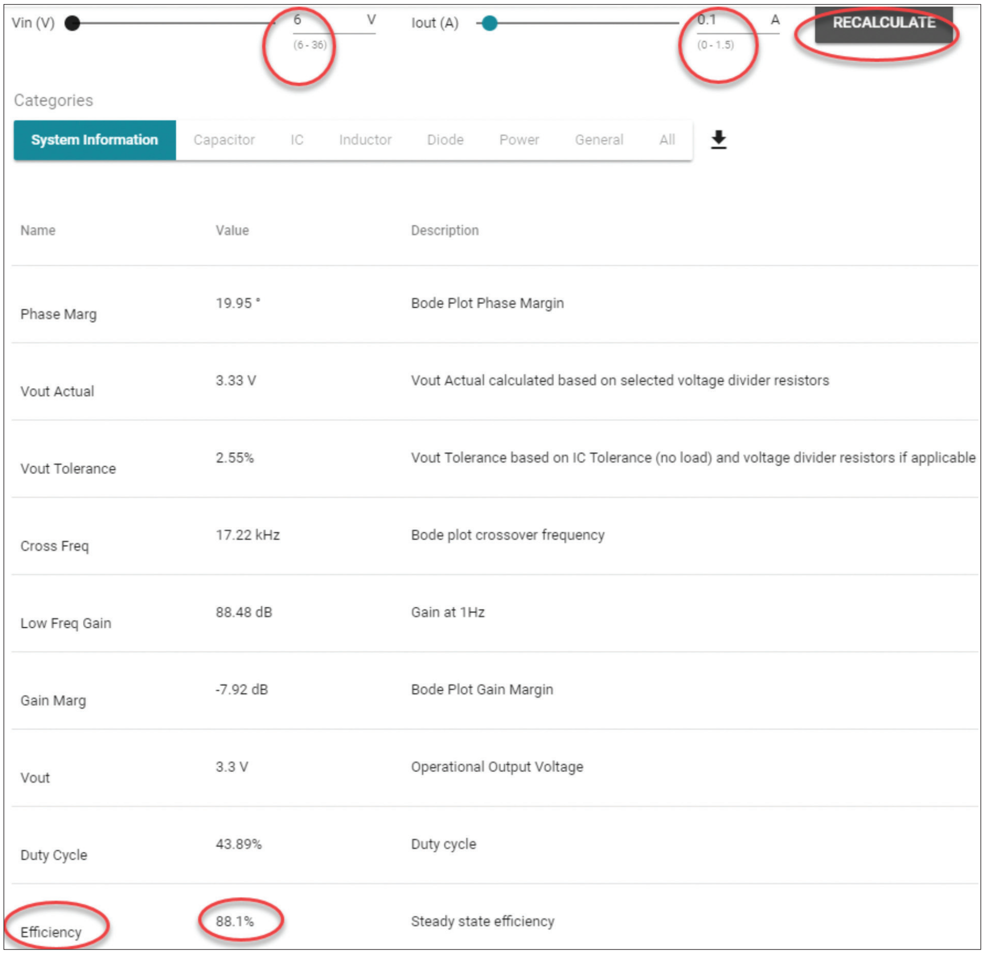


Figure 3.

Scroll down and record the value of efficiency from the **Operating Values** table as shown in **Figure 4**. Compare it wth the calculated theoretical efficiency as per the formula mentioned in **Calculation** section.

Measurements at 250KHz	Experimental / Theoretical efficiency (%)	0.1A	0.2A	0.5A	1A	1.2A	1.5A
V_{IN} = 6V	Exp. Eff.						
	The. Eff.						
V_{IN} = 24V	Exp. Eff.						
	The. Eff.						

Table 1. *Experimental vs theoretical efficiency of TPS54160 operating at switching frequency of 250kHz.*

Repeat the process to change the operating conditions and enter the values of efficiency for all combinations of input voltage and output current as mentioned in **Table 1**.

Record the values of **Duty Cycle**, **I_{IN} Avg** and **L I_{pp}** from the Operating Values table as shown in **figure 4**. Use these values in the formula in given in the **Theory Background** section of **TI-PMLK** book.

Duty Cycle	43.89%	Duty cycle
Efficiency	88.1%	Steady state efficiency
Frequency	247.63 kHz	Switching frequency
IC Tj	31.36 °C	IC junction temperature
ICThetaJA	62.5 °C/W	IC junction-to-ambient thermal resistance
L Ipp	263.98 mA	Peak-to-peak inductor ripple current
L Pd	880 µW	Inductor power dissipation
IC Pd	21.74 mW	IC power dissipation
Diode Pd	21.95 mW	Diode power dissipation
D1 Tj	30.55 °C	D1 junction temperature
Pout	330 mW	Total output power
Iin Avg	62.43 mA	Average input current
	0 A	Peak switch current in IC

Figure 4.

Test #2:

You will change the operating frequency from 250KHz to 500KHz and analyze variation in efficiency due to change in line voltage and load current at the switching frequency of 500kHz. Compare experimental efficiency with theoretically obtained efficiency.

Calculations

Calculate the theoretical efficiency of the converter by

$$\eta theo = P_{out}/(P_{out} + P_{loss}) \text{ x } 100$$

$$\text{where } P_{out} = V_{out} {}^{*} I_{out}$$

$$P_{loss} = P_{MOS,c} + P_{MOS,sw} + P_{MOS,g} + P_{diode} + PL{,}w + P_{L,c} + P_{Cin} + P_{Cout} + P_{IC}$$

using the **Loss Formulas** given in the **Theory Background** section of **TI-PMLK** book.

Click on the link to open the V_{OUT} = 3.3V, F_{sw} = 500KHz, TPS54160 design in WEBENCH® Power Designer.

Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment.

Follow the instructions as in **Test 1** to note down the values for efficiency for various V_{IN}, I_{OUT} conditions as shown in **Table 2** below.

Measurements at 500KHz	Experimental / Theoretical efficiency (%)	0.1A	0.2A	0.5A	1A	1.2A	1.5A
V_{IN}= 6V	Exp. Eff.						
	The. Eff.						
V_{IN} = 24V	Exp. Eff.						
	The. Eff.						

Table 2. Experimental vs theoretical efficiency of TPS54160 operating at switching frequency of 500kHz.

Record the values of **Duty Cycle**, I_{IN} Avg and L I_{pp} from the **Operating Values** table as well. Use these values in the formula in given in the **Theory Background** section of **TI-PMLK** book.

TI-PMLK Buck Experiment 2

Impact of passive devices and switching frequency on current and voltage ripple

Using TI WEBENCH® Power Designer

Buck (TPS54160)

TI-PMLK Buck Experiment 2

Pre-Work

Before starting with this exercise, please refer to [TI-PMLK LDO experiment book], review the sections on **Case Study** and **Theory Background**. Refer the [TI-PMLK Buck board] to configure design in **WEBENCH**. Login or register for your [my.ti.com] account to access **WEBENCH**.

Goal

The goal of this experiment is to analyze the influence of switching frequency and the capacitance and series resistance of the input and output capacitors on the output ripple voltage and input ripple current of the buck regulator. **WEBENCH® Power Designer Tool** will be used to provide analysis and simulation results to compare with your **TI-PMLK** lab experiments.

Test #1:

Measure the output voltage and input current ripples of the TPS54160 buck regulator, for different input voltage, switching frequency and load current.

Procedure

1. Click on the [link] to open the V_{OUT} = 3.3V TPS54160 design in [WEBENCH® Power Designer].
   Note: You may be required to login or register for your [my.ti.com] account to access **WEBENCH**.

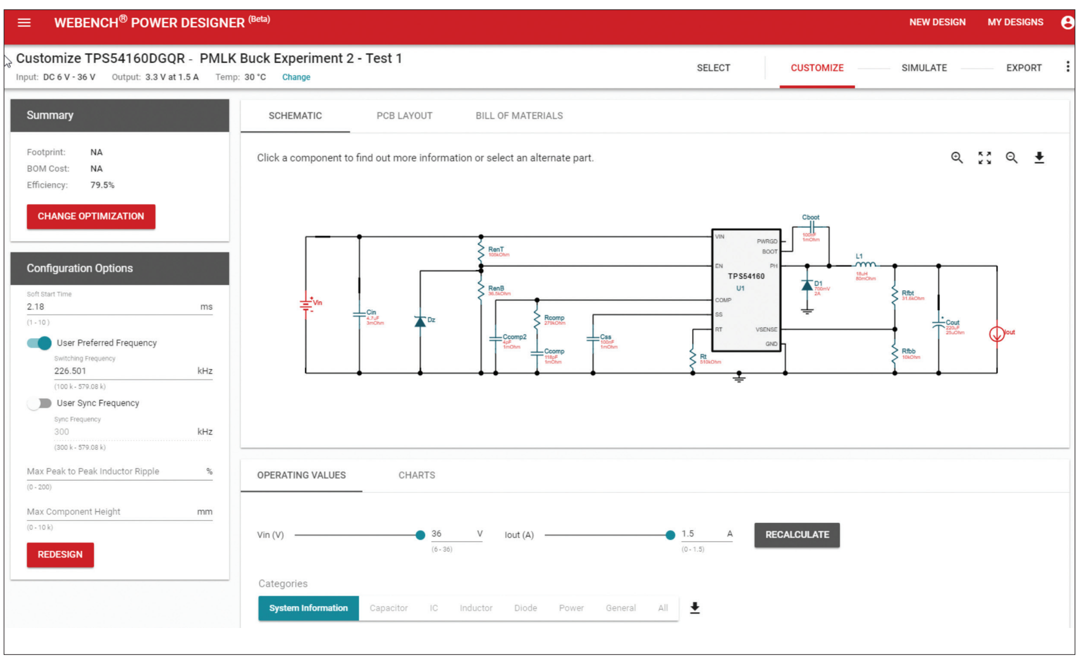


Figure 1.

2. In **WEBENCH**, scroll down to the **'Operating Values'** menu to view the operating values for your experiment measurements.

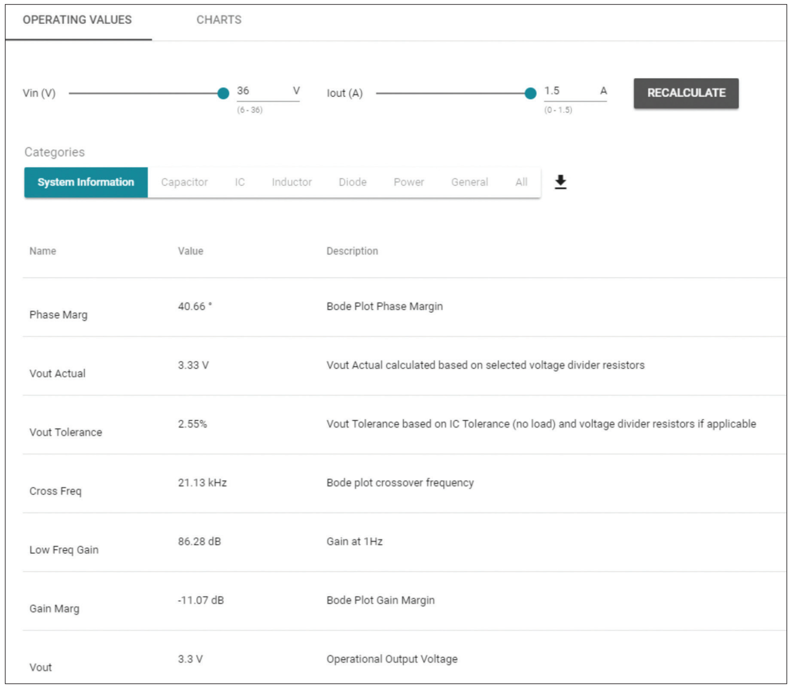


Figure 2.

3. In the **'Modify Operating Point'** window **Figure 3**, enter 6V for V_{IN} and 0.15 for I_{OUT} and **Recalculate**.

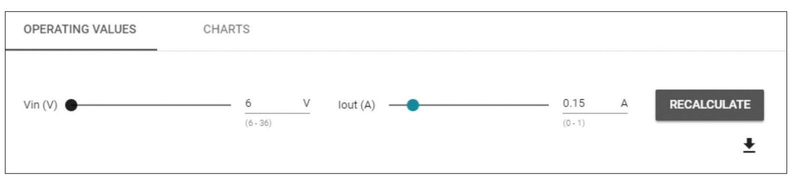


Figure 3.

4. Record the value of **Output Voltage** ripple, $V_{OUT\ p\text{-}p}$ from the **Operating Values** table in Op_Point category as shown in **Figure 4**.

Gain Marg	-11.07 dB	Bode Plot Gain Margin
Vout	3.3 V	Operational Output Voltage
Duty Cycle	10.54%	Duty cycle
Efficiency	79.5%	Steady state efficiency
Frequency	247.63 kHz	Switching frequency
Pout	4.95 W	Total output power
Mode	CCM	Conduction Mode
Vout p-p	1.77 mV	Peak-to-peak output ripple voltage
FootPrint	281 mm²	Total Foot Print Area of BOM components
Vin	36 V	Vin operating point
Iout	1.5 A	Iout operating point

Note: All above values are estimates. For more accurate values, please run electrical simulation.

Figure 4.

5. Click on the link to open the V_{OUT} = 3.3V, F_{sw} = 500KHz TPS54160 design in WEBENCH® Power Designer for 500kHz switching frequency.

6. Repeat **Steps 3-5** for the values provided in the **Table 1**, enter the values for all combinations of input voltage and output current.

ΔV_{OUTpp} (mV)	f_s = 250kHz						f_s = 500kHz					
ΔI_{INpp}	I_{OUT} = 0.15A		I_{OUT} = 0.5A		I_{OUT} = 1.5A		I_{OUT} = 0.15A		I_{OUT} = 0.5A		I_{OUT} = 1.5A	
V_{IN} = 6V												
V_{IN} = 18V												
V_{IN} = 36V												

Table 1. *Measured output voltage ripple of TPS54160 buck regulator vs load current, input voltage and switching frequency.*

Note: Input current ripple cannot be obtained from operating values. You can leave it blank for now.

Test #2:

Measure the output voltage and input current ripples of the TPS54160 buck regulator with a fixed switching frequency, but with different combinations of input and output capacitors.

Calculations

Calculate the output voltage ripple and input current ripple for

High ESR output filter capacitor: $\Delta V_{OUTpp} = ESR*\Delta I_{pp}$

Low ESR output filter capacitor: $\Delta V_{OUTpp} = \Delta I_{pp}/(8*fs*C_{OUT})$

High capacitance input filter capacitor: $\Delta I_{INpp} = I_{OUT} *D'*D/(fs*C_{IN})$

Low capacitance input filter capacitor: $\Delta I_{INpp} = I_{OUT} + \Delta I_{pp}/2$

using the **Formulae** for D,D' and ΔI_{pp} given in the **Theory Background** section of **TI-PMLK** book.

Procedure

1. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer for the case where C_{OUT} = 10μF, C_{IN} = 4.7μF.
   Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 5**.

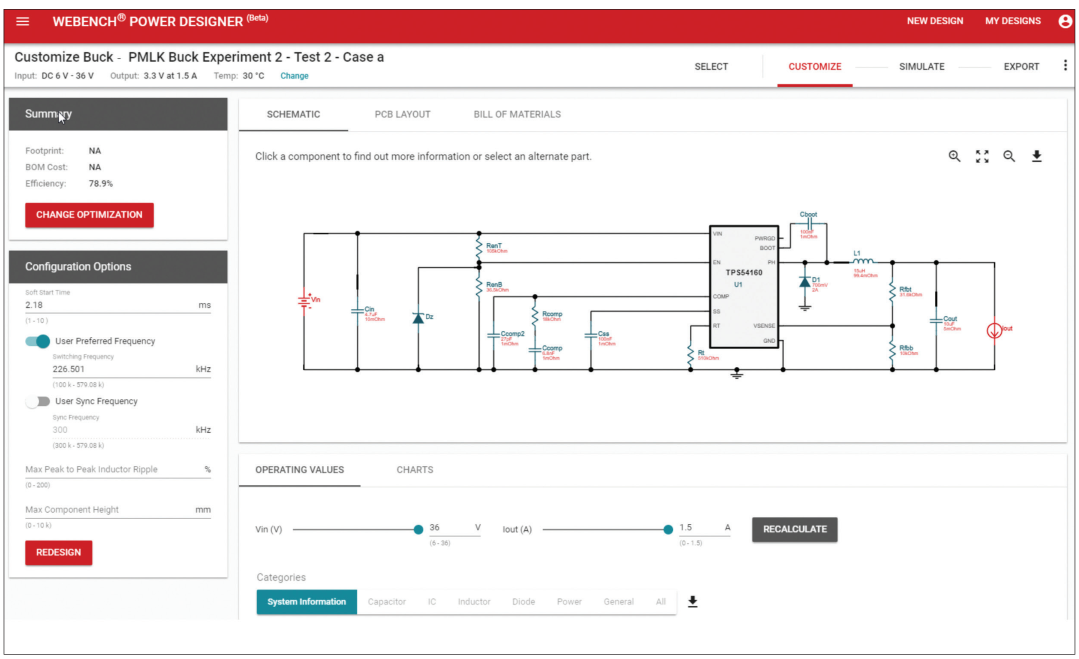


Figure 5.

2. In **WEBENCH**, scroll down to the **'Operating Values'** menu.

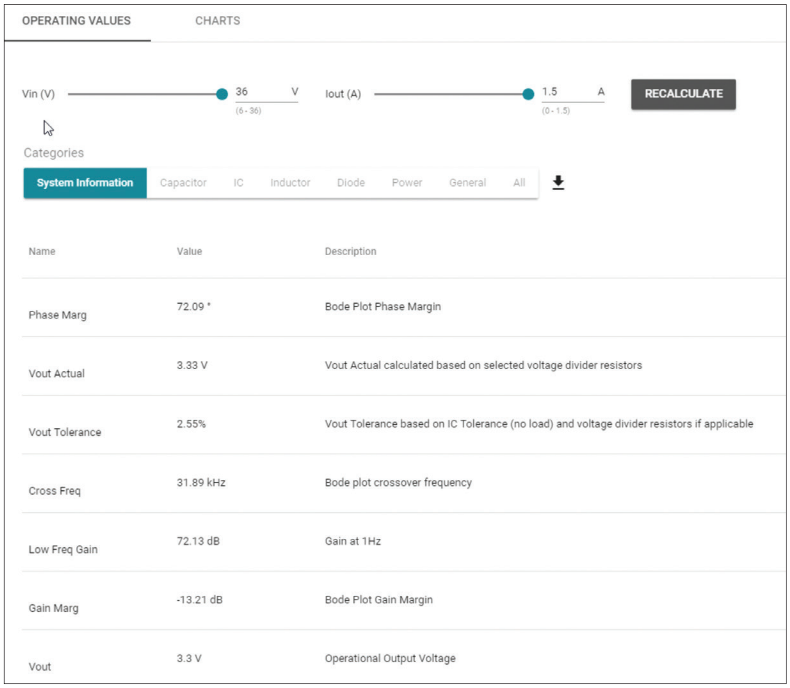


Figure 6.

3. In the **'Modify Operating Point'** window **Figure 6**, enter 6V for V_{IN} and 0.15 for I_{OUT} and **Recalculate,** shown in **Figure 7**.

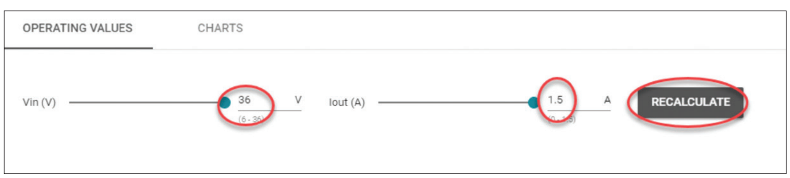


Figure 7.

4. Record the value of **Output Voltage** ripple, $V_{OUTp\text{-}p}$ from the **Operating Values** table as shown in **Figure 9**.

Gain Marg	-13.21 dB	Bode Plot Gain Margin
Vout	3.3 V	Operational Output Voltage
Duty Cycle	10.54%	Duty cycle
Efficiency	78.9%	Steady state efficiency
Frequency	247.63 kHz	Switching frequency
Pout	4.95 W	Total output power
Mode	CCM	Conduction Mode
Vout p-p	47.16 mV	Peak-to-peak output ripple voltage
FootPrint	303 mm²	Total Foot Print Area of BOM components

Figure 9.

5. Click on the [link]() to open the V_{OUT} = 3.3V TPS54160 design in [WEBENCH® Power Designer]() for case b with C_{OUT} = 220µF and C_{IN}=23.5µF.

6. Repeat **Steps 3-6** for the values provided in the **Table 2**, enter the values for all combinations of input voltage and output current.

ΔV_{OUTpp} exp (mV)	ΔI_{INpp} exp (mA)	case (a) C_{OUT} = C17=10µF, C_{IN} = C7 = 4.7µF						case (b) C_{OUT} = C16 = 220µF, C_{IN} = 23.5µF					
ΔV_{OUTpp} theo (mV)	**ΔI_{INpp} theo (mA)**	**0.15A**		**0.5A**		**1.5A**		**0.15A**		**0.5A**		**1.5A**	
V_{IN} = 6V													
V_{IN} = 18V													
V_{IN} = 36V													

Table 2. Measured and calculated output voltage ripple and input current ripple of TPS54160 buck regulator vs load current, input voltage and capacitance of input and output capacitors.

Calculations

For theoretical output voltage ripple and input current ripple calculation.

Record the values of **duty cycle**, from the **Operating Point** category as shown in **Figure 10** and also record the value of inductor current **L I_{pp}** from **Current** category. Use these values in the formula in given in the **Theory Background** section of **TI-PMLK** book calculate ripple voltage and ripple current.

Cin Pd	189.32 µW	Input capacitor power dissipation
Cout IRMS	267.92 mA	Output capacitor RMS ripple current
Cout Pd	1.79 mW	Output capacitor power dissipation
Duty Cycle	10.54%	Duty cycle
Efficiency	78.9%	Steady state efficiency
Frequency	247.63 kHz	Switching frequency
IC Tj	52.37 °C	IC junction temperature
ICThetaJA	62.5 °C/W	IC junction-to-ambient thermal resistance
L Ipp	928.11 mA	Peak-to-peak inductor ripple current
L Pd	246.02 mW	Inductor power dissipation
IC Pd	357.97 mW	IC power dissipation
Diode Pd	718.76 mW	Diode power dissipation

Figure 10.

TI-PMLK Buck Experiment 3

Impact of cross-over frequency and passive devices on load transient response

Using TI WEBENCH® Power Designer

Buck (TPS54160)

TI-PMLK Buck Experiment 3

Pre-Work

Before starting with this exercise, please refer to [TI-PMLK LDO experiment book](), review the sections on **Case Study** and **Theory Background**. Refer the [TI-PMLK Buck board]() to configure design in **WEBENCH**. Login or register for your [my.ti.com]() account to access **WEBENCH**.

Goal

The goal of this experiment is to analyze the influence of the feedback compensation on the load transient response of a current mode controlled buck regulator. **WEBENCH® Power Designer Tool** will be used to provide analysis and simulation results to compare with the **TI-PMLK** lab experiments.

Test #1:

Measure the magnitude ΔV_{OUT} of output voltage transient surges after the step-up and step-down load transients of TPS54160 buck regulator. This test shows the influence of the dynamic compensation on the magnitude of voltage transient surges.

Procedure

1. Click on the [link]() to open the V_{OUT} = 3.3V, 500KHz, 220µF, 25_{mohm}, 18µH with C_{comp2} = 4pF R_{comp} = 279kohm, C_{comp} = 118pF TPS54160 design in [WEBENCH® Power Designer]().
   Note: You may be required to login or register for your [my.ti.com]() account to access **WEBENCH**.

   Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 1**.

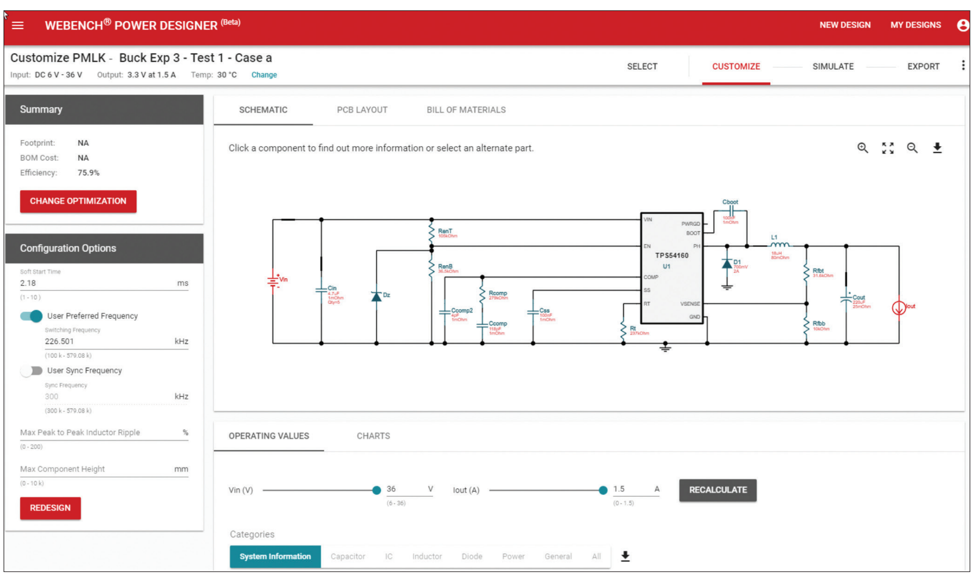


Figure 1.

2. Click on the **Simulate** icon in the top of the window to open **Electrical Simulation**.

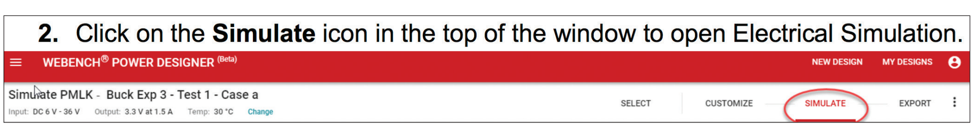


Figure 2.

3. In the **Simulations** box on the left side of the screen, select **Load Transient** as shown in **Figure 3**.

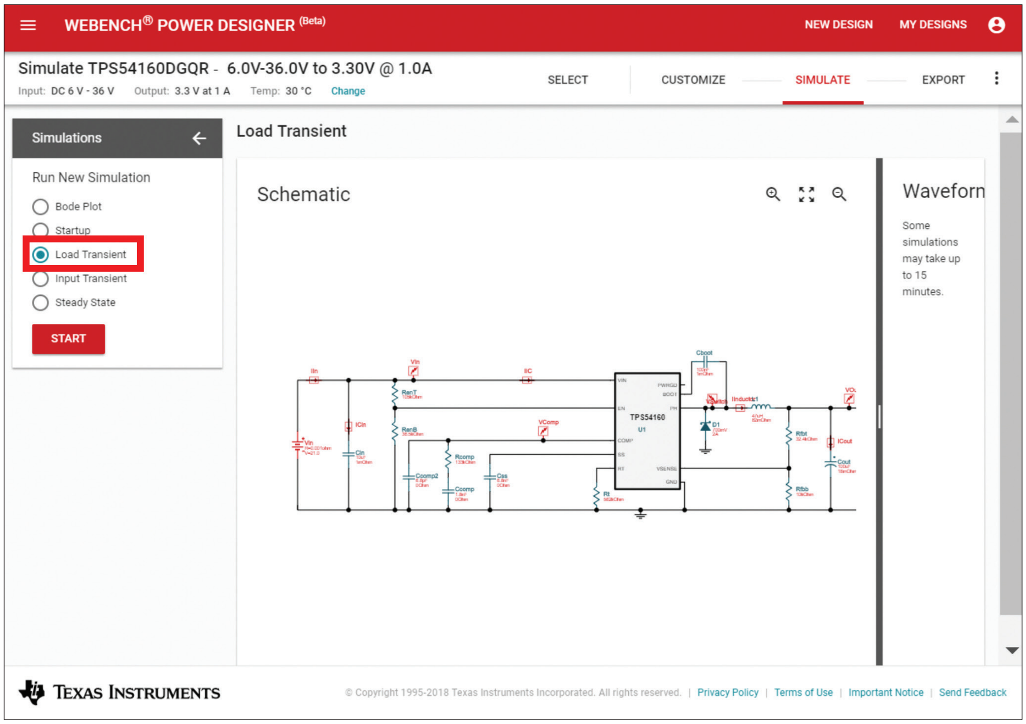


Figure 3.

4. Click the **input voltage source** (V_{IN}) on the schematic.

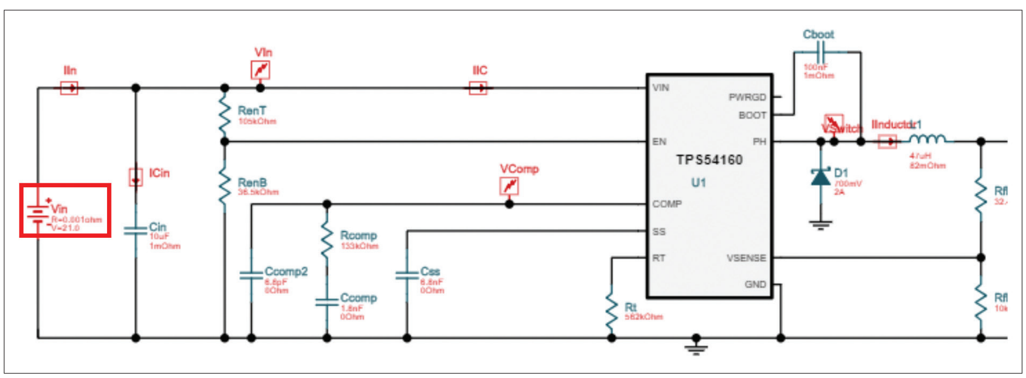


Figure 4.

5. In the window that appears, click **'Update'**

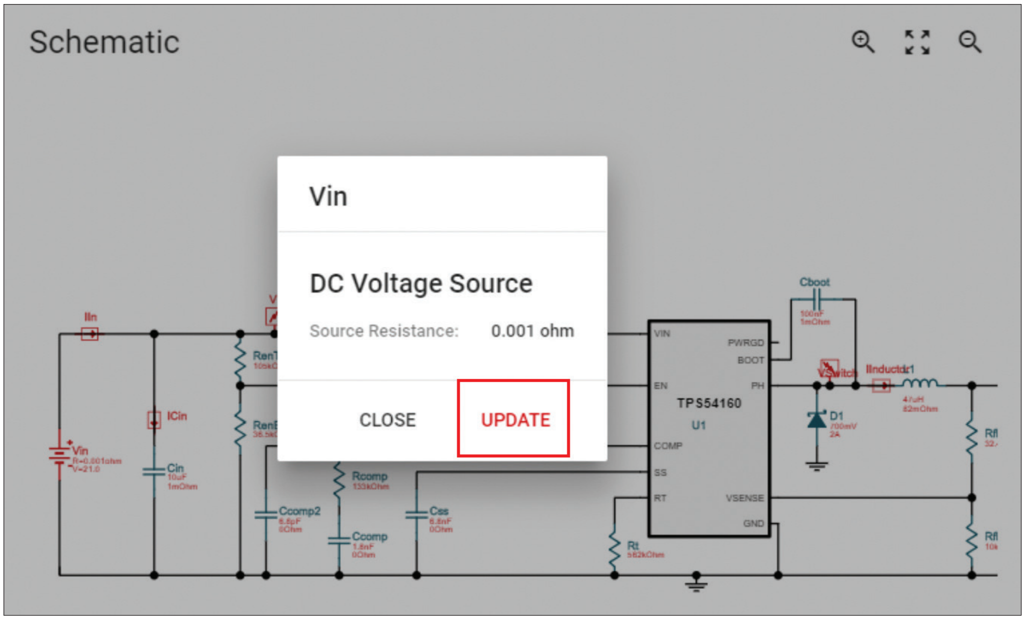


Figure 5.

6. In the next window, change the **Input Voltage** to 6V and click **'Save'**.

Figure 6.

7. Click $\mathbf{I_{OUT}}$, which indicates load current. Using the same process as with V_{IN}, get to the window that allows you to edit the parameters. Change the **Initial current (A)** value to 0.5A, the **Peak Current (A)** value to 1.5A, the **Initial Delay Time** to **0.003 Seconds**, and the **Pulse Width** to **0.005 Seconds**. Once complete, click **'Save'**.

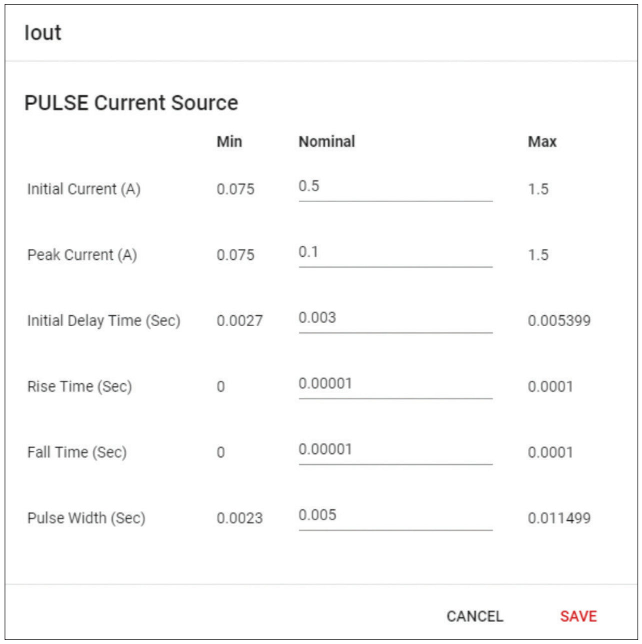


Figure 7.

8. Click **'Start'** in the **Simulations** menu.

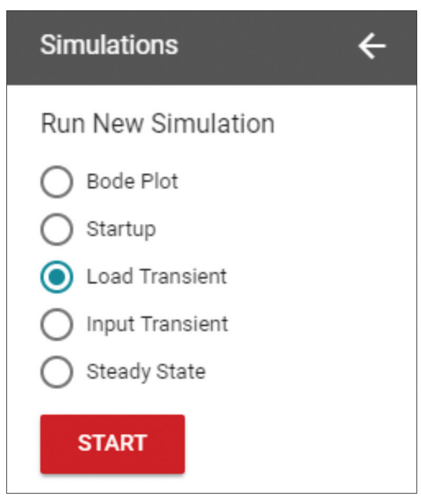


Figure 8.

9. After the end of simulation, V_{OUT} and I_{OUT} are plotted on the right side of the screen, as shown in **Figure 9**. (To enlarge this, click and drag the black bar separating the **'Schematic'** and the **'WAVEFORM'** to the left.) The performance summary pane which is below WAVEFORM shows maximum and minimum values of output voltage, V_{OUT} as shown in **Figure 10**. Calculate the difference between these two values and record it in **Table1**.

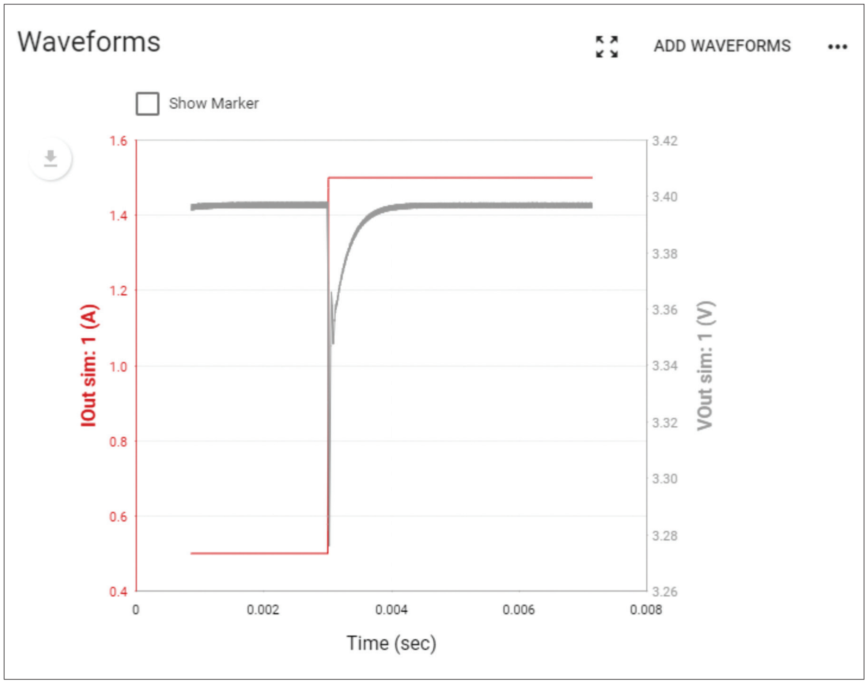


Figure 9.

Performance Summary

Sim ID	VOut Maximum	VOut Minimum	Overshoot Settle Time	Undershoot Settle Time	Overshoot	Undershoot
1	3.40 V	3.28 V				

Figure 10.

10. To change input voltage, follow **Steps 4-6**. To run step down load transient, swap the values of **Initial current** and **Peak current** in component simulation parameters window of I_{OUT} by following **step 7**.

11. Repeat **Steps 4-10** to complete the **Table 1** for different input voltages.
12. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in **WEBENCH Power Designer** for case b with another compensation setup.
13. Follow the **Steps 2-9** and complete case b part of **Table 1**.

<table>
<tr><th>ΔV_{OUT} [mV] 0.5A → 1.5A</th><th>ΔV_{OUT} [mV] 1.5A → 0.5A</th><th colspan="2">case (a): C_{f1} = 4pF, C_{f2} = 118pF, R_{f2} = 279kΩ</th><th colspan="2">case (b): C_{f1} = 27pF, C_{f2} = 6.8nF, R_{f2} = 18kΩ</th></tr>
<tr><td colspan="2" rowspan="2">V_{IN} = 6V</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="2" rowspan="2">V_{IN} = 18V</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="2" rowspan="2">V_{IN} = 36V</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
</table>

Table 1. *Load transient performances of TPS54160 buck regulator vs output capacitor and input voltage.*

Test #2:

Predict the combinations of output capacitor and compensation that correspond to minimum and maximum voltage loop cross-over frequency and measure the magnitude ΔV_{OUT} of output voltage transient surges after the step-up and step-down load transients.

Calculations:

Find the combinations of C_{OUT} and compensation that correspond to maximum and minimum cross-over frequency, plot the bode plot of transfer function

$$T(s) \cong \frac{T_o}{H_s} \frac{1+s/\omega_{zps}}{1+s/\omega_{pps}} \frac{\omega_{oea}}{s} \frac{1+s/\omega_{zea}}{1+s/\omega_{pea}}$$

using the list of **Formulae** given in the **Theory Background** section of **TI-PMLK** book.

Procedure

1. In **MATLAB**, plot the bode plot of the transfer function given in the **calculation section** for 8 different combination of compensation capacitors (Refer **Table 2** of **Experiment 3** in **TI-PMLK** book) and Identify the combinations which result in stable output and correspond to maximum and minimum crossover frequency. (Refer to the **Theory Background** section of **TI-PMLK** book to find the cross-over frequency). Identified capacitor combinations are used to develop schematic in **WEBENCH**.
2. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer which corresponds to highest cross-over frequency.
   Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 11**.

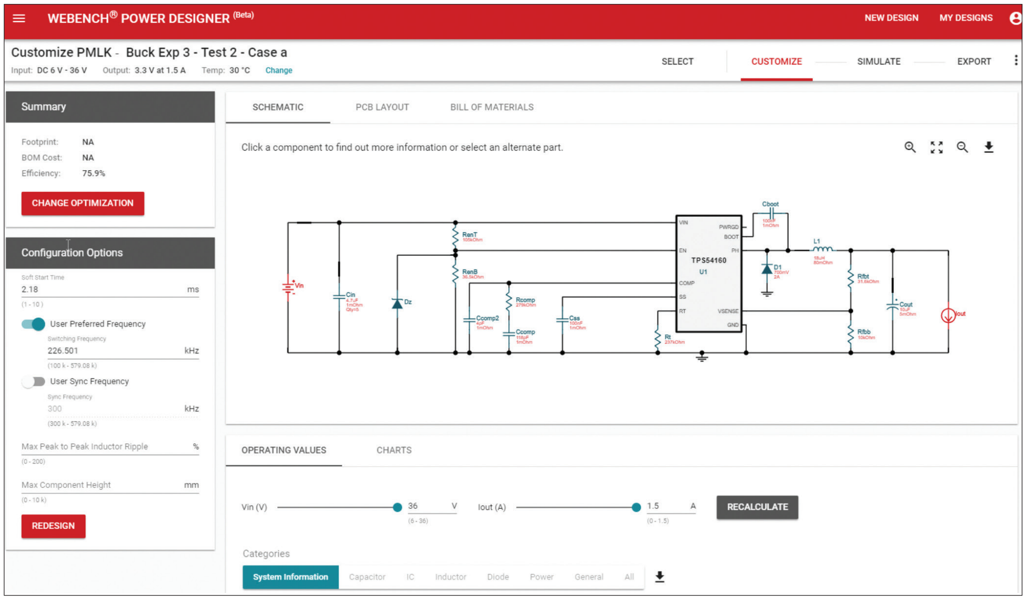


Figure 11.

3. Click on the **Simulate** icon in the top of the window to open **Electrical Simulation**.

Figure 12.

4. In the **Select Simulation** type, select **Load Transient** list of simulations as shown in **Figure 13**.

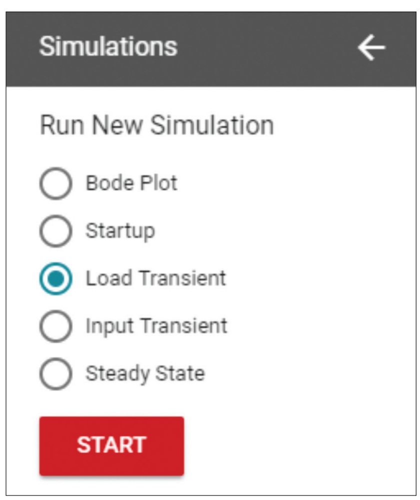


Figure 13.

5. Click the **'Input voltage'** source. Select **Input V_{IN}** on the schematic and change its nominal value to **12V** in the window. Click **'Save'**.

Figure 14.

6. Click **I_{OUT}**, which indicates load current. Using the same process as with V_{IN}, get to the window that allows you to edit the parameters. Change the **Initial current (A)** value to **0.5A**, the **Peak Current (A)** value to **1.5A**, the **Initial Delay Time** to **0.003 Seconds**, and the **Pulse Width** to **0.005 Seconds**. Once complete, click **'Save'**.

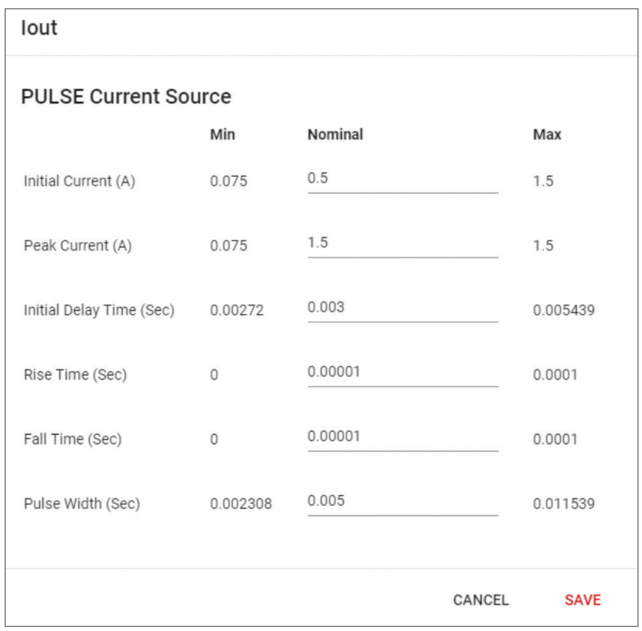


Figure 15.

7. Click **'Start'** in the **'Simulations'** menu.

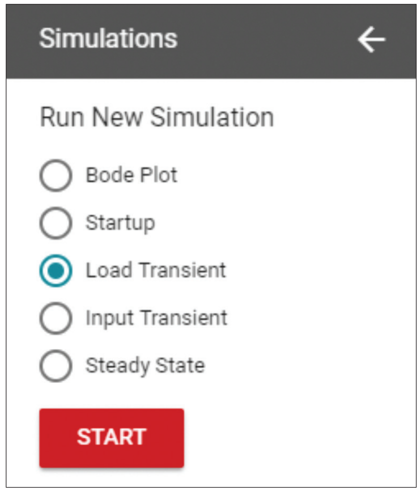


Figure 14.

8. After the end of simulation, V_{OUT} and I_{OUT} are plotted as shown in **Figure 17**. The performance summary pane which is below waveform shows maximum and minimum values of output voltage, V_{OUT} as shown in **Figure 18**. Calculate the difference between these two values and record it in **Table 2**.

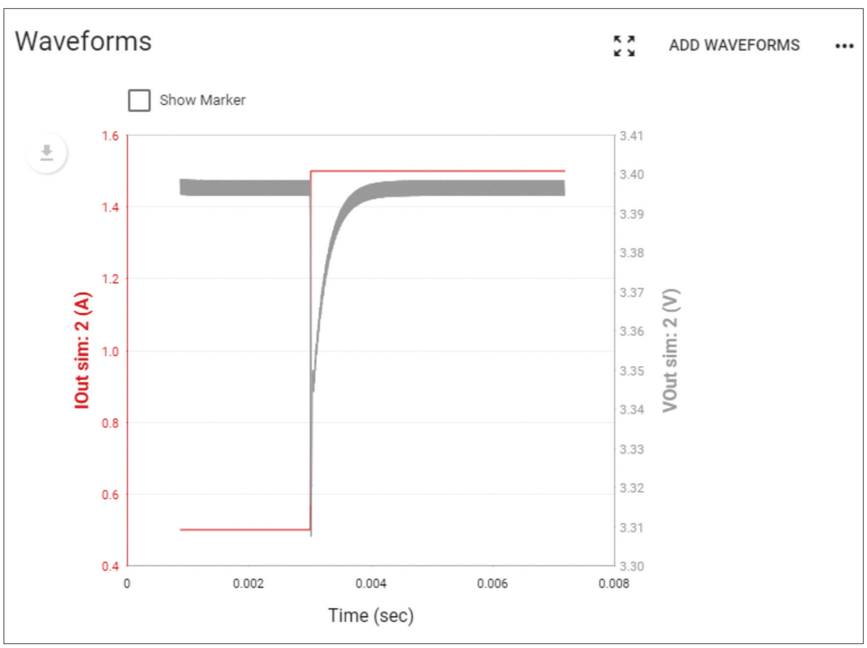


Figure 17.

Performance Summary

Sim ID	VOut Maximum	VOut Minimum	Overshoot Settle Time	Undershoot Settle Time	Overshoot	Undershoot
2	3.40 V	3.31 V				

Figure 18.

9. To change input voltage, follow **step 5**. To run step down load transient, swap the values of **Initial current** and **Peak current** in component simulation parameters window of I_{OUT} by following **step 6**.
10. Repeat **steps 4-8** to complete the **Table 2** for different input voltages.
11. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in **WEBENCH Power Designer** for lowest cross-over frequency.
12. Follow the **steps 2-9** and complete the lowest cross-over frequency part of **Table 2**.

<table>
<tr><th>ΔV_{OUT} [mV]
0.5A → 1.5A</th><th>ΔV_{OUT} [mV]
1.5A → 0.5A</th><th colspan="2">Highest cross-over frequency, ωch
C_{OUT} = 10μF; C_{f1} = 4pF,
C_{f2} = 118pF, R_{f2} = 279kΩ</th><th colspan="2">Lowest cross-over frequency, ωcl
C_{OUT} = 10μF; C_{f1} = 27pF,
C_{f2} = 6.8nF, R_{f2} = 18kΩ</th></tr>
<tr><td colspan="2" rowspan="2">V_{IN} = 12V</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="2" rowspan="2">V_{IN} = 24V</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td colspan="2" rowspan="2">V_{IN} = 36V</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
</table>

Table 2. *Load transient performances of TPS54160 buck regulator vs output capacitor and compensation.*

Calculations:

For predicting the combinations of C_{OUT} and compensation that correspond to maximum and minimum cross-over frequency, bode plot of the transfer function,

$$T(s) \cong \frac{T_o}{H_s} \frac{1+s/\omega_{zps}}{1+s/\omega_{pps}} \frac{\omega_{oea}}{s} \frac{1+s/\omega_{zea}}{1+s/\omega_{pea}}$$

was plotted in **MATLAB**.

TI-PMLK Buck Experiment 4

Impact of cross-over frequency and passive devices on load transient response

Using TI WEBENCH® Power Designer

Buck (TPS54160)

TI-PLMK Buck Experiment 4

Pre-Work

Before starting with this exercise, please refer to [TI-PMLK LDO experiment book](), review the sections on **Case Study** and **Theory Background**. Refer the [TI-PMLK Buck board]() to configure design in **WEBENCH**. Login or register for your [my.ti.com]() account to access **WEBENCH**.

Goal

The goal of this experiment is to analyze the influence of core material and core saturation of inductor on the current ripple and voltage ripple of a buck regulator. **WEBENCH® Power Designer Tool** will be used to provide analysis and simulation results to compare with the **TI-PMLK** lab experiments.

Test #1:

Measure the inductor current ripple and the output voltage ripple determined by the two optional inductors available in the TPS54160 buck regulator, for different input voltage and load current conditions. This test shows the influence of the dynamic compensation on the magnitude of voltage transient surges.

Procedure

1. Click on the link to open the V_{OUT} = 3.3V, 18µH inductor TPS54160 design in WEBENCH® Power Designer.
   Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 1**.

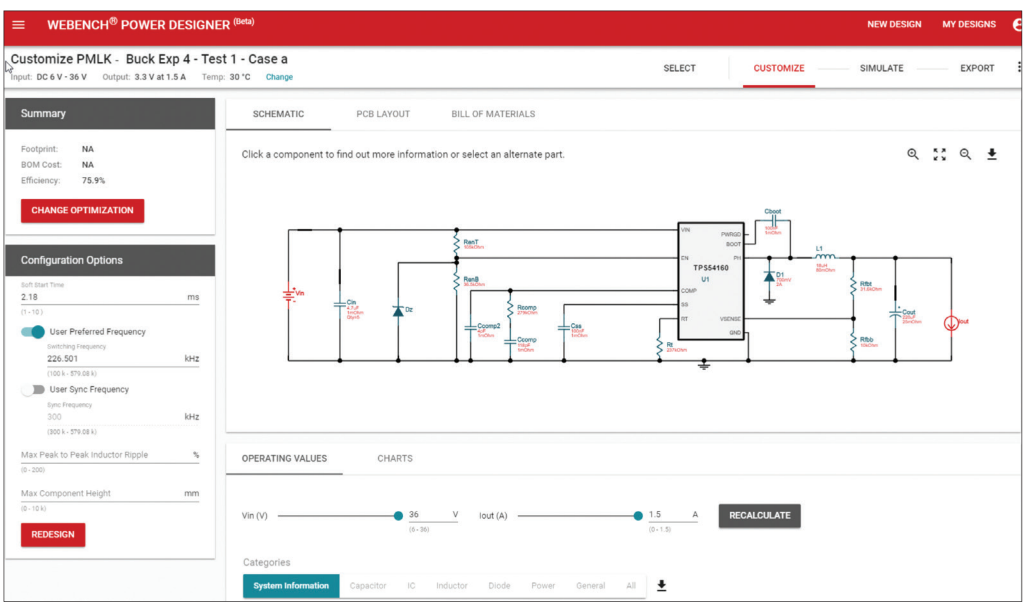


Figure 1.

2. As we wanted to change the inductance (to see the effect of saturation), let us use the following **Table** to set the inductance values based on the peak current.

I_{OUT} (A)	Inductance for 18μH inductor (μH) Use DCR of 65mohm	Inductance for 15μH inductorL3 (μH) Use DCR of 109mohm
0.15	16.7	13.7
0.75	16.1	13.25
1.5	14	12.2

To start with 0.15A current and to change the inductance value to 16.7μH, go to the schematic and click on the inductor symbol. This should open up the component properties window for the inductor. Click on the **'Choose Alternate'** in this window.

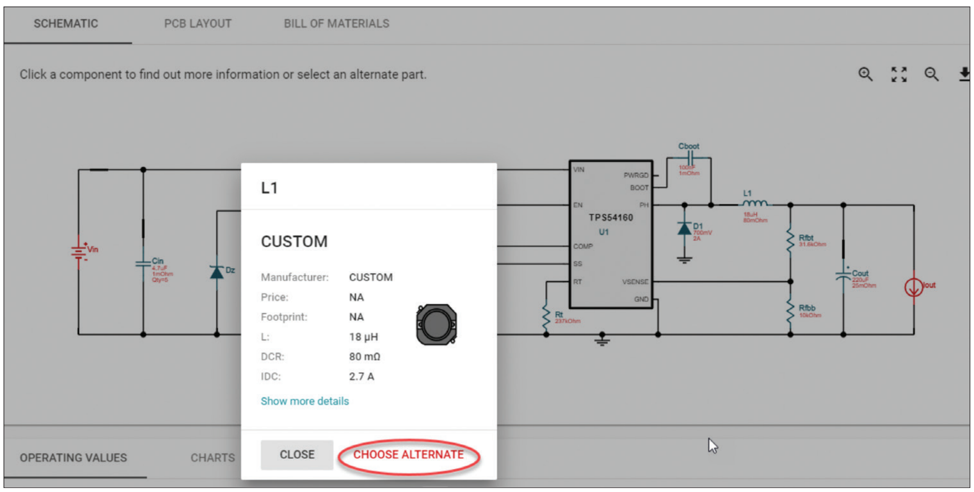


Figure 2.

In the **alternate part** selection window, click on **'Create a custom part'**.

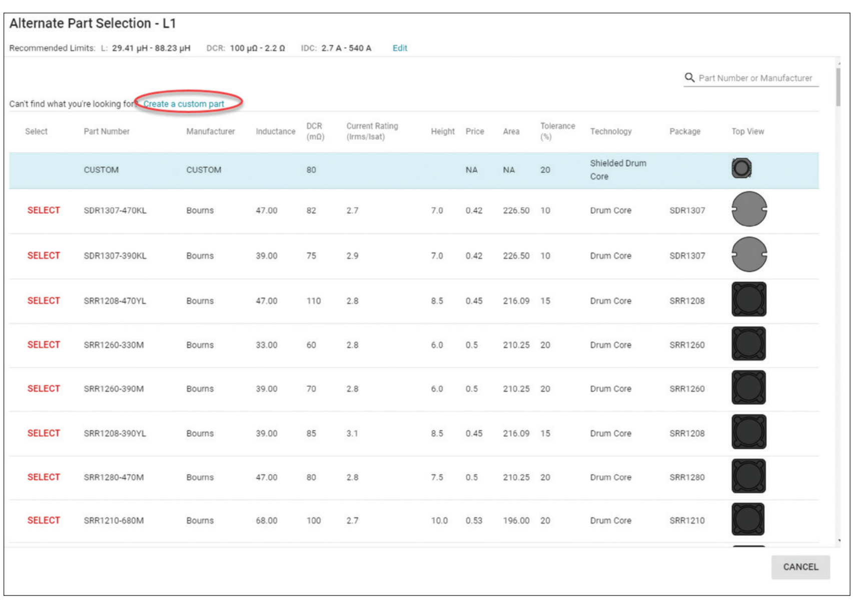


Figure 3.

Change the value of L to 16.1µH and DCR to 0.065 as shown in **Figure 9** and select **'Save'**.

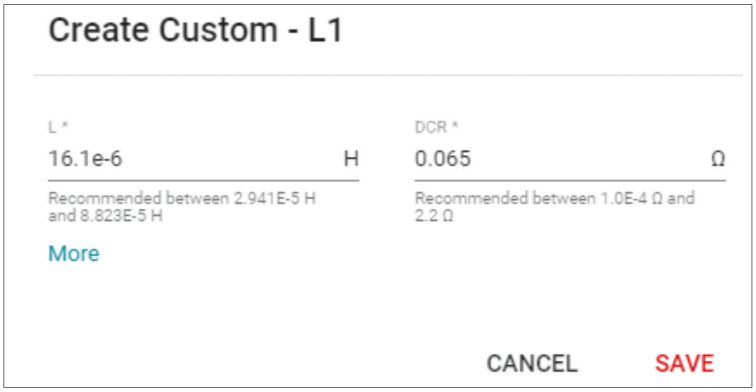


Figure 4.

In **WEBENCH**, scroll down to the **Operating Values** menu at the bottom of the window to view the operating values for your experiment measurements.

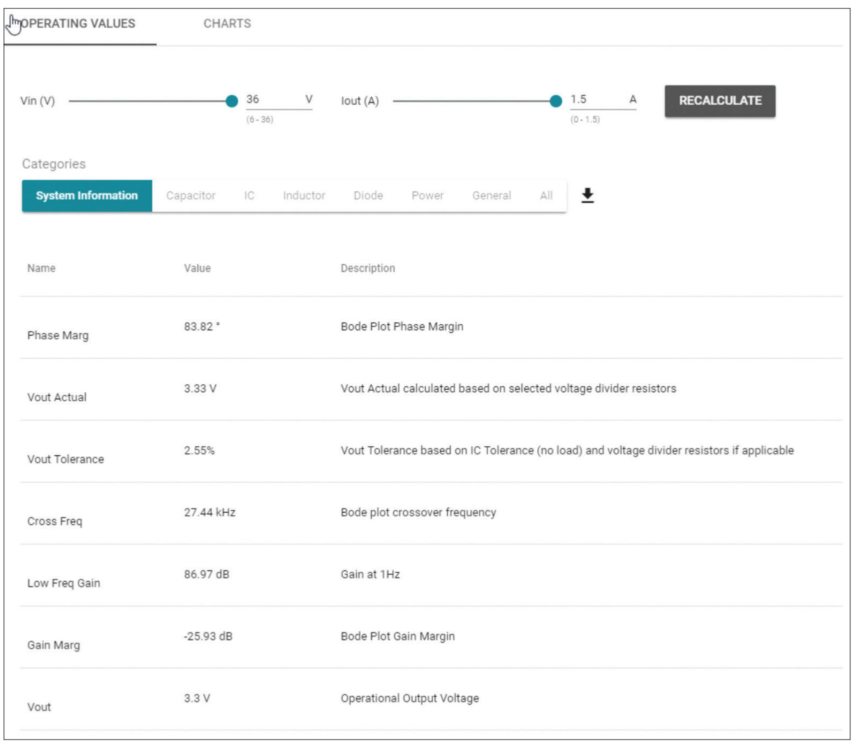


Figure 5.

3. In this menu, enter **12V** for V_{IN} and **0.15** for I_{OUT} and **Recalculate**.

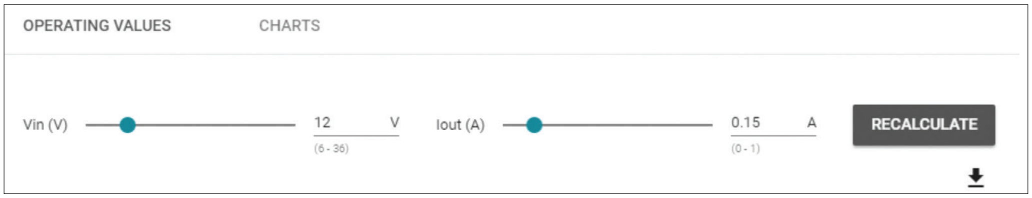


Figure 6.

4. Record the value of **Output Voltage** ripple, $\mathbf{V_{OUTp\text{-}p}}$ from the **Operating Values** table in **Op_Point** category as shown in **Figure 4**.

Vout Tolerance	2.55%	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
Cross Freq	27.44 kHz	Bode plot crossover frequency
Low Freq Gain	86.97 dB	Gain at 1Hz
Gain Marg	-25.93 dB	Bode Plot Gain Margin
Vout	3.3 V	Operational Output Voltage
Duty Cycle	10.55%	Duty cycle
Efficiency	75.9%	Steady state efficiency
Frequency	500.58 kHz	Switching frequency
Pout	4.95 W	Total output power
Mode	CCM	Conduction Mode
Vout p-p	9.57 mV	Peak-to-peak output ripple voltage
FootPrint	321 mm²	Total Foot Print Area of BOM components

Figure 7.

5. Record the value of **Inductor current** ripple, **L I_{pp}** from the **Operating Values** table in **Current** category as shown in **Figure 5**.

Duty Cycle	10.55%	Duty cycle
Efficiency	75.9%	Steady state efficiency
Frequency	500.58 kHz	Switching frequency
IC Tj	70.79 °C	IC junction temperature
ICThetaJA	62.5 °C/W	IC junction-to-ambient thermal resistance
L Ipp	382.72 mA	Peak-to-peak inductor ripple current
L Pd	198 mW	Inductor power dissipation
IC Pd	652.59 mW	IC power dissipation
Diode Pd	718.74 mW	Diode power dissipation
D1 Tj	47.97 °C	D1 junction temperature
Pout	4.95 W	Total output power

Figure 8.

6. Repeat the **Steps 2-5** for remaining values of V_{IN} at various I_{OUTs} given in the table. At each of the I_{OUTs}, remember to change the inductance value and the DCR and note the value of V_{OUT} ripple, L I_{pp} in the **Operating Values** section.

I_{OUT} (A)	Inductance for 18μH inductor (μH) Use DCR of 65mohm	Inductance for 15μH inductorL3 (μH) Use DCR of 109mohm
0.15	16.7	13.7
0.75	16.1	13.25
1.5	14	12.2

Table 2. *Inductance Value vs Current .*

7. Repeat **steps 2-6** and complete the **Table 3**. Click on the link to open the V_{OUT} = 3.3V, 18µH inductor TPS54160 design in WEBENCH® Power Designer.

ΔV_{OUTpp} (mV) / ΔI_{pp} (mA)	$L = L_2$ = 18µH (use effective inductance and DCR in Table 2)						$L = L_3$ = 15µH (use effective inductance and DCR in Table 2)					
	I_{OUT}						I_{OUT}					
	0.15A		0.75A		1.5A		0.15A		0.75A		1.5A	
V_{IN} = 12V												
V_{IN} = 18V												
V_{IN} = 24V												

Table 3. *Output voltage ripple and inductor current ripple of TPS54160 buck regulator vs load current and input voltage.*

Test #2:

Use the experimental measurements of ΔI_{pp}, V_{IN}, V_{OUT} and fs to estimate the value of the inductance of two inductors, for different values of input voltage, load current and switching frequency.

Calculations:

To estimate the equivalent inductance, use the formula

$$L_d = (V_{IN}-V_{OUT})*V_{OUT}/(V_{IN}*f_s*\Delta I_{pp})$$

Procedure

1. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer.

Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 9**.

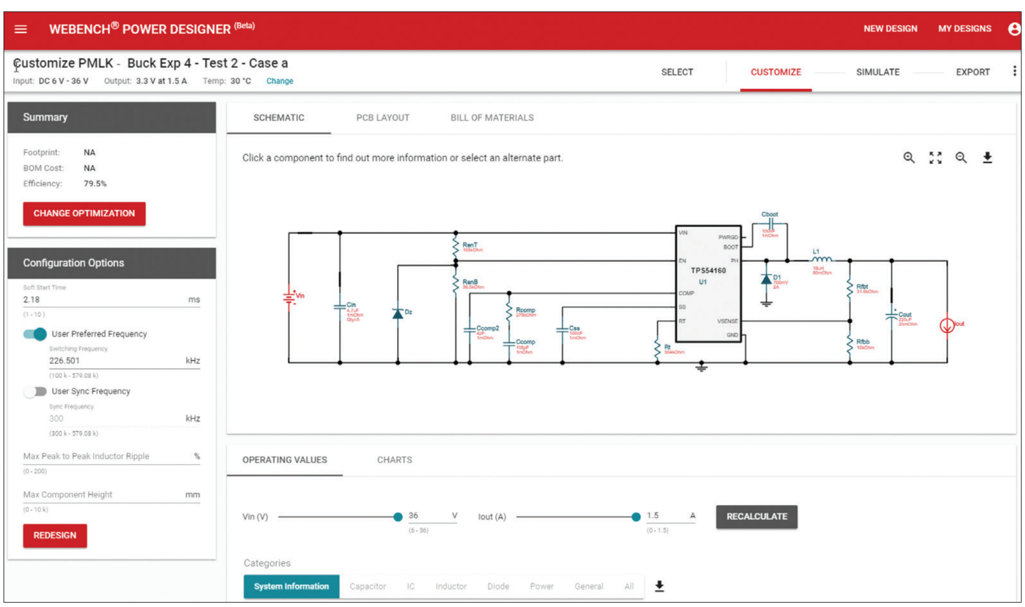


Figure 9.

2. As we wanted to change the inductance (to see the effect of saturation), let us use the following **Table** to set the inductance values based on the peak current.

I_{OUT} (A)	Inductance for 18µH inductor (µH) Use DCR of 65mohm	Inductance for 15µH inductorL3 (µH) Use DCR of 109mohm
0.15	16.7	13.7
0.75	16.1	13.25
1.5	14	12.2

To start with 0.15A current and to change the inductance value to 16.7µH, go to the schematic and click on the inductor symbol. This should open up the component properties window for the inductor. Click on the **'Choose Alternate'** in this window.

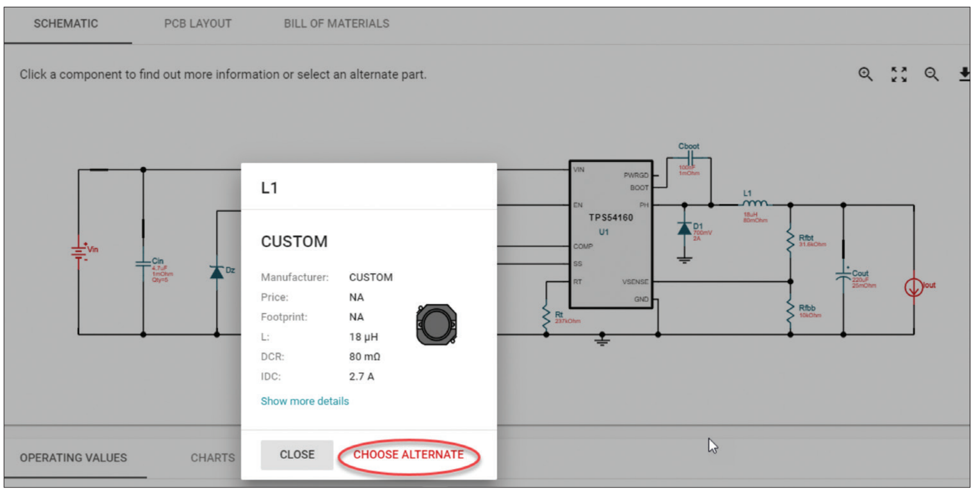


Figure 2.

In the alternate part selection window, click on **'Create a custom part'**.

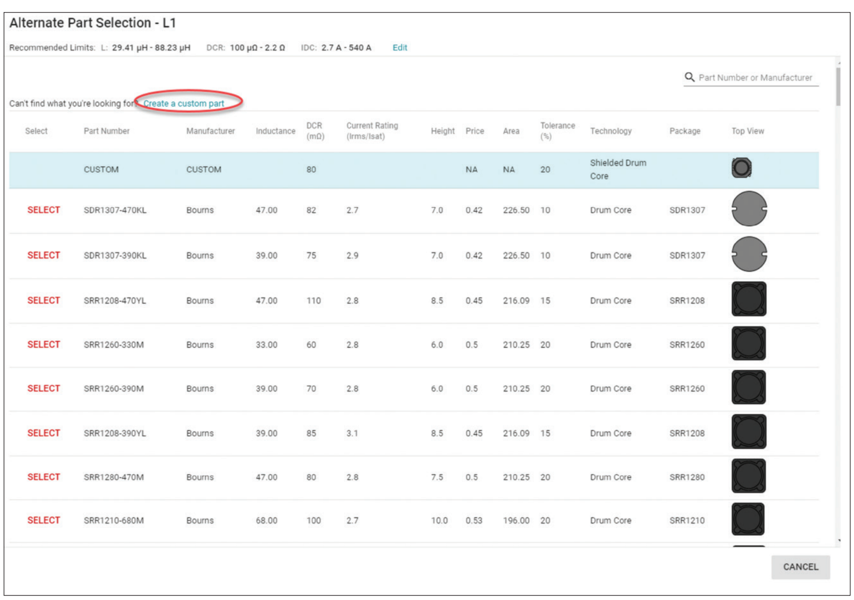


Figure 3.

Change the value of L to 16.1µH and DCR to 0.065 as shown in **Figure 9** and select **'Save'**.

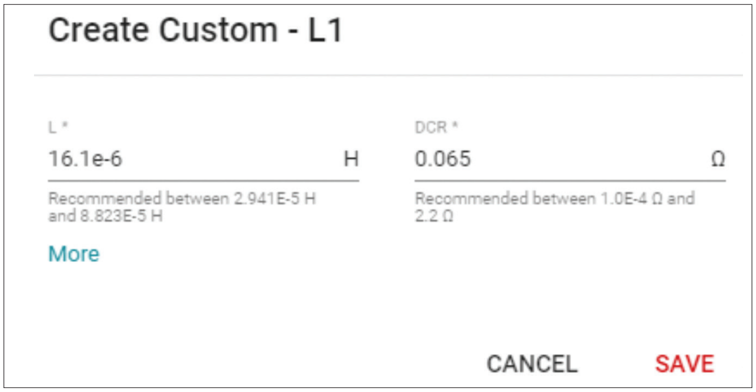


Figure 4.

In **WEBENCH**, scroll down to the **Operating Values** menu at the bottom of the window to view the operating values for your experiment measurements.

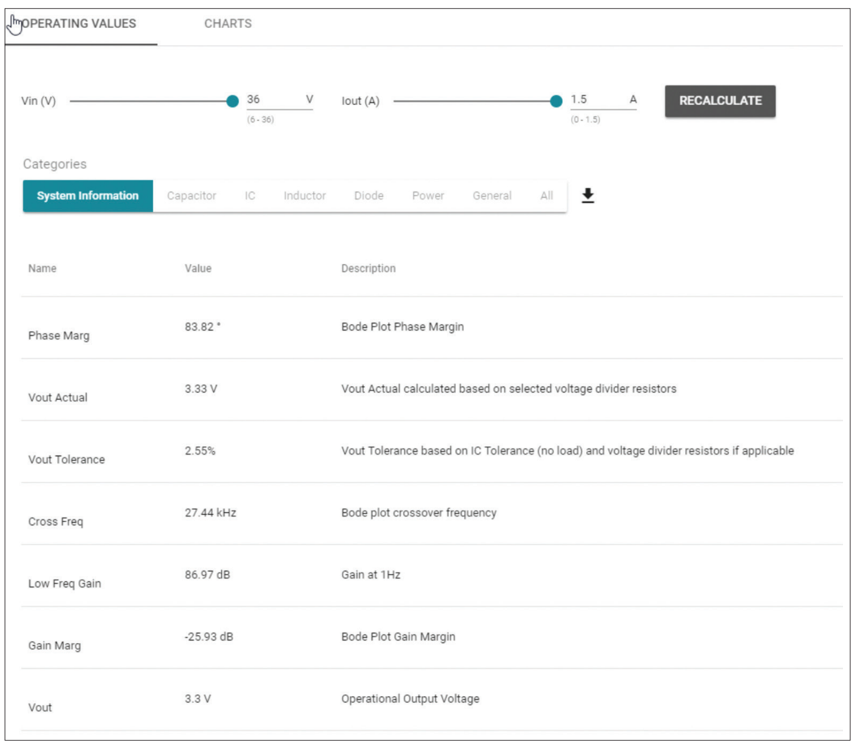


Figure 5.

3. In this menu, enter 6V for V_{IN} and 0.15 for I_{OUT} and **Recalculate**.

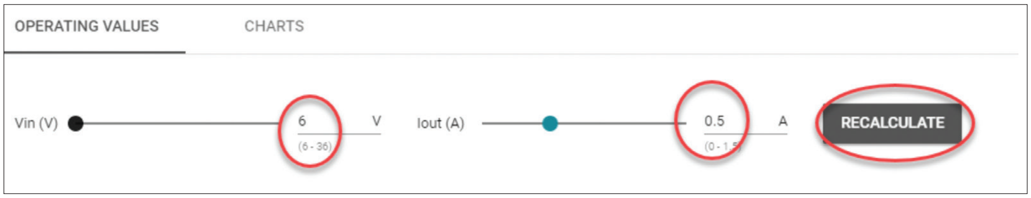
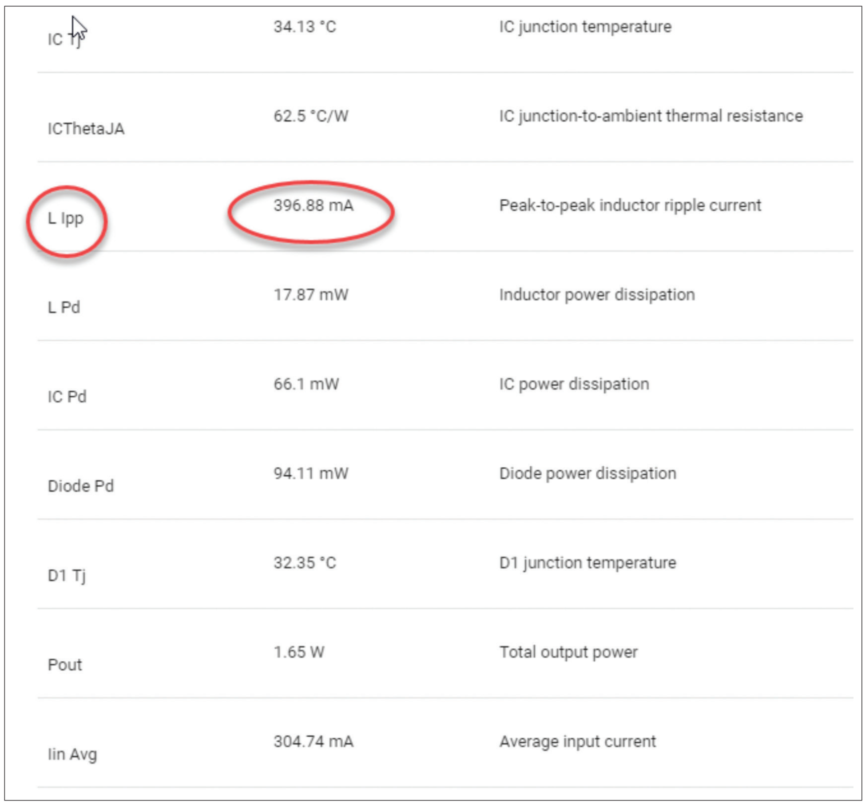


Figure 6a.

4. Record the value of Inductor current ripple, **L I_{pp}** from the **Operating Values** table in **Current** category as shown in **Figure 7a**.



IC Tj	34.13 °C	IC junction temperature
ICThetaJA	62.5 °C/W	IC junction-to-ambient thermal resistance
L Ipp	396.88 mA	Peak-to-peak inductor ripple current
L Pd	17.87 mW	Inductor power dissipation
IC Pd	66.1 mW	IC power dissipation
Diode Pd	94.11 mW	Diode power dissipation
D1 Tj	32.35 °C	D1 junction temperature
Pout	1.65 W	Total output power
Iin Avg	304.74 mA	Average input current

Figure 7a.

5. Repeat the **Steps 2-5** for remaining values of V_{IN} at various I_{OUTs} given in the **Table**. At each of the I_{OUTs}, remember to change the inductance value and the DCR and note the value of V_{OUT} ripple, L I_{pp} in the **Operating Values** section.

I_{OUT} (A)	Inductance for 18µH inductor (µH) Use DCR of 65mohm	Inductance for 15µH inductor L_3 (µH) Use DCR of 109mohm
0.15	16.7	13.7
0.75	16.1	13.25
1.5	14	12.2

Table 2. *Inductance Value vs Current .*

6. Repeat **Steps 2-6** and complete the **Table 3**. Click on the link to open the V_{OUT} = 3.3V, 15µH inductor TPS54160 design in [WEBENCH® Power Designer]().

7. Leave the table data corresponding to I_{OUT} = 2A since current limit of TPS54160 is 1.5A.

ΔI_{pp} (A)	L [µH] estimated	L = L_2 = 18µH						L = L_3 = 15µH					
		I_{OUT}						I_{OUT}					
		1A		1.5A		2.0A		1A		1.5A		2.0A	
V_{IN} = 6V						NA	NA					NA	NA
V_{IN} = 36V						NA	NA					NA	NA

Table 4. Output voltage ripple and inductor current ripple of TPS54160 buck regulator vs load current and input voltage.

8. Click on the link to open the V_{OUT} = 3.3V, 18µH TPS54160 design for f_s = 500kHz in [WEBENCH® Power Designer]().

9. Click on the link to open the V_{OUT} = 3.3V, 15µH TPS54160 design for f_s = 500kHz in [WEBENCH® Power Designer]().

10. Follow the **Steps 2-7** and complete the **Table 5**.

ΔI_{pp} (A)	L [µH] estimated	L = L_2 = 18µH						L = L_3 = 15µH					
		I_{OUT}						I_{OUT}					
		1A		1.5A		2.0A		1A		1.5A		2.0A	
V_{IN} = 6V						NA	NA					NA	NA
V_{IN} = 36V						NA	NA					NA	NA

Table 5. Inductor current ripple and estimated inductance of TPS54160 buck regulator operating at **f_s=500 kHz**.

Note: In **Tables 4** and **5**, data corresponds to I_{OUT} = 2A are not filled since it cannot be simulated in **WEBENCH** due to the current limit of TPS54160.

TI-PMLK Buck Experiment 5

Impact of inductor characteristics on current and voltage ripple

Using TI [WEBENCH® Power Designer]

Buck (TPS54160)

TI-PLMK Buck Experiment 5

Pre-Work

Before starting with this exercise, please refer to TI-PMLK LDO experiment book, review the sections on **Case Study** and **Theory Background**. Refer the TI-PMLK Buck board to configure design in **WEBENCH**. Login or register for your my.ti.com account to access **WEBENCH**.

Goal

The goal of this experiment is to analyze how the inductor influences the current limit of buck regulator, depending on the effect of magnetic core saturation. **WEBENCH® Power Designer Tool** will be used to provide analysis and simulation results to compare with the **TI-PMLK** lab experiments.

Test #1:

Measure the maximum current the regulator is able to deliver to the load, by increasing the load current up to the point where the current limit shuts down the regulator. The test is executed with different input voltage and with the two optional inductors of the TPS54160 buck regulator.

Procedure

1. Click on the link to open the V_{OUT} = 3.3V design in WEBENCH® Power Designer.
   Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

   Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 1**.

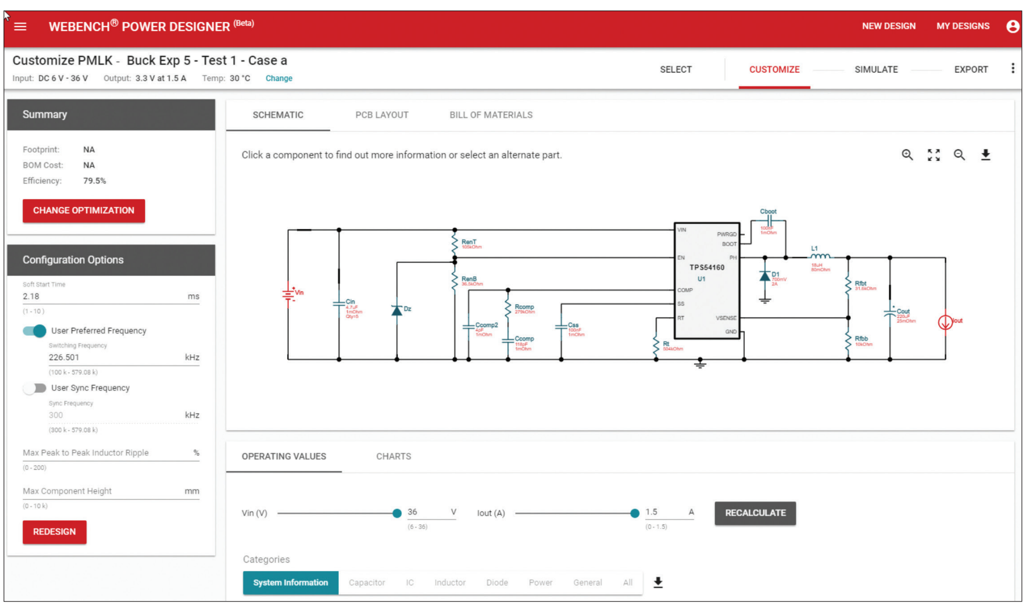


Figure 1.

2. Click on the **'Simulate'** icon in the top of the window to open **Electrical Simulation**.

Figure 2.

3. In the **'Simulations'** menu, select **Steady State** from the list of simulations as shown in **Figure 3**.

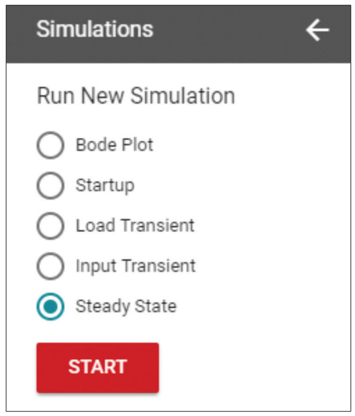


Figure 3.

4. Click the **'input voltage'** source. Select **Input Voltage** and change its nominal value to **12V** in **Component Simulation Parameters** window. Click **'Save'**.

Figure 4.

5. Click $\mathbf{I_{OUT}}$, which indicates load current, and change its **Nominal** value to **1A**. Click **'Save'**.

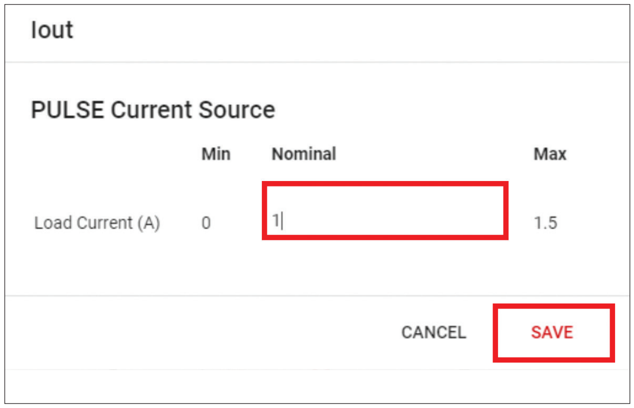


Figure 5.

6. Click **'Start'**.

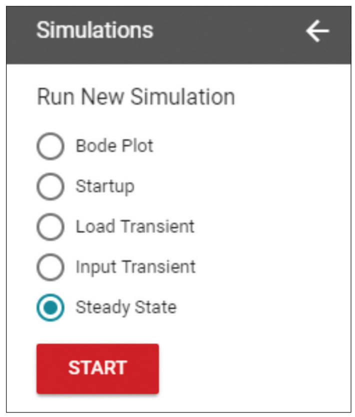


Figure 6.

7. After the end of simulation, Click on **'Add Waveforms'** and check $\mathbf{V_{Comp}}$ to plot the control voltage. The plot appears as shown in **Figure 7**.

8. Check the **Marker** to enable it and find the minimum and maximum voltages by moving cursor along the WAVEFORM as shown in **Figure 8**. Calculate the average of these two values and enter it in **Table 1**.

9. Repeat **Steps 4-8** to complete the **Table 1** for different input voltages. I_{OUTmax} is fixed as 1.5A due to the current limit of TPS54160. Repeat **Steps 4-8** to find Vc @ I_{OUTmax}.

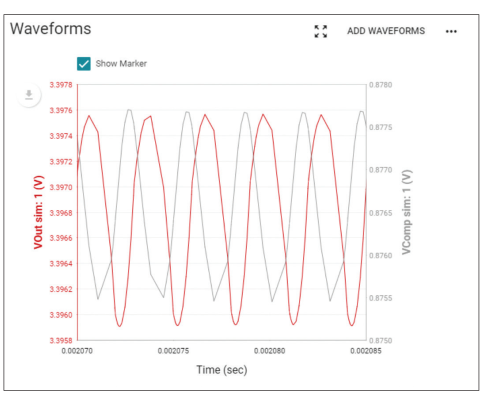


Figure 7.

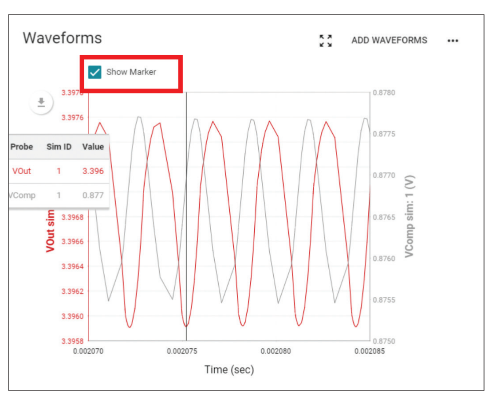


Figure 8.

10. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer for L = L_3 = 15µH.

11. Follow the **Steps 2-9** and complete L_3 part of **Table 1**.

V_{IN}	L = L_2 = 18µH			L = L_3 = 15µH		
	V_c @ 1A	I_{OUTmax} (A)	V_c @ I_{OUTmax} (V)	V_c @ 1A	I_{OUTmax} (A)	V_c @ I_{OUTmax} (V)
12V						
18V						
36V						

Table 1. *Control voltage and maximum output current of TPS54160 buck regulator operating with ferrite and powder inductor, vs input voltage.*

Test #2:

Measure the maximum current the regulator is able to deliver to the load, by increasing the load current up to the point where the current limit shuts down the regulator with different output capacitor and switching frequency, to observe if and how the ripple on the control voltage V can influence the current limit action.

Procedure

1. Click on the link to open the V_{OUT} = 3.3V, C_{OUT} = 220µF, F_{sw} = 250KHz TPS54160 design in WEBENCH® Power Designer.

Note: You may be required to login or register for your my.ti.com account to access **WEBENCH**.

Your design will be ready within **WEBENCH Power Designer** configured for this experiment, see **Figure 9**.

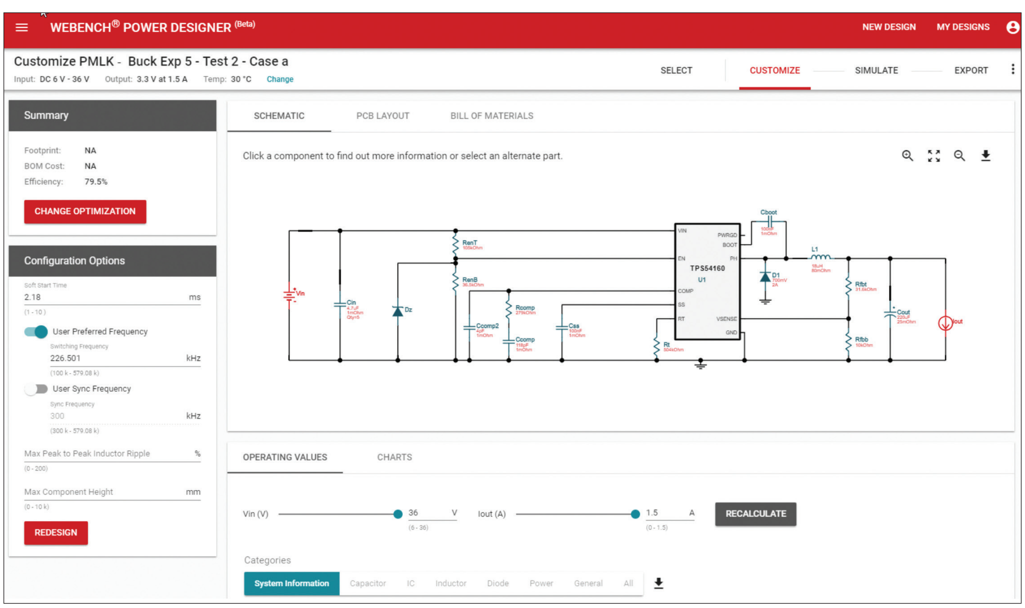


Figure 9.

2. Click on the **'Simulate'** icon in the top of the window to open **Electrical Simulation**.

Figure 10.

3. In the **'Simulations'** menu, select **Steady State** from the list of simulations as shown in **Figure 11**.

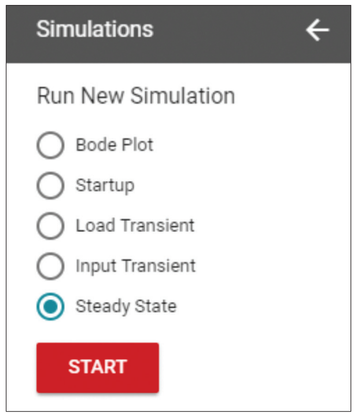


Figure 11.

4. Click the **'Input voltage'** source and change its nominal value to **12V**. Click **'Save'**.

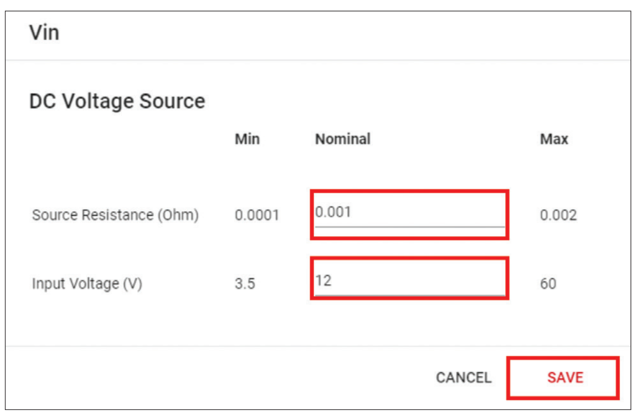


Figure 12.

5. Click $\mathbf{I_{OUT}}$, which indicates load current, and change its nominal value to **1A**. Click **'Save'**.

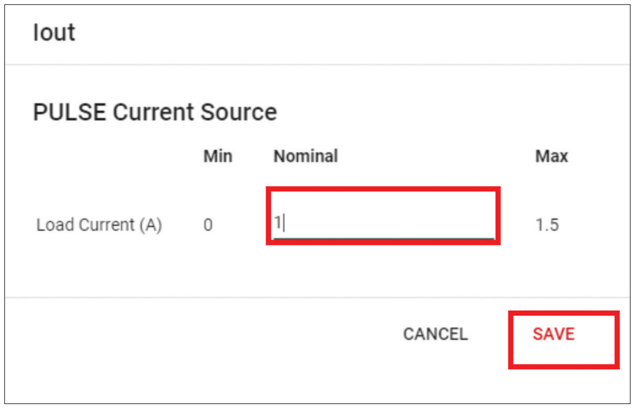


Figure 13.

6. Click **'Start'**.

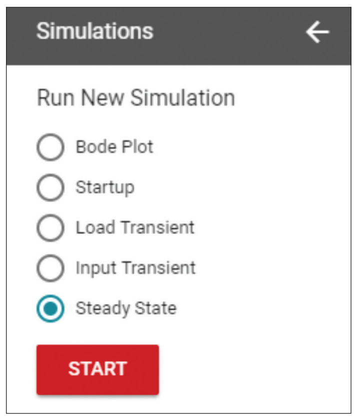


Figure 11.

7. After the end of simulation, Click on V_{comp} voltage probe to plot the control voltage. The plot appears as shown in **Figure 15**.

8. Check the **'Marker'** to enable it and find the minimum and maximum voltages by moving cursor along the waveform as shown in **Figure 16**. Calculate the average of these two values and enter it in **Table 2**.

9. Repeat **Steps 4-8** to complete the **Table 2** for different input voltages. I_{OUTmax} is fixed as 1.5A due to the current limit of TPS54160. Repeat **Steps 4-8 to** find Vc @ I_{OUTmax}.

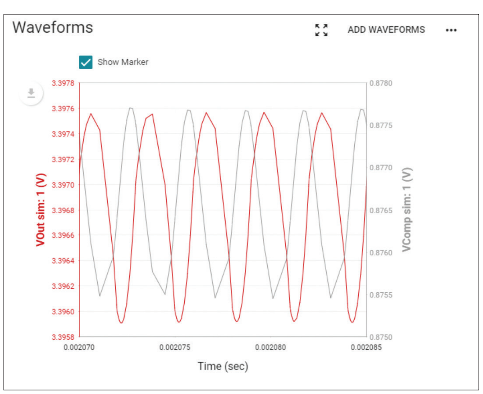


Figure 15.

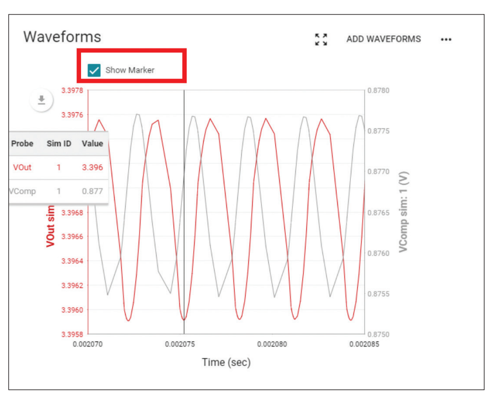


Figure 16.

10. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer for switching frequency of 500kHz.

11. Follow the **Steps 2-9** and complete f_s = 500kHz part of **Table 2** under $C_{OUT} = C_{16}$ = 220µF.

12. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer for $C_{OUT}= C_{17}$=10µF and switching frequency of 250kHz.

13. Follow the **Steps 2-9** and complete f_s = 250kHz part of **Table 2** under $C_{OUT} = C_{17}$ = 10µF.

14. Click on the link to open the V_{OUT} = 3.3V TPS54160 design in WEBENCH® Power Designer for $C_{OUT}= C_{17}$=10µF and switching frequency of 500kHz.

15. Follow the **Steps 2-9** and complete f_s = 500kHz part of **Table 2** under $C_{OUT} = C_{17}$ = 10µF.

V_{IN}	$C_{OUT} = C_{16}$ = 220µF						$C_{OUT} = C_{17}$ = 10µF					
	f_s = 250kHz			f_s = 500kHz			f_s = 250kHz			f_s = 500kHz		
	V_c @ 1A	I_{OUTmax} (A)	V_c @ I_{OUTmax} (V)	V_c @ 1A	I_{OUTmax} (A)	V_c @ I_{OUTmax} (V)	V_c @ 1A	I_{OUTmax} (A)	V_c @ I_{OUTmax} (V)	V_c @ 1A	I_{OUTmax} (A)	V_c @ I_{OUTmax} (V)
12V												
36V												

Table 4. Control voltage and maximum output current of TPS54160 buck regulator operating with ferrite inductor, with different input voltage, switching frequency and output capacitor setup.

Note: The maximum current limit is decided by inductor current ripple in **TI-PMLK** board whereas in webench it is fixed as 1.5A, maximum current of TPS54160. So I_{OUTmax} is fixed as 1.5A in both the tests of this experiment.

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