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OMAP4460/4470 Multimedia Devices TRM Addendum - Functional Differences Highlights between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0

Texas Instruments OMAP™Family of Products

Technical Reference Manual

Literature Number: SWPU316

August-2012

OMAP4460/4470 Multimedia Devices TRM Addendum - Functional Differences Highlights between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0

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Delta Readers' Guide

The purpose of this document is to highlight functional modifications between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0. To easily locate the updates and focus on the modified functionalities, the document is organized as follows:

- For all sections, except the Register Manual section:
  - A high level description of the differences between the two devices is given in the most appropriate location
  - The high level changes appear in red color
  - The full versions of chapters updated are available in the regular TRM
- For the Register Manual section, only modified or added registers are given:
  - Old bit-fields or registers appear in strikethrough
  - New or updated bit-fields or registers appear in red color
  - Unchanged information remains in the regular formatting

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History

The following table summarizes the OMAP4460/4470 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 versions.

Table 1. TRM Addendum versions

Version	Literature Number	Date	Notes
1.10	SWPU316	August 2012	OMAP4470 Multimedia Device TRM Addendum - Functional difference highlights from OMAP4460 ES1.x to OMAP4470 ES1.0 multimedia devices - Initial release (SWPU316).

Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

This chapter describes the differences in the features, supporting subsystems, and architecture between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices

Note

Exhaustive lists of functional differences are presented in the respective chapters of this document.

1.1. Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

1.2. Environment

The OMAP4470 target companion devices are changed as follows:

- TWL6032 replaces the TWL6030 power-management device
- TWL6041 replaces the TWL6040 audio device
- TPS62361 auxiliary power-supply device is not used
- BQ24156 battery charger IC is not mandatory. TWL6032 has embedded battery charger functionality.

1.3. Description

1.3.1. Cortex-A9 MPU Subsystem Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.2. DSP Subsystem Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.3. IVA-HD Subsystem Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.4. Cortex-M3 MPU Subsystem Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.5. Display Subsystem Description

The NTSC/PAL Video Encoder (VENC) and associated video digital-to-analog converter (VDAC) are removed from OMAP4470.

1.3.6. ABE Subsystem Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.7. ISS Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.8. 2D/3D Graphics Accelerator Description

New 3-D graphics accelerator core is introduced. POWERVR® SGX544-SC replaces the SGX540 3-D graphics accelerator core. It offers faster performance and new API support.

New 2-D graphics accelerator subsystem (BitBlt 2D (BB2D)) is introduced. It is based on the GC320 2-D core from Vivante Corporation.

1.3.9. Face Detect Module Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.10. On-Chip Debug Support Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.11. Power, Reset, and Clock Management Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.12. On-Chip Memory Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.13. Memory Management Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.14. External Memory Interface Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.15. DSP Subsystem Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.3.16. System and Connection Peripherals

The one-port Full-Speed (FS) USB host controller is removed from OMAP4470.

1.4. Package-On-Package Concept

Refer to OMAP4470 Silicon Revision 1.0 TRM

1.5. OMAP4470 Family and Device Identification

ID_CODE register is changed as follows:

- Ramp system number is 0xB975 in OMAP4470 ES1.0
- Revision number is 0x0 in OMAP4470 ES1.0
- The ID_CODE register value is 0x0B97 502F in OMAP4470 ES1.0.

Silicon performance register is changed as follows:

Table 1.1. STD_FUSE_PROD_ID_1

Address Offset	0x0000 0218		
Physical Address	0x4A00 2218	**Instance**	GENERAL
Description	This register shows the device type.		
Type	R		

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x-
17:16	SILICON_TYPE	Define the silicon performance type 0x0: Reserved 0x1: Standard performance (~~1.2~~1.3GHz) 0x2: High performance (1.5GHz) 0x3: Reserved	R	0x-
15:0	RESERVED	Reserved	R	0x-

Chapter 2. Memory Mapping

This chapter describes differences in the memory mapping between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

2.1. Introduction

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.2. L3 Memory Space Mapping

Table 2.1. Global Memory Space Mapping

Quarter	Module Name	Start Address (hex)	End Address (hex)	Size	Description
Q0 (1GB)	Boot space GPMC	0x0000 0000	0x3FFF FFFF	1GB	
	GPMC	0x0000 0000	0x3FFF FFFF	1GB	8/16 Ex/R/W[1]
Q1 (1GB)	On-chip memory	0x4000 0000	0x7FFF FFFF	1GB	ROM/SRAM address space
	Reserved	0x4000 0000	0x4002 FFFF	192KB	Reserved
	Boot ROM internal	0x4003_0000	0x4003_BFFF	48KB	32-bit Ex/R Boot ROM[2]
	Reserved	0x4003 C000	0x400F FFFF	784KB	Reserved
	Audio back-end (ABE)	0x4010 0000	0x401F FFFF	1MB	ABE domain (direct Cortex-A9 MPU access). SeeSection 2.3.4.
	Reserved	0x4020 0000	0x402F FFFF	1MB	Reserved
	L3 OCMC_RAM	0x4030 0000	0x4030 DFFF	56KB	32bit Ex/R/W
	Reserved	0x4030 E000	0x43FF FFFF	61MB	Reserved
	L3 configuration registers	0x4400 0000	0x47FF FFFF	64MB	L3 configuration registers
	L4_PER domain	0x4800 0000	0x48FF FFFF	16MB	Peripheral domain (seeSection 2.3.3)
	L4_ABE domain	0x4900 0000	0x49FF FFFF	16MB	ABE domain (double-mapped for Cortex-A9 MPU)
	L4_CFG domain	0x4A00 0000	0x4AFF FFFF	16MB	Configuration register domain (see ,*L3 Memory Space Mapping*). Also Includes L4_WKUP.
	Reserved	0x4B00 0000	0x4BFF FFFF	16MB	Reserved
	EMIF1 registers	0x4C00 0000	0x4CFF FFFF	16MB	Configuration registers
	EMIF2 registers	0x4D00 0000	0x4DFF FFFF	16MB	Configuration registers
	DMM registers	0x4E00 0000	0x4FFF FFFF	32MB	Configuration registers
	GPMC	0x5000 0000	0x51FF FFFF	32MB	Configuration registers
	ISS	0x5200 0000	0x53FF FFFF	32MB	ISP5 (128KB) + SIMCOP (128KB)
	L3_EMU domain	0x5400 0000	0x54FF FFFF	16MB	Emulation domain (see)
	Dual Cortex-M3 subsystem target	0x5500 0000	0x55FF FFFF	16MB	Dual Cortex-M3 subsystem target
	SGX	0x5600 0000	0x57FF FFFF	32MB	3D SGX54~~0~~4domain
	Display subsystem	0x5800 0000	0x58FF FFFF	16MB	Display subsystem domain
	BB2D	0x5900 0000	0x59FF FFFF	16MB	2D Blitter (GC3x0) domain
	IVA-HD configuration	0x5A00 0000	0x5AFF FFFF	16MB	IVA-HD domain
	IVA-HD SL2	0x5B00 0000	0x5BFF FFFF	16MB	IVA-HD SL2 domain
	C2C	0x5C00 0000	0x5FFF FFFF	64MB	Chip-to-chip domain
	Tiler	0x6000 0000	0x7FFF FFFF	512MB	Tiler address mapping
Q2 (1GB)	DRAM address space	0x8000 0000	0xBFFF FFFF	1GB	DDR-SDRAM CS0 address space

Quarter	Module Name	Start Ad dress (hex)	End Ad- dress (hex)	Size	Description
	EMIF1-CS0 SDRAM	0x8000 0000	0xBFFF FFFF	1GB	DDR Ctrl1 chip-select 0
	EMIF2-CS0 SDRAM	0x8000 0000	0xBFFF FFFF	1GB	DDR Ctrl2 chip-select 0
Q3 (1GB)	DRAM address space	0xC000 0000	0xFFFF FFFF	1 GB	DDR-SDRAM CS1 address space
	EMIF1-CS1 SDRAM	0xC000 0000	0xFFFF FFFF	1GB	DDR Ctrl1 chip-select 1
	EMIF2-CS1 SDRAM	0xC000 0000	0xFFFF FFFF	1GB	DDR Ctrl2 chip-select 1
	Tiler view (visible only for ISS and display subsystem)				
	Tiler view 0	0x1 0000 0000	0x1 1FFF FFFF	512MB	Natural view
	Tiler view 1	0x1 2000 0000	0x1 3FFF FFFF	512MB	0° view with vertical mirror
	Tiler view 2	0x1 4000 0000	0x1 5FFF FFFF	512MB	0° view with horizontal mirror
	Tiler view 3	0x1 6000 0000	0x1 7FFF FFFF	512MB	180° view
	Tiler view 4	0x1 8000 0000	0x1 9FFF FFFF	512MB	90° view with vertical mirror
	Tiler view 5	0x1 A000 0000	0x1 BFFF FFFF	512MB	270° view
	Tiler view 6	0x1 C000 0000	0x1 DFFF FFFF	512MB	90° view
	Tiler view 7	0x1 E000 0000	0x1 FFFF FFFF	512MB	90° view with horizontal mirror

1. Boot space location depends on the external sys_boot[5:0] pins.
2. Ex = Executable

2.2.1. L3_EMU Memory Space Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.3. L4 Memory Space Mapping

2.3.1. L4_CFG Memory Space Mapping

Table 2.2. L4_CFG Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
L4_CFG configuration	0x4A00 0000	0x4A00 07FF	2KB	Address/protection (AP)
	0x4A00 0800	0x4A00 0FFF	2KB	Link agent (LA)
	0x4A00 1000	0x4A00 1FFF	4KB	Initiator port (IP0)
SYSCTRL_GENERAL_ CORE	0x4A00 2000	0x4A00 2FFF	4KB	Module
	0x4A00 3000	0x4A00 3FFF	4KB	L4 interconnect
CM1: Manages Cortex-A9 MPU, DSP, IVA, ABE, m emory interface, digital pha se-locked loops (DPLLs) for Cortex-A9 MPU, DSP, ABE, CORE	0x4A00 4000	0x4A00 4FFF	4KB	Module region A
	0x4A00 5000	0x4A00 5FFF	4KB	L4 interconnect
Reserved	0x4A00 6000	0x4A00 7FFF	8KB	Reserved
CM2 (manages all others)	0x4A00 8000	0x4A00 9FFF	8KB	Module
	0x4A00 A000	0x4A00 AFFF	4KB	L4 interconnect
Reserved	0x4A00 B000	0x4A05 5FFF	300KB	Reserved
System DMA (sDMA)	0x4A05 6000	0x4A05 6FFF	4KB	Module
	0x4A05 7000	0x4A05 7FFF	4KB	L4 interconnect
HSI	0x4A05 8000	0x4A05 8FFF	4KB	HSI top
	0x4A05 9000	0x4A05 9FFF	4KB	HSI DMA
	0x4A05 A000	0x4A05 AFFF	4KB	HSI port 1
	0x4A05 B000	0x4A05 BFFF	4KB	HSI port 2
	0x4A05 C000	0x4A05 CFFF	4KB	L4 interconnect

Module Name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	0x4A05 D000	0x4A05 DFFF	4KB	Reserved
SAR_ROM (save and restor e)	0x4A05 E000	0x4A05 FFFF	8KB	Module
	0x4A06 0000	0x4A06 0FFF	4KB	L4 interconnect
Reserved	0x4A06 1000	0x4A06 1FFF	4KB	Reserved
HSUSBTLL	0x4A06 2000	0x4A06 2FFF	4KB	Module
	0x4A06 3000	0x4A06 3FFF	4KB	L4 interconnect
HSUSBHOST	0x4A06 4000	0x4A06 4FFF	4KB	Module
	0x4A06 5000	0x4A06 5FFF	4KB	L4 interconnect
DSP subsystem	0x4A06 6000	0x4A06 6FFF	4KB	Module
	0x4A06 7000	0x4A06 7FFF	4KB	L4 interconnect
Reserved	0x4A06 8000	~~0x4A0A 8FFF~~ 0x4A0A AFFF	~~266~~ 274KB	Reserved
FSUSB	~~0x4A0A 9000~~	~~0x4A0A 9FFF~~	~~4KB~~	~~Module~~
	~~0x4A0A A000~~	~~0x4A0A AFFF~~	~~4KB~~	~~L4 interconnect~~
HSUSBOTG	0x4A0A B000	0x4A0A BFFF	4KB	Module
	0x4A0A C000	0x4A0A CFFF	4KB	L4 interconnect
USBPHY	0x4A0A D000	0x4A0A D07F	~~4KB~~ 128B	~~Module~~ OCP2SCP Module
	0x4A0A D080	0x4A0A DFFF	3968B	USB PHY module
	0x4A0A E000	0x4A0A EFFF	4KB	L4 interconnect
Reserved	0x4A0A F000	~~0x4A0D 8FFF~~ 0x4A0B 5FFF	~~144KB~~ 28KB	Reserved
MODEM_ICR Port A	0x4A0B 6000	0x4A0B 6FFF	4KB	Module
	0x4A0B 7000	0x4A0B 7FFF	4KB	L4 interconnect
Reserved	0x4A0B 8000	0x4A0C CFFF	16KB	Reserved
MODEM_ICR Port B	0x4A0C D000	0x4A0C DFFF	4KB	Module
	0x4A0C E000	0x4A0C EFFF	4KB	L4 interconnect
Reserved	0x4A0C F000	0x4A0D 8FFF	40KB	Reserved
SR_MPU (SmartReflex™ MPU)	0x4A0D 9000	0x4A0D 9FFF	4KB	Port SR MPU
	0x4A0D A000	0x4A0D AFFF	4KB	L4 interconnect
SR_IVA (SmartReflex IVA)	0x4A0D B000	0x4A0D BFFF	4KB	Port SR IVA
	0x4A0D C000	0x4A0D CFFF	4KB	L4 interconnect
SR_CORE (SmartReflex core)	0x4A0D D000	0x4A0D DFFF	4KB	Port SR core
	0x4A0D E000	0x4A0D EFFF	4KB	L4 interconnect
Reserved	0x4A0D F000	0x4A0D FFFF	86KB	Reserved
EFUSE_CTRL_CUST	0x4A0E 0000	0x4A0E 0FFF	4KB	Module
	0x4A0E 1000	0x4A0E 1FFF	4KB	L4 interconnect
Reserved	0x4A0E 2000	0x4A0F 3FFF	72KB	Reserved
Mailbox	0x4A0F 4000	0x4A0F 4FFF	4KB	Module
	0x4A0F 5000	0x4A0F 5FFF	4KB	L4 interconnect
Spinlock	0x4A0F 6000	0x4A0F 6FFF	4KB	Module
	0x4A0F 7000	0x4A0F 7FFF	4KB	L4 interconnect
Reserved	0x4A0F 8000	0x4A0F FFFF	32KB	Reserved
SYSCTRL_PADCONF_ CORE	0x4A10 0000	0x4A10 0FFF	4KB	Module
	0x4A10 1000	0x4A10 1FFF	4KB	L4 interconnect

Module Name	Start Address (hex)	End Address (hex)	Size	Description
OCP-WP – Shared	0x4A10 2000	0x4A10 2FFF	4KB	Module
	0x4A10 3000	0x4A10 3FFF	4KB	L4 interconnect
Reserved	0x4A10 4000	0x4A10 9FFF	24KB	Reserved
Face detect	0x4A10 A000	0x4A10 AFFF	4KB	Module
	0x4A10 B000	0x4A10 BFFF	4KB	L4 interconnect
Reserved	0x4A10 C000	0x4A20 3FFF	992KB	Reserved
C2C-Init firewall	0x4A20 4000	0x4A20 4FFF	4KB	Module
	0x4A20 5000	0x4A20 5FFF	4KB	L4 interconnect
C2C-Target firewall	0x4A20 6000	0x4A20 6FFF	4KB	Module
	0x4A20 7000	0x4A20 7FFF	4KB	L4 interconnect
Reserved	0x4A20 8000	0x4A20 9FFF	8KB	Reserved
MA firewall	0x4A20 A000	0x4A20 AFFF	4KB	Memory adapter configuration registers
	0x4A20 B000	0x4A20 BFFF	4KB	L4 interconnect
EMIF firewall	0x4A20 C000	0x4A20 CFFF	4KB	Configuration registers
	0x4A20 D000	0x4A20 DFFF	4KB	L4 interconnect
Reserved	0x4A20 E000	0x4A20 FFFF	8KB	Reserved
GPMC firewall	0x4A21 0000	0x4A21 0FFF	4KB	Configuration registers
	0x4A21 1000	0x4A21 1FFF	4KB	L4 interconnect
OCMC RAM firewall	0x4A21 2000	0x4A21 2FFF	4KB	Module
	0x4A21 3000	0x4A21 3FFF	4KB	L4 interconnect
GFX-T firewall	0x4A21 4000	0x4A21 4FFF	4KB	Module
	0x4A21 5000	0x4A21 5FFF	4KB	L4 interconnect
ISS-T firewall	0x4A21 6000	0x4A21 6FFF	4KB	Module
	0x4A21 7000	0x4A21 7FFF	4KB	L4 interconnect
Dual Cortex-M3-T firewall	0x4A21 8000	0x4A21 8FFF	4KB	Module
	0x4A21 9000	0x4A21 9FFF	4KB	L4 interconnect
Reserved	~~0x4A21 A000~~	~~0x4A21 BFFF~~	~~8KB~~	~~Reserved~~
BB2D	0x4A21 A000	0x4A21 AFFF	4KB	Module
	0x4A21 B000	0x4A21 BFFF	4KB	L4 interconnect
DSS-T firewall	0x4A21 C000	0x4A21 CFFF	4KB	Module
	0x4A21 D000	0x4A21 DFFF	4KB	L4 interconnect
SL2-T firewall	0x4A21 E000	0x4A21 EFFF	4KB	Module
	0x4A21 F000	0x4A21 FFFF	4KB	L4 interconnect
IVAHD-CFG-T firewall	0x4A22 0000	0x4A22 0FFF	4KB	Module
	0x4A22 1000	0x4A22 1FFF	4KB	L4 interconnect
Reserved	0x4A22 2000	0x4A22 5FFF	16KB	Reserved
L4-EMU firewall	0x4A22 6000	0x4A22 6FFF	4KB	Module
	0x4A22 7000	0x4A22 7FFF	4KB	L4 interconnect
L4_ABE firewall	0x4A22 8000	0x4A22 8FFF	4KB	Module
	0x4A22 9000	0x4A22 9FFF	4KB	L4 interconnect
Reserved	0x4A22 A000	0x4A2F FFFF	856KB	Reserved
L4_WKUP	0x4A30 0000	0x4A33 FFFF	256KB	WKUP domain (see ,*L4_WKUP Memory Space Mapping*)
	0x4A34 0000	0x4A34 0FFF	4KB	L4 interconnect
Reserved	0x4A34 1000	0x4AFF FFFF	13052KB	Reserved

2.3.2. L4_WKUP Memory Space Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.3.3. L4_PER Memory Space Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.3.4. L4_ABE Memory Space Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.4. Dual Cortex-M3 Subsystem Memory Space Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.5. DSP Subsystem Memory Space Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.6. Display Subsystem Memory Space Mapping

The display subsystem integrates a dispaly controller (DISPC), a remote frame buffer interface (RFBI), two MIPI® display serial interfaces (DSI1 with four data lanes, and DSI2 with two data lanes), ~~an~~ and HDMI link with its PHY (high-definition multimedia interface, digital part)~~, and a video PAL/NTSC encoder (VENC) with video DAC (and TV out buffer)~~.

The DISPC is connected through an interconnect master port to the L3 interconnect and has its own DMAs to fetch the data from the system memory.

There are two views (from the L3_PER and L4_PER interconnects) of the display subsystem memory space mapping.

Note

~~The video DAC (VDAC) function is not supported~~.

2.6.1. L3 Interconnect View of the Display Memory Space

Refer to OMAP4470 Silicon Revision 1.0 TRM.

2.6.2. L4 Interconnect View of the Display Memory Space

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 3. Power, Reset, and Clock Management

This chapter describes the differences in the Power, Reset, and Clock Management between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

3.1. Device Power Management Introduction

In section **AVS Overview**, SmartReflex Class-3 is removed. OMAP4470 ES1.0 device supports only SmartReflex Class-1.5, but in a different way than the SmartReflex Class-1.5 supported in OMAP4460 ES1.x device. In OMAP4470 ES1.0 device, the additional temperature margins are fused, thus no user software is involved.

3.2. PRCM Subsystem Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.3. PRCM Subsystem Environment

3.3.1. External Clock Signals

The reference to the Video DAC, from table **External Clock Signals**, is removed.

3.3.2. External Boot Signals

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.3.3. External Reset Signals

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.3.4. External Power Control Signals

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.3.5. External Voltage Inputs

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.3.6. External Wake-Up Signals

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.4. PRCM Subsystem Integration

The BB2D module is added in, the FSUSB module is removed from the **PMFW Device-Level Layout** table.

Table 3.1. PMFW Device-Level Layout

Voltage Domain	Power Domain	Clock Domain	Module
LDO_WAKEUP	PD_EMU	CD_EMU	DEBUG
....	....	....	....
	PD_DSS	CD_DSS	DSS
			BB2D

Voltage Domain	Power Domain	Clock Domain	Module
	PD_SGX	CD_SGX	SGX
	PD_L3_INIT	CD_L3_INIT	HSI
			HSMMC1
			HSMMC2
			USBPHY
-	-	-	~~FSUSB~~
			HSUSBHOST
			HSUSBOTG
			HSUSBTLL
....	....	....	....
	PD_MPU	CD_CORTEXA9	CORTEXA9

3.5. Reset Management Functional Description

3.5.1. Overview

3.5.1.1. SCRM Reset Management Functional Description

3.5.1.1.1. Power-On Reset

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.5.1.1.2. Warm Reset

New warm reset source is added - TSHUT.

The device warm reset can be received from an external source through:

- warm reset pad sys_nreswarm
- general core Control Module thermal shutdown output – TSHUT
- device PRM module as a result of internal event

The SCRM extends the device pad warm reset duration to the device PRM module.

The SCRM routes a warm reset source (that is, sys_nreswarm pad/PRM module) to a warm reset destination (that is, PRM module).

This routing of reset from the device pad to the PRM is enabled and disabled using the SCRM.EXTWARMRSTCTRL register. It is enabled by default.

The source of a warm reset, for each destination is logged in the corresponding SCRM.EXTWARMRSTST_REG register. The status of the reset source is logged when the destination reset is released. This is done at 32-kHz clock.

Software must clear the reset status bit.

The general core Control Module thermal shutdown output (TSHUT) can be programmed as a source of a hardware warm reset, which is triggered when the device die temperature crosses a programmable FATAL threshold. For more information about the TSHUT warm reset generation, see section **Thermal Shutdown Functionality Comparators** of the **Control Module** chapter.

3.5.1.2. PRM Reset Management Functional Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.5.2. General Characteristics of Reset Signals

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.5.3. Reset Sources

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.5.4. Reset Domains

The BB2D module is added in, the FSUSB module is removed from the **Modules, Power Domains and Reset Domains Association** table.

Table 3.2. Modules, Power Domains and Reset Domains Association

Module	Power Domain	Reset Domains
CM1	PD_ALWON_CORE	ALWON_CM1_PWRON_RST, ALWON_CM1_RST
......	....	....
DSS	PD_DSS	DSS_RET_RST, DSS_RST
BB2D	PD_DSS	DSS_RST
....	....	....
USBPHY	PD_L3_INIT	L3_INIT_RST
~~FSUSB~~	~~PD_L3_INIT~~	~~L3_INIT_RET_RST~~
HSUSBHOST	PD_L3_INIT	L3_INIT_RET_RST
....	....	....
L4_WKUP interconnect	PD_WKUP	WKUP_RST

3.5.5. Reset Logging

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.5.6. Reset Sequences

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6. Clock Management Functional Description

3.6.1. Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.2. External Clock Inputs

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3. Internal Clock Sources/Generators

3.6.3.1. PRM Clock Source

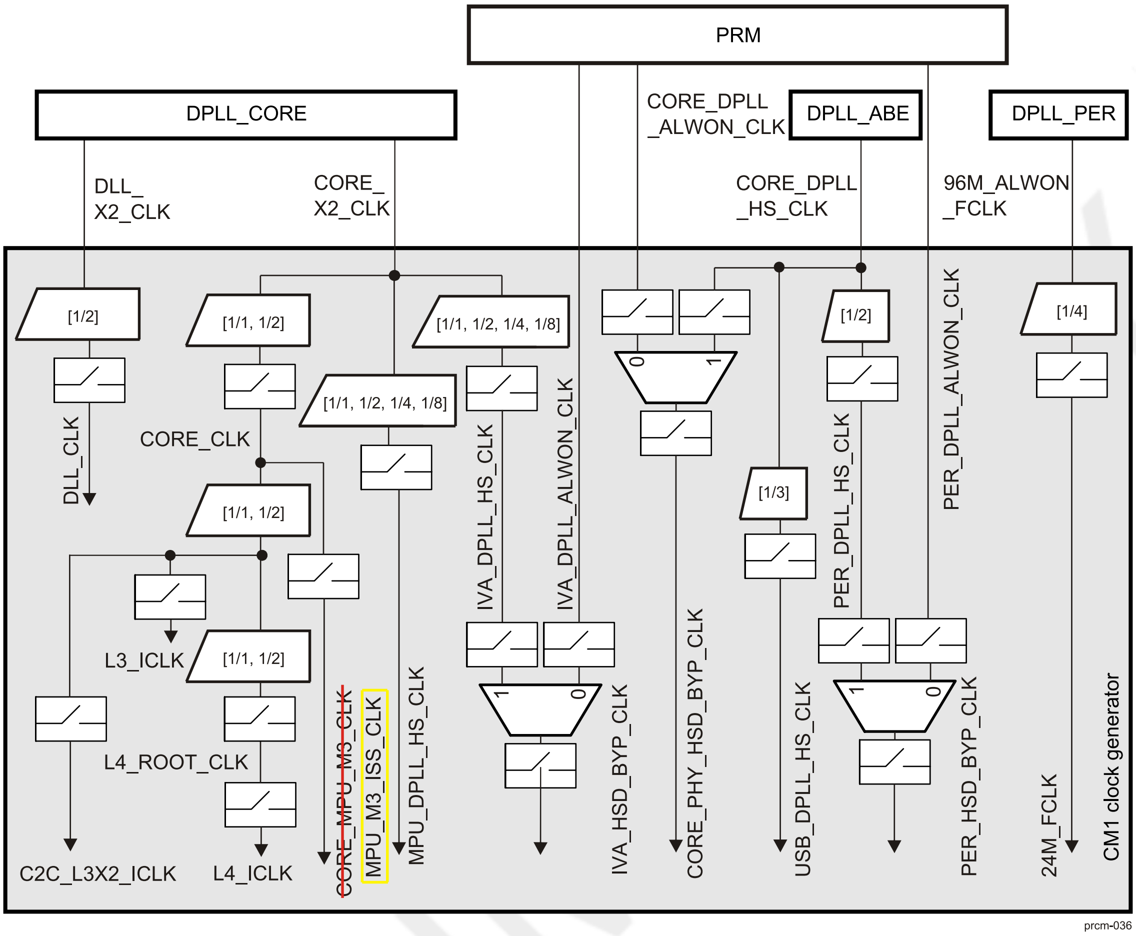
Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.2. CM Clock Source

3.6.3.2.1. CM1 Clock Generator

The CORE_MPU_M3_CLK is replaced with the MPU_M3_ISS_CLK.

Figure 3.1. CM1 Overview



3.6.3.2.2. CM1_USB Clock Generator

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.2.3. CM1_ABE Clock Generator

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.2.4. CM2 Clock Generator

The CM2 Clock Generator is updated as follows:

- SGX clock signals, switches and multiplexer are removed from the CM2
- Cortex-M3 MPU and ISS clock signals tree is updated
- BB2D clock signals, switches and multiplexer are added in the CM2

Figure 3.2. CM2 Overview (a)

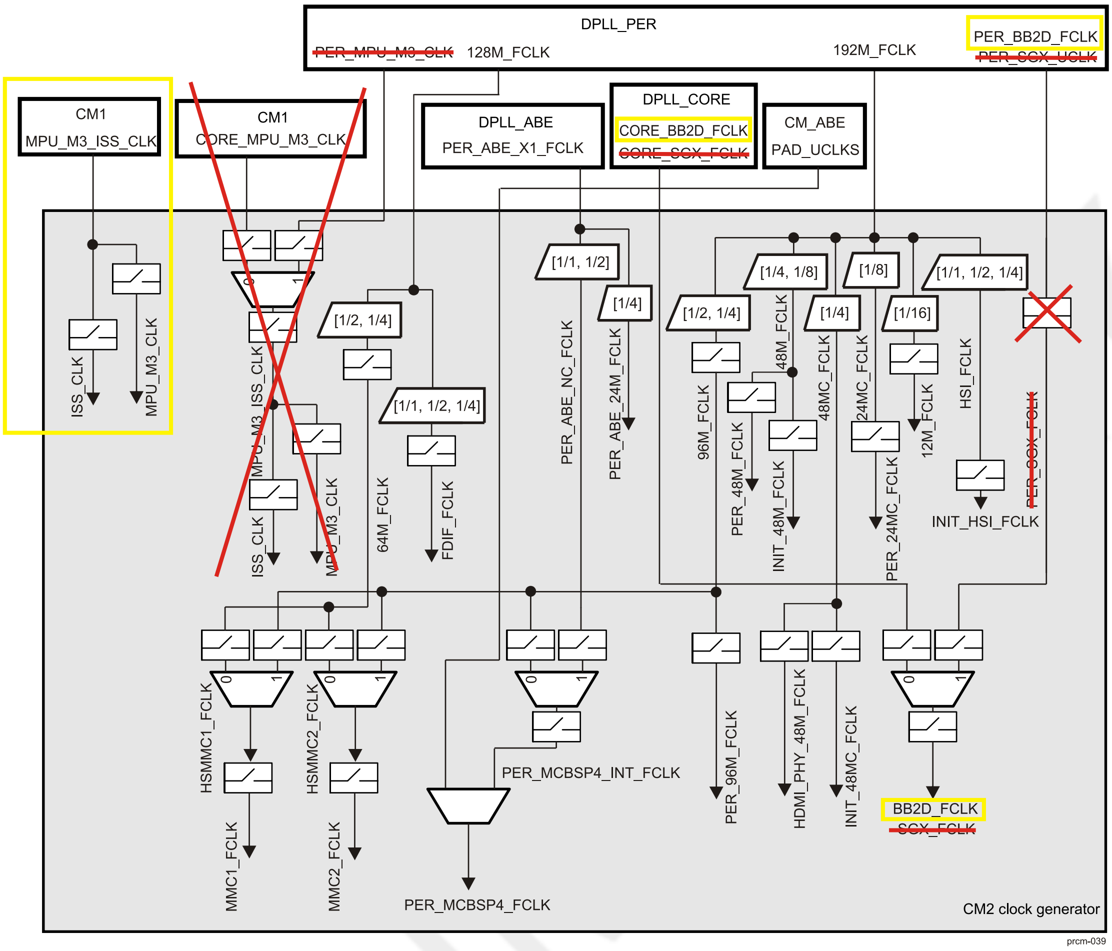


Table **CM2 Clock Division and Muxing Control** is updated as follows:

- SGX_FCLK mux is removed from the table
- MPU_M3_ISS_CLK mux is removed from the table
- BB2D_FCLK mux is added to the table

Table 3.3. CM2 Clock Division and Muxing Control

Divider/Mux	Control Bit Field
Divider FDIF_FCLK	CM_CAM_FDIF_CLKCTRL[25:24] CLKSEL_FCLK
Divider HSI_FCLK	CM_L3INIT_HSI_CLKCTRL[25:24] CLKSEL
Mux HSMMC1_FCLK	CM_L3INIT_HSMMC1_CLKCTRL[24] CLKSEL
Mux HSMMC2_FCLK	CM_L3INIT_HSMMC2_CLKCTRL[24] CLKSEL
~~Mux MPU_M3_ISS_CLK~~	~~CM_CLKSEL_MPU_M3_ISS_ROOT[0] CLKSEL~~
Mux PER_MCBSP4_FCLK	CM_L4PER_MCBSP4_CLKCTRL[24] CLKSEL_SOURCE
Mux PER_MCBSP4_INT_FCLK	CM_L4PER_MCBSP4_CLKCTRL[25] CLKSEL_INTERNAL_SOURCE
~~Mux SGX_FCLK~~	~~CM_SGX_SGX_CLKCTRL[24] CLKSEL_SGX_FCLK~~
Mux BB2D_FCLK	CM_DSS_BB2D_CLKCTRL[24] CLKSEL_BB2D_FCLK
Divider PER_ABE_NC_FCLK, 96M_FCLK, 64M_FCLK and 48M_FCLK	CM_SCALE_FCLK[0] SCALE_FCLK

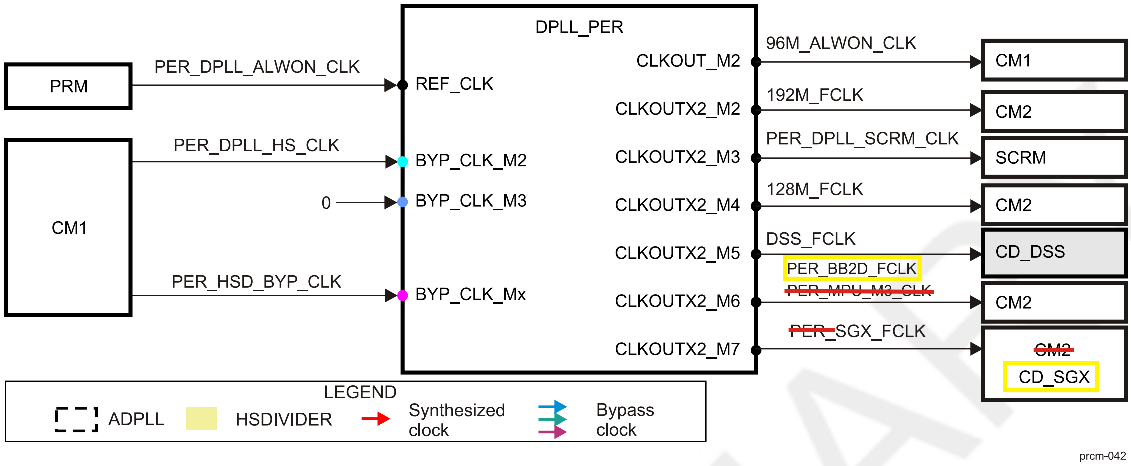
3.6.3.3. Generic DPLL Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.4. DPLL_PER Description

The PER_MPU_M3_CLK is replaced with the PER_BB2D_FCLK. The PER_SGX_FCLK is renamed to SGX_FCLK and is going directly into the CD_SGX instead of going into the CM2 Clock Generator.

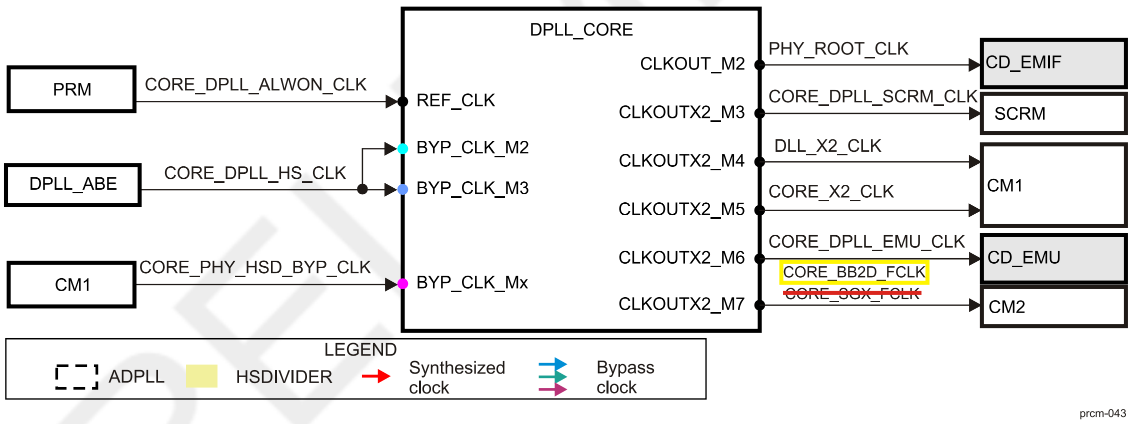
Figure 3.3. DPLL_PER Overview



3.6.3.5. DPLL_CORE Description

The CORE_SGX_FCLK is replaced with the CORE_BB2D_FCLK.

Figure 3.4. DPLL_CORE Overview



3.6.3.6. DPLL_ABE Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.7. DPLL_MPU Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.8. DPLL_IVA Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.9. DPLL_USB Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.3.10. DPLLs Cascading

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.4. CD_WKUP Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.5. CD_DSP Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.6. CD_STD_EFUSE Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.7. CD_CORTEXA9 Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.8. CD_L4_PER Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.9. CD_L3_INIT Clock Domain

The FSUSB module is removed from the subsection as follows:

3.6.9.1. Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.9.2. Clock Domain Modes

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.9.3. Clock Domain Dependency

3.6.9.3.1. Static Dependency

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.9.3.2. Dynamic Dependency

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.9.3.3. Wake-Up Dependency

Table 3.4. CD_L3_INIT Wake-Up Dependency Association Parameters

Originator Module	Originator Clock Domain	Servicing Clock Domain	Default Setting	Control Bit Field	Access Type
HSI	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_HSI_WKDEP[8] WKUPDEP_WGM_HSI_WAKE_MPU	Read/Write
....	....	....	....	....	....
HSMMC2	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_MMC2_WKDEP[0] WKUPDEP_MMC2_MPU	Read/Write
~~FSUSB~~	~~CD_L3_INIT~~	~~CD_CORTEXM3~~	~~Disabled~~	~~PM_L3INIT_FSUSB_WKDEP[1] WKUPDEP_FSUSB_MPU_M3~~	~~Read/Write~~
~~FSUSB~~	~~CD_L3_INIT~~	~~CD_CORTEXA9~~	~~Disabled~~	~~PM_L3INIT_FSUSB_WKDEP[0] WKUPDEP_FSUSB_MPU~~	~~Read/Write~~
HSUSBHOST	CD_L3_INIT	CD_CORTEXM3	Disabled	PM_L3INIT_HSUSBHOST_WKDEP[1] WKUPDEP_HSUSBHOST_MPU_M3	Read/Write
....	....	....	....	....	....
HSUSBTLL	CD_L3_INIT	CD_CORTEXA9	Disabled	PM_L3INIT_HSUSBTLL_WKDEP[0] WKUPDEP_HSUSBTLL_MPU	Read/Write

3.6.9.4. Clock Domain Module Attributes

Table 3.5. CD_L3_INIT Modules Clocks Association

Module	Clock	Clock Type
HSI	INIT_HSI_FCLK	Interface and functional
	INIT_L3_ICLK	Interface
	INIT_L4_ICLK	Interface
....	....	....
~~FSUSB~~	~~INIT_48MC_FCLK~~	~~Functional~~
-	~~INIT_L3_ICLK~~	~~Interface~~
-	~~INIT_L4_ICLK~~	~~Interface~~
....	....	....
HSUSBTLL	INIT_L4_ICLK	Interface
	TLL_CH0_FCLK	Functional
	TLL_CH1_FCLK	Functional

Table 3.6. CD_L3_INIT Modules Wake-Up Request

Module	Wake-Up Feature
HSI	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP-IRQ)/Master wake-up request
....	....
USBPHY	None
~~FSUSB~~	~~Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)/Master wake-up request~~
....	....
HSUSBTLL	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ)

Table 3.7. CD_L3_INIT Modules Clock-Management Modes and Control

Module	Clock-Management Protocol	Status Bit Field	Role
HSI	Slave/Master	CM_L3INIT_HSI_CLKCTRL[18] STBYST	Standby status
		CM_L3INIT_HSI_CLKCTRL[17] IDLEST	Idle status
....	....	....	....
~~FSUSB~~	~~Slave/Master~~	~~CM_L3INIT_FSUSB_CLKCTRL[18] STBYST~~	~~Standby status~~
-	-	~~CM_L3INIT_FSUSB_CLKCTRL[17] IDLEST~~	~~Idle status~~
....	....	....	....
HSUSBTLL	Slave/Master	CM_L3INIT_HSUSBTLL_CLKCTRL[17:16] STBYST	Idle status
		CM_L3INIT_HSUSBTLL_CLKCTRL_RESTORE[17:16] IDLEST	Idle status

Table 3.8. CD_L3_INIT Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
HSI	Available	Available	N/A	CM_L3INIT_HSI_CLKCTRL[1:0] MODULEMODE	Read/Write
....	....	.....	....	....	....
~~FSUSB~~	~~Available~~	~~N/A~~	~~Available~~	~~CM_L3INIT_FSUSB_CLKCTRL[1:0] MODULEMODE~~	~~Read/Write~~
....	....	.....	....	....	....
HSUSBTLL	Available	Available	N/A	CM_L3INIT_HSUSBTLL_CLKCTRL[1:0] MODULEMODE	Read/Write

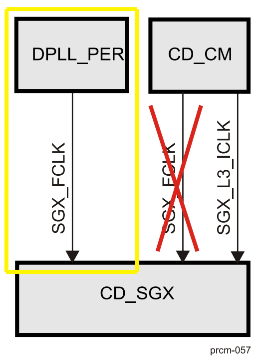
3.6.10. CD_IVAHD Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.11. CD_SGX Clock Domain

The SGX_FCLK is sourced directly from the DPLL_PER, instead of the CM2 Clock Generator.

Figure 3.5. CD_SGX Overview



3.6.12. CD_EMU Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.13. CD_DSS Clock Domain

New module is added in the CD_DSS Clock Domain - BB2D. The DSS_TV_FCLK is removed. The BB2D module and its functional clock (BB2D_FCLK) are added as follows:

Figure 3.6. CD_DSS Overview

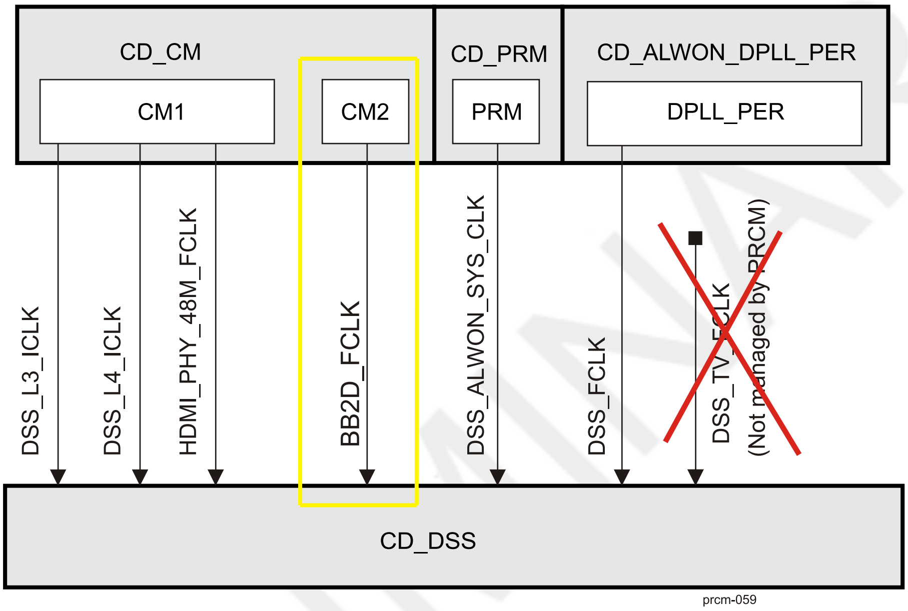


Table 3.9. CD_DSS Control and Status Parameters

Parameter Name	Control/Status Bit Field
DSS_ALWON_SYS_CLK clock status	CM_DSS_CLKSTCTRL[10] CLKACTIVITY_DSS_ALWON_SYS_CLK
DSS_FCLK clock status	CM_DSS_CLKSTCTRL[9] CLKACTIVITY_DSS_FCLK
HDMI_PHY_48M_FCLK clock status	CM_DSS_CLKSTCTRL[11] CLKACTIVITY_HDMI_PHY_48M_FCLK
DSS_L3_ICLK clock status	CM_DSS_CLKSTCTRL[8] CLKACTIVITY_DSS_L3_ICLK
BB2D_FCLK clock status	CM_DSS_CLKSTCTRL[12] CLKACTIVITY_BB2D_FCLK
Clock Domain State Transition Control	CM_DSS_CLKSTCTRL[1:0] CLKTRCTRL

The DSS Clock Domain Static Dependency towars CD_L3_2 is updated from Disabled to Always enabled:

Table 3.10. CD_DSS Static Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_IVAHD	Disabled	CM_DSS_STATICDEP [2] IVAHD_STATDEP	Read/Write
CD_L3_1	Always enabled	CM_DSS_STATICDEP [5] L3_1_STATDEP	Read only
CD_L3_2	~~Disabled~~Always enabled	CM_DSS_STATICDEP [6] L3_2_STATDEP	~~Read/Write~~Read only
CD_EMIF	Disabled	CM_DSS_STATICDEP [4] MEMIF_STATDEP	Read/Write

The DSS Clock Domain Dynamic Dependancy towards CD_L3_2 is updated:

Table 3.11. CD_DSS Dynamic Dependency Association Parameters

Clock Domain Name	Default Setting	Control Bit Field	Access Type
CD_L3_1	Always disabled	CM_DSS_DYNAMICDEP[5] L3_1_DYNDEP	Read only
CD_L3_2	Always disabled	CM_DSS_DYNAMICDEP[6] L3_2_DYNDEP	Read only

Table 3.12. CD_DSS Modules Clocks Association

Module	Clock	Clock Type
DSS	DSS_ALWON_SYS_CLK	Functional
	DSS_FCLK	Functional
	~~DSS_TV_FCLK~~	~~Functional~~
	HDMI_PHY_48M_FCLK	Functional
	DSS_L3_ICLK	Interface
	DSS_L4_ICLK	Interface
BB2D	BB2D_FCLK	Functional
	DSS_L3_ICLK	Interface

~~Note~~

~~DSS_TV_FCLK is sourced from fref_slicer_in input pin. To enable DSS_TV_FCLK it must be ungated in ALT-CLKSRC[3] ENABLE_EXT and must be enabled in CM_DSS_DSS_CLKCTRL[11] OPTFCLKEN_TV_FCLK.~~

Table 3.13. CD_DSS Modules Wake-Up Request

Module	Wake-Up Feature
DSS	Slave wake-up request (MPU_A9 -IRQ, MPU_M3 -IRQ, DSP -IRQ, sDMA -DMA)
BB2D	None

Table 3.14. CD_DSS Dynamic Dependency Association Parameters

Module	Clock-Management Protocol	Status Bit Field	Role
DSS	Master/Slave	CM_DSS_DSS_CLKCTRL[18] STBYST	Standby status
		CM_DSS_DSS_CLKCTRL[17:16] IDLEST	Idle status
BB2D	Master/Slave	CM_DSS_BB2D_CLKCTRL[18] STBYST	Standby status
		CM_DSS_BB2D_CLKCTRL[17:16] IDLEST	Idle status

Table 3.15. CD_DSS Modules Slave Clock-Management Modes and Control

Module	Disabled	Auto	Enabled	Control Bit Field	Access Type
DSS	Available	N/A	Available	CM_DSS_DSS_CLKCTRL[1:0] MODULEMODE	Read/Write
BB2D	Available	N/A	Available	CM_DSS_BB2D_CLKCTRL[1:0] MODULEMODE	Read/Write

3.6.14. CD_L4_CFG Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.15. CD_L3_INSTR Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.16. CD_L3_2 Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.17. CD_L3_1 Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.18. CD_EMIF Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.19. CD_CORTEXM3 Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.20. CD_DMA Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.21. CD_C2C Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.22. CD_CAM Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.23. CD_ABE Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.6.24. CD_L4_ALWON_CORE Clock Domain

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7. Power Management Functional Description

3.7.1. PD_WKUP Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.2. PD_DSP Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.3. PD_STD_EFUSE Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.4. PD_MPU Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.5. PD_L4_PER Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.6. PD_L3_INIT Description

The FSUSB module is removed from the subsection as follows:

Table 3.16. PD_L3_INIT Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
CM1_USB	No	None	None
....	.....	......	.....
USBPHY	No	RM_L3INIT_USBPHY _CONTEXT[0] LOST CONTEXT_DFF	None
~~FSUSB~~	~~Full~~	~~None~~	~~RM_L3INIT_USB_HO ST_FS_CONTEXT[1] LOSTCONTEXT_RFF~~
HSUSBHOST	Full	None	RM_L3INIT_USB_HO ST_CONTEXT[1] LO STCONTEXT_RFF
....	.....	......	.....
HSUSBTLL	Full	None	RM_L3INIT_HSUS-BTLL_CONTEXT[1] LOSTCONTEXT_RFF

3.7.7. PD_IVAHD Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.8. PD_SGX Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.9. PD_EMU Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.10. PD_DSS Description

The BB2D module is added in the subsection as follows:

Table 3.17. PD_DSS Modules Power Attributes

Module	Logic Retention	DFF Context Status	RFF Context Status
DSS	Partial	RM_DSS_DSS_CONTEXT[0] LOSTCONTEXT_DFF	RM_DSS_DSS_CONTEXT[1] LOSTCONTEXT_RFF
BB2D	No	RM_DSS_BB2D_CONTEXT[0] LOSTCONTEXT_DFF	N/A

Table 3.18. PD_DSS Memory Area Power Modes

Memory Bank	Module - Memory	Logic On	Logic Retention	Logic Off	RTA Feature
DSS_MEM		ON	OFF	OFF	
	DSS - DSSMEM	always_on	always_off		always_enabled
BB2D_MEM		ON	OFF	OFF	
	BB2D - BB2D_MEM	always_on	always_off		always_enabled

3.7.11. PD_CORE Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.12. PD_CAM Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.13. PD_AUDIO Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.14. PD_ALWON_MPU Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.15. PD_ALWON_DSP Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.7.16. PD_ALWON_CORE Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.8. Voltage Management Functional Description

3.8.1. Overview

The CORE voltage domain (VDD_CORE_L) does not support **OPP100** in its first set of OPPs.

The PRCM module supports the AVS technique on the VDD_MPU_L, VDD_CORE_L and VDD_IVA_L voltage domains, through automatic monitoring and adjustments of voltages by their dedicated SmartReflex modules. The VDD_MPU_L and VDD_IVA_L voltage domains support five DVFS OPPs.
The VDD_CORE_L voltage domain supports ~~three~~ two sets of DVFS OPPs. First VDD_CORE_L set has two OPPs (OPP50 and OPP119), second set has three OPPs (OPP50, OPP100 and OPP119) and is used in legacy mode (for old software com-

patability). The device can not switch dynamically between these two sets of OPPs. The difference between the two sets (except the number of OPPs supported) is in the frequency that correspond to each OPP.

The PRCM module automatically scales down the LDO_MPU_M, LDO_CORE_M, and LDO_IVA_M to retention voltage level whenever all memory banks on these domain have transitioned to the RETENTION or OFF power state.

Table 3.19. Supported DVFS OPPs Summary

Voltage Domain	Operating Point	Control
IVDD_MPU_L (vdd_mpu)	OFF	Hardware and software
	RETENTION	
	OPP50	
	OPP100	
	OPP_TURBO	
	OPP_NITRO	
	OPP_NITROSB	
VDD_IVA_L (vdd_iva)	OFF	Hardware and software
	RETENTION	
	OPP50	
	OPP100	
	OPP_TURBO	
	OPP_NITRO	
	OPP_NITROSB	
VDD_CORE_L (vdd)	OFF	Hardware and software
	RETENTION	
	OPP50	
	OPP100[1]	
	OPP119	

1. VDD_CORE_L OPP100 is available only for second set of OPPs.

3.8.2. Voltage-Control Architecture

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.8.3. VDD_MPU_L, VDD_CORE_L, and VDD_IVA_L Control

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.8.4. Internal LDOs Control

The ABB strategy for Cortex-A9 MPU operating at OPP_TURBO is updated.

If(CONTROL_STD_FUSE_OPP_DPLL_1[20] MPU_RBB_TURBO == 1) **then** enable ABB Set2 at OPP_TURBO (PRM_LDO_ABB_MPU_SETUP[1] ACTIVE_RBB_SEL = 0x1) ~~Else if (CONTROL_STD_FUSE_OPP_DPLL_1[19:18] MPU_DPLL_TRIM_FREQ = 0x1 or 0x3 then enable ABB Set1 at OPP_TURBO (PRM_LDO_ABB_MPU_SETUP[2] ACTIVE_FBB_SEL = 0x1)~~ **Else** no ABB is available for OPP_TURBO.

3.8.5. Voltage Domain State Transitions

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.8.6. DVFS

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.9. Device Low-Power States

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.10. PRCM Module Programming Guide

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11. PRCM Register Manual

3.11.1. PRM Instance Summary

Table 3.20. PRM Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_PRM	0x4A30 6000	256Bytes
CKGEN_PRM	0x4A30 6100	256Bytes
MPU_PRM	0x4A30 6300	256Bytes
DSP_PRM	0x4A30 6400	256Bytes
ABE_PRM	0x4A30 6500	256Bytes
ALWAYS_ON_PRM	0x4A30 6600	256Bytes
CORE_PRM	0x4A30 6700	2KBytes
IVAHD_PRM	0x4A30 6F00	256Bytes
CAM_PRM	0x4A30 7000	256Bytes
DSS_PRM	0x4A30 7100	256Bytes
SGX_PRM	0x4A30 7200	256Bytes
L3INIT_PRM	0x4A30 7300	256Bytes
L4PER_PRM	0x4A30 7400	512Bytes
WKUP_PRM	0x4A30 7700	256Bytes
WKUP_CM	0x4A30 7800	256Bytes
EMU_PRM	0x4A30 7900	256Bytes
EMU_CM	0x4A30 7A00	256Bytes
DEVICE_PRM	0x4A30 7B00	256Bytes
INSTR_PRM	0x4A30 7F00	256Bytes

3.11.2. INTRCONN_SOCKET_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.3. CKGEN_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.4. MPU_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.5. DSP_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.6. ABE_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.7. ALWAYS_ON_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.8. CORE_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.9. IVAHD_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.10. CAM_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.11. DSS_PRM Registers

3.11.11.1. DSS_PRM Register Summary

Table 3.21. DSS_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_PRM L4 Base Address
PM_DSS_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7100
PM_DSS_PWRSTST	R	32	0x0000 0004	0x4A30 7104
PM_DSS_DSS_WKDEP	RW	32	0x0000 0020	0x4A30 7120
RM_DSS_DSS_CONTEXT	RW	32	0x0000 0024	0x4A30 7124
RM_DSS_BB2D_CONTEXT	RW	32	0x0000 002C	0x4A30 712C

3.11.11.2. DSS_PRM Register Description

Note

This section contains only modified registers.

Table 3.22. RM_DSS_BB2D_CONTEXT

Address Offset	0x0000 002C		
Physical Address	0x4A30 712C	**Instance**	DSS_PRM
Description	This register contains dedicated BB2D context statuses. [warm reset insensitive]		
Type	RW		

31–9	8	7–1	0
RESERVED	LOSTMEM_BB2D_MEM	RESERVED	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:9	RESERVED		R	0x00000
8	LOSTMEM_BB2D_MEM	Specify if memory-based context in BB2D_MEM memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W 1toClr	1
7:1	RESERVED		R	0x00
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of DSS_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W 1toClr	1

Table 3.23. Register Call Summary for Register RM_DSS_BB2D_CONTEXT

Power Management Functional Description

- PD_DSS Description:[0]

PRCM Register Manual

- DSS_PRM Register Summary:[1]

3.11.12. SGX_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.13. L3INIT_PRM Registers

3.11.13.1. L3INIT_PRM Register Summary

Table 3.24. L3INIT_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_PRM L4 Base Address
PM_L3INIT_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7300
PM_L3INIT_PWRSTST	R	32	0x0000 0004	0x4A30 7304
PM_L3INIT_MMC1_WKDEP	RW	32	0x0000 0028	0x4A30 7328
RM_L3INIT_MMC1_CONTEXT	RW	32	0x0000 002C	0x4A30 732C

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_PRM L 4 Base Address
PM_L3INIT_MMC2_W KDEP	RW	32	0x0000 0030	0x4A30 7330
RM_L3INIT_MMC2_C ONTEXT	RW	32	0x0000 0034	0x4A30 7334
PM_L3INIT_HSI_WK DEP	RW	32	0x0000 0038	0x4A30 7338
RM_L3INIT_HSI_CO NTEXT	RW	32	0x0000 003C	0x4A30 733C
RESERVED	RW	32	0x0000 0040	0x4A30 7340
RESERVED	RW	32	0x0000 0044	0x4A30 7344
PM_L3INIT_HSUS-BHOST_WKDEP	RW	32	0x0000 0058	0x4A30 7358
RM_L3INIT_HSUS-BHOST_CONTEXT	RW	32	0x0000 005C	0x4A30 735C
PM_L3INIT_HSUS-BOTG_WKDEP	RW	32	0x0000 0060	0x4A30 7360
RM_L3INIT_HSUS-BOTG_CONTEXT	RW	32	0x0000 0064	0x4A30 7364
PM_L3INIT_HSUS-BTLL_WKDEP	RW	32	0x0000 0068	0x4A30 7368
RM_L3INIT_HSUS-BTLL_CONTEXT	RW	32	0x0000 006C	0x4A30 736C
RESERVED	RW	32	0x0000 007C	0x4A30 737C
RESERVED	RW	32	0x0000 0084	0x4A30 7384
RESERVED	RW	32	0x0000 0088	0x4A30 7388
RESERVED	RW	32	0x0000 008C	0x4A30 738C
RESERVED	RW	32	0x0000 0094	0x4A30 7394
RESERVED	RW	32	0x0000 0098	0x4A30 7398
RESERVED	RW	32	0x0000 009C	0x4A30 739C
RESERVED	RW	32	0x0000 00AC	0x4A30 73AC
RESERVED	R	32	0x0000 00C0	0x4A30 73C0
RESERVED	RW	32	0x0000 00C4	0x4A30 73C4
RESERVED	RW	32	0x0000 00C8	0x4A30 73C8
RESERVED	RW	32	0x0000 00CC	0x4A30 73CC
~~PM_L3INIT_FSUSB_WKDEP~~RESERVED	RW	32	0x0000 00D0	0x4A30 73D0
~~RM_L3INIT_FSUSB_CONTEXT~~RESERVED	RW	32	0x0000 00D4	0x4A30 73D4
RM_L3INIT_USBPHY _CONTEXT	RW	32	0x0000 00E4	0x4A30 73E4

3.11.13.2. L3INIT_PRM Register Description

The PM_L3INIT_FSUSB_WKDEP and RM_L3INIT_FSUSB_CONTEXT registers are removed from the subsection.

3.11.14. L4PER_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.15. WKUP_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.16. WKUP_CM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.17. EMU_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.18. EMU_CM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.19. DEVICE_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.20. INSTR_PRM Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.21. CM1 Instance Summary

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.22. INTRCONN_SOCKET_CM1 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.23. CKGEN_CM1 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.24. MPU_CM1 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.25. DSP_CM1 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.26. ABE_CM1 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.27. RESTORE_CM1 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.28. INSTR_CM1 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.29. CM2 Instance Summary

Table 3.25. CM2 Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_CM2	0x4A00 8000	256Bytes
CKGEN_CM2	0x4A00 8100	256Bytes
ALWAYS_ON_CM2	0x4A00 8600	256Bytes
CORE_CM2	0x4A00 8700	2KBytes
IVAHD_CM2	0x4A00 8F00	256Bytes
CAM_CM2	0x4A00 9000	256Bytes
DSS_CM2	0x4A00 9100	256Bytes
SGX_CM2	0x4A00 9200	256Bytes
L3INIT_CM2	0x4A00 9300	256Bytes
L4PER_CM2	0x4A00 9400	512Bytes
RESTORE_CM2	0x4A00 9E00	256Bytes
INSTR_CM2	0x4A00 9F00	256Bytes

3.11.30. INTRCONN_SOCKET_CM2 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.31. CKGEN_CM2 Registers

3.11.31.1. CKGEN_CM2 Register Summary

Table 3.26. CKGEN_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM2 L4 Base Address
CM_CLKSEL_MPU_M3_ISS_ROOT	R~~W~~	32	0x0000 0000	0x4A00 8100
CM_CLKSEL_USB_60MHZ	RW	32	0x0000 0004	0x4A00 8104
CM_SCALE_FCLK	RW	32	0x0000 0020	0x4A00 8108
CM_CORE_DVFS_PERF1	RW	32	0x0000 0024	0x4A00 8110
....	....	....	....	....

3.11.31.2. CKGEN_CM2 Register Description

Note

This section contains only modified registers.

Table 3.27. CM_CLKSEL_MPU_M3_ISS_ROOT

Address Offset	0x0000 0000		
Physical Address	0x4A00 8100	**Instance**	CKGEN_CM2
Description	MPU_M3/ISS root clock~~selection~~status(MPU_M3_ISS_CLK).		
Type	R~~W~~		

31–1	0
RESERVED	CLKSEL

Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x00000
0	CLKSEL	~~Select the source for~~This bit gives the status ofthe root clock of MPU_M3/ISS Read0x0: Root clock is sourced from CORE_CLK ~~0x1: Functional clock is sourced from DPLL_PER~~	R~~W~~	0

Table 3.28. Register Call Summary for Register CM_CLKSEL_MPU_M3_ISS_ROOT

PRCM Register Manual

- CKGEN_CM2 Register Summary:[0]

3.11.32. ALWAYS_ON_CM2 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.33. CORE_CM2 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.34. IVAHD_CM2 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.35. CAM_CM2 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.36. DSS_CM2 Registers

3.11.36.1. DSS_CM2 Register Summary

Table 3.29. DSS_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_CM2 L4 Base Address
CM_DSS_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9100
CM_DSS_STATICDEP	RW	32	0x0000 0004	0x4A00 9104
CM_DSS_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9108
CM_DSS_DSS_CLKCTRL	RW	32	0x0000 0020	0x4A00 9120
CM_DSS_BB2D_CLKCTRL	RW	32	0x0000 0028	0x4A00 9128

3.11.36.2. DSS_CM2 Register Description

Note

This section contains only modified registers.

Table 3.30. CM_DSS_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	0x4A00 9100	**Instance**	DSS_CM2
Description	This register enables the DSS domain power state transition. It controls the hardware supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also holds 1 status bit per clock input of the domain.		
Type	RW		

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12	11	10	9	8	7 6 5 4 3 2	1 0
RESERVED	~~RESERVED~~ CLKACTIVITY_BB2D_FCLK	CLKACTIVITY_HDMI_PHY_48M_FCLK	CLKACTIVITY_DSS_ALWON_SYS_CLK	CLKACTIVITY_DSS_FCLK	CLKACTIVITY_DSS_L3_ICLK	RESERVED	CLKTRCTRL

Bits	Field Name	Description	Type	Reset
31:~~12~~13	RESERVED		R	0x00000
12	CLKACTIVITY_BB2D_FCLK	This field indicates the state of the BB2D_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gati ng/ungating transition is ongoing	R	0
11	CLKACTIVITY_HD-MI_PHY_48M_FCLK	This field indicates the state of the HDMI_PHY_4 8MHz_FCLK clock in the domain. [warm reset i nsensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gati ng/ungating transition is ongoing	R	0
10	CLKACTIVITY_DSS_AL-WON_SYS_CLK	This field indicates the state of the DSS_ALWON_SYS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gati ng/ungating transition is ongoing	R	0
9	CLKACTIVITY_DSS_FCLK	This field indicates the state of the DSS_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gati ng/ungating transition is ongoing	R	0
8	CLKACTIVITY_DSS_L3_I CLK		R	0

Bits	Field Name	Description	Type	Reset
		This field indicates the state of the DSS_L3_ICLK (and DSS_L4_ICLK) clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gati ng/ungating transition is ongoing		
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the DSS clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. 0x1: SW_SLEEP: Start a software forced sleep tra nsition on the domain. 0x2: SW_WKUP: Start a software forced wake-up transition on the domain. 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hard-ware conditions.	RW	3

Table 3.31. Register Call Summary for Register CM_DSS_CLKSTCTRL

Clock Management Functional Description

- CD_DSS Clock Domain:[0][1][2][3][4][5]

PRCM Register Manual

- DSS_CM2 Register Summary:[6]

Table 3.32. CM_DSS_STATICDEP

Address Offset	0x0000 0004		
Physical Address	0x4A00 9104	**Instance**	DSS_CM2
Description	This register controls the static domain depedencies from DSS domain towards 'target' domains. It is relevant only for domain having system initiator(s).		
Type	RW		

Bits	31–7	6	5	4	3	2	1	0
Field	RESERVED	L3_2_STATDEP	L3_1_STATDEP	MEMIF_STATDEP	RESERVED	IVAHD_STATDEP	RESERVED	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x00000
6	L3_2_STATDEP	Static dependency towards L3_2 clock domain ~~0x0: Dependency is disabled~~ Read0x1: Dependency is enabled	RWRreturns1s	01
5	L3_1_STATDEP	Static dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
4	MEMIF_STATDEP	Static dependency towards MEMIF clock domain 0x0: Dependency is disabled	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: Dependency is enabled		
3	RESERVED		R	0
2	IVAHD_STATDEP	Static dependency towards IVAHD clock domain 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1:0	RESERVED		R	0x0

Table 3.33. Register Call Summary for Register CM_DSS_STATICDEP

Clock Management Functional Description

- CD_DSS Clock Domain:[0][1][2][3]

PRCM Register Manual

- DSS_CM2 Register Summary:[4]

Table 3.34. CM_DSS_DYNAMICDEP

Address Offset	0x0000 0008		
Physical Address	0x4A00 9108	**Instance**	DSS_CM2
Description	This register controls the dynamic domain depedencies from DSS domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	R		

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7	6	5	4 3 2 1 0
RESERVED	RESERVED- L3_2_DYNDEP	L3_1_DYNDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:67	RESERVED		R	0x00000
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 domain Read 0x0: Dependency is disabled	R	0
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 domain Read 0x0: Dependency is disabled	R	0
4:0	RESERVED		R	0x0

Table 3.35. Register Call Summary for Register CM_DSS_DYNAMICDEP

Clock Management Functional Description

- CD_DSS Clock Domain:[0][1]

PRCM Register Manual

- DSS_CM2 Register Summary:[2]

Table 3.36. CM_DSS_DSS_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9120	**Instance**	DSS_CM2
Description	This register manages the DSS clocks.		
Type	RW		

31 30 29 28 27 26 25 24 23 22 21 20 19	18	17 16	15 14 13 12	11	10	9	8	7 6 5 4 3 2	1 0
RESERVED	STBYST	IDLEST	RESERVED	OPTFCLKEN_TV_CLK RESERVED	OPTFCLKEN_SYS_CLK	OPTFCLKEN_48MHZ_CLK	OPTFCLKEN_DSSCLK	RESERVED	MODULEMODE

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18	STBYST	Module standby status. [warm reset insensitive] Read 0x1: Module is in standby Read 0x0: Module is functional (not in standby)	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x3: Module is disabled and cannot be acces sed Read 0x2: Module is in Idle mode (only OCP part). It is functional if using separate functional clock Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x0: Module is fully functional, including OCP	R	0x3
15:~~12~~11	RESERVED		R	0x0
~~11~~	~~OPTFCLKEN_TV_CLK~~	~~Optional functional clock control.~~ ~~0x0: Optional functional clock is disabled~~ ~~0x1: Optional functional clock is enabled~~	~~RW~~	~~0~~
10	OPTFCLKEN_SYS_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
9	OPTFCLKEN_48MHZ_CLK	Optional functional clock control. 0x0: Optional functional clock is disabled	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: Optional functional clock is enabled		
8	OPTFCLKEN_DSSCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any OCP access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x3: Reserved Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen.	RW	0x0

Table 3.37. Register Call Summary for Register CM_DSS_DSS_CLKCTRL

Clock Management Functional Description

- CD_DSS Clock Domain:[0][1][2]

PRCM Register Manual

- DSS_CM2 Register Summary:[3]

Table 3.38. CM_DSS_BB2D_CLKCTRL

Address Offset	0x0000 0028		
Physical Address	0x4A00 9128	**Instance**	DSS_CM2
Description	This register manages the BB2D clocks.		
Type	RW		

31 30 29 28 27 26 25	24	23 22 21 20 19	18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
RESERVED	CLKSEL_BB2D_FCLK	RESERVED	STBYST	IDLEST	RESERVED	MODULEMODE

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL_BB2D_FCLK	Select the source of BB2D_FCLK 0x0: Functional clock is sourced from DPLL_CORE 0x1: Functional clock is sourced from DPLL_PER	RW	1

Bits	Field Name	Description	Type	Reset
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be acces sed	R	0x3
15:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition cannot happen. Read 0x3: Reserved	RW	0

Table 3.39. Register Call Summary for Register CM_DSS_BB2D_CLKCTRL

Clock Management Functional Description

- CM2 Clock Generator:[0]
- CD_DSS Clock Domain:[1][2][3]

PRCM Register Manual

- DSS_CM2 Register Summary:[4]

3.11.37. SGX_CM2 Registers

3.11.37.1. SGX_CM2 Register Summary

Table 3.40. SGX_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SGX_CM2 L4 Base Address
CM_SGX_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9200
CM_SGX_STATICDEP	RW	32	0x0000 0004	0x4A00 9204
CM_SGX_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9208
CM_SGX_SGX_CLKCTRL	RW	32	0x0000 0020	0x4A00 9220

3.11.37.2. SGX_CM2 Register Description

Note

This section contains only modified registers.

Table 3.41. CM_SGX_SGX_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	0x4A00 9220	**Instance**	SGX_CM2
Description	This register manages the SGX clocks.		
Type	RW		

31 30 29 28 27 26 25	24	23 22 21 20 19	18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2	1 0
RESERVED	CLKSEL_SGX_FCLK	RESERVED	STBYST	IDLEST	RESERVED	MODULEMODE

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL_SGX_FCLK	~~Select the source of the SGX_FCLK~~This bit gives s tatus of the SGX_FCLK source. ~~0x0: Functional clock is sourced from DPLL_CORE HSDIVIDER~~ Read0x1: Functional clock is sourced from DP LL_PER HSDIVIDER	RW	~~0~~1
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including IN-TRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be acces sed	R	0x3
15:2	RESERVED		R	0x00
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by software. Any IN-TRCONN access to module results in an er-ror, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition can-not happen. Read 0x3: Reserved	RW	0

Table 3.42. Register Call Summary for Register CM_SGX_SGX_CLKCTRL

PRCM Register Manual

- SGX_CM2 Register Summary:[0]

3.11.38. L3INIT_CM2 Registers

3.11.38.1. L3INIT_CM2 Register Summary

Table 3.43. L3INIT_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	L3INIT_CM2 L4 Base Address
CM_L3INIT_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 9300
CM_L3INIT_STATICDEP	RW	32	0x0000 0004	0x4A00 9304
CM_L3INIT_DYNAMICDEP	R	32	0x0000 0008	0x4A00 9308
CM_L3INIT_HSMMC1_CLKCTRL	RW	32	0x0000 0028	0x4A00 9328
CM_L3INIT_HSMMC2_CLKCTRL	RW	32	0x0000 0030	0x4A00 9330
CM_L3INIT_HSI_CLKCTRL	RW	32	0x0000 0038	0x4A00 9338
RESERVED	RW	32	0x0000 0040	0x4A00 9340
CM_L3INIT_HSUSBHOST_CLKCTRL	RW	32	0x0000 0058	0x4A00 9358
CM_L3INIT_HSUSBHOST_CLKCTRL	RW	32	0x0000 0060	0x4A00 9360
CM_L3INIT_HSUSBTLL_CLKCTRL	RW	32	0x0000 0068	0x4A00 9368
RESERVED	R	32	0x0000 0078	0x4A00 9378
RESERVED	RW	32	0x0000 0080	0x4A00 9380
RESERVED	RW	32	0x0000 0088	0x4A00 9388
RESERVED	RW	32	0x0000 0090	0x4A00 9390
RESERVED	RW	32	0x0000 0098	0x4A00 9398
RESERVED	RW	32	0x0000 00A8	0x4A00 93A8
RESERVED	RW	32	0x0000 00C0	0x4A00 93C0
RESERVED	RW	32	0x0000 00C8	0x4A00 93C8
~~CM_L3INIT_FSUSB_CLKCTRL~~RESERVED	~~RW~~	32	0x0000 00D0	0x4A00 93D0
CM_L3INIT_USBPHY_CLKCTRL	RW	32	0x0000 00E0	0x4A00 93E0

3.11.38.2. L3INIT_CM2 Register Description

The CM_L3INIT_FSUSB_CLKCTRL register is removed from the subsection.

3.11.39. L4PER_CM2 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.11.40. RESTORE_CM2 Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.12. SCRM Register Manual

Refer to OMAP4470 Silicon Revision 1.0 TRM.

3.13. SR Register Manual

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 4. Dual Cortex-A9 MPU Subsystem

This chapter describes differences in Dual Cortex-A9 MPU Subsystem between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 5. DSP Subsystem

This chapter describes differences in the DSP Subsystem between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 6. IVA-HD Subsystem

This chapter describes the differences in the IVA-HD subsystem between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM

Chapter 7. Dual Cortex-M3 MPU Subsystem

This chapter describes the differences in the Dual Cortex-M3 MPU Subsystem between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM

Chapter 8. Imaging Subsystem

This chapter describes the differences in the Imaging Subsystem between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

8.1. ISS Overview

- ISS pixel throughput incresed from 200 to 233 MPix/s.
- ISS_FCLK increased to 233 MHz.

Note

The above functional change is applicable only when the VDD_CORE_L voltage domain is defined for the first supported set of OPPs.

8.2. ISS Interfaces

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.3. ISS ISP

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4. ISS Still Image Coprocessor

8.4.1. ISS SIMCOP Overview

The clock frequency of ISS_FCLK, the functional clock of ISS SIMCOP module, has been increased. This change affects the following registers:

- SIMCOP_HL_HWINFO

8.4.1.1. ISS SIMCOP Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.1.2. ISS SIMCOP Functional Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.1.3. ISS SIMCOP Programming Models

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.1.4. ISS SIMCOP Register Manual

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.1.4.1. SIMCOP Instance Summary

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.1.4.2. SIMCOP Registers

8.4.1.4.2.1. SIMCOP Register Summary

Table 8.1. SIMCOP _CONTROL Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
SIMCOP_HL_REVISION	R	32	0x0000 0000	0x5202 0000	0x5506 0000
SIMCOP_HL_HWINFO	R	32	0x0000 0004	0x5202 0004	0x5506 0004
SIMCOP_HL_SYSCONFIG	RW	32	0x0000 0010	0x5202 0010	0x5506 0010
RESERVED	R	32	0x0000 001C	0x5202 001C	0x5506 001C
SIMCOP_HL_IRQSTATUS_RAW_i[1]	RW	32	0x0000 0020 + (0x10 * i)	0x5202 0020 + (0x10 * i)	0x5506 0020 + (0x10 * i)
SIMCOP_HL_IRQSTATUS_i[1]	RW	32	0x0000 0024 + (0x10 * i)	0x5202 0024 + (0x10 * i)	0x5506 0024 + (0x10 * i)
SIMCOP_HL_IRQENABLE_SET_i[1]	RW	32	0x0000 0028 + (0x10 * i)	0x5202 0028 + (0x10 * i)	0x5506 0028 + (0x10 * i)
SIMCOP_HL_IRQENABLE_CLR_i[1]	RW	32	0x0000 002C + (0x10 * i)	0x5202 002C + (0x10 * i)	0x5506 002C + (0x10 * i)
SIMCOP_CTRL	RW	32	0x0000 0060	0x5202 0060	0x5506 0060
SIMCOP_CLKCTRL	RW	32	0x0000 0064	0x5202 0064	0x5506 0064

1. i = 0 to 3

8.4.1.4.2.2. SIMCOP_CONTROL Register Descriptions

Note

This section contains only modified registers.

Table 8.2. SIMCOP_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5202 0004 0x5506 0004	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description			
Type	RW		

31:15	14	13	12:10	9:8	7	6	5	4	3	2	1	0
RESERVED	LDCIMXNSF_BOOST	RY22_LDCMEM	LDCR_RESP_FIFO	IMAGE_BUFFERS	RESERVED	ROT_A_ENABLE	IMX_B_ENABLE	IMX_A_ENABLE	NSF_ENABLE	VLCDJ_ENABLE	DCT_ENABLE	LDC_ENABLE

Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Read returns 0.	R	0x00000
14	LDCIMXNSF_BOOST	Read 0x1: SIMCOP receives a~~400~~466MHz clock. Some modules receive the~~400~~466Mhz clock and others receive~~400~~466/2 =~~200~~233Mhz Read 0x0: SIMCOP receives a~~200~~233MHz clock driving all sub-modules	R	0x1
13	RY22_LDCMEM		R	0x0

Bits	Field Name	Description	Type	Reset
		Chooses the LDC working memory configuration Read 0x1: Working memory only populated for YUV420 operation A: 1024x32 B: 1024x32 C: 1024x16 D: 1024x16 Read 0x0: Working memory fully populated. Supports YUV422 operation. A: 512x32 B: 512x32 C: 1024x16 D: 1024x16 E: 512x32 F: 512x32 G: 1024x16 H: 1024x16		
12:10	LDCR_RESP_FIFO	Defines the size of the LDC read master response FIFO in words of 128-bits. Read 0x2: 8x128 bits Read 0x3: 16x128 bits Read 0x4: 32x128 bits Read 0x5: 64x128 bits Read 0x6: 128x128 bits Read 0x7: 256x256 bits	R	0x4
9:8	IMAGE_BUFFERS	This parameter defines the image buffer count. Read 0x0: 4 Image buffers (e, f, g, h) Read 0x1: 8 Image buffers	R	0x1
7	RESERVED	Read returns 0.	R	0
6	ROT_A_ENABLE	The ROT a is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
5	IMX_B_ENABLE	The iMX B module and the CMD b, COEFF b memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
4	IMX_A_ENABLE	The iMX A module and the CMD a, COEFF a memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
3	NSF_ENABLE	The NSF2 is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
2	VLCDJ_ENABLE	The VLCD module and the QUANT, HUFFMAN, BITSTREAM memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
1	DCT_ENABLE	The DCT module is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
0	LDC_ENABLE	The LDC module and the LDC LUT are present w hen this parameter is set. Read 0x0: Disabled at design time	R	1

Bits	Field Name	Description	Type	Reset
		Read 0x1: Enabled at design time		

8.4.1.5. ISS SIMCOP Memory Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.2. ISS SIMCOP Hardware Sequencer and Buffers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.3. ISS SIMCOP DMA Module

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.4. ISS SIMCOP LDC Module

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.5. ISS SIMCOP Discrete Cosine Transform Module

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.6. ISS SIMCOP Variable Length Coder/Decoder for JPEG Module

Refer to OMAP4470 Silicon Revision 1.0 TRM.

8.4.7. ISS SIMCOP Rotation Accelerator Module

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 9. Face Detect

This chapter describes the differences in the Face Detect between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM

Chapter 10. Display Subsystem

This chapter describes the differences in the Display Subsystem between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

10.1. Display Subsystem Overview

The Video Encoder (VENC) and Video DAC (VDAC) modules are removed from OMAP4470 device.

Resolution of up to 2048x1536 can be supported on dual DSI interface, through DSI1 and DSI2 linked simultaneously to a single external bridge.

The DSS_L3_ICLK interface clock on L3 interconnect can go up to 233 MHz (for OPP119) and up to 116.5 MHz (for OPP50), when the VDD_CORE_L voltage domain is defined for the first supported set of OPPs.

10.2. Display Controller

10.2.1. Display Controller Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

The following new features associated with the DISPC DMA engine are added:

- Support for immediate flip of the base address (GFX, VID1, VID2 and VID3 pipelines)
- Support for MFLAG mechanism (dynamic increase of the priority of real time data traffic)

10.2.2. Display Controller Environment

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.3. Display Controller Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4. Display Controller Functional Description

10.2.4.1. Clock configuration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.2. Software Reset

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.3. Power Management

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.4. Interrupt Requests

New FLIPIMMEDIATEDONE_IRQ is added, associated with the immediate base address flip mechanism. The following registers are affected:

- DISPC_IRQSTATUS
- DISPC_IRQENABLE

10.2.4.5. sDMA Requests

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.6. DMA Engine

10.2.4.6.1. Addressing and Bursts

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.6.2. Immediate Base Address Flip Mechanism

New section, describing the immediate base address flip mechanism associated with the GFX, VID1, VID2 and VID3 pipelines.

The following new register is added:

- DISPC_BA0_FLIPIMMEDIATE_EN

10.2.4.6.3. DMA Buffers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.6.4. MFLAG Mechanism and Arbitration

New section, describing the MFLAG mechanism for dynamic increase of the priority of real time data traffic for the GFX, VID1, VID2, VID3 and WB pipelines.

The following new registers are added:

- DISPC_GLOBAL_MFLAG_ATTRIBUTE
- DISPC_GFX_MFLAG_THRESHOLD__1
- DISPC_VID1_MFLAG_THRESHOLD
- DISPC_VID2_MFLAG_THRESHOLD__1
- DISPC_VID3_MFLAG_THRESHOLD__1
- DISPC_WB_MFLAG_THRESHOLD

10.2.4.6.5. Predecimation

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.6.6. Progressive-to-Interlaced Format Conversion

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.6.7. Arbitration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.6.8. DMA Power Modes

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.7. Rotation and Mirroring

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.8. Memory Format

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.9. Graphics Pipeline

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.10. Video Pipelines

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.11. Write-back Pipeline

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.12. LCD Outputs

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.4.13. TV Output

Due to the removal of VENC and VDAC modules, the DISPC TV output is connected only to the HDMI module and DPI parallel interface.

10.2.4.14. Shadow Registers

Information on the new registers associated with Immediate Base Address Flip Mechanism and MFLAG Mechanism is added.

10.2.5. Display Controller Register Manual

10.2.5.1. Display Controller Instance Summary

Table 10.1. DISPC Instance Summary

Module Name	L4_PER Base Address	L3 Base Address	Size
DISPC	0x4804 1000	0x5800 1000	4KB

10.2.5.2. Display Controller Logical Register Mapping

Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.2.5.3. Display Controller Registers

10.2.5.3.1. Display Controller Register Summary

Table 10.2. Display Controller Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_REVISION	R	32	0x0000 0000	0x4804 1000	0x5800 1000
DISPC_SYSCONFIG	RW	32	0x0000 0010	0x4804 1010	0x5800 1010
DISPC_SYSSTATUS	R	32	0x0000 0014	0x4804 1014	0x5800 1014
DISPC_IRQSTATUS	RW	32	0x0000 0018	0x4804 1018	0x5800 1018
DISPC_IRQENABLE	RW	32	0x0000 001C	0x4804 101C	0x5800 101C
DISPC_CONTROL1	RW	32	0x0000 0040	0x4804 1040	0x5800 1040
DISPC_CONFIG1	RW	32	0x0000 0044	0x4804 1044	0x5800 1044
RESERVED	R	32	0x0000 0048	0x4804 1048	0x5800 1048
DISPC_DEFAULT_COLOR0	RW	32	0x0000 004C	0x4804 104C	0x5800 104C
DISPC_DEFAULT_COLOR1	RW	32	0x0000 0050	0x4804 1050	0x5800 1050
DISPC_TRANS_COLOR0	RW	32	0x0000 0054	0x4804 1054	0x5800 1054
DISPC_TRANS_COLOR1	RW	32	0x0000 0058	0x4804 1058	0x5800 1058
DISPC_LINE_STATUS	R	32	0x0000 005C	0x4804 105C	0x5800 105C
DISPC_LINE_NUMBER	RW	32	0x0000 0060	0x4804 1060	0x5800 1060

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_TIMING_H1	RW	32	0x0000 0064	0x4804 1064	0x5800 1064
DISPC_TIMING_V1	RW	32	0x0000 0068	0x4804 1068	0x5800 1068
DISPC_POL_FREQ1	RW	32	0x0000 006C	0x4804 106C	0x5800 106C
DISPC_DIVISOR1	RW	32	0x0000 0070	0x4804 1070	0x5800 1070
DISPC_GLOBAL_ALPHA	RW	32	0x0000 0074	0x4804 1074	0x5800 1074
DISPC_SIZE_TV	RW	32	0x0000 0078	0x4804 1078	0x5800 1078
DISPC_SIZE_LCD1	RW	32	0x0000 007C	0x4804 107C	0x5800 107C
DISPC_GFX_BA_j[1]	RW	32	0x0000 0080 + (0x4 * j)	0x4804 1080 + (0x4 * j)	0x5800 1080 + (0x4 * j)
DISPC_GFX_POSITION	RW	32	0x0000 0088	0x4804 1088	0x5800 1088
DISPC_GFX_SIZE	RW	32	0x0000 008C	0x4804 108C	0x5800 108C
DISPC_GFX_ATTRIBUTES	RW	32	0x0000 00A0	0x4804 10A0	0x5800 10A0
DISPC_GFX_BUF_THRESHOLD	RW	32	0x0000 00A4	0x4804 10A4	0x5800 10A4
DISPC_GFX_BUF_SIZE_STATUS	R	32	0x0000 00A8	0x4804 10A8	0x5800 10A8
DISPC_GFX_ROW_INC	RW	32	0x0000 00AC	0x4804 10AC	0x5800 10AC
DISPC_GFX_PIXEL_INC	RW	32	0x0000 00B0	0x4804 10B0	0x5800 10B0
DISPC_GFX_WINDOW_SKIP	R	32	0x0000 00B4	0x4804 10B4	0x5800 10B4
DISPC_GFX_TABLE_BA	RW	32	0x0000 00B8	0x4804 10B8	0x5800 10B8
DISPC_VID1_BA_j[1]	RW	32	0x0000 00BC + (0x4 * j)	0x4804 10BC + (0x4 * j)	0x5800 10BC + (0x4 * j)
DISPC_VID1_POSITION	RW	32	0x0000 00C4	0x4804 10C4	0x5800 10C4
DISPC_VID1_SIZE	RW	32	0x0000 00C8	0x4804 10C8	0x5800 10C8
DISPC_VID1_ATTRIBUTES	RW	32	0x0000 00CC	0x4804 10CC	0x5800 10CC
DISPC_VID1_BUF_THRESHOLD	RW	32	0x0000 00D0	0x4804 10D0	0x5800 10D0
DISPC_VID1_BUF_SIZE_STATUS	R	32	0x0000 00D4	0x4804 10D4	0x5800 10D4
DISPC_VID1_ROW_INC	RW	32	0x0000 00D8	0x4804 10D8	0x5800 10D8
DISPC_VID1_PIXEL_INC	RW	32	0x0000 00DC	0x4804 10DC	0x5800 10DC
DISPC_VID1_FIR	RW	32	0x0000 00E0	0x4804 10E0	0x5800 10E0
DISPC_VID1_PICTURE_SIZE	RW	32	0x0000 00E4	0x4804 10E4	0x5800 10E4
DISPC_VID1_ACCU_j[1]	RW	32	0x0000 00E8 + (0x4 * j)	0x4804 10E8 + (0x4 * j)	0x5800 10E8 + (0x4 * j)
DISPC_VID1_FIR_COEF_H_i[2]	RW	32	0x0000 00F0 + (0x8 * i)	0x4804 10F0 + (0x8 * i)	0x5800 10F0 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV_i[2]	RW	32	0x0000 00F4 + (0x8 * i)	0x4804 10F4 + (0x8 * i)	0x5800 10F4 + (0x8 * i)
DISPC_VID1_CONV_COEF0	RW	32	0x0000 0130	0x4804 1130	0x5800 1130
DISPC_VID1_CONV_COEF1	RW	32	0x0000 0134	0x4804 1134	0x5800 1134
DISPC_VID1_CONV_COEF2	RW	32	0x0000 0138	0x4804 1138	0x5800 1138
DISPC_VID1_CONV_COEF3	RW	32	0x0000 013C	0x4804 113C	0x5800 113C
DISPC_VID1_CONV_COEF4	RW	32	0x0000 0140	0x4804 1140	0x5800 1140
DISPC_VID2_BA_j[1]	RW	32	0x0000 014C + (0x4 * j)	0x4804 114C + (0x4 * j)	0x5800 114C + (0x4 * j)
DISPC_VID2_POSITION	RW	32	0x0000 0154	0x4804 1154	0x5800 1154
DISPC_VID2_SIZE	RW	32	0x0000 0158	0x4804 1158	0x5800 1158
DISPC_VID2_ATTRIBUTES	RW	32	0x0000 015C	0x4804 115C	0x5800 115C
DISPC_VID2_BUF_THRESHOLD	RW	32	0x0000 0160	0x4804 1160	0x5800 1160
DISPC_VID2_BUF_SIZE_STATUS	R	32	0x0000 0164	0x4804 1164	0x5800 1164
DISPC_VID2_ROW_INC	RW	32	0x0000 0168	0x4804 1168	0x5800 1168
DISPC_VID2_PIXEL_INC	RW	32	0x0000 016C	0x4804 116C	0x5800 116C
DISPC_VID2_FIR	RW	32	0x0000 0170	0x4804 1170	0x5800 1170

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_VID2_PICTURE_SIZE	RW	32	0x0000 0174	0x4804 1174	0x5800 1174
DISPC_VID2_ACCU_j[1]	RW	32	0x0000 0178 + (0x4 * j)	0x4804 1178 + (0x4 * j)	0x5800 1178 + (0x4 * j)
DISPC_VID2_FIR_COEF_H_i[2]	RW	32	0x0000 0180 + (0x8 * i)	0x4804 1180 + (0x8 * i)	0x5800 1180 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV_i[2]	RW	32	0x0000 0184 + (0x8 * i)	0x4804 1184 + (0x8 * i)	0x5800 1184 + (0x8 * i)
DISPC_VID2_CONV_COEF0	RW	32	0x0000 01C0	0x4804 11C0	0x5800 11C0
DISPC_VID2_CONV_COEF1	RW	32	0x0000 01C4	0x4804 11C4	0x5800 11C4
DISPC_VID2_CONV_COEF2	RW	32	0x0000 01C8	0x4804 11C8	0x5800 11C8
DISPC_VID2_CONV_COEF3	RW	32	0x0000 01CC	0x4804 11CC	0x5800 11CC
DISPC_VID2_CONV_COEF4	RW	32	0x0000 01D0	0x4804 11D0	0x5800 11D0
DISPC_DATA1_CYCLE1	RW	32	0x0000 01D4	0x4804 11D4	0x5800 11D4
DISPC_DATA1_CYCLE2	RW	32	0x0000 01D8	0x4804 11D8	0x5800 11D8
DISPC_DATA1_CYCLE3	RW	32	0x0000 01DC	0x4804 11DC	0x5800 11DC
DISPC_VID1_FIR_COEF_V_i[2]	RW	32	0x0000 01E0 + (0x4 * i)	0x4804 11E0 + (0x4 * i)	0x5800 11E0 + (0x4 * i)
DISPC_VID2_FIR_COEF_V_i[2]	RW	32	0x0000 0200 + (0x4 * i)	0x4804 1200 + (0x4 * i)	0x5800 1200 + (0x4 * i)
DISPC_CPR1_COEF_R	RW	32	0x0000 0220	0x4804 1220	0x5800 1220
DISPC_CPR1_COEF_G	RW	32	0x0000 0224	0x4804 1224	0x5800 1224
DISPC_CPR1_COEF_B	RW	32	0x0000 0228	0x4804 1228	0x5800 1228
DISPC_GFX_PRELOAD	RW	32	0x0000 022C	0x4804 122C	0x5800 122C
DISPC_VID1_PRELOAD	RW	32	0x0000 0230	0x4804 1230	0x5800 1230
DISPC_VID2_PRELOAD	RW	32	0x0000 0234	0x4804 1234	0x5800 1234
DISPC_CONTROL2	RW	32	0x0000 0238	0x4804 1238	0x5800 1238
DISPC_VID3_ACCU_j[1]	RW	32	0x0000 0300 + (0x4 * j)	0x4804 1300 + (0x4 * j)	0x5800 1300 + (0x4 * j)
DISPC_VID3_BA_j[1]	RW	32	0x0000 0308 + (0x4 * j)	0x4804 1308 + (0x4 * j)	0x5800 1308 + (0x4 * j)
DISPC_VID3_FIR_COEF_H_i[2]	RW	32	0x0000 0310 + (0x8 * i)	0x4804 1310 + (0x8 * i)	0x5800 1310 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV_i[2]	RW	32	0x0000 0314 + (0x8 * i)	0x4804 1314 + (0x8 * i)	0x5800 1314 + (0x8 * i)
DISPC_VID3_FIR_COEF_V_i[2]	RW	32	0x0000 0350 + (0x4 * i)	0x4804 1350 + (0x4 * i)	0x5800 1350 + (0x4 * i)
DISPC_VID3_ATTRIBUTES	RW	32	0x0000 0370	0x4804 1370	0x5800 1370
DISPC_VID3_CONV_COEF0	RW	32	0x0000 0374	0x4804 1374	0x5800 1374
DISPC_VID3_CONV_COEF1	RW	32	0x0000 0378	0x4804 1378	0x5800 1378
DISPC_VID3_CONV_COEF2	RW	32	0x0000 037C	0x4804 137C	0x5800 137C
DISPC_VID3_CONV_COEF3	RW	32	0x0000 0380	0x4804 1380	0x5800 1380
DISPC_VID3_CONV_COEF4	RW	32	0x0000 0384	0x4804 1384	0x5800 1384
DISPC_VID3_BUF_SIZE_STATUS	R	32	0x0000 0388	0x4804 1388	0x5800 1388
DISPC_VID3_BUF_THRESHOLD	RW	32	0x0000 038C	0x4804 138C	0x5800 138C
DISPC_VID3_FIR	RW	32	0x0000 0390	0x4804 1390	0x5800 1390
DISPC_VID3_PICTURE_SIZE	RW	32	0x0000 0394	0x4804 1394	0x5800 1394
DISPC_VID3_PIXEL_INC	RW	32	0x0000 0398	0x4804 1398	0x5800 1398
DISPC_VID3_POSITION	RW	32	0x0000 039C	0x4804 139C	0x5800 139C
DISPC_VID3_PRELOAD	RW	32	0x0000 03A0	0x4804 13A0	0x5800 13A0
DISPC_VID3_ROW_INC	RW	32	0x0000 03A4	0x4804 13A4	0x5800 13A4
DISPC_VID3_SIZE	RW	32	0x0000 03A8	0x4804 13A8	0x5800 13A8

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_DEFAULT_COLOR2	RW	32	0x0000 03AC	0x4804 13AC	0x5800 13AC
DISPC_TRANS_COLOR2	RW	32	0x0000 03B0	0x4804 13B0	0x5800 13B0
DISPC_CPR2_COEF_B	RW	32	0x0000 03B4	0x4804 13B4	0x5800 13B4
DISPC_CPR2_COEF_G	RW	32	0x0000 03B8	0x4804 13B8	0x5800 13B8
DISPC_CPR2_COEF_R	RW	32	0x0000 03BC	0x4804 13BC	0x5800 13BC
DISPC_DATA2_CYCLE1	RW	32	0x0000 03C0	0x4804 13C0	0x5800 13C0
DISPC_DATA2_CYCLE2	RW	32	0x0000 03C4	0x4804 13C4	0x5800 13C4
DISPC_DATA2_CYCLE3	RW	32	0x0000 03C8	0x4804 13C8	0x5800 13C8
DISPC_SIZE_LCD2	RW	32	0x0000 03CC	0x4804 13CC	0x5800 13CC
DISPC_TIMING_H2	RW	32	0x0000 0400	0x4804 1400	0x5800 1400
DISPC_TIMING_V2	RW	32	0x0000 0404	0x4804 1404	0x5800 1404
DISPC_POL_FREQ2	RW	32	0x0000 0408	0x4804 1408	0x5800 1408
DISPC_DIVISOR2	RW	32	0x0000 040C	0x4804 140C	0x5800 140C
DISPC_WB_ACCU_j[1]	RW	32	0x0000 0500 + (0x4 * j)	0x4804 1500 + (0x4 * j)	0x5800 1500 + (0x4 * j)
DISPC_WB_BA_j[1]	RW	32	0x0000 0508 + (0x4 * j)	0x4804 1508 + (0x4 * j)	0x5800 1508 + (0x4 * j)
DISPC_WB_FIR_COEF_H_i[2]	RW	32	0x0000 0510 + (0x8 * i)	0x4804 1510 + (0x8 * i)	0x5800 1510 + (0x8 * i)
DISPC_WB_FIR_COEF_HV_i[2]	RW	32	0x0000 0514 + (0x8 * i)	0x4804 1514 + (0x8 * i)	0x5800 1514 + (0x8 * i)
DISPC_WB_FIR_COEF_V_i[2]	RW	32	0x0000 0550 + (0x4 * i)	0x4804 1550 + (0x4 * i)	0x5800 1550 + (0x4 * i)
DISPC_WB_ATTRIBUTES	RW	32	0x0000 0570	0x4804 1570	0x5800 1570
DISPC_WB_CONV_COEF0	RW	32	0x0000 0574	0x4804 1574	0x5800 1574
DISPC_WB_CONV_COEF1	RW	32	0x0000 0578	0x4804 1578	0x5800 1578
DISPC_WB_CONV_COEF2	RW	32	0x0000 057C	0x4804 157C	0x5800 157C
DISPC_WB_CONV_COEF3	RW	32	0x0000 0580	0x4804 1580	0x5800 1580
DISPC_WB_CONV_COEF4	RW	32	0x0000 0584	0x4804 1584	0x5800 1584
DISPC_WB_BUF_SIZE_STATUS	R	32	0x0000 0588	0x4804 1588	0x5800 1588
DISPC_WB_BUF_THRESHOLD	RW	32	0x0000 058C	0x4804 158C	0x5800 158C
DISPC_WB_FIR	RW	32	0x0000 0590	0x4804 1590	0x5800 1590
DISPC_WB_PICTURE_SIZE	RW	32	0x0000 0594	0x4804 1594	0x5800 1594
DISPC_WB_PIXEL_INC	RW	32	0x0000 0598	0x4804 1598	0x5800 1598
DISPC_WB_ROW_INC	RW	32	0x0000 05A4	0x4804 15A4	0x5800 15A4
DISPC_WB_SIZE	RW	32	0x0000 05A8	0x4804 15A8	0x5800 15A8
DISPC_VID1_BA_UV_j[1]	RW	32	0x0000 0600 + (0x4 * j)	0x4804 1600 + (0x4 * j)	0x5800 1600 + (0x4 * j)
DISPC_VID2_BA_UV_j[1]	RW	32	0x0000 0608 + (0x4 * j)	0x4804 1608 + (0x4 * j)	0x5800 1608 + (0x4 * j)
DISPC_VID3_BA_UV_j[1]	RW	32	0x0000 0610 + (0x4 * j)	0x4804 1610 + (0x4 * j)	0x5800 1610 + (0x4 * j)
DISPC_WB_BA_UV_j[1]	RW	32	0x0000 0618 + (0x4 * j)	0x4804 1618 + (0x4 * j)	0x5800 1618 + (0x4 * j)
DISPC_CONFIG2	RW	32	0x0000 0620	0x4804 1620	0x5800 1620
DISPC_VID1_ATTRIBUTES2	RW	32	0x0000 0624	0x4804 1624	0x5800 1624
DISPC_VID2_ATTRIBUTES2	RW	32	0x0000 0628	0x4804 1628	0x5800 1628
DISPC_VID3_ATTRIBUTES2	RW	32	0x0000 062C	0x4804 162C	0x5800 162C
DISPC_GAMMA_TABLE0	W	32	0x0000 0630	0x4804 1630	0x5800 1630
DISPC_GAMMA_TABLE1	W	32	0x0000 0634	0x4804 1634	0x5800 1634

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_GAMMA_TABLE2	W	32	0x0000 0638	0x4804 1638	0x5800 1638
DISPC_VID1_FIR2	RW	32	0x0000 063C	0x4804 163C	0x5800 163C
DISPC_VID1_ACCU2_j[1]	RW	32	0x0000 0640 + (0x4 * j)	0x4804 1640 + (0x4 * j)	0x5800 1640 + (0x4 * j)
DISPC_VID1_FIR_COEF_H2_i[2]	RW	32	0x0000 0648 + (0x8 * i)	0x4804 1648 + (0x8 * i)	0x5800 1648 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV2_i[2]	RW	32	0x0000 064C + (0x8 * i)	0x4804 164C + (0x8 * i)	0x5800 164C + (0x8 * i)
DISPC_VID1_FIR_COEF_V2_i[2]	RW	32	0x0000 0688 + (0x4 * i)	0x4804 1688 + (0x4 * i)	0x5800 1688 + (0x4 * i)
DISPC_VID2_FIR2	RW	32	0x0000 06A8	0x4804 16A8	0x5800 16A8
DISPC_VID2_ACCU2_j[1]	RW	32	0x0000 06AC + (0x4 * j)	0x4804 16AC + (0x4 * j)	0x5800 16AC + (0x4 * j)
DISPC_VID2_FIR_COEF_H2_i[2]	RW	32	0x0000 06B4 + (0x8 * i)	0x4804 16B4 + (0x8 * i)	0x5800 16B4 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV2_i[2]	RW	32	0x0000 06B8 + (0x8 * i)	0x4804 16B8 + (0x8 * i)	0x5800 16B8 + (0x8 * i)
DISPC_VID2_FIR_COEF_V2_i[2]	RW	32	0x0000 06F4 + (0x4 * i)	0x4804 16F4 + (0x4 * i)	0x5800 16F4 + (0x4 * i)
DISPC_VID3_FIR2	RW	32	0x0000 0724	0x4804 1724	0x5800 1724
DISPC_VID3_ACCU2_j[1]	RW	32	0x0000 0728 + (0x4 * j)	0x4804 1728 + (0x4 * j)	0x5800 1728 + (0x4 * j)
DISPC_VID3_FIR_COEF_H2_i[2]	RW	32	0x0000 0730 + (0x8 * i)	0x4804 1730 + (0x8 * i)	0x5800 1730 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV2_i[2]	RW	32	0x0000 0734 + (0x8 * i)	0x4804 1734 + (0x8 * i)	0x5800 1734 + (0x8 * i)
DISPC_VID3_FIR_COEF_V2_i[2]	RW	32	0x0000 0770 + (0x4 * i)	0x4804 1770 + (0x4 * i)	0x5800 1770 + (0x4 * i)
DISPC_WB_FIR2	RW	32	0x0000 0790	0x4804 1790	0x5800 1790
DISPC_WB_ACCU2_j[1]	RW	32	0x0000 0794 + (0x4 * j)	0x4804 1794 + (0x4 * j)	0x5800 1794 + (0x4 * j)
DISPC_WB_FIR_COEF_H2_i[2]	RW	32	0x0000 07A0 + (0x8 * i)	0x4804 17A0 + (0x8 * i)	0x5800 17A0 + (0x8 * i)
DISPC_WB_FIR_COEF_HV2_i[2]	RW	32	0x0000 07A4 + (0x8 * i)	0x4804 17A4 + (0x8 * i)	0x5800 17A4 + (0x8 * i)
DISPC_WB_FIR_COEF_V2_i[2]	RW	32	0x0000 07E0 + (0x4 * i)	0x4804 17E0 + (0x4 * i)	0x5800 17E0 + (0x4 * i)
DISPC_GLOBAL_BUFFER	RW	32	0x0000 0800	0x4804 1800	0x5800 1800
DISPC_DIVISOR	RW	32	0x0000 0804	0x4804 1804	0x5800 1804
DISPC_WB_ATTRIBUTES2	RW	32	0x0000 0810	0x4804 1810	0x5800 1810
DISPC_BA0_FLIPIMMEDIATE_EN	RW	32	0x0000 0854	0x4804 1854	0x5800 1854
DISPC_GLOBAL_MFLAG_ATTRIBUTE	RW	32	0x0000 085C	0x4804 185C	0x5800 185C
DISPC_GFX_MFLAG_THRESHOLD__1	RW	32	0x0000 0860	0x4804 1860	0x5800 1860
DISPC_VID1_MFLAG_THRESHOLD	RW	32	0x0000 0864	0x4804 1864	0x5800 1864
DISPC_VID2_MFLAG_THRESHOLD__1	RW	32	0x0000 0868	0x4804 1868	0x5800 1868
DISPC_VID3_MFLAG_THRESHOLD__1	RW	32	0x0000 086C	0x4804 186C	0x5800 186C
DISPC_WB_MFLAG_THRESHOLD	RW	32	0x0000 0870	0x4804 1870	0x5800 1870

1. j = 0 to 1
2. i = 0 to 7

10.2.5.3.2. Display Controller Register Description

Note

This section contains only modified registers.

Table 10.3. DISPC_IRQSTATUS

Address Offset	0x0000 0018
Physical Address	Please refer to Table 10.2
Description	This register regroups all the status of the module internal events that generate an interrupt. Write 1 to a given bit resets this bit
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FLIPIMMEDIATEDONE_IRQ	RESERVED				WBUNCOMPLETEERROR_IRQ	WBBUFFEROVERFLOW_IRQ	FRAMEDONETV_IRQ	FRAMEDONEWB_IRQ	FRAMEDONE2_IRQ	ACBIASCOUNTSTATUS2_IRQ	VID3BUFFERUNDERFLOW_IRQ	VID3ENDWINDOW_IRQ	VSYNC2_IRQ	SYNCLOST2_IRQ	WAKEUP_IRQ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYNCLOSTTV_IRQ	SYNCLOST1_IRQ	VID2ENDWINDOW_IRQ	VID2BUFFERUNDERFLOW_IRQ	VID1ENDWINDOW_IRQ	VID1BUFFERUNDERFLOW_IRQ	OCPERROR_IRQ	PALETTEGAMMALOADING_IRQ	GFXENDWINDOW_IRQ	GFXBUFFERUNDERFLOW_IRQ	PROGRAMMEDLINENUMBER_IRQ	ACBIASCOUNTSTATUS1_IRQ	EVSYNC_ODD_IRQ	EVSYNC_EVEN_IRQ	VSYNC1_IRQ	FRAMEDONE1_IRQ

Bits	Field Name	Description	Type	Reset
31	FLIPIMMEDIATEDONE_IRQ	Flip Immediate Done. The DMA engine has acknowledged the immediate BA change, and software can write the new BA0. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
30:27	RESERVED		R	0x0
26	WBUNCOMPLETEERROR_IRQ	Write-back DMA buffer is flushed before it is completely drained. In WB capture mode, if the new frame starts before the WB DMA buffers are fully drained (onto external memory), then the contents of the WB DMA buffers are lost (implying last few pixels/lines are corrupted in the captured frame in memory). This interrupt is an indication of that case and will trigger every frame. 0x0: READS: Event is false. 0x0: WRITES: Status bit unchanged. 0x1: READS: Event is true (Pending). 0x1: WRITES: Status bit is reset	RW W1toClr	0
25	WBBUFFEROVERFLOW_IRQ	Write-back DMA Buffer Overrflow. The DMA buffer is full. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W1toClr	0
24	FRAMEDONETV_IRQ	Frame Done for the TV. The TV output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending).	RW W1toClr	0

Bits	Field Name	Description	Type	Reset
		WRITES: Status bit is reset.		
23	FRAMEDONEWB_IRQ	Frame Done for the write-back channel. The write-back channel has output the frame. All the data of the frame have been sent to the memory.There is no pending data inside the DMA engine for the write-back channel to be transfered to memory. It is available only when the write-back pipeline transfers back to memory the output of one of the pipelines. In case of overlay capture, the interrupt is not generated and the user shall use the Frame-Done for the corresponding captured output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
22	FRAMEDONE2_IRQ	Frame Done for the secondary LCD. The secondary LCD output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
21	ACBIAS-COUNTSTATUS2_IRQ	AC Bias Count Status for the secondary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
20	VID3BUFFERUNDERFLOW_IRQ	Video#3 DMA Buffer Underflow. The DMA buffer is not necessarly empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
19	VID3ENDWINDOW_IRQ	The end of the video#3 Window has been reached. It is detected by the overlay manager when the full video#3 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
18	VSYNC2_IRQ	Vertical Synchronization for the secondary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
17	SYNCLOST2_IRQ	Synchronization Lost on the secondary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the secondary LCD output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
16	WAKEUP_IRQ	Wake-up 0x0: READS: Event is false. WRITES: Status bit unchanged.	RW W 1toClr	0

Bits	Field Name	Description	Type	Reset
		0x1: READS: Event is true (pending). WRITES: Status bit is reset.		
15	SYNCLOSTTV_IRQ	Synchronization Lost on the TV output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the TV output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
14	SYNCLOST1_IRQ	Synchronization Lost on the primary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the primary LCD output. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
13	VID2ENDWINDOW_IRQ	The end of the video#2 Window has been reached. It is detected by the overlay manager when the full video#2 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
12	VID2BUFFERUNDERFLOW_IRQ	Video#2 DMA Buffer Underflow. The DMA buffer is not necessarly empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
11	VID1ENDWINDOW_IRQ	The end of the video#1 Window has been reached. It is detected by the overlay manager when the full video#1 has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
10	VID1BUFFERUNDERFLOW_IRQ	Video#1 DMA Buffer Underflow. The DMA buffer is not necessarly empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
9	OCPERROR_IRQ	OCP Error. L3 Inteconnect has sent SResp=ERR. It can be due to security violation. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
8	PALETTEGAMMALOADING_IRQ	Palette Gamma Loading status. The palette used as Color Look Up Table (CLUT) for the graphics BITMAP formats (1-, 2-, 4-, or 4-bpp) or as gamme	RW W 1toClr	0

Bits	Field Name	Description	Type	Reset
		table for the overlay output for the primary LCD output has been loaded succesfully. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.		
7	GFXENDWINDOW_IRQ	The end of the graphics Window has been reached. It is detected by the overlay manager when the full graphics has been displayed. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
6	GFXBUFFERUNDER-FLOW_IRQ	Graphics DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order res-ponses) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
5	PROGRAMMEDLINENU MBER_IRQ	Programmed Line Number. It indicates that the scan of the primary LCD has reached the progra mmed user line number. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
4	ACBIAS-COUNTSTATUS1_IRQ	AC Bias Count Status for the primary LCD 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
3	EVSYNC_ODD_IRQ	VSYNC for odd field from the TV encoder (HDMI) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
2	EVSYNC_EVEN_IRQ	VSYNC for even field from the TV encoder (HDMI) 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
1	VSYNC1_IRQ	Vertical Synchronization for the primary LCD. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0
0	FRAMEDONE1_IRQ	Frame Done for the primary LCD. The primary LCD output has been disabled by user. All the data have been sent. 0x0: READS: Event is false. WRITES: Status bit unchanged. 0x1: READS: Event is true (pending). WRITES: Status bit is reset.	RW W 1toClr	0

Table 10.4. Register Call Summary for Register DISPC_IRQSTATUS

Display Controller Functional Description

- Interrupt Requests:[0]

Table 10.5. DISPC_IRQENABLE

Address Offset	0x0000 001C
Physical Address	Please refer toTable 10.2
Description	This register allows to mask/unmask the module internal sources of interrupt, on an event-by-event basis
Type	RW

31	30	29	28	27	26	25	24
FLIPIMMEDIATEDONE_EN	RESERVED				WBUNCOMPLETEERROR_EN	WBBUFFEROVERFLOW_EN	FRAMEDONETV_EN

23	22	21	20	19	18	17	16
FRAMEDONEWB_EN	FRAMEDONE2_EN	ACBIASCOUNTSTATUS2_EN	VID3BUFFERUNDERFLOW_EN	VID3ENDWINDOW_EN	VSYNC2_EN	SYNCLOST2_EN	WAKEUP_EN

15	14	13	12	11	10	9	8
SYNCLOSTTV_EN	SYNCLOST1_EN	VID2ENDWINDOW_EN	VID2BUFFERUNDERFLOW_EN	ENDVID1WINDOW_EN	VID1BUFFERUNDERFLOW_EN	OCPERROR_EN	PALETTEGAMMA_EN

7	6	5	4	3	2	1	0
GFXENDWINDOW_EN	GFXBUFFERUNDERFLOW_EN	PROGRAMMEDLINENUMBER_EN	ACBIASCOUNTSTATUS1_EN	EVSYNC_ODD_EN	EVSYNC_EVEN_EN	VSYNC1_EN	FRAMEDONE_EN

Bits	Field Name	Description	Type	Reset
31	FLIPIMMEDIATEDONE_EN	Flip Immediate Done. The DMA engine has acknowledged the immediate BA change, and software can write the new BA0. 0x0: Flip Immediate Done is masked 0x1: Flip Immediate Done generates an interrupt when it occurs	RW	0
30:27	RESERVED	Write 0s for future compatibility. Reads returns 0	R	0x0
26	WBUNCOMPLETEERROR_EN	The write back buffer has been flushed before been fully drained. Enable. 0x0: Interrupt is masked. 0x1: Interrupt is enabled.	RW	0
25	WBBUFFEROVERFLOW_EN	Write-back DMA Buffer Overflow. The DMA buffer is full 0x0: WBBufferOverflow is masked 0x1: WBBufferOverflow generates an interrupt whe n it occurs	RW	0
24	FRAMEDONETV_EN	Frame Done for the TV. The TV output has been disabled by user. All the data have been sent. 0x0: Frame Done for the TV output is masked 0x1: Frame Done for the TV output generates an interrupt when it occurs	RW	0
23	FRAMEDONEWB_EN	Frame Done for the write-back channel. The write-back channel has output the frame. All the data have been sent for the frame have been sent to the memory. There is no pending data inside the DMA engine for the write-back channel to be transferred to memory. 0x0: Frame Done for the write-back is masked 0x1: Frame Done for the write-back generates an interrupt when it occurs	RW	0
22	FRAMEDONE2_EN		RW	0

Bits	Field Name	Description	Type	Reset
		Frame Done for the secondary LCD. The secondary LCD output has been disabled by user. All the data have been sent. 0x0: Frame Done for the secondary LCD is masked 0x1: Frame Done for the secondary LCD generates an interrupt when it occurs		
21	ACBIAS-COUNTSTATUS2_EN	AC Bias Count Status for the secondary LCD 0x0: ACBiasCountStatus for the secondary LCD output is masked 0x1: ACBiasCountStatus for the secondary LCD output generates an interrupt when it occurs	RW	0
20	VID3BUFFERUNDERFLOW_EN	Video#3 DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid3BufferUnderflow is masked 0x1: Vid3BufferUnderflow generates an interrupt when it occurs	RW	0
19	VID3ENDWINDOW_EN	The end of the video#3 Window has been reached. It is detected by the overlay manager when the full video#3 has been displayed. 0x0: Vid3EndWindow is masked 0x1: Vid3EndWindow generates an interrupt when it occurs	RW	0
18	VSYNC2_EN	Vertical Synchronization for the secondary LCD 0x0: VSYNC for the secondary LCD output is m asked 0x1: VSYNC for the secondary LCD output generates an interrupt when it occurs	RW	0
17	SYNCLOST2_EN	Synchronization Lost on the secondary LCD output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the secondary LCD output. 0x0: Synchronization Lost on the secondary LCD output is masked 0x1: Synchronization Lost on the secondary LCD output generates an interrupt when it occurs	RW	0
16	WAKEUP_EN	Wake Up Mask 0x0: WakeUp is masked 0x1: WakeUp generates an interrupt when it occurs	RW	0
15	SYNCLOSTTV_EN	Synchronization Lost on the TV output. The required data are not output at the correct time due to too short blanking periods or stall of at least one pipelines associated with the TV output. 0x0: Synchronization Lost on the TV output is ma sked 0x1: Synchronization Lost on the TV output generates an interrupt when it occurs	RW	0
14	SYNCLOST1_EN	Synchronization Lost for the primary LCD 0x0: SyncLost for the primary LCD output is mask ed 0x1: SyncLost for the primary LCD output generates an interrupt when it occurs	RW	0
13	VID2ENDWINDOW_EN	The end of the video#2 Window has been reached. It is detected by the overlay manager when the full video#2 has been displayed.	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Vid2EndWindow is masked 0x1: Vid2EndWindow generates an interrupt when it occurs		
12	VID2BUFFERUNDERFLOW_EN	Video#2 DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid2BufferUnderflow is masked 0x1: Vid2BufferUnderflow generates an interrupt when it occurs	RW	0
11	ENDVID1WINDOW_EN	The end of the video#1 Window has been reached. It is detected by the overlay manager when the full video#1 has been displayed. 0x0: EndVid1Window is masked 0x1: EndVid1Window generates an interrupt when it occurs	RW	0
10	VID1BUFFERUNDERFLOW_EN	Video#1 DMA Buffer Underflow. The DMA buffer is not necessary empty but required data are not present in the DMA buffer (due to out of order responses) 0x0: Vid1BufferUnderflow is masked 0x1: Vid1BufferUnderflow generates an interrupt when it occurs	RW	0
9	OCPERROR_EN	OCP Error. L3 Inteconnect has sent SResp=ERR. It can be due to security violation. 0x0: OCPError is masked 0x1: OCPError generates an interrupt when it occurs	RW	0
8	PALETTEGAMMA_EN	Palette Gamma Loading mask. The palette used as Color Look Up Table (CLUT) for the graphics BITMAP formats (1-, 2-, 4-, or 4-bpp) or as gamme table for the overlay output for the primary LCD output has been loaded succesfully. 0x0: PaletteGamma is masked 0x1: PaletteGamma generates an interrupt when it occurs	RW	0
7	GFXENDWINDOW_EN	The end of the graphics Window has been reached. It is detected by the overlay manager when the full graphics has been displayed. 0x0: GfxEndWindow is masked 0x1: GfxEndWindow generates an interrupt when it occurs	RW	0
6	GFXBUFFERUNDER-FLOW_EN	Graphics DMA Buffer Underflow. The DMA buffer is not necessarly empty but required data are not present in the DMA buffer (due to out of order res-ponses) 0x0: GfxBufferUnderflow is masked 0x1: GfxBufferUnderflow generates an interrupt when it occurs	RW	0
5	PROGRAMMEDLINENUMBER_EN	Programmed Line Number. It indicates that the scan of the primary LCD has reached the progra mmed user line number. 0x0: ProgrammedLineNumber is masked 0x1: ProgrammedLineNumber generates an interrupt when it occurs	RW	0

Bits	Field Name	Description	Type	Reset
4	ACBIAS-COUNTSTATUS1_EN	AC Bias Count Status for the primary LCD 0x0: ACBiasCountStatus for the primary LCD output is masked 0x1: ACBiasCountStatus for the primary LCD output generates an interrupt when it occurs	RW	0
3	EVSYNC_ODD_EN	VSYNC for odd field from the TV encoder (HDMI) 0x0: EVSYNC_ODD for the TV output is masked 0x1: EVSYNC_ODD for the TV output generates an interrupt when it occurs	RW	0
2	EVSYNC_EVEN_EN	VSYNC for even field from the TV encoder (HDMI) 0x0: EVSYNC_EVEN for the TV output is masked 0x1: EVSYNC_EVEN for the TV output generates an interrupt when it occurs	RW	0
1	VSYNC1_EN	Vertical Synchronization for the primary LCD. 0x0: VSYNC for the primary LCD output is masked 0x1: VSYNC for the primary LCD output generates an interrupt when it occurs	RW	0
0	FRAMEDONE_EN	Frame Done for the primary LCD. The primary LCD output has been disabled by user. All the data have been sent. 0x0: FrameDone for the primary LCD output is masked 0x1: FrameDone for the primary LCD output generates an interrupt when it occurs	RW	0

Table 10.6. Register Call Summary for Register DISPC_IRQENABLE

Display Controller Functional Description

- Interrupt Requests:[0]

Table 10.7. DISPC_BA0_FLIPIMMEDIATE_EN

Address Offset	0x0000 0854
Physical Address	Please refer toTable 10.2
Description	Indicates for individual pipeline when a new BA is written into BA0 register.
Type	RW

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4	3	2	1	0
RESERVED	VID3_IMMEDIATE_EN	VID2_IMMEDIATE_EN	VID1_IMMEDIATE_EN	GFX_IMMEDIATE_EN

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x000 0000

Bits	Field Name	Description	Type	Reset
3	VID3_IMMEDIATE_EN	Indicates when there is a new BA for video3 pipeline. HW resets it when the new BA0 can be modified by SW. 0x1: New BA is available inside BA0 Read 0x0: HW resets it to 0 to indicate that BA0 can be modified by SW.	RW	0
2	VID2_IMMEDIATE_EN	Indicates when there is a new BA for video2 pipeline. HW resets it when the new BA0 can be modified by SW. 0x1: New BA is available inside BA0 Read 0x0: HW resets it to 0 to indicate that BA0 can be modified by SW.	RW	0
1	VID1_IMMEDIATE_EN	Indicates when there is a new BA for video1 pipeline. HW resets it when the new BA0 can be modified by SW. 0x1: New BA is available inside BA0 Read 0x0: HW resets it to 0 to indicate that BA0 can be modified by SW.	RW	0
0	GFX_IMMEDIATE_EN	Indicates when there is a new BA for Gfx pipeline. HW resets it when the new BA0 can be modified by SW. 0x1: New BA is available inside BA0 Read 0x0: HW resets it to 0 to indicate that BA0 can be modified by SW.	RW	0

Table 10.8. Register Call Summary for Register DISPC_BA0_FLIPIMMEDIATE_EN

Display Controller Functional Description

- Immediate Base Address Flip Mechanism:[0]

Table 10.9. DISPC_GLOBAL_MFLAG_ATTRIBUTE

Address Offset	0x0000 085C
Physical Address	Please refer toTable 10.2
Description	Controls the MFLAG out of band signal generation.
Type	RW

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3	2	1 0
RESERVED				MFLAG_START	MFLAG_CTRL

Bits	Field Name	Description	Type	Reset
31:3	RESERVED		R	0x0000 0000

Bits	Field Name	Description	Type	Reset
2	MFLAG_START	MFLAG Start 0x0: When the DMA buffer is empty at the beginning of the frame, MFLAG signal of each pipeline is kept at 0 until PRELOAD is reached, then based on MFLAG_CTRL bitfield MFLAG is generated and internal logic is arbitrating between pipeline requests 0x1: Even at the beginning of the frame when the DMA buffer is empty, MFLAG_CTRL bitfield is used to determine how MFLAG signal for each pipeline shall be driven.	RW	0
1:0	MFLAG_CTRL	MFLAG control 0x0: MFLAG mechanism is disabled: MFLAG out of band signal is set to 0 0x1: MFLAG mechanism is enabled: MFLAG out o f band signal is always set to 1 (force mode for deb ug) 0x2: MFLAG mechanism is enabled and MFLAG out of band signal is dynamically set and reset depending on MFLAG rules.	RW	0x0

Table 10.10. Register Call Summary for Register DISPC_GLOBAL_MFLAG_ATTRIBUTE

Display Controller Functional Description

- MFLAG Mechanism and Arbitration:[0]

Table 10.11. DISPC_GFX_MFLAG_THRESHOLD__1

Address Offset	0x0000 0860
Physical Address	Please refer toTable 10.2
Description	MFLAG thresholds for graphics pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	Graphics High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MF LAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Graphics Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10.12. Register Call Summary for Register DISPC_GFX_MFLAG_THRESHOLD__1

Display Controller Functional Description

- MFLAG Mechanism and Arbitration:[0]

Table 10.13. DISPC_VID1_MFLAG_THRESHOLD

Address Offset	0x0000 0864
Physical Address	Please refer toTable 10.2
Description	MFLAG thresholds for video1 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	Video1 High Thresholds (in 128bits) for MFLAG ge neration: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Video1 Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10.14. Register Call Summary for Register DISPC_VID1_MFLAG_THRESHOLD

Display Controller Functional Description

- MFLAG Mechanism and Arbitration:[0]

Table 10.15. DISPC_VID2_MFLAG_THRESHOLD__1

Address Offset	0x0000 0868
Physical Address	Please refer toTable 10.2
Description	MFLAG thresholds for video2 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HT_MFLAG																LT_MFLAG															

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	Video2 High Thresholds (in 128bits) for MFLAG ge neration: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Video2 Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10.16. Register Call Summary for Register DISPC_VID2_MFLAG_THRESHOLD__1

Display Controller Functional Description

- MFLAG Mechanism and Arbitration:[0]

Table 10.17. DISPC_VID3_MFLAG_THRESHOLD__1

Address Offset	0x0000 086C
Physical Address	Please refer to Table 10.2
Description	MFLAG thresholds for video3 pipeline. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or external VSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory.
Type	RW

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
HT_MFLAG	LT_MFLAG

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	Video3 High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MFLAG level, MFLAG is reset to 0	RW	0x0000
15:0	LT_MFLAG	Video3 Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is set to 1	RW	0x0000

Table 10.18. Register Call Summary for Register DISPC_VID3_MFLAG_THRESHOLD__1

Display Controller Functional Description

- MFLAG Mechanism and Arbitration:[0]

Table 10.19. DISPC_WB_MFLAG_THRESHOLD

Address Offset	0x0000 0870
Physical Address	Please refer to Table 10.2
Description	MFLAG thresholds for write-back pipeline. Shadow register, updated when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline), when the WB pipeline is directly connected to one of the pipelines (graphics or video). Otherwise, updated on VFP start period of primary LCD or VFP start period of secondary LCD or external VSYNC, depending on which overlay output is selected as an input to the WB pipeline.
Type	RW

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
HT_MFLAG	LT_MFLAG

Bits	Field Name	Description	Type	Reset
31:16	HT_MFLAG	Write-back High Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches HT_MFLA G level, MFLAG is set to 1	RW	0x0000
15:0	LT_MFLAG	Write-back Low Thresholds (in 128bits) for MFLAG generation: when FIFO fullness reaches LT_MFLAG level, MFLAG is reset to 0	RW	0x0000

Table 10.20. Register Call Summary for Register DISPC_WB_MFLAG_THRESHOLD

Display Controller Functional Description

- MFLAG Mechanism and Arbitration:[0]

10.3. MIPI Display Serial Interface

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.4. High-Definition Multimedia Interface

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

10.5. Remote Frame Buffer Interface

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 11. 3D Graphics Accelerator

This chapter describes differences in 3D graphics accelerator (SGX) between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

The SGX subsystem is an instantiation by Texas Instruments of the POWERVR™ SGX544 core from Imagination Technologies Ltd.

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11.1. SGX Overview

The 3D graphics accelerator subsystem is based on a new core: the SGX544-SC from Imagination Technologies replaces the SGX540 core.

- offers 2.5x increase in overall graphics performance
- support for Direct3D™ Feature Level 9.3

11.2. SGX Integration

The 3D graphics accelerator subsystem has two 128-bit master interfaces to L3 interconnect instead of one in OMAP4460.

11.3. SGX Functional Description

Refer to OMAP4470 silicon revision 1.0 TRM.

11.4. SGX Register Manual

Note

This section describes only the modified TI-specific registers.

Because of the two master L3 ports in OMAP4470, the OCP_DEBUG_STATUS register has two instances: SGX_DEBUG_STATUS_0 and SGX_DEBUG_STATUS_1, for port 0 and port 1 respectively.

Table 11.1. SGX Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address
~~OCP_DEBUG_STATUS~~SGX_DEBUG_STATUS_0	R	32	0x0000 FF0C	0x5600 FF0C
SGX_DEBUG_STATUS_1	R	32	0x0000 FF10	0x5600 FF10

Chapter 12. 2D Graphics Accelerator

This chapter describes the differences in the 2D graphics accelerator subsystem between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

The 2D graphics accelerator is a new subsystem introduced in the OMAP4470 Silicon Revision 1.0. Refer to OMAP4470 Silicon Revision 1.0 TRM for details.

Chapter 13. ABE

This chapter describes the differences in the ABE between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 14. Interconnect

This chapter describes differences in the Interconnect between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

The L3 interconnect is instantiation of the NoC interconnect from Arteris, Inc. Arteris is a registered trademark of Arteris, Inc.

NoC is an abbreviation for Network On Chip.

Note

The L4 interconnects are instantiations of the Sonics3220™ interconnect from Sonics, Inc.

SMX is an abbreviation for SonicsMX.®

14.1. Interconnect Overview

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2. L3 Interconnect

14.2.1. L3 Interconnect Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.2. L3 Interconnect Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.3. L3 Interconnect Functional Description

Added 2D Blitter grapics accelerator (BB2D port1 (BB2D P1) and port2 (BB2D P2)) and BB2D Firewall. SGX module is divided in two ports. FS USB is removed. As a result the BW critical masters are changed to: IVAHD, BB2D and SGX. This impacts the following tables:

- Master NIUs
- Slave NIUs
- L3 Clock Domains and Elements
- ConnID values
- L3 Firewall Exported Values Mapping
- Slave NIU Firewall and Region Configuration
- Connectivity Holes and Error Routing
- Interconnect Flag Mapping

- L3 Firewall Instance Summary
- L3 Firewall Register Summary
- TARG Instance Summary
- TARG Registers Summary
- BW_REGULATOR Instance Summary
- BW_REGULATOR Registers Summary
- Added new BW registers Group: BW_LIMITER

The following figures are also impacted:

- L3 Interconnect Overview
- L3 Connectivity Matrix

14.2.4. L3 Interconnect Programming Guide

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.5. L3 Interconnect Register Manual

14.2.5.1. L3 Register Group Summary

The registers in the L3 interconnect are divided into eight groups:

- Firewall registers
- HOST registers
- TARG registers
- PWR_DISK registers
- BW_REGULATORS registers
- BW_LIMITER registers added
- FLAGMUX registers
- RA registers
- STATCOLL registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.5.1.1. L3 Firewall Registers Summary and Description

Table 14.1. L3 Firewall Instance Summary

Module Name	Base Address	Size
C2C-Master NIU firewall	0x4A20 4000	4KB
C2C-Slave NIU firewall	0x4A20 6000	4KB
MA firewall	0x4A20 A000	4KB
EMIF firewall	0x4A20 C000	4KB
GPMC firewall	0x4A21 0000	4KB
L3 RAM firewall	0x4A21 2000	4KB
SGX firewall	0x4A21 4000	4KB
ISS firewall	0x4A21 6000	4KB
Dual Cortex-M3 firewall	0x4A21 8000	4KB
BB2D Fireawall	0x4A21 A000	4KB
DSS firewall	0x4A21 C000	4KB
SL2 firewall	0x4A21 E000	4KB
IVA-HD firewall	0x4A22 0000	4KB
Debug firewall	0x4A22 6000	4KB
L4-ABE firewall	0x4A22 8000	4KB

14.2.5.1.1.1. L3 Firewall Registers Summary

Table 14.2. L3 Firewall Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SGX Firewall L3 Physical Address	ISS Firewall L3 Physical Address	Dual Cortex-M3 Firewall L3 Physical Address	BB2D Firewall L3 Physical Address
ERROR_LOG_k	RW	32	0x000+(0x10*k)	0x4A21 4000+(0x10*k)	0x4A21 6000+(0x10*k)	0x4A21 8000+(0x10*k)	0x4A21 A000 + (0x10*k)
LOGICAL_ADDR_ERRLOG_k	RO	32	0x004+(0x10*k)	0x4A21 4004+(0x10*k)	0x4A21 6004+(0x10*k)	0x4A21 8004+(0x10*k)	0x4A21 A004 + (0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A21 4040	0x4A21 6040	0x4A21 8040	0x4A21 A040
START_REGION_i	RW	32	0x080+(0x10*i)	N/A	N/A	N/A	N/A
END_REGION_i	RW	32	0x084+(0x10*i)	N/A	N/A	N/A	N/A
MRM_PERMISSION_REGION_HIGH_j	RW	32	0x08C+(0x10*j)	0x4A21 408C +(0x10*j)	0x4A21 608C +(0x10*j)	0x4A21 808C+(0x10*j)	0x4A21 A08C + (0x10*j)
MRM_PERMISSION_REGION_LOW_j	RW	32	0x088+(0x10*j)	0x4A21 4088 +(0x10*j)	0x4A21 6088 +(0x10*j)	0x4A21 8088+(0x10*j)	0x4A21 A088 + (0x10*j)

1. k = 0 for SGX Firewallk = 0 for ISS Firewallk = 0 for Dual Cortex-M3 Firewall
2. i = 0 for SGX Firewalli = 0 for ISS Firewalli = 0 for Dual Cortex-M3 Firewall
3. j = 0 for SGX Firewallj = 0 for ISS Firewallj = 0 for Dual Cortex-M3 Firewall

14.2.5.1.1.2. L3 Firewall Registers Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.5.1.2. L3 Host Register Summary and Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.5.1.3. L3 TARG Register Summary and Description

Table 14.3. TARG Instance Summary

Module Name	Base Address	Size
CLK1_DMM1_TARG	0x4400 0100	4KB
CLK1_DMM2_TARG	0x4400 0200	4KB
CLK1_ABE_TARG	0x4400 0300	4KB
CLK1_L4CFG_TARG	0x4400 0400	4KB
CLK2_GPMC_TARG	0x4480 0100	4KB
CLK2_OCMRAM_TARG	0x4480 0200	4KB
CLK2_DSS_TARG	0x4480 0300	4KB
CLK2_ISS_TARG	0x4480 0400	4KB
CLK2_CORTEXM3_TARG	0x4480 0500	4KB
CLK2_SGX_TARG	0x4480 0600	4KB
CLK2_IVAHD_TARG	0x4480 0700	4KB
CLK2_SL2_TARG	0x4480 0800	4KB
CLK2_L4PER0_TARG	0x4480 0900	4KB
CLK2_L4PER1_TARG	0x4480 0A00	4KB
CLK2_L4PER2_TARG	0x4480 0B00	4KB

Module Name	Base Address	Size
CLK2_L4PER3_TARG	0x4480 0C00	4KB
CLK2_C2C_TARG	0x4480 1600	4KB
CLK2_BB2D_TARG	0x4480 1900	4KB
CLK3_L4EMU_TARG	0x4500 0100	4KB

14.2.5.1.3.1. L3 TARG Registers Summary

Table 14.4. TARG Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_C2C	CLK2_C2C_TARG L3 Physical Address	CLK2_BB2D_TARG L3 Physical Address	Address Offset for CLK2_L4EMU	CLK3_L4EMU_TARG L3 Physical Address
L3_TARG_STDHOSTHDR_COREREG	R	32	0x0080 1600	0x4480 1600	0x4480 1900	0x0100 0100	0x4500 0100
L3_TARG_STDHOSTHDR_VERSIONREG	R	32	0x0080 1604	0x4480 1604	0x4480 1904	0x0100 0104	0x4500 0104
L3_TARG_STDHOSTHDR_MAINCTLREG	RW	32	0x0080 1608	0x4480 1608	0x4480 1908	0x0100 0108	0x4500 0108
L3_TARG_STDHOSTHDR_NTTPADDR_0	R	32	0x0080 1610	0x4480 1610	0x4480 1910	0x0100 0110	0x4500 0110
L3_TARG_STDERRLOG_SVRTSTDLVL	RW	32	0x0080 1640	0x4480 1640	0x4480 1940	0x0100 0140	0x4500 0140
L3_TARG_STDERRLOG_SVRTCUSTOMLVL	RW	32	0x0080 1644	0x4480 1644	0x4480 1944	0x0100 0144	0x4500 0144
L3_TARG_STDERRLOG_MAIN	RW	32	0x0080 1648	0x4480 1648	0x4480 1948	0x0100 0148	0x4500 0148
L3_TARG_STDERRLOG_HDR	R	32	0x0080 164C	0x4480 164C	0x4480 194C	0x0100 014C	0x4500 014C
L3_TARG_STDERRLOG_MSTADDR	R	32	0x0080 1650	0x4480 1650	0x4480 1950	0x0100 0150	0x4500 0150
L3_TARG_STDERRLOG_SLVADDR	R	32	0x0080 1654	0x4480 1654	0x4480 1954	0x0100 0154	0x4500 0154
L3_TARG_STDERRLOG_INFO	R	32	0x0080 1658	0x4480 1658	0x4480 1958	0x0100 0158	0x4500 0158
L3_TARG_STDERRLOG_SLVOFSLSB	R	32	0x0080 165C	0x4480 165C	0x4480 195C	0x0100 015C	0x4500 015C
L3_TARG_STDERRLOG_SLVOFSMSB	R	32	0x0080 1660	0x4480 1660	0x4480 1960	0x0100 0160	0x4500 0160
L3_TARG_STDERRLOG_CUSTOMINFO_INFO	R	32	0x0080 1664	0x4480 1664	0x4480 1964	0x0100 0164	0x4500 0164
L3_TARG_STDERRLOG_CUSTOMINFO_MSTADDR	R	32	0x0080 1668	0x4480 1668	0x4480 1968	0x0100 0168	0x4500 0168
L3_TARG_STDERRLOG_CUSTOMINFO_OPCODE	R	32	0x0080 166C	0x4480 166C	0x4480 196C	0x0100 016C	0x4500 016C
L3_TARG_ADDRSPACESIZELOG	RW	32	0x0080 1680	0x4480 1680	0x4480 1980	0x0100 0180	0x4500 0180

14.2.5.1.4. L3 PWR_DISC Register Summary and Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.5.1.5. L3 FLAGMUX Register Summary and Description

Registers L3_FLAGMUX_MASK0, L3_FLAGMUX_REGERR0, L3_FLAGMUX_MASK1 and L3_FLAGMUX_MASK1 are modified. For complete description of these registers refer to OMAP 4470 Silicon Revision 1.0 TRM.

14.2.5.1.6. L3 BW Regulator Register Summary and Description

Table 14.5. BW_REGULATOR Instance Summary

Module Name	Base Address	Size
~~CLK1_DSS_BW_REGULATOR~~	~~0x4400 0700~~	~~256 bytes~~
~~CLK2_ISS_BW_REGULATOR~~	~~0x4480 1300~~	~~256 bytes~~
CLK2_IVAHD_BW_REGULATOR	0x4480 1400	256 bytes
CLK2_SGX_M1_BW_REGULATOR	0x4480 1700	256 bytes
CLK2_SGX_M2_BW_REGULATOR	0x4480 1800	256 bytes
CLK2_BB2D_M1_BW_REGULATOR	0x4480 1A00	256 bytes
CLK2_BB2D_M2_BW_REGULATOR	0x4480 1B00	256 bytes

14.2.5.1.6.1. 1.5.1.6.1 L3 BW Regulator Register Summary

Table 14.6. BW_REGULATOR Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_IVAHD_BW_REGULATOR	CLK2_IVAHD_BW_REGULATOR L3 Physical Address	Address Offset for CLK2_SGX_M1_BW_REGULATOR	CLK2_SGX_M1_BW_REGULATOR L3 Physical Address	Address Offset for CLK2_SGX_M2_BW_REGULATOR	CLK2_SGX_M2_BW_REGULATOR L3 Physical Address
L3_BW_R_STDHOSTHDR_COREREG	R	32	0x0080 1400	0x4480 1400	0x0080 1700	0x4480 1700	0x0080 1800	0x4480 1800
L3_BW_R_STDHOSTHDR_VERSIONREG	R	32	0x0080 1404	0x4480 1404	0x0080 1704	0x4480 1704	0x0080 1804	0x4480 1804
L3_BW_R_BANDWIDTH	RW	32	0x0080 1408	0x4480 1408	0x0080 1708	0x4480 1708	0x0080 1808	0x4480 1808
L3_BW_R_WATERMARK	RW	32	0x0080 140C	0x4480 140C	0x0080 170C	0x4480 170C	0x0080 180C	0x4480 180C
L3_BW_R_PRESS	R	32	0x0080 1410	0x4480 1410	0x0080 1710	0x4480 1710	0x0080 1810	0x4480 1810
L3_BW_R_CLEARHISTORY	RW	32	0x0080 1414	0x4480 1414	0x0080 1714	0x4480 1714	0x0080 1814	0x4480 1814

Table 14.7. BW_REGULATOR Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_BB2D_M1_BW_REGULATOR	CLK2_BB2D_M1_BW_REGULATOR L3 Physical Address	Address Offset for CLK2_BB2D_M2_BW_REGULATOR	CLK2_BB2D_M2_BW_REGULATOR L3 Physical Address
L3_BW_R_STDHOSTHDR_COREREG	R	32	0x0080 1A00	0x4480 1A00	0x0080 1B00	0x4480 1B00
L3_BW_R_STDHOSTHDR_VERSIONREG	R	32	0x0080 1A04	0x4480 1A04	0x0080 1B04	0x4480 1B04
L3_BW_R_BANDWIDTH	RW	32	0x0080 1A08	0x4480 1A08	0x0080 1B08	0x4480 1B08
L3_BW_R_WATERMARK	RW	32	0x0080 1A0C	0x4480 1A0C	0x0080 1B0C	0x4480 1B0C
L3_BW_R_PRESS	R	32	0x0080 1A10	0x4480 1A10	0x0080 1B10	0x4480 1B10
L3_BW_R_CLEARHISTORY	RW	32	0x0080 1A14	0x4480 1A14	0x0080 1B14	0x4480 1B14

14.2.5.1.6.2. L3 BW Limiter Register Summary and Description

Table 14.8. BW Limiter Instance Summary

Module Name	Base Address	Size
CLK2_BB2D_M1_BW_LIMITER	0x4480 1C00	256 bytes
CLK2_BB2D_M2_BW_LIMITER	0x4480 1D00	256 bytes

14.2.5.1.6.2.1. L3 BW Limiter Register Summary

Table 14.9. BW_LIMITER Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset for CLK2_BB2D_M1_BW_LIMITER	CLK2_BB2D_M1_BW_LIMITER L3 Physical Address	Address Offset for CLK2_BB2D_M2_BW_LIMITER	CLK2_BB2D_M2_BW_LIMITER L3 Physical Address
L3_BW_L_STDHOSTHDR_COREREG	R	32	0x0080 1C00	0x4480 1C00	0x0080 1D00	0x4480 1D00
L3_BW_L_STDHOSTHDR_VERSIONREG	R	32	0x0080 1C04	0x4480 1C04	0x0080 1D04	0x4480 1D04
L3_BW_L_BANDWIDTH_FRACTIONAL	RW	32	0x0080 1C08	0x4480 1C08	0x0080 1D08	0x4480 1D08
L3_BW_L_BANDWIDTH_INTEGER	RW	32	0x0080 1C0C	0x4480 1C0C	0x0080 1D0C	0x4480 1D0C
L3_BW_L_WATERMARK	R	32	0x0080 1C10	0x4480 1C10	0x0080 1D10	0x4480 1D10
L3_BW_L_CLEARHISTORY	RW	32	0x0080 1C14	0x4480 1C14	0x0080 1D14	0x4480 1D14

14.2.5.1.6.2.2. L3 BW LIMITER Register Description

For detailed L3 BW LIMITER registers description refer to OMAP4470 Silicon Revision 1.0 TRM.

14.2.5.1.7. L3 Rate Adapt Register Summary and Description

Refer to OMAP4470 Silicon Revision 1.0 TRM

14.2.5.1.8. L3 STATCLOLL Register Summary and Description

14.2.5.1.8.1. L3 STATCLOLL Register Summary

Table 14.10. STATCOLL Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOL_SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOL_LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOL_LAT1 L3 Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0100 1000	0x4500 1000	0x0100 2000	0x4500 2000	0x0100 3000	0x4500 3000
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0100 1004	0x4500 1004	0x0100 2004	0x4500 2004	0x0100 3004	0x4500 3004
L3_STCOL_EN	RW	32	0x0100 1008	0x4500 1008	0x0100 2008	0x4500 2008	0x0100 3008	0x4500 3008
L3_STCOL_SOFTEN	RW	32	0x0100 100C	0x4500 100C	0x0100 200C	0x4500 200C	0x0100 300C	0x4500 300C
L3_STCOL_IGNORESUSPEND	RW	32	0x0100 1010	0x4500 1010	0x0100 2010	0x4500 2010	0x0100 3010	0x4500 3010
L3_STCOL_TRIGEN	RW	32	0x0100 1014	0x4500 1014	0x0100 2014	0x4500 2014	0x0100 3014	0x4500 3014
L3_STCOL_REQEVT	RW	32	0x0100 1018	0x4500 1018	0x0100 2018	0x4500 2018	0x0100 3018	0x4500 3018
L3_STCOL_RSPEVT	RW	32		0x4500 101C	0x0100 201C		0x0100 301C	0x4500 301C

Register Name	Type	Re-gister Width (Bits)	Address Offset for SDRAM	CLK3_STATCOL_L_SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOL_L_LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOL_L_LAT1 L3 Physical Address
			0x0100 101C			0x4500 201C		
L3_STCOL_EVTMUX_SEL0	RW	32	0x0100 1020	0x4500 1020	0x0100 2020	0x4500 2020	0x0100 3020	0x4500 3020
L3_STCOL_EVTMUX_SEL1	RW	32	0x0100 1024	0x4500 1024	0x0100 2024	0x4500 2024	0x0100 3024	0x4500 3024
L3_STCOL_EVTMUX_SEL2	RW	32	0x0100 1028	0x4500 1028	0x0100 2028	0x4500 2028	0x0100 3028	0x4500 3028
L3_STCOL_EVTMUX_SEL3	RW	32	0x0100 102C	0x4500 102C	0x0100 202C	0x4500 202C	0x0100 302C	0x4500 302C
L3_STCOL_EVTMUX_SEL4	RW	32	0x0100 1030	0x4500 1030	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL5	RW	32	0x0100 1034	0x4500 1034	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL6	RW	32	0x0100 1038	0x4500 1038	N/A	N/A	N/A	N/A
L3_STCOL_EVTMUX_SEL7	RW	32	0x0100 103C	0x4500 103C	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_IDEN-TIFIER	R	32	0x0100 1040	0x4500 1040	0x0100 2040	0x4500 2040	0x0100 3040	0x4500 3040
L3_STCOL_DUMP_COLLECTTIME	RW	32	0x0100 1044	0x4500 1044	0x0100 2044	0x4500 2044	0x0100 3044	0x4500 3044
L3_STCOL_DUMP_SLVADDR	R	32	0x0100 1048	0x4500 1048	0x0100 2048	0x4500 2048	0x0100 3048	0x4500 3048
L3_STCOL_DUMP_MSTADDR	R	32	0x0100 104C	0x4500 104C	0x0100 204C	0x4500 204C	0x0100 304C	0x4500 304C
L3_STCOL_DUMP_SLVOFS	RW	32	0x0100 1050	0x4500 1050	0x0100 2050	0x4500 2050	0x0100 3050	0x4500 3050
~~L3_STCOL_DUMP_MANUAL~~	~~RW~~	32	~~0x0100 1054~~	~~0x4500 1054~~	~~0x0100 2054~~	~~0x4500 2054~~	~~0x0100 3054~~	~~0x4500 3054~~
L3_STCOL_DUMP_MODE	RW	32	0x0100 1054	0x4500 1054	0x0100 2054	0x4500 2054	0x0100 3054	0x4500 3054
L3_STCOL_DUMP_SEND	RW	32	0x0100 1058	0x4500 1058	0x0100 2058	0x4500 2058	0x0100 3058	0x4500 3058
L3_STCOL_DUMP_DISABLE	RW	32	0x0100 105C	0x4500 105C	0x0100 205C	0x4500 205C	0x0100 305C	0x4500 305C
L3_STCOL_DUMP_ALARM_TRIG	RW	32	0x0100 1060	0x4500 1060	0x0100 2060	0x4500 2060	0x0100 3060	0x4500 3060
L3_STCOL_DUMP_ALARM_MINVAL	RW	32	0x0100 1064	0x4500 1064	0x0100 2064	0x4500 2064	0x0100 3064	0x4500 3064
L3_STCOL_DUMP_ALARM_MAXVAL	RW	32	0x0100 1068	0x4500 1068	0x0100 2068	0x4500 2068	0x0100 3068	0x4500 3068
L3_STCOL_DUMP_ALARM_MODE0	RW	32	0x0100 106C	0x4500 106C	0x0100 206C	0x4500 206C	0x0100 306C	0x4500 306C
L3_STCOL_DUMP_ALARM_MODE1	RW	32	0x0100 1070	0x4500 1070	0x0100 2070	0x4500 2070	0x0100 3070	0x4500 3070
L3_STCOL_DUMP_ALARM_MODE2	RW	32	0x0100 1074	0x4500 1074	0x0100 2074	0x4500 2074	0x0100 3074	0x4500 3074
L3_STCOL_DUMP_ALARM_MODE3	RW	32	0x0100 1078	0x4500 1078	0x0100 2078	0x4500 2078	0x0100 3078	0x4500 3078
L3_STCOL_DUMP_ALARM_MODE4	RW	32	0x0100 107C	0x4500 107C	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE5	RW	32	0x0100 1080	0x4500 1080	N/A	N/A	N/A	N/A

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOL_L_SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOL_L_LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOL_L_LAT1 L3 Physical Address
L3_STCOL_DUMP_ALARM_MODE6	RW	32	0x0100 1084	0x4500 1084	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_ALARM_MODE7	RW	32	0x0100 1088	0x4500 1088	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT0	RW	32	0x0100 108C	0x4500 108C	0x0100 208C	0x4500 208C	0x0100 308C	0x4500 308C
L3_STCOL_DUMP_CNT1	RW	32	0x0100 1090	0x4500 1090	0x0100 2090	0x4500 2090	0x0100 3090	0x4500 3090
L3_STCOL_DUMP_CNT2	RW	32	0x0100 1094	0x4500 1094	0x0100 2094	0x4500 2094	0x0100 3094	0x4500 3094
L3_STCOL_DUMP_CNT3	RW	32	0x0100 1098	0x4500 1098	0x0100 2098	0x4500 2098	0x0100 3098	0x4500 3098
L3_STCOL_DUMP_CNT4	RW	32	0x0100 109C	0x4500 109C	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT5	RW	32	0x0100 10A0	0x4500 10A0	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT6	RW	32	0x0100 10A4	0x4500 10A4	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_CNT7	RW	32	0x0100 10A8	0x4500 10A8	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_GLOBALEN	RW	32	0x0100 10AC	0x4500 10AC	0x0100 20AC	0x4500 20AC	0x0100 30AC	0x4500 30AC
L3_STCOL_FILTER_i_ADDR-MIN	RW	32	0x0100 10B0	0x4500 10B0	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_ADDR-MAX	RW	32	0x0100 10B4	0x4500 10B4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_ADDREN	RW	32	0x0100 10B8	0x4500 10B8	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_EN_k	RW	32	0x0100 10BC	0x4500 10BC	0x0100 20BC	0x4500 20BC	0x0100 30BC	0x4500 30BC
L3_STCOL_FILTER_i_MASK_m_MSTAD-DR	RW	32	0x0100 10C8	0x4500 10C8	0x0100 20C8	0x4500 20C8	0x0100 30C8	0x4500 30C8
L3_STCOL_FILTER_i_MASK_m_RD	RW	32	0x0100 10C0	0x4500 10C0	0x0100 20C0	0x4500 20C0	0x0100 30C0	0x4500 30C0
L3_STCOL_FILTER_i_MASK_m_WR	RW	32	0x0100 10C4	0x4500 10C4	0x0100 20C4	0x4500 20C4	0x0100 30C4	0x4500 30C4
L3_STCOL_FILTER_i_MASK_m_ERR	RW	32	0x0100 10D0	0x4500 10D0	0x0100 20D0	0x4500 20D0	0x0100 30D0	0x4500 30D0
L3_STCOL_FILTER_i_MASK_m_USERINFO	RW	32	0x0100 10D4	0x4500 10D4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MATCH_m_MSTADDR	RW	32	0x0100 10E8	0x4500 10E8	0x0100 20E8	0x4500 20E8	0x0100 30E8	0x4500 30E8
L3_STCOL_FILTER_i_MATCH_m_RD	RW	32	0x0100 10E0	0x4500 10E0	0x0100 20E0	0x4500 20E0	0x0100 30E0	0x4500 30E0
L3_STCOL_FILTER_i_MATCH_m_WR	RW	32	0x0100 10E4	0x4500 10E4	0x0100 20E4	0x4500 20E4	0x0100 30E4	0x4500 30E4
L3_STCOL_FILTER_i_MATCH_m_ERR	RW	32	0x0100 10F0	0x4500 10F0	0x0100 20F0	0x4500 20F0	0x0100 30F0	0x4500 30F0
L3_STCOL_FILTER_i_MATCH_m_USERINFO	RW	32	0x0100 10F4	0x4500 10F4	N/A	N/A	N/A	N/A
L3_STCOL_OP_i_THRESHOLD_MINVAL	RW	32	0x0100 11F0	0x4500 11F0	0x0100 21F0	0x4500 21F0	0x0100 31F0	0x4500 31F0

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOL_L_SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOL_L_LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOL_L_LAT1 L3 Physical Address
L3_STCOL_OP_i_THRESHOLD_MAXVAL	RW	32	0x0100 11F4	0x4500 11F4	0x0100 21F4	0x4500 21F4	0x0100 31F4	0x4500 31F4
L3_STCOL_OP_i_EVTINFOSEL	RW	32	0x0100 11F8	0x4500 11F8	0x0100 21F8	0x4500 21F8	0x0100 31F8	0x4500 31F8
L3_STCOL_OP_i_SEL	RW	32	0x0100 11FC	0x4500 11FC	0x0100 21FC	0x4500 21FC	0x0100 31FC	0x4500 31FC

1. i = from 0 to 47 for CLK3_STATCOLL_SDRAMi = 0 to 3 for CLK3_STATCOLL_LAT0 and L3_STATCOLL_LAT1
2. m = 0 to 1 for CLK3_STATCOLL_SDRAMm = 0 for CLK3_STATCOLL_LAT0m = 0 for CLK3_STATCOLL_LAT1
3. k = 0 to 1 for CLK3_STATCOLL_SDRAMk = 0 to 1 for CLK3_STATCOLL_LAT0k = 0 to 1 for CLK3_STATCOLL_LAT1

14.2.5.1.8.2. L3 STATCLOLL Register Description

Register L3_STCOL_DUMP_MANUAL is replaced by L3_STCOL_DUMP_MODE.

Added 22 new registers:

- L3_STCOL_IGNORESUSPEND
- L3_STCOL_EVTMUX_SEL5
- L3_STCOL_EVTMUX_SEL6
- L3_STCOL_EVTMUX_SEL7
- L3_STCOL_DUMP_MODE
- L3_STCOL_DUMP_ALARM_MODE0 to L3_STCOL_DUMP_ALARM_MODE7
- L3_STCOL_DUMP_CNT0 to L3_STCOL_DUMP_CNT7

Bitfields in L3_STCOL_FILTER_i_MASK_m_MSTADDR, L3_STCOL_FILTER_i_MATCH_m_MSTADDR, L3_STCOL_DUMP_COLLECTTIME, L3_STCOL_DUMP_ALARM_MINVAL and L3_STCOL_OP_i_THRESHOLD_MINVAL register are corrected.

14.3. L4 Interconnects

14.3.1. L4-Interconnect Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM

14.3.2. L4-Interconnect Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3. L4-Interconnect Functional Description

BB2D Firewall is added (BB2D FW), this impacts the following figure:

- L4 Interconnect Overview

and tables:

- L4 CFG TAs
- Region Allocations for L4 CFG Interconnect
- L4_CFG Instance Summary
- CFG_TA Register Mapping Summary

14.3.3.1. Module Distribution

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3.1.1. L4 PER Interconnect Agent

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3.1.2. L4 CFG Interconnect Agents

Table 14.11. L4_CFG TAs

Module Target Name	Description
CFG_TA_SYSCTRL_GENERAL_CORE	System control general core module
CFG_TA_SYSCTRL_PADCONF_CORE	System control padconf core module
CFG_TA_CM_CORE_AON	Clock manager 1 module
CFG_TA_CM_CORE	Clock manager 1 module core
CFG_TA_DMA_SYSTEM	sDMA module
CFG_TA_HSI	HS SSI module
CFG_TA_SAR_ROM	Save-and-restore ROM
CFG_TA_HSUSBOTG	HS USB OTG module
CFG_TA_HSUSBHOST	HS USB host module
CFG_TA_HSUSBPHY	HS USB PHY module
CFG_TA_HSUSBTLL	USB TTL module
CFG_TA_DSP	DSP subsystem
CFG_TA_SR1	SmartReflex1 module
CFG_TA_SR2	SmartReflex2 module
CFG_TA_SR3	SmartReflex3 module
CFG_TA_MAILBOX	Mailbox module
CFG_TA_SPINLOCK	Spinlock module
CFG_TA_FACEDETECT	Face detect module
CFG_TA_MAFW	Memory adapter firewall
CFG_TA_EMIFFW	EMIF firewall
CFG_TA_GPMCFW	GPMC firewall
CFG_TA_OCMCRAMFW	OCMC_RAM firewall
CFG_TA_SGXFW	SGX firewall
CFG_TA_BB2DFW	BB2D firewall
CFG_TA_ISSFW	ISS firewall
CFG_TA_CORTEXM3FW	Cortex-M3 firewall
CFG_TA_DSSFW	Dispay subsystem (DSS) firewall
CFG_TA_SL2FW	SL2 firewall
CFG_TA_IVAHDFW	IVA-HD firewall
CFG_TA_L3_INSTR	EMU subsystem firewall
CFG_TA_ABEFW	ABE firewall
CFG_TA_L4_WKUP	L4_WKUP connection
CFG_TA_MODEM_ICR_PA/PB	Modem intercommunication register

14.3.3.1.3. L4_WKUP Interconnect Agnets

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3.2. Power Management

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3.3. L4 Firewalls

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3.3.1. Protection Group

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3.3.2. Segments and Regions

Table 14.12. Region Allocations for L4_CFG Interconnect

Module	Region	Description
L4_CFG CONFIG	0	Firewall
	1	CFG_IA_0
	2	Link agent
CFG_SYSCTRL_GENERAL_CORE	3	TA
	4	Module
CM1	5	TA
	6	Module
sDMA	7	TA
	8	Module
HSI	9	TA
	10	Module
HSUSBTLL	11	TA
	12	Module
SR1	13	TA
	14	Module
SR2	15	TA
	16	Module
SR3	17	TA
	18	Module
CFG_SYSCTRL_PADCONF_CORE	21	TA
	22	Module
CM2	23	TA
	24	Module
DSP subsystem	25	TA
	26	Module
Mailbox	27	TA
	28	Module
SPINLOCK	29	TA
	30	Module
SL2FW	31	TA
	32	Module
MAFW	33	TA
	34	Module
C2CFW	35	TA
	36	Module
MODEMFW	37	TA

Module	Region	Description
	38	Module
OCMCRAMFW	39	TA
	40	Module
EMIFFW	41	TA
	42	Module
GPMCFW	43	TA
	44	Module
ISSFW	45	TA
	46	Module
SGXFW	47	TA
	48	Module
CORTEXM3FW	49	TA
	50	Module
IVAHDFW	51	TaA
	52	Module
EMUSSFW	53	TA
	54	Module
ABEFW	55	TA
	56	Module
DSSFW	59	TA
	60	Module
FACEDETECT	65	TA
	66	Module
L4WKUP	67	L4_WKUP regions 0, 1, 2, 3, 4, 15, 16, 17, 18, 19, 20
	68	Module
MODEMICRA	69	TA
	70	Module
L4WKUP	71	L4_WKUP regions 23, 24, 25, 26
	72	L4_WKUP regions 27, 28
	73	L4_WKUP region 13
	74	L4_WKUP region 29
	75	L4_WKUP region 30
	76	L4_WKUP region 31
MODEMICRB	78	TA
	79	Module
SAR_ROM	80	TA
	81	Module
~~USBFS~~	82	~~TA~~
	83	~~Module~~
USBOTGHS	84	TA
	85	Module
USBHOSTHS	86	TA
	87	Module
USBPHY	88	TA
	89	Module

Module	Region	Description
L4WKUP	90	L4_WKUP region 14
	91	–
	92	L4_WKUP region (5, 6, 7, 8)
	93	L4_WKUP region (9, 10)
	94	L4_WKUP region (11, 12)
	95	L4_WKUP region (21, 22)
BB2DFW	96	TA
	97	Module

14.3.3.3.3. L4 Firewall Address and Protection Register Settings

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.3.4. L4 Error Detection and Reporting

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.4. L4-Interconnect Programming Guide

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.5. L4-Interconnects Register Manual

14.3.5.1. L4 Interconnects Instance Summary

Table 14.13. L4_CFG Instance Summary

Module Name	L3 Base Address	Size
CFG_AP	0x4A00 0000	2KB
CFG_IA_0	0x4A00 1000	128B
CFG_LA	0x4A00 0800	4KB
CFG_TA_SYSCTRL_GENERAL_CORE	0x4A00 3000	4KB
CFG_TA_CM1	0x4A00 5000	4KB
CFG_TA_CM2	0x4A00 A000	4KB
CFG_TA_SDMA	0x4A05 7000	4KB
CFG_TA_HSI	0x4A05 C000	4KB
CFG_TA_SAR_ROM	0x4A06 0000	4KB
CFG_TA_HSUSBTLL	0x4A06 3000	4KB
CFG_TA_USBHOSTHS	0x4A06 5000	4KB
CFG_TA_DSP	0x4A06 7000	4KB
~~CFG_TA_USBFS~~	~~0x4A0A A000~~	~~4KB~~
CFG_TA_USBOTGHS	0x4A0A C000	4KB
CFG_TA_USBPHY	0x4A0A E000	4KB
CFG_TA_SR1	0x4A0D A000	4KB
CFG_TA_SR2	0x4A0DC000	4KB
CFG_TA_SR3	0x4A0D E000	4KB
CFG_TA_CUSTEFUSECTRL	0x4A0E 1000	4KB
CFG_TA_MAILBOX	0x4A0F 5000	4KB
CFG_TA_SPINLOCK	0x4A0F 7000	4KB
CFG_TA_SYSCTRL_PADCONF_CORE	0x4A10 1000	4KB
CFG_TA_FACEDETECT	0x4A10 B000	4KB

Module Name	L3 Base Address	Size
CFG_TA_MAFW	0x4A20 A000	4KB
CFG_TA_EMIFFW	0x4A20 D000	4KB
CFG_TA_GPMCFW	0x4A21 1000	4KB
CFG_TA_OCMCRAMFW	0x4A21 3000	4KB
CFG_TA_SGXFW	0x4A21 5000	4KB
CFG_TA_ISSFW	0x4A21 7000	4KB
CFG_TA_CORTEXM3FW	0x4A21 9000	4KB
CFG_TA_BB2DFW	0x4A21 B000	4KB
CFG_TA_DSSFW	0x4A21 D000	4KB
CFG_TA_SL2FW	0x4A21 F000	4KB
CFG_TA_IVAHDFW	0x4A22 1000	4KB
CFG_TA_EMUSSFW	0x4A22 7000	4KB
CFG_TA_ABEFW	0x4A22 9000	4KB
CFG_TA_L4WKUP	0x4A34 0000	4KB

14.3.5.2. L4 Initiator Agent (L4 IA)

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.5.3. L4 Target Agent (L4 TA)

14.3.5.3.1. L4 Target Agent (L4 TA) Register Summary

Table 14.14. CFG_TA Register Mapping Summary 11

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_CORTEXM3FW L3 Physical Address	CFG_TA_BB2DFW L3 Physical Address	CFG_TA_DSSFW L3 Physical Address	CFG_TA_SL2FW L3 Physical Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A21 9000	0x4A21 B000	0x4A21 D000	0x4A21 F000
L4_TA_COMPONENT_L	R	32	0x0000 0004	0x4A21 9004	0x4A21 B004	0x4A21 D004	0x4A21 F004
L4_TA_CORE_L	R	32	0x0000 0018	0x4A21 9018	0x4A21 B018	0x4A21 D018	0x4A21 F018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A21 901C	0x4A21 B01C	0x4A21 D01C	0x4A21 F01C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A21 9020	0x4A21 B020	0x4A21 D020	0x4A21 F020
L4__TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A21 9024	0x4A21 B024	0x4A21 D024	0x4A21 F024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A21 9028	0x4A21 B028	0x4A21 D028	0x4A21 F028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A21 902C	0x4A21 B02C	0x4A21 D02C	0x4A21 F02C

14.3.5.3.2. L4 Target Agent (L4 TA) Register Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.5.4. L4 Link Agent (L4 LA)

Refer to OMAP4470 Silicon Revision 1.0 TRM.

14.3.5.5. L4 Address Protection (L4 AP)

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 15. Chip-to-Chip Interface (C2C)

This chapter describes the differences in the C2C between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0.

15.1. C2C Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

15.2. C2C Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

15.4. C2C L3 Interconnect

Refer to OMAP4470 Silicon Revision 1.0 TRM.

15.5. C2C SSCM

15.5.1. SSCM Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

15.5.2. SSCM Interrupts

15.5.2.1. SSCM GPI Interrupt Mapping

Table 15.1. SSCM GPI Interrupt Mapping

C2C_SSCM_GPI	Source	Description
C2C_SSCM_GPI[0]	SYS.IRQ1n	External interrupt
C2C_SSCM_GPI[1]	MAIL_U3_C2C_IRQ	Device to DD mailbox interrupt
C2C_SSCM_GPI[2]	MODEM_ICR_IRQ	Distant (Modem) ICR Interrupt
C2C_SSCM_GPI[3]	UART1_IRQ	UART module 1
C2C_SSCM_GPI[4]	UART2_IRQ	UART module 2
C2C_SSCM_GPI[5]	UART3_IRQ	UART module 3
C2C_SSCM_GPI[6]	GPT6_IRQ	General-purpose timer 6
C2C_SSCM_GPI[7]	GPT7_IRQ	General-purpose timer 7
C2C_SSCM_GPI[8]	GPT8_IRQ	General-purpose timer 8
C2C_SSCM_GPI[9]	GPT9_IRQ	General-purpose timer 9
C2C_SSCM_GPI[10]	GPIO1_MPU_IRQ	GPIO module 1
C2C_SSCM_GPI[11]	GPIO2_MPU_IRQ	GPIO module 2
C2C_SSCM_GPI[12]	GPIO3_MPU_IRQ	GPIO module 3
C2C_SSCM_GPI[13]	GPIO4_MPU_IRQ	GPIO module 4
C2C_SSCM_GPI[14]	HS_USB_MC_NINT	Module HS USB OTG
C2C_SSCM_GPI[15]	HS_USB_DMA_NINT	Module HS USB OTG DMA controller interrupt
C2C_SSCM_GPI[16]	~~FSUSB_IRQ~~Reserved	~~FS USB-HOST controller interrupt~~Reserved
C2C_SSCM_GPI[17]	~~FSUSB_SMI_IRQ~~Reserved	~~FS USB-HOST controller SMI~~Reserved

C2C_SSCM_GPI	Source	Description
C2C_SSCM_GPI[18]	L3_APP_IRQ	Application errors on L3
C2C_SSCM_GPI[19]	ONCHI_IRQ	HSUSB MP host interrupt
C2C_SSCM_GPI[20]	EHCI_IRQ	HSUSB MP host interrupt
C2C_SSCM_GPI[21]	TLL_IRQ	TLL interrupt
C2C_SSCM_GPI[22]	SYS.IRQ2n	External interrupt
C2C_SSCM_GPI[23:29]	Reserved	Reserved
C2C_SSCM_GPI[30]	Modem_shutdown_irqModem_wake_irq	PRCM Modem_shutdown_irq
C2C_SSCM_GPI[31]	Modem_wake_irq	PRCM Modem_wake_irq

15.5.3. SSCM GPO

Refer to OMAP4470 Silicon Revision 1.0 TRM.

15.6. Intersystem Communication Register Module

Refer to OMAP4470 Silicon Revision 1.0 TRM.

15.7. C2C Register Manual

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 16. Memory Subsystem

This chapter describes the differences in the Memory Subsystem between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

16.1. Memory Subsystem Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.2. Dynamic Memory Manager

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.3. EMIF Controller

16.3.1. EMIF Module Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.3.2. EMIF Environment

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.3.3. EMIF Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.3.4. EMIF Functional Description

The [28] REG_ZQ_SFEXITEN bit behavior in the EMIF_ZQ_CONFIG register is changed to only issue a ZQ calibration long command when exiting self-refresh, not when exiting power-down. With power-down as the PM mode, refresh would wake up device, and perform a zq_long, which was consuming lot of power. Now, when running in this mode, zq short calibration occurs in the refresh slots when time expires.

16.3.5. EMIF Programming Guide

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.3.6. EMIF Register Manual

16.3.6.1. EMIF Instance Summary

Table 16.1. EMIF Instance Summary

Module Name	Base Address	Size
EMIF1	0x4C00 0000	16 MB
EMIF2	0x4D00 0000	16 MB

16.3.6.2. EMIF Registers

16.3.6.2.1. EMIF Register Summary

Table 16.2. EMIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_MOD_ID_REV	R	32	0x0000 0000	0x4C00 0000	0x4D00 0000
EMIF_STATUS	R	32	0x0000 0004	0x4C00 0004	0x4D00 0004

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_SDRAM_CONFIG	RW	32	0x0000 0008	0x4C00 0008	0x4D00 0008
EMIF_SDRAM_CONFIG_2	RW	32	0x0000 000C	0x4C00 000C	0x4D00 000C
EMIF_SDRAM_REF_CTRL	RW	32	0x0000 0010	0x4C00 0010	0x4D00 0010
EMIF_SDRAM_REF_CTRL_SHDW	RW	32	0x0000 0014	0x4C00 0014	0x4D00 0014
EMIF_SDRAM_TIM_1	RW	32	0x0000 0018	0x4C00 0018	0x4D00 0018
EMIF_SDRAM_TIM_1_SHDW	RW	32	0x0000 001C	0x4C00 001C	0x4D00 001C
EMIF_SDRAM_TIM_2	RW	32	0x0000 0020	0x4C00 0020	0x4D00 0020
EMIF_SDRAM_TIM_2_SHDW	RW	32	0x0000 0024	0x4C00 0024	0x4D00 0024
EMIF_SDRAM_TIM_3	RW	32	0x0000 0028	0x4C00 0028	0x4D00 0028
EMIF_SDRAM_TIM_3_SHDW	RW	32	0x0000 002C	0x4C00 002C	0x4D00 002C
EMIF_LPDDR2_NVM_TIM	RW	32	0x0000 0030	0x4C00 0030	0x4D00 0030
EMIF_LPDDR2_NVM_TIM_SHDW	RW	32	0x0000 0034	0x4C00 0034	0x4D00 0034
EMIF_PWR_MGMT_CTRL	RW	32	0x0000 0038	0x4C00 0038	0x4D00 0038
EMIF_PWR_MGMT_CTRL_SHDW	RW	32	0x0000 003C	0x4C00 003C	0x4D00 003C
EMIF_LPDDR2_MODE_REG_DATA	RW	32	0x0000 0040	0x4C00 0040	0x4D00 0040
EMIF_LPDDR2_MODE_REG_CFG	RW	32	0x0000 0050	0x4C00 0050	0x4D00 0050
EMIF_L3_CONFIG	RW	32	0x0000 0054	0x4C00 0054	0x4D00 0054
EMIF_L3_CFG_VAL_1	R	32	0x0000 0058	0x4C00 0058	0x4D00 0058
EMIF_L3_CFG_VAL_2	R	32	0x0000 005C	0x4C00 005C	0x4D00 005C
EMIF_PERF_CNT_1	R	32	0x0000 0080	0x4C00 0080	0x4D00 0080
EMIF_PERF_CNT_2	R	32	0x0000 0084	0x4C00 0084	0x4D00 0084
EMIF_PERF_CNT_CFG	RW	32	0x0000 0088	0x4C00 0088	0x4D00 0088
EMIF_PERF_CNT_SEL	RW	32	0x0000 008C	0x4C00 008C	0x4D00 008C
EMIF_PERF_CNT_TIM	R	32	0x0000 0090	0x4C00 0090	0x4D00 0090
EMIF_READ_IDLE_CTRL	RW	32	0x0000 0090	0x4C00 0098	0x4D00 0098
EMIF_READ_IDLE_CTRL_SHDW	RW	32	0x0000 0090	0x4C00 009C	0x4D00 009C
EMIF_IRQSTATUS_RAW_SYS	RW	32	0x0000 00A4	0x4C00 00A4	0x4D00 00A4
EMIF_IRQSTATUS_RAW_LL	RW	32	0x0000 00A8	0x4C00 00A8	0x4D00 00A8

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_IRQSTATUS_SYS	RW	32	0x0000 00AC	0x4C00 00AC	0x4D00 00AC
EMIF_IRQSTATUS_LL	RW	32	0x0000 00B0	0x4C00 00B0	0x4D00 00B0
EMIF_IRQENABLE_SET_SYS	RW	32	0x0000 00B4	0x4C00 00B4	0x4D00 00B4
EMIF_IRQENABLE_SET_LL	RW	32	0x0000 00B8	0x4C00 00B8	0x4D00 00B8
EMIF_IRQENABLE_CLR_SYS	RW	32	0x0000 00BC	0x4C00 00BC	0x4D00 00BC
EMIF_IRQENABLE_CLR_LL	RW	32	0x0000 00C0	0x4C00 00C0	0x4D00 00C0
EMIF_ZQ_CONFIG	RW	32	0x0000 00C8	0x4C00 00C8	0x4D00 00C8
EMIF_TEMP_ALERT_CONFIG	RW	32	0x0000 00CC	0x4C00 00CC	0x4D00 00CC
EMIF_L3_ERR_LOG	R	32	0x0000 00D0	0x4C00 00D0	0x4D00 00D0
EMIF_DDR_PHY_CTRL_1	RW	32	0x0000 00E4	0x4C00 00E4	0x4D00 00E4
EMIF_DDR_PHY_CTRL_1_SHDW	RW	32	0x0000 00E8	0x4C00 00E8	0x4D00 00E8
EMIF_DDR_PHY_CTRL_2	RW	32	0x0000 00EC	0x4C00 00EC	0x4D00 00EC

16.3.6.2.2. EMIF Register Description

Note

This section contains only modified registers.

Table 16.3. EMIF_ZQ_CONFIG

Address Offset	0x0000 00C8		
Physical Address		**Instance**	EMIF
Description	SDRAM Output Impedance Calibration Config Register		
Type	RW		

31	30	29	28	27 26 25 24 23 22 21 20	19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
REG_ZQ_CS1EN	REG_ZQ_CS0EN	REG_ZQ_DUALCALEN	REG_ZQ_SFEXITEN	RESERVED	REG_ZQ_ZQINIT_MULT	REG_ZQ_ZQCL_MULT	REG_ZQ_REFINTERVAL

Bits	Field Name	Description	Type	Reset
31	REG_ZQ_CS1EN	Writing a 1 enables ZQ calibration for CS1.	RW	0x0
30	REG_ZQ_CS0EN	Writing a 1 enables ZQ calibration for CS0.	RW	0x0
29	REG_ZQ_DUALCALEN	ZQ Dual Calibration enable. Allows both ranks to be ZQ calibrated simultaneously. Setting this bit requires both chip selects to have a separate calibration resistor per device.	RW	0x0

Bits	Field Name	Description	Type	Reset
28	REG_ZQ_SFEXITEN	ZQCL on Self-Refresh, Active Power-Down, and Precharge Power-Down exit enable. Writing a 1 enables the issuing of ZQCL on Self-Refresh,~~Active Power-Down, and Precharge Power-Down~~exit.	RW	0x0
27:20	RESERVED	Reserved	R	0x00
19:18	REG_ZQ_ZQINIT_MULT	Indicates the number of ZQCL intervals that make up a ZQINIT interval, minus one..	RW	0x0
17:16	REG_ZQ_ZQCL_MULT	Indicates the number of ZQCS intervals that make up a ZQCL interval, minus one. ZQCS interval is defined by reg_zq_zqcs in EMIF_SDRAM_TIM_3.	RW	0x0
15:0	REG_ZQ_REFINTERVAL	Number of refresh periods between ZQCS commands. This field supports between one refresh period to 256 ms between ZQCS calibration commands. Refresh period is defined by reg_refresh_rate in EMIF_SDRAM_REF_CTRL register.	RW	0x0000

16.4. General-Purpose Memory Controller

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.5. Error Location Module

Refer to OMAP4470 Silicon Revision 1.0 TRM.

16.6. On-Chip Memory (OCM) Subsystem

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 17. SDMA

This chapter describes differences in the SDMA between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

17.1. sDMA Module Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.2. sDMA Controller Environment

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.3. sDMA Module Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4. sDMA Functional Description

17.4.1. sDMA Controller Power Management

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.2. sDMA Controller Interrupt Requests

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.3. Logical Channel Transfer Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.4. FIFO Queue Memory Pool

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.5. Addressing Modes

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.6. Packed Accesses

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.7. Burst Transactions

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.8. Endianism Conversion

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.9. Transfer Synchronization

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.10. Thread Budget Allocation

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.11. FIFO Budget Allocation

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.12. Chained Logical Channel Transfers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.13. Reprogramming an Active Channel

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.14. Packet Synchronization

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.15. Graphics Acceleration Support

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.16. Supervisor Modes

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.17. Posted and Nonposted Writes

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.18. Disabling a Channel During Transfer

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.19. FIFO Draining Mechanism

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.20. Linked List

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.21. Auto-Restore Feature

17.4.21.1. Save Process

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.21.2. Restore Process

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.21.3. SAR RAM

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.4.21.4. SAR ROM

The consecutive address registers that cannot be saved/restored with burst are changed.

17.4.21.5. SAR RAM Memory Allocation Reserved for Save and Restore

The percents of the SAR_RAM banks that are reserved for the SAR mechanism are slightly increased.

17.4.21.6. Register Mapping in SAR RAM

The following registers are added in SAR_RAM_1:

- CLK2_SGX_M1_BW_REGULATOR.L3_BW_R_BANDWIDTH
- CLK2_SGX_M1_BW_REGULATOR.L3_BW_R_WATERMARK
- CLK2_SGX_M2_BW_REGULATOR.L3_BW_R_BANDWIDTH
- CLK2_SGX_M2_BW_REGULATOR.L3_BW_R_WATERMARK
- CLK2_BB2D_M1_BW_REGULATOR.L3_BW_R_BANDWIDTH
- CLK2_BB2D_M1_BW_REGULATOR.L3_BW_R_WATERMARK
- CLK2_BB2D_M2_BW_REGULATOR.L3_BW_R_BANDWIDTH
- CLK2_BB2D_M2_BW_REGULATOR.L3_BW_R_WATERMARK
- CLK2_BB2D_M1_BW_LIMITER.L3_BW_LIMITER_BANDWIDTH_FRACTIONAL
- CLK2_BB2D_M1_BW_LIMITER.L3_BW_LIMITER_BANDWIDTH_INTEGER
- CLK2_BB2D_M1_BW_LIMITER.L3_BW_LIMITER_WATERMARK_0
- CLK2_BB2D_M2_BW_LIMITER.L3_BW_LIMITER_BANDWIDTH_FRACTIONAL
- CLK2_BB2D_M2_BW_LIMITER.L3_BW_LIMITER_BANDWIDTH_INTEGER
- CLK2_BB2D_M2_BW_LIMITER.L3_BW_LIMITER_WATERMARK_0
- CLK3_FLAGMUX_CLK3.L3_STATCOLL_MASK0
- SYSCTRL_PADCONF_CORE.CONTROL_HDMI_TX_PHY

The following registers are removed from the SAR_RAM_1:

- SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_1
- CLK1_DSS_BW_REGULATOR.L3_BW_R_BANDWIDTH
- CLK1_DSS_BW_REGULATOR.L3_BW_R_WATERMARK
- CLK2_ISS_BW_REGULATOR.L3_BW_R_BANDWIDTH
- CLK2_ISS_BW_REGULATOR.L3_BW_R_WATERMARK
- CLK2_SGX_BW_REGULATOR.L3_BW_R_BANDWIDTH
- CLK2_SGX_BW_REGULATOR.L3_BW_R_WATERMARK

The following register is added in SAR_RAM_3:

- CFG_AP.L4_AP_REGION_96_L

By the reason some registers are added, other removed inside the SAR_RAM banks, the Order and the SAR_RAM addresses are updated.

17.5. sDMA Basic Programming Model

Refer to OMAP4470 Silicon Revision 1.0 TRM.

17.6. sDMA Register Manual

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 18. Interrupt Controllers

This chapter describes differences in Interrupt Controllers between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

18.1. Interrupt Controllers Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

18.2. Interrupt Controllers Environment

Refer to OMAP4470 Silicon Revision 1.0 TRM.

18.3. Interrupt Controllers Integration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

18.3.1. Interrupts Mapping

- BB2D module is added. It can generate an interrupt (BB2D_IRQ) to the INTC_MPU (interrupt line MA_IRQ_125)
- L3 NoC statistics collector now supports an alarm mode. Statistics collector can generate an interrupt (L3_STAT_ALARM_IRQ) to the INTC_MPU (interrupt line MA_IRQ_60)
- The Full-Speed USB host controller (FSUSB) is removed. The following interrupt lines are now RESERVED (previously FSUSB interrupts):
  - MA_IRQ_89
  - MA_IRQ_90
  - MM_IRQ_56
  - MM_IRQ_59

18.4. Interrupt Controllers Functional Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

18.5. Interrupt Controllers Register Manual

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 19. Control Module

This chapter describes differencies in the Control Module between the OMAP4470 Silicon Revision 1.0 and OMAP4460 Silicon Revision 1.x.

19.1. Control Module Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.2. Control Module Environment

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.3. Control Module Integration

There are following changes in integration :

- In OMAP4470 Silicon Revision 1.0 device, the General Core control module, NOT only delivers the TSHUT signal to a GPIO3 controller input, but can be also optionally mapped to SCRM external warm reset logic.

This change in integration impacts figure *Control Module Integration*.

19.4. Control Module Functional Description

19.4.1. Control Module Block Diagram

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.2. Control Module Clock Configuration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.3. Control Module Software Reset

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.4. Control Module Power Management

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.5. Hardware Requests

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.6. Control Module Initialization

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.7. Control Module Instances

19.4.7.1. General Core Control Module Instance

Register CONTROL_STD_FUSE_OPP_DPLL_1 [19:18] MPU_DPLL_TRIM_FREQ bitfield is removed in OMAP4470 Silicon Revision 1.0 device. There is no need, software to analyze this bit, since ABB Set1 is NO longer applied at OPP_TURBO for MPU.

19.4.7.2. General Wakeup Control Module Instance

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.7.3. Device Core Control Module Instance

The OMAP4460 registers - CONTROL_AVDAC (physical address: 0x4A10 060C) and CONTROL_EFUSE_1 (physical address: 0x4A10 0700) are RESERVED in OMAP4470 Silicon Revision 1.0.

19.4.7.4. Device Wakeup Control Module Instance

The OMAP4460 register - CONTROL_GPIOWK (physical address: 0x4A31 E600) is RESERVED in OMAP4470 Silicon Revision 1.0.

19.4.8. PAD Functional Multiplexing and Configuration

Following updates are done to pad functional multiplexing and configuration schema :

- Pad multiplexing schema in WAKEUP domain is updated as follows:
  - The gpio_wk0-gpio_wk4 signals are also available in MuxMode=0x0 on their corresponding WKUP domain pads with identical names (gpio_wk0 - gpio_wk4). This impacts MuxMode bitfield value set of the registers, as follows:
    - CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1
    - CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3
    - CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL

  Refer to Table 19.1 for more details on WKUP mux mapping .
- Pad multiplexing schema in CORE domain is updated as follows:
  - The venc_656_data0 - venc_656_data7 signals are no longer present in MuxMode=0x4 at their corresponding pads in OMAP4460 Silicon Revision 1.x : gpmc_a16 - gpmc_a23. This impacts, MuxMode bitfield value set of the registers, as follows:
    - CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17
    - CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19
    - CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21
    - CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23
  - Signals usbc1_icusb_dp and usbc1_icusb_dm available in MuxMode=0x0 on their corresponding identically named pads (supporting 3V-compatible I/Os) in the OMAP4460 Silicon Revsion 1.x device, are replaced in OMAP4470 Silicon Revision 1.0 with the gpio_98 and gpio_99 signals (no longer supporting 3V I/Os) in MuxMode=0x0, respectively. As a consequence the impacted registers are also renamed, as follows:
    - CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP is renamed to CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_GPIO_98
    - CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK is renamed to CONTROL_CORE_PAD0_GPIO_99_PAD1_SDMMC1_CLK
  - Due to FS USB interface removal in the OMAP4470 Silicon Revision 1.0 device, the signal usbc1_icusb_txen muxed on the gpmc_wait2 pad (MuxMode=0x1) and signals usbc1_icusb_dp, usbc1_icusb_dm, usbc1_icusb_rcv, usbc1_icusb_txen (MuxMode2) muxed on the SDMMC5 i/f pads in OMAP4460 Silicon Revision 1.x, are no longer available on same pads in the OMAP4470 Silicon Revision 1.0 device. This impacts MuxMode bitfield values (which is changed to "reserved" for these signals) in following padconfiguration registers:
    - CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2
    - CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD
    - CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1

    The FS USB i/f removal also impacts table Table 19.2, Device Core Control Module Pad Configuration Register Fields.
- Other core and wakeup domain padconfiguration control register updates :
  - Register CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL - the I2C1_SDA_PULLUDENABLE and the I2C1_SDA_PULLTYPESELECT bit power-on reset values are changed from '1' to '0'. The internal weak PU/PD resistor at i2c1_sda pad is disabled by default.
  - Register CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP - the USBA0_OTG_DP_MUXMODE bitfield power-on reset value is changed form 0x7 (safe_mode) to 0x0 - to select the usba0_otg_dp signal by default at the usba0_otg_dp pad.
  - Register CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT - the USBA0_OTG_DM_MUXMODE bitfield power-on reset value is changed form 0x7 (safe_mode) to 0x0 - to select the usba0_otg_dm signal by default at the usba0_otg_dm pad.
  - Register CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K - the FREF_CLK4_OUT_PULLUDENABLE bit power-on reset value is changed from '1' to '0', i.e. the internal weak PU/PD resistor at the fref_clk4_out pad is disabled by default.
  - Register CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM - the bits [3] and [4] are no longer RESERVED. In OMAP4470 Silicon Revision 1.0 device -bitfields SYS_NRESPWRON_PULLUDENABLE and SYS_NRESPWRON_PULLTYPESELECT are added at these positions, respectively, to control associated internal weak PU/PD resistors at the sys_nrespwron pad.

- Register CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC - the JTAG_RTCK_PULLUDENABLE bit power-on-reset value is changed from '1' to '0' to disable jtag_rtck weak PU/PD resistor by default.
- Register CONTROL_I2C_0 - the power-on reset values of [18:17] I2C1_SDA_LOAD_BITS and [2:1] I2C1_SCL_LOAD_BITS are changed from 0x2 to 0x1.

- Duplicate wake-up event monitoring feature is updated as follows:
  - Register CONTROL_PADCONF_WAKEUPEVENT_2- because of usbc1_icusb_dp / usbc1_icusb_dm signals replacement with gpio_98 / gpio_99 signals in MuxMode=0x0, respectively, the OMAP4460 Silicon Revision 1.x - bits CONTROL_PADCONF_WAKEUPEVENT_2 [15] and CONTROL_PADCONF_WAKEUPEVENT_2 [16] are reassigned to monitor wakeupevent for gpio_98 and gpio_99 pads. As a consequence:
    - Bit CONTROL_PADCONF_WAKEUPEVENT_2[15] USBC1_ICUSB_DP_DUPLICATEWAKEUPEVENT is renamed to GPIO_98_DUPLICATEWAKEUPEVENT
    - Bit CONTROL_PADCONF_WAKEUPEVENT_2 [16] USBC1_ICUSB_DM_DUPLICATEWAKEUPEVENT is renamed to GPIO_99_DUPLICATEWAKEUPEVENT

Refer to Table 19.2 for more details on CORE domain mux mapping .

The pad-configuration muxmode sets are updated as follows:

Table 19.1. Device Wakeup Control Module Pad Configuration Register Fields

SYSCTRL_PADCONF_WKUP.[Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1[15:0]	0x040	~~reserved~~ gpio_wk0			gpio_wk0	c2c_pwkup		hw_dbg1	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1[31:16]	0x040	~~reserved~~ gpio_wk1			gpio_wk1			hw_dbg2	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3[15:0]	0x044	~~reserved~~ gpio_wk2			gpio_wk2			hw_dbg3	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3[31:16]	0x044	~~reserved~~ gpio_wk3			gpio_wk3			hw_dbg4	safe_mode
CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL[15:0]	0x048	~~reserved~~ gpio_wk4			gpio_wk4			hw_dbg5	safe_mode

Table 19.2. Device Core Control Module Pad Configuration Register Fields

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17 [15:0]	0x060	gpmc_a16	kpd_row4	c2c_datain0	gpio_40	~~venc_656_data0~~			safe_mode
CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17 [31:16]	0x060	gpmc_a17	kpd_row5	c2c_datain1	gpio_41	~~venc_656_data1~~			safe_mode
CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19 [15:0]	0x064	gpmc_a18	kpd_row6	c2c_datain2	gpio_42	~~venc_656_data2~~			safe_mode
CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19 [31:16]	0x064	gpmc_a19	kpd_row7	c2c_datain3	gpio_43	~~venc_656_data3~~			safe_mode
CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21 [15:0]	0x068	gpmc_a20	kpd_col4	c2c_datain4	gpio_44	~~venc_656_data4~~			safe_mode
CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21 [31:16]	0x068	gpmc_a21	kpd_col5	c2c_datain5	gpio_45	~~venc_656_data5~~			safe_mode
CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23 [15:0]	0x06C	gpmc_a22	kpd_col6	c2c_datain6	gpio_46	~~venc_656_data6~~			safe_mode

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23 [31:16]	0x06C	gpmc_a23	kpd_col7	c2c_datain7	gpio_47	~~venc_656_data7~~			safe_mode
CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2[31:16]	0x08C	gpmc_wait2	~~usbc1_icusb_txen~~ reserved	c2c_dataout3	gpio_100	sys_ndmareq0			safe_mode
~~CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP[15:0]~~ CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_GPIO_98[15:0]	0x0DC	usbb1_hsic_strobe			gpio_97				safe_mode
~~CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP[31:16]~~ CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_GPIO_98[31:16]	0x0DC	~~usbc1_icusb_dp~~ gpio_98			gpio_98				safe_mode
~~CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK[15:0]~~	0x0E0	~~usbc1_icusb_dm~~ gpio_99			gpio_99				safe_mode

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_GPIO_99_PAD1_SDMMC1_CLK [15:0]									
~~CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK [31:16]~~ CONTROL_CORE_PAD0_GPIO_99_PAD1_SDMMC1_CLK [31:16]	0x0E0	sdmmc1_clk		dpm_emu19	gpio_100				safe_mode
CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD [15:0]	0x148	sdmmc5_clk	mcspi2_clk	~~usbc1_icusb_dp~~ reserved	gpio_145		sdmmc2_clk		safe_mode
CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD [31:16]	0x148	sdmmc5_cmd	mcspi2_simo	~~usbc1_icusb_dm~~ reserved	gpio_146		sdmmc2_cmd		safe_mode
CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1 [15:0]	0x14C	sdmmc5_dat0	mcspi2_somi	~~usbc1_icusb_rcv~~ reserved	gpio_147		sdmmc2_dat0		safe_mode
CONTROL_CORE_PAD0_SD	0x14C	sdmmc5_dat1		~~usbc1_icusb_txen~~ reserved	gpio_148		sdmmc2_dat1		safe_mode

SYSCTRL_PADCONF_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
MMC5_DAT0_PAD1_SDMMC5_DAT1 [31:16]									

19.4.9. Extended-Drain I/O and PBIAS Cell

There are several functional changes:

- The PBIAS1 cell as well as the 3V-compatible extended drain I/O cells associated with the gpio_wk0 - gpio_wk2, usbc1_icusb_dp and usbc1_icusb_dm signals (MuxMode=0x0) in OMAP4460 Silicon Revision 1.x device are NO longer used in the OMAP4470 Silicon Revision 1.0 device. These I/Os supply voltage range is limited to 1.8V.
- As a consequence of the 1.8V I/O cell implementation for the gpio_wk0 - gpio_wk2, gpio_98 and gpio_99 pads in OMAP4470 Silicon Revision 1.0, the signals from their multiplexing sets, are also limited to support 1.8V operation. For more information about these pad sets of multiplexed signals , see Table 19.1 and Table 19.2.
- As a consequence of the PBIAS1 cell removal, all PBIAS1cell related bits from the CONTROL_PBIASLITE register are changed to RESERVED, as follows:
  - CONTROL_PBIASLITE [31] PBIASLITE1_HIZ_MODE
  - CONTROL_PBIASLITE [30] PBIASLITE1_SUPPLY_HI_OUT
  - CONTROL_PBIASLITE [29] PBIASLITE1_VMODE_ERROR
  - CONTROL_PBIASLITE [28] PBIASLITE1_PWRDNZ
  - CONTROL_PBIASLITE [27] PBIASLITE1_VMODE
  - CONTROL_PBIASLITE [20] USBC1_ICUSB_PWRDNZ
- As a consequence of the usbc1_icusb (3V-compatible) extended drain I/O cell removal, various related control bits from the CONTROL_MMC1 register are changed to RESERVED, as follows:
  - CONTROL_MMC1[24] USBC1_DR0_SPEEDCTRL
  - CONTROL_MMC1[22] USBC1_ICUSB_DP_PDDIS
  - CONTROL_MMC1[21] USBC1_ICUSB_DM_PDDIS
- As a consequence of the gpio_wk0 - gpio_wk4 (3V-compatible) extended drain I/O cell removal, the whole CONTROL_GPIOWK register is RESERVED.
- The above stated changes impact following figures/tables in section *Band Gap Voltage and Temperature Sensor, as follows:*
  - Updated figure *Functional Block Diagram*
  - Updated table - *PBIAS Cell and Extended-Drain I/O Pin CONTROL_PBIAS_LITE Bit Control*
  - Section *PBIAS Cell*
  - Section and Figures - *Extended-Drain I/O, PBIAS/Extended-Drain I/O Cells Control Signals*
  - Section - *PBIAS Error Generation*
  - Section - *Critical Timing Requirements*

19.4.10. Band Gap Voltage and Temperature Sensor

Thermal management schema is updated as follows :

- Besides the GPIO3 controller interrupt the OMAP4470 Silicon Revision 1.0 TSHUT signal can be otpionally configured to generate a hardware warm reset to the PRCM module.
- The SYSCTRL_PADCONF_WKUP. CONTROL_WKUP_CONTROL_SPARE_RW [0] bit (RESERVED in OMAP4460 Silicon Revision 1.0) is used to enable the hardware warm reset generation when the on-die measured hottest spot temperature crosses a programmable fatal threshold.
- The SYSCTRL_GENERAL_CORE. CONTROL_BANDGAP_CTRL [31] SINGLE_MODE power-on reset value is changed from 0b0 to 0b1(the repeated single conversions mode is the default mode).
- The SYSCTRL_PADCONF_CORE.CONTROL_TSHUT_THRESHOLD register bitfields:
  - CONTROL_TSHUT_THRESHOLD [25:16] TSHUT_HOT in OMAP4470 Silicon Revision 1.0 device is writable only once after power-on reset
  - CONTROL_TSHUT_THRESHOLD [9:0] TSHUT_COLD in OMAP4470 Silicon Revision 1.0 device is writable only once after power-on reset
- The above stated changes impact section *Band Gap Voltage and Temperature Sensor, as follows:*

- Updated figure *Functional Block Diagram*
- Updated table - *General Core Control Thermal Logic Outputs Description*
- Updated section *Temperature Sensor*
- Section - *Programmable-Delay Repeated Single Conversions*
- Section - *Thermal Shutdown Functionality Comparators*
  - A new figure - *TSHUT Output Mapping Diagram* is added to better explain updated TSHUT mapping capabilities in the OMAP4470 Silicon Revision 1.0 device.
- A new section called *Thermal Data Post-Processing Logic* is added
- Table *ADC Code Versus Temperature* is updated

19.4.11. Hardware Observability

19.4.11.1. Device Internal Signals Observability Overview

Figure Device Internal Signals Observability Overview is impacted. The DSS block observability is removed and BB2D observability is added.

19.4.11.2. Observability Gating Capabilities

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.11.3. Observability Signals Multiplexing at General Core/Wakeup Control Level

The General Core Control Module observability Core domain multiplex sets are updated with following new input signals:

- Added power management observability inputs from the new module - BB2D accelerator, as follows:
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_1[3:0] MODE =0xC : hwobs_bb2d_sys_interrupt_reqz
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_2[3:0] MODE =0xC : hwobs_bb2d_mconnect_1
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_3[3:0] MODE =0xC: hwobs_bb2d_mconnect_0
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_4[3:0] MODE =0xC: hwobs_bb2d_sconnect_2
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_5[3:0] MODE =0xC: hwobs_bb2d_sconnect_1
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_6[3:0] MODE =0xC: hwobs_bb2d_sconnect_0
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_7[3:0] MODE =0xC: hwobs_bb2d_pgoodin
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_8[3:0] MODE =0xC: hwobs_bb2d_ponin
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_9[3:0] MODE =0xC: hwobs_bb2d_ponout
- Removed DSS (display subsystem) observability inputs because of the removed VDAC functionality.
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_9 [3:0] MODE = 0xB: hwobs_dssvenctvdetgp signal is removed and changed to RESERVED
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_10[3:0] MODE =0xB : hwobs_dssdacpwrdndaczcvbs_y signal is removed and changed to RESERVED
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_11[3:0] MODE =0xB : hwobs_dssdacpwrdndaczchroma signal is removed and changed to RESERVED
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_12[3:0] MODE =0xB : hwobs_dssdacpwrdndaccvbs signal is removed and changed to RESERVED
  - CONTROL_CORE_CONF_DEBUG_SEL_TST_13[3:0] MODE =0xB : hwobs_dssdacpwrdnbgz signal is removed and changed to RESERVED

19.4.11.4. Observability Signals Multiplexing at Device Core Control Level

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.11.5. Observability Signals Sourced at Module Level

DSS observability signals section is removed. *A section , BB2D Accelerator Observable Signals* with observability description table is added.

The PRCM observability multiplexing sets described into tables - CM2 Observable Signals, CM1 Observable signals and PRM Observable Signals are updated. See the OMAP4470 Silicon Revision 1.0 TRM.

19.4.12. Functional Register Description

19.4.12.1. DSP Boot Register

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.12.4. CSI Receiver Control Register

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.12.5. Protection Status Registers

Two bitfields are added at positions CONTROL_SEC_ERR_STATUS_FUNC [9] and CONTROL_SEC_ERR_STATUS_DEBUG [9], respectively, due to addition of the BB2D accelerator in the OMAP4470 Silicon Revision 1.0 Device.

19.4.12.6. Protection SDRAM Configuration Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.12.7. Register Controls for the LPDDR2IO1/LPDDR2IO2 PHY Buffer Modes

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.12.8. Reference voltage for OMAP LPDDR2IO1/LPDDR2IO2 I/O buffers and LPDDR2 memory

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.12.9. EMIF DLL Master/Slave Specific Registers

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.12.10. Force MPU Write Nonposted Transactions Control Register

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.4.12.11. Signal Integrity Parameter Control Registers With Pad Group Assignment

Following updates impacts tables - *Core Domain GPIO I/O Signal Group Parameter Controls to Different Interface I/O Pads Mapping* and *Wake-Up Domain GPIO Signal Group Parameter Controls to Different Interface I/O Pads Mapping* of the section - *Device Interfaces Signal Group Controls Mapping* :

- Core and wakeup domain pad group signal control register updates:
  - GPIO_DR12_SC bitfield is added at previous RESERVED location CONTROL_SMART1IO_PADCONF_2 [21:20] as a slew mode control of the newly defined signal parameter pad group - gpio_dr12.
  - GPIO_DR12_LB bitfield is added at previous RESERVED location CONTROL_SMART1IO_PADCONF_3 [21:20] as a load control of the newly defined signal parameter pad group - gpio_dr12.
  - CONTROL_SMART1NOPMIO_PADCONF_0 [13:12] GPIOWK4_DR0_SC bitfield is changed to RESERVED, and the bit-field GPIO_DR11_SC is added at the previous RESERVED [11:10] location as a slew mode control of the newly defined signal parameter pad group - gpio_dr11.
  - CONTROL_SMART1NOPMIO_PADCONF_1 [13:12] GPIOWK4_DR0_LB bitfield is changed to RESERVED, and the bit-field GPIO_DR11_LB is added at the previous [11:10] RESERVED location as a load control of the newly defined signal parameter pad group - gpio_dr11.

19.4.12.12. Dual Voltage-Supplied Peripheral Controls

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.6. Control Module Register Manual

19.6.1. Control Module Instance Summary

Table 19.3. Control Module Instance Summary

Module instance	Base Address	Size	Description
SYSCTRL_GENERAL_CORE	0x4A00 2000	4KB	Module
SYSCTRL_GENERAL_WKUP	0x4A30 C000	4KB	Module
SYSCTRL_PADCONF_CORE	0x4A10 0000	4KB	Module
SYSCTRL_PADCONF_WKUP	0x4A31 E000	4KB	Module

19.6.2. SYSCTRL_GENERAL_CORE Register Summary

Table 19.4. SYSCTRL_GENERAL_CORE Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_GEN_CORE_REVISION	R	32	0x00000000	0x4A002000
CONTROL_GEN_CORE_HWINFO	R	32	0x00000004	0x4A002004
CONTROL_GEN_CORE_SYSCONFIG	RW	32	0x00000010	0x4A002010
CONTROL_STD_FUSE_DIE_ID_0	R	32	0x0000 0200	0x4A00 2200
CONTROL_ID_CODE	R	32	0x0000 0204	0x4A00 2204
CONTROL_STD_FUSE_DIE_ID_1	R	32	0x0000 0208	0x4A00 2208
CONTROL_STD_FUSE_DIE_ID_2	R	32	0x0000 020C	0x4A00 220C
CONTROL_STD_FUSE_DIE_ID_3	R	32	0x0000 0210	0x4A00 2210
CONTROL_STD_FUSE_PROD_ID_0	R	32	0x0000 0214	0x4A00 2214
CONTROL_STD_FUSE_PROD_ID_1	R	32	0x0000 0218	0x4A00 2218
CONTROL_STD_FUSE_USB_CONF	R	32	0x0000 021C	0x4A00 221C
CONTROL_STD_FUSE_CONF	R	32	0x0000 0220	0x4A00 2220
CONTROL_STD_FUSE_OPP_VDD_WKUP	R	32	0x0000 0228	0x4A00 2228
CONTROL_STD_FUSE_OPP_VDD_IVA_0	R	32	0x0000 022C	0x4A00 222C
CONTROL_STD_FUSE_OPP_VDD_IVA_1	R	32	0x0000 0230	0x4A00 2230
CONTROL_STD_FUSE_OPP_VDD_IVA_2	R	32	0x0000 0234	0x4A00 2234
CONTROL_STD_FUSE_OPP_VDD_IVA_3	R	32	0x0000 0238	0x4A00 2238
RESERVED	R	32	0x0000 023C	0x4A00 223C
CONTROL_STD_FUSE_OPP_VDD_MPU_0	R	32	0x0000 0240	0x4A00 2240
CONTROL_STD_FUSE_OPP_VDD_MPU_1	R	32	0x0000 0244	0x4A00 2244

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_STD_FUSE_OPP_VDD_MPU_2	R	32	0x0000 0248	0x4A00 2248
CONTROL_STD_FUSE_OPP_VDD_MPU_3	R	32	0x0000 024C	0x4A00 224C
RESERVED	R	32	0x0000 0250	0x4A00 2250
CONTROL_STD_FUSE_OPP_VDD_CORE_0	R	32	0x0000 0254	0x4A00 2254
CONTROL_STD_FUSE_OPP_VDD_CORE_1	R	32	0x0000 0258	0x4A00 2258
CONTROL_STD_FUSE_OPP_VDD_CORE_2	R	32	0x0000 025C	0x4A00 225C
CONTROL_STD_FUSE_OPP_BGAP	R	32	0x0000 0260	0x4A00 2260
CONTROL_STD_FUSE_OPP_DPLL_0	R	32	0x0000 0264	0x4A00 2264
CONTROL_STD_FUSE_OPP_DPLL_1	R	32	0x0000 0268	0x4A00 2268
CONTROL_STATUS	R	32	0x0000 02C4	0x4A00 22C4
CONTROL_SEC_ERR_STATUS_FUNC	RW	32	0x0000 02D0	0x4A00 22D0
CONTROL_SEC_ERR_STATUS_DEBUG	RW	32	0x0000 02D4	0x4A00 22D4
RESERVED	R	32	0x0000 02D8	0x4A00 22D8
RESERVED	R	32	0x0000 02DC	0x4A00 22DC
CONTROL_DEV_CONF	RW	32	0x0000 0300	0x4A00 2300
CONTROL_DSP_BOOTADDR	RW	32	0x0000 0304	0x4A00 2304
CONTROL_LDOVBB_IVA_VOLTAGE_CTRL	RW	32	0x0000 0314	0x4A00 2314
CONTROL_LDOVBB_MPU_VOLTAGE_CTRL	RW	32	0x0000 0318	0x4A00 2318
CONTROL_LDOSRAM_IVA_VOLTAGE_CTRL	RW	32	0x0000 0320	0x4A00 2320
CONTROL_LDOSRAM_MPU_VOLTAGE_CTRL	RW	32	0x0000 0324	0x4A00 2324
CONTROL_LDOSRAM_CORE_VOLTAGE_CTRL	RW	32	0x0000 0328	0x4A00 2328
CONTROL_TEMP_SENSOR	RW	32	0x0000 032C	0x4A00 232C
CONTROL_DPLL_NWELL_TRIM_0	RW	32	0x0000 0330	0x4A00 2330
CONTROL_DPLL_NWELL_TRIM_1	RW	32	0x0000 0334	0x4A00 2334
RESERVED	RW	32	0x0000 0338	0x4A00 2338
CONTROL_USBOTGHS_CONTROL	RW	32	0x0000 033C	0x4A00 233C
CONTROL_DSS_CONTROL	RW	32	0x0000 0340	0x4A00 2340
RESERVED	RO	32	0x0000 0344	0x4A00 2344
CONTROL_CORTEX_	RW	32	0x0000 0348	0x4A00 2348

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
M3_MMUADDRTRANSLTR				
CONTROL_CORTEX_M3_MMUADDR-LOGICTR	RW	32	0x0000 034C	0x4A00 234C
CONTROL_HWOBS_CONTROL	RW	32	0x0000 0350	0x4A00 2350
CONTROL_EMIF1_OFFSET	RW	32	0x0000 0360	0x4A00 2360
CONTROL_EMIF2_OFFSET	RW	32	0x0000 0364	0x4A00 2364
CONTROL_EMIF1_MASTER_CODE_0	R	32	0x0000 0368	0x4A00 2368
CONTROL_EMIF1_MASTER_CODE_1	R	32	0x0000 036C	0x4A00 236C
CONTROL_EMIF2_MASTER_CODE_0	R	32	0x0000 0370	0x4A00 2370
CONTROL_EMIF2_MASTER_CODE_1	R	32	0x0000 0374	0x4A00 2374
CONTROL_BANDGAP_CTRL	RW	32	0x0000 0378	0x4A00 2378
CONTROL_BANDGAP_COUNTER	RW	32	0x0000 037C	0x4A00 237C
CONTROL_BANDGAP_THRESHOLD	RW	32	0x0000 0380	0x4A00 2380
CONTROL_TSHUT_THRESHOLD	RW	32	0x0000 0384	0x4A00 2384
CONTROL_BANDGAP_STATUS	R	32	0x0000 0388	0x4A00 2388
CONTROL_FORCEWRNP	RW	32	0x0000 03C0	0x4A00 23C0
CONTROL_GEN_CORE_OCPREG_SPARE	RW	32	0x0000 03FC	0x4A00 23FC
CONTROL_DEBOBS_FINAL_MUX_SEL	RW	32	0x0000 0400	0x4A00 2400
RESERVED	RO	32	0x0000 0404	0x4A00 2404
CONTROL_DE-BOBS_MMR_MPU	RW	32	0x0000 0408	0x4A00 2408
RESERVED	RO	32	0x0000 0410	0x4A00 2410
RESERVED	RO	32	0x0000 0414	0x4A00 2414
RESERVED	RO	32	0x0000 0418	0x4A00 2418
RESERVED	RO	32	0x0000 041C	0x4A00 241C
RESERVED	RO	32	0x0000 0420	0x4A00 2420
RESERVED	RO	32	0x0000 0424	0x4A00 2424
CONTROL_CONF_SDMA_REQ_SEL0	RW	32	0x0000 042C	0x4A00 242C
CONTROL_CONF_SDMA_REQ_SEL1	RW	32	0x0000 0430	0x4A00 2430
CONTROL_CONF_SDMA_REQ_SEL2	RW	32	0x0000 0434	0x4A00 2434
CONTROL_CONF_SDMA_REQ_SEL3	RW	32	0x0000 0438	0x4A00 2438
CONTROL_CONF_CLK_SEL0	RW	32	0x0000 0440	0x4A00 2440

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_CONF_CLK_SEL1	RW	32	0x0000 0444	0x4A00 2444
CONTROL_CONF_CLK_SEL2	RW	32	0x0000 0448	0x4A00 2448
CONTROL_CONF_DPLL_FREQ-LOCK_SEL	RW	32	0x0000 044C	0x4A00 244C
CONTROL_CONF_DPLL_TINITZ_SEL	RW	32	0x0000 0450	0x4A00 2450
CONTROL_CONF_DPLL_PHASELOCK_SEL	RW	32	0x0000 0454	0x4A00 2454
RESERVED	RW	32	0x0000 0458	0x4A00 2458
CONTROL_CONF_DPLL_TENABLE_SEL	RW	32	0x0000 045C	0x4A00 245C
CONTROL_CONF_DPLL_BYPASSACK_SEL	RW	32	0x0000 0464	0x4A00 2464
CONTROL_CONF_DPLL_IDLE_SEL	RW	32	0x0000 0468	0x4A00 2468
CONTROL_CORE_CONF_DEBUG_SEL_TST_0	RW	32	0x0000 0480	0x4A00 2480
CONTROL_CORE_CONF_DEBUG_SEL_TST_1	RW	32	0x0000 0484	0x4A00 2484
CONTROL_CORE_CONF_DEBUG_SEL_TST_2	RW	32	0x0000 0488	0x4A00 2488
CONTROL_CORE_CONF_DEBUG_SEL_TST_3	RW	32	0x0000 048C	0x4A00 248C
CONTROL_CORE_CONF_DEBUG_SEL_TST_4	RW	32	0x0000 0490	0x4A00 2490
CONTROL_CORE_CONF_DEBUG_SEL_TST_5	RW	32	0x0000 0494	0x4A00 2494
CONTROL_CORE_CONF_DEBUG_SEL_TST_6	RW	32	0x0000 0498	0x4A00 2498
CONTROL_CORE_CONF_DEBUG_SEL_TST_7	RW	32	0x0000 049C	0x4A00 249C
CONTROL_CORE_CONF_DEBUG_SEL_TST_8	RW	32	0x0000 04A0	0x4A00 24A0
CONTROL_CORE_CONF_DEBUG_SEL_TST_9	RW	32	0x0000 04A4	0x4A00 24A4
CONTROL_CORE_CONF_DEBUG_SEL_TST_10	RW	32	0x0000 04A8	0x4A00 24A8
CONTROL_CORE_CONF_DEBUG_SEL_TST_11	RW	32	0x0000 04AC	0x4A00 24AC
CONTROL_CORE_CONF_DEBUG_SEL_TST_12	RW	32	0x0000 04B0	0x4A00 24B0

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_CORE_CONF_DEBUG_SEL_TST_13	RW	32	0x0000 04B4	0x4A00 24B4
CONTROL_CORE_CONF_DEBUG_SEL_TST_14	RW	32	0x0000 04B8	0x4A00 24B8
CONTROL_CORE_CONF_DEBUG_SEL_TST_15	RW	32	0x0000 04BC	0x4A00 24BC
CONTROL_CORE_CONF_DEBUG_SEL_TST_16	RW	32	0x0000 04C0	0x4A00 24C0
CONTROL_CORE_CONF_DEBUG_SEL_TST_17	RW	32	0x0000 04C4	0x4A00 24C4
CONTROL_CORE_CONF_DEBUG_SEL_TST_18	RW	32	0x0000 04C8	0x4A00 24C8
CONTROL_CORE_CONF_DEBUG_SEL_TST_19	RW	32	0x0000 04CC	0x4A00 24CC
CONTROL_CORE_CONF_DEBUG_SEL_TST_20	RW	32	0x0000 04D0	0x4A00 24D0
CONTROL_CORE_CONF_DEBUG_SEL_TST_21	RW	32	0x0000 04D4	0x4A00 24D4
CONTROL_CORE_CONF_DEBUG_SEL_TST_22	RW	32	0x0000 04D8	0x4A00 24D8
CONTROL_CORE_CONF_DEBUG_SEL_TST_23	RW	32	0x0000 04DC	0x4A00 24DC
CONTROL_CORE_CONF_DEBUG_SEL_TST_24	RW	32	0x0000 04E0	0x4A00 24E0
CONTROL_CORE_CONF_DEBUG_SEL_TST_25	RW	32	0x0000 04E4	0x4A00 24E4
CONTROL_CORE_CONF_DEBUG_SEL_TST_26	RW	32	0x0000 04E8	0x4A00 24E8
CONTROL_CORE_CONF_DEBUG_SEL_TST_27	RW	32	0x0000 04EC	0x4A00 24EC
CONTROL_CORE_CONF_DEBUG_SEL_TST_28	RW	32	0x0000 04F0	0x4A00 24F0
CONTROL_CORE_CONF_DEBUG_SEL_TST_29	RW	32	0x0000 04F4	0x4A00 24F4
CONTROL_CORE_CONF_DEBUG_SEL_TST_30	RW	32	0x0000 04F8	0x4A00 24F8
CONTROL_CORE_CONF_DEBUG_SEL_TST_31	RW	32	0x0000 04FC	0x4A00 24FC

19.6.3. SYSCTRL_GENERAL_CORE Register Description

Note

This section contains only modified registers.

Table 19.5. CONTROL_STD_FUSE_CONF

Address Offset	0x0000 0220		
Physical Address	Please refer toTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard fuse configuration register. The register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read only		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															STD_FUSE_FACE_DETECT_DISABLE	STD_FUSE_CRYPTO_DISABLE	STD_FUSE_MODEM3G_DISABLE	STD_FUSE_CH_SPEEDUP_DISABLE	STD_FUSE_ROM_HIDE	STD_FUSE_DPLL_CLK_TRIMMING_DISABLE	STD_FUSE_MAGICGATE_EN	RESERVED	STD_FUSE_ISS_EFUSE1_EN	STD_FUSE_ISS_EFUSE2_EN	STD_FUSE_ISS_EFUSE3_EN	STD_FUSE_ISS_EFUSE4_EN	STD_FUSE_SGX544_3D_CLOCK_SOURCE	STD_FUSE_SGX544_3D_DISABLE	STD_FUSE_CORTEXA9_MPU_DISABLE	BSC_ACCESS_PROTECT	CUST_IEEE1500_DISABLE

Bits	Field Name	Description	Type	Reset
31:17	RESERVED	Reserved	R	0x0000
16	STD_FUSE_FACE_DETECT _DISABLE	Disables face detect Read 0x1: disables face detect Read 0x0: enables face detect	R	0x-
15	STD_FUSE_CRYPTO_DISA BLE	Disables cryptographic modules Read 0x1: disables cryptographic modules Read 0x0: enables cryptographic modules	R	0x-
14	STD_FUSE_MODEM3G_DIS ABLE	Disables the 3G modem. Read 0x1: disables 3G modem Read 0x0: enables 3G modem	R	0x-
13	STD_FUSE_CH_SPEEDUP_ DISABLE	ROM code settings for configuration header block and speedup block. Only SW access (no hardware access). Read 0x1: disables CH and speedup Read 0x0: enables CH and speedup	R	0x-
12	STD_FUSE_ROM_HIDE	MPU BOOT ROM space (4KB ROM code protect ion). Connects to MPU.PIROMPROTECT Read 0x1: BOOT ROM upper 4KB region becomes reserved Read 0x0: BOOT ROM space is 128KB	R	0x-
		Controls DPLLs		

Bits	Field Name	Description	Type	Reset
11	STD_FUSE_DPLL_CLK_TRIMMING_DISABLE	Read 0x1: disables DPLL trimming Read 0x0: enables DPLL trimming	R	0x-
~~9~~	~~STD_FUSE_DSS_VENC_MVENAB~~	~~Enables implementation specific features. Controls DSS_VENC_MVENAB.~~ ~~Read 0x1: enables DSS_VENC_MVENAB~~ ~~Read 0x0: disables DSS_VENC_MVENAB~~	~~R~~	~~0~~
10:9	RESERVED	Reserved	R	0
8	STD_FUSE_ISS_EFUSE4_EN	Enables implementation specific features. Controls ISS.EFUSE4_EN. Sets to 1. Read 0x1: enables ISS EFUSE4 Read 0x0: disables ISS EFUSE4	R	0x1
7	STD_FUSE_ISS_EFUSE3_EN	Enables implementation specific features. Controls ISS.EFUSE3_EN. Sets to 0. Read 0x1: enables ISS EFUSE3 Read 0x0: disables ISS EFUSE3	R	0x0
6	STD_FUSE_ISS_EFUSE2_EN	Enables implementation specific features. Controls ISS.EFUSE2_EN. Sets to 0. Read 0x1: enables ISS EFUSE2 Read 0x0: disables ISS EFUSE2	R	0x0
5	STD_FUSE_ISS_EFUSE1_EN	Enables implementation specific features. Controls ISS.EFUSE1_EN. Sets to 0. Read 0x1: enables ISS EFUSE1 Read 0x0: disables ISS EFUSE1	R	0x0
4	STD_FUSE_SGX544_3D_CLOCK_SOURCE	force 3D graphic engine clock source	R	0x-
3	STD_FUSE_SGX544_3D_DISABLE	disable the 3D Gx engine (SGX544) Read 0x1: disables SGX Read 0x0: enables SGX	R	0x-
2	STD_FUSE_CORTEXA9_MPU_DISABLE	Configures Cortex-A9 MPU boot mode. It disables one Cortex-A9 core. Read 0x1: boot IP mode Read 0x0: boot SMP mode	R	0x-
1	BSC_ACCESS_PROTECT	reserved for bsc_access protect	R	0x-
0	CUST_IEEE1500_DISABLE	Customer E-Fuse control / IEEE1500 access path disable	R	0x-

Table 19.6. CONTROL_STD_FUSE_OPP_DPLL_1

Address Offset	0x0000 0268		
Physical Address	Please refer toTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP DPLL. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										IVA_RBB_TURBO	MPU_RBB_TURBO	RESERVED																			

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21	IVA_RBB_TURBO	If trimmed, ABB (Adaptive Body Bias) set2 mode c an be enabled at OPP TURBO on IVA 0x0: IVA ABB set2 voltage is NOT trimmed 0x1: IVA ABB set2 voltage is trimmed	R	0x-[1]
20	MPU_RBB_TURBO	IIf trimmed, ABB set2 mode can be enabled at OPP TURBO on MPU. 0x0: MPU ABB set2 voltage is NOT trimmed 0x1: MPU ABB set2 voltage is trimmed	R	0x-[1]
~~19:18~~	MPU_DPLL_TRIM_FREQ	~~Lock frequency at which the MPU DPLL is trim med. The DPLL can be locked at any valid frequen cies up to this value.~~ ~~0x0: 2 GHz~~ ~~0x1: 2.4 GHz~~ ~~0x2: Reserved~~ ~~0x3: 3 GHz~~	R	0x-
~~17~~19:0	RESERVED		R	0x000

1. The default value is the value fused during device production

Table 19.7. Register Call Summary for Register CONTROL_STD_FUSE_OPP_DPLL_1

Control Module Functional Description

- General Core Control Module Instance:[0]

Table 19.8. CONTROL_SEC_ERR_STATUS_FUNC

Address Offset	0x0000 02D0		
Physical Address	Please refer toTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Firewall Error Status functional Register Access conditions. Read Only		
Type	R		

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="11">RESERVED</td><td>C2C_INIT_FW_ERROR</td><td>L4_AUDIOBE_FW_ERROR</td><td>DEBUGSS_FW_ERROR</td><td>L4_CONFIG_FW_ERROR</td><td>L4_PERIPH_FW_ERROR</td><td>ISS_FW_ERROR</td><td>DSS_FW_ERROR</td><td>SGX_FW_ERROR</td><td>C2C_FW_ERROR</td><td colspan="2">RESERVED</td><td>BB2D_FW_ERROR</td><td colspan="2">RESERVED</td><td>SL2_FW_ERROR</td><td>DUAL_CORTEX_M3_FW_ERROR</td><td>IVAHD_FW_ERROR</td><td>EMIF_FW_ERROR</td><td>GPMC_FW_ERROR</td><td>L3RAM_FW_ERROR</td><td>RESERVED</td></tr>
</table>

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	C2C_INIT_FW_ERROR	C2C init firewall. MID config: unused (reserved) 0x0: No error from firewall 0x1: Error from firewall	R	0
19	L4_AUDIOBE_FW_ERROR	L4 AudioBE firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
		DebugSS firewall		

Bits	Field Name	Description	Type	Reset
18	DEBUGSS_FW_ERROR	0x0: No error from firewall 0x1: Error from firewall	R	0
17	L4_CONFIG_FW_ERROR	L4 Config firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
16	L4_PERIPH_FW_ERROR	L4 PER firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
15	ISS_FW_ERROR	ISS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
14	DSS_FW_ERROR	DSS firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
13	SGX_FW_ERROR	SGX firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
12	C2C_FW_ERROR	C2C firewall. MID config: unused (reserved). 0x0: No error from firewall 0x1: Error from firewall	R	0
11:~~7~~10	RESERVED	Reserved	R	0
9	~~RESERVED~~ BB2D_FW_ERROR	~~Reserved~~BB2D firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
8:7	RESERVED	Reserved	R	0
6	SL2_FW_ERROR	SL2 firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
5	DUAL_CORTEX_M3_FW_ERROR	Dual Cortex M3 firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
4	IVAHD_FW_ERROR	IVAHD firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
3	EMIF_FW_ERROR	EMIF firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
2	GPMC_FW_ERROR	GPMC firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
1	L3RAM_FW_ERROR	L3RAM firewall 0x0: No error from firewall 0x1: Error from firewall	R	0
0	RESERVED	Reserved	R	0

Table 19.9. Register Call Summary for Register CONTROL_SEC_ERR_STATUS_FUNC

Control Module Functional Description

- Protection Status Registers:[0]

Table 19.10. CONTROL_SEC_ERR_STATUS_DEBUG

Address Offset	0x0000 02D4		
Physical Address	Please refer to Table 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Error Status debug Register. Read All / Write All. Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	31:21	20	19	18	17	16	15	14	13	12	11:10	9	8:7	6	5	4	3	2	1	0
Field	RESERVED	C2C_INIT_DBGFW_ERROR	L4_AUDIOBE_DBGFW_ERROR	DEBUGSS_DBGFW_ERROR	L4_CONFIG_DBGFW_ERROR	L4_PERIPH_DBGFW_ERROR	ISS_DBGFW_ERROR	DSS_DBGFW_ERROR	SGX_DBGFW_ERROR	C2C_DBGFW_ERROR	RESERVED	BB2D_DBGFW_ERROR	RESERVED	SL2_DBGFW_ERROR	DUAL_CORTEX_M3_DBGFW_ERROR	IVAHD_DBGFW_ERROR	EMIF_DBGFW_ERROR	GPMC_DBGFW_ERROR	L3RAM_DBGFW_ERROR	RESERVED

Bits	Field Name	Description	Type	Reset
31:21	RESERVED		R	0x000
20	C2C_INIT_DBGFW_ERROR	C2C init debug firewall. MID config: unused (res erved). 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
19	L4_AUDIOBE_DBGFW_ERR OR	L4 AudioBE debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
18	DEBUGSS_DBGFW_ERROR	DebugSS debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
17	L4_CONFIG_DBGFW_ER-ROR	L4 Config debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
16	L4_PERIPH_DBGFW_ER-ROR	L4 PER debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
15	ISS_DBGFW_ERROR	ISS debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
14	DSS_DBGFW_ERROR	DSS debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
13	SGX_DBGFW_ERROR	SGX debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
12	C2C_DBGFW_ERROR	c2c debug firewall. MID config: unused (reserved). 0x0: No error from firewall	RW Wr1toClr	0

Bits	Field Name	Description	Type	Reset
		0x1: Error from firewall		
11:~~7~~10	RESERVED	Reserved	R	0
9	~~RESERVED~~ BB2D_DBGFW_ERROR	~~Reserved~~BB2D debug firewall 0x0: No error from firewall 0x1: Error from firewall	~~R~~RW Wr1toClr	0
8:7	RESERVED	Reserved	R	0
6	SL2_DBGFW_ERROR	SL2 debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
5	DUAL_CORTEX_M3_DBGFW_ERROR	Dual Cortex M3 debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
4	IVAHD_DBGFW_ERROR	IVAHD debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
3	EMIF_DBGFW_ERROR	EMIF debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
2	GPMC_DBGFW_ERROR	GPMC debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
1	L3RAM_DBGFW_ERROR	L3RAM debug firewall 0x0: No error from firewall 0x1: Error from firewall	RW Wr1toClr	0
0	RESERVED	Reserved	R	0

Table 19.11. Register Call Summary for Register CONTROL_SEC_ERR_STATUS_DEBUG

Control Module Functional Description

- Protection Status Registers:[0]

Table 19.12. CONTROL_BANDGAP_CTRL

Address Offset	0x0000 0378		
Physical Address	0x4A00 2378	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30–2	1	0
SINGLE_MODE	RESERVED	MASK_HOT	MASK_COLD

Bits	Field Name	Description	Type	Reset
31	SINGLE_MODE	Toggles between single mode or continuous mode (repeated single mode) 0x0: Single mode selected	RW	~~0~~1

Bits	Field Name	Description	Type	Reset
		0x1: Continuous mode selected		
30:2	RESERVED		R	0x0000 0000
1	MASK_HOT	Mask for hot events 0x0: hot event is masked 0x1:	RW	0
0	MASK_COLD	Mask for cold events 0x0: cold event is masked 0x1:	RW	0

Table 19.13. Register Call Summary for Register CONTROL_BANDGAP_CTRL

Control Module Functional Description

- Band Gap Voltage and Temperature Sensor:[0]

Table 19.14. CONTROL_TSHUT_THRESHOLD

Address Offset	0x0000 0384		
Physical Address	0x4A00 2384	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap tshut threshold Access conditions. Read: unrestricted, Write: unrestricted One time writable only (after device power-on reset) register		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TSHUT_HOT										RESERVED						TSHUT_COLD									

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	TSHUT_HOT	Tshut Threshold for hot temperature. Code value must not exceed the device junction (hottest spot) maximal allowed temperature minus the device temperature sensor offset estimated at current conditions.	RW[1]	0x000
15:10	RESERVED		R	0x00
9:0	TSHUT_COLD	Tshut Threshold for cold temperature	RW[1]	0x000

1. One time writable only (after device power-on reset) bitfield

Table 19.15. Register Call Summary for Register CONTROL_TSHUT_THRESHOLD

Control Module Functional Description

- Band Gap Voltage and Temperature Sensor:[0][1][2]

Table 19.16. CONTROL_CORE_CONF_DEBUG_SEL_TST_1

Address Offset	0x0000 0484		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_1 0x1: clk_view_1 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_1 0x6: hwobs_int_ivahd_1 0x7: reserved 0x8: hwobs_int_abe_1 0x9: hwobs_int_dspss_1 0xA: reserved 0xB: reserved 0xC: hwobs_bb2d_sys_interrupt_reqz	RW	0x0

Table 19.17. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_1

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.18. CONTROL_CORE_CONF_DEBUG_SEL_TST_2

Address Offset	0x0000 0488		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_2 0x1: clk_view_2 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_2 0x6: hwobs_int_ivahd_2 0x7: reserved 0x8: hwobs_int_abe_2 0x9: hwobs_int_dspss_2 0xA: reserved 0xB: reserved	RW	0x0

Bits	Field Name	Description	Type	Reset
		0xC: hwobs_bb2d_mconnect_1		

Table 19.19. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_2

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.20. CONTROL_CORE_CONF_DEBUG_SEL_TST_3

Address Offset	0x0000 048C		
Physical Address	See Table 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31–4	3–0
RESERVED	MODE

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_3 0x1: dpll_freqlock 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_3 0x6: hwobs_int_ivahd_3 0x7: reserved 0x8: hwobs_int_abe_3 0x9: hwobs_int_dspss_3 0xA: reserved 0xB: reserved 0xC: hwobs_bb2d_mconnect_0	RW	0x0

Table 19.21. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_3

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.22. CONTROL_CORE_CONF_DEBUG_SEL_TST_4

Address Offset	0x0000 0490		
Physical Address	See Table 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31–4	3–0
RESERVED	MODE

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000

Bits	Field Name	Description	Type	Reset
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_4 0x1: dpll_tinitz 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_4 0x6: hwobs_int_ivahd_4 0x7: reserved 0x8: hwobs_int_abe_4 0x9: hwobs_int_dspss_4 0xA: reserved 0xB: reserved 0xC: hwobs_bb2d_sconnect_2	RW	0x0

Table 19.23. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_4

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.24. CONTROL_CORE_CONF_DEBUG_SEL_TST_5

Address Offset	0x0000 0494		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_5 0x1: dpll_phaselock 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_5 0x6: hwobs_int_ivahd_5 0x7: reserved 0x8: hwobs_int_abe_5 0x9: hwobs_int_dspss_5 0xA: reserved 0xB: reserved 0xC: hwobs_bb2d_sconnect_1	RW	0x0

Table 19.25. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_5

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.26. CONTROL_CORE_CONF_DEBUG_SEL_TST_6

Address Offset	0x0000 0498		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31–4	3–0
RESERVED	MODE

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_6 0x1: reserved 0x2: reserved 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_6 0x6: hwobs_int_ivahd_6 0x7: reserved 0x8: hwobs_int_abe_6 0x9: hwobs_int_dspss_6 0xA: reserved 0xB: reserved 0xC: hwobs_bb2d_sconnect_0	RW	0x0

Table 19.27. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_6

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.28. CONTROL_CORE_CONF_DEBUG_SEL_TST_7

Address Offset	0x0000 049C		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31–4	3–0
RESERVED	MODE

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_7 0x1: dpll_tenable 0x2: sdma_req_view_0 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_7	RW	0x0

Bits	Field Name	Description	Type	Reset
		0x6: hwobs_int_ivahd_7 0x7: reserved 0x8: hwobs_int_abe_7 0x9: hwobs_int_dspss_7 0xA: reserved 0xB: reserved 0xC: hwobs_bb2d_pgoodin		

Table 19.29. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_7

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.30. CONTROL_CORE_CONF_DEBUG_SEL_TST_8

Address Offset	0x0000 04A0		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_8 0x1: dpll_tenablediv 0x2: sdma_req_view_1 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_8 0x6: hwobs_int_ivahd_8 0x7: reserved 0x8: hwobs_int_abe_8 0x9: hwobs_int_dspss_8 0xA: reserved 0xB: reserved 0xC: hwobs_bb2d_ponin	RW	0x0

Table 19.31. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_8

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.32. CONTROL_CORE_CONF_DEBUG_SEL_TST_9

Address Offset	0x0000 04A4		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_9 0x1: dpll_bypassack 0x2: sdma_req_view_2 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_9 0x6: hwobs_int_ivahd_9 0x7: reserved 0x8: hwobs_int_abe_9 0x9: hwobs_int_dspss_9 0xA: reserved 0xB:~~hwobs_dssvenctvdetgp~~reserved 0xC: hwobs_bb2d_ponout	RW	0x0

Table 19.33. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_9

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0][1]

Table 19.34. CONTROL_CORE_CONF_DEBUG_SEL_TST_10

Address Offset	0x0000 04A8		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_10 0x1: dpll_idle 0x2: sdma_req_view_3 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_10 0x6: hwobs_int_ivahd_10 0x7: reserved 0x8: hwobs_int_abe_10 0x9: hwobs_int_dspss_10 0xA: reserved 0xB:~~hwobs_dssdacpwrdndaczcvbs_y~~reserved	RW	0x0

Table 19.35. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_10

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.36. CONTROL_CORE_CONF_DEBUG_SEL_TST_11

Address Offset	0x0000 04AC		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_11 0x1: hwobs_hsusbotg_sofpulse 0x2: sdma_req_view_all 0x3: reserved 0x4: reserved 0x5: hwobs_int_cm2_11 0x6: hwobs_int_ivahd_11 0x7: reserved 0x8: hwobs_int_abe_11 0x9: hwobs_int_dspss_11 0xA: reserved ~~0xB: hwobs_dssdacpwrdndaczchroma~~reserved	RW	0x0

Table 19.37. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_11

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.38. CONTROL_CORE_CONF_DEBUG_SEL_TST_12

Address Offset	0x0000 04B0		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals: 0x0: hwobs_int_mpu_12 0x1: reserved	RW	0x0

Bits	Field Name	Description	Type	Reset
		0x2: hwobs_coredivider_clkout3		
		0x3: reserved		
		0x4: reserved		
		0x5: hwobs_int_cm2_12		
		0x6: hwobs_int_ivahd_12		
		0x7: reserved		
		0x8: hwobs_int_abe_12		
		0x9: hwobs_int_dspss_12		
		0xA: reserved		
		0xB:~~hwobs_dssdacpwrdndaccvbs~~reserved		

Table 19.39. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_12

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

Table 19.40. CONTROL_CORE_CONF_DEBUG_SEL_TST_13

Address Offset	0x0000 04B4		
Physical Address	SeeTable 19.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Select mode for debug port Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												MODE			

Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3:0	MODE	Select one of the following signals:	RW	0x0
		0x0: hwobs_int_mpu_13		
		0x1: reserved		
		0x2: hwobs_perdivider_clkout4		
		0x3: reserved		
		0x4: reserved		
		0x5: hwobs_int_cm2_13		
		0x6: hwobs_int_ivahd_13		
		0x7: reserved		
		0x8: hwobs_int_abe_13		
		0x9: hwobs_int_dspss_13		
		0xA: reserved		
		0xB:~~hwobs_dssdacpwrdnbgz~~reserved		

Table 19.41. Register Call Summary for Register CONTROL_CORE_CONF_DEBUG_SEL_TST_13

Control Module Functional Description

- Observability Signals Multiplexing at General Core/Wakeup Control Level:[0]

19.6.5. SYSCTRL_GENERAL_WKUP Register Description

Refer to OMAP4470 Silicon Revision 1.0 TRM.

19.6.6. SYSCTRL_PADCONF_CORE Register Summary

Table 19.42. SYSCTRL_PADCONF_CORE Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_PADCONF_CORE_REVISION	R	32	0x00000000	0x4A10 0000
CONTROL_PADCONF_CORE_HWINFO	R	32	0x00000004	0x4A10 0004
CONTROL_PADCONF_CORE_SYSCONFIG	RW	32	0x00000010	0x4A10 0010
CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1	RW	32	0x00000040	0x4A10 0040
CONTROL_CORE_PAD0_GPMC_AD2_PAD1_GPMC_AD3	RW	32	0x00000044	0x4A10 0044
CONTROL_CORE_PAD0_GPMC_AD4_PAD1_GPMC_AD5	RW	32	0x00000048	0x4A10 0048
CONTROL_CORE_PAD0_GPMC_AD6_PAD1_GPMC_AD7	RW	32	0x0000004C	0x4A10 004C
CONTROL_CORE_PAD0_GPMC_AD8_PAD1_GPMC_AD9	RW	32	0x00000050	0x4A10 0050
CONTROL_CORE_PAD0_GPMC_AD10_PAD1_GPMC_AD11	RW	32	0x00000054	0x4A10 0054
CONTROL_CORE_PAD0_GPMC_AD12_PAD1_GPMC_AD13	RW	32	0x00000058	0x4A10 0058
CONTROL_CORE_PAD0_GPMC_AD14_PAD1_GPMC_AD15	RW	32	0x0000005C	0x4A10 005C
CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17	RW	32	0x00000060	0x4A10 0060
CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19	RW	32	0x00000064	0x4A10 0064
CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21	RW	32	0x00000068	0x4A10 0068
CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23	RW	32	0x0000006C	0x4A10 006C
CONTROL_CORE_PAD0_GPMC_A24_PAD1_GPMC_A25	RW	32	0x00000070	0x4A10 0070
CONTROL_CORE_PAD0_GPMC_NCS0_PAD1_GPMC_NCS1	RW	32	0x00000074	0x4A10 0074
CONTROL_CORE_PAD0_GPMC_NCS2_PAD1_GPMC_NCS3	RW	32	0x00000078	0x4A10 0078
CONTROL_CORE_PAD0_GPMC_N	RW	32	0x0000007C	0x4A10 007C

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
WP_PAD1_GPMC_CLK				
CONTROL_CORE_PAD0_GPMC_NADV_ALE_PAD1_GPMC_NOE	RW	32	0x00000080	0x4A10 0080
CONTROL_CORE_PAD0_GPMC_NWE_PAD1_GPMC_NBE0_CLE	RW	32	0x00000084	0x4A10 0084
CONTROL_CORE_PAD0_GPMC_NBE1_PAD1_GPMC_WAIT0	RW	32	0x00000088	0x4A10 0088
CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2	RW	32	0x0000008C	0x4A10 008C
CONTROL_CORE_PAD0_GPMC_NCS4_PAD1_GPMC_NCS5	RW	32	0x00000090	0x4A10 0090
CONTROL_CORE_PAD0_GPMC_NCS6_PAD1_GPMC_NCS7	RW	32	0x00000094	0x4A10 0094
CONTROL_CORE_PAD0_GPIO63_PAD1_GPIO64	RW	32	0x00000098	0x4A10 0098
CONTROL_CORE_PAD0_GPIO65_PAD1_GPIO66	RW	32	0x0000009C	0x4A10 009C
CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0	RW	32	0x000000A0	0x4A10 00A0
CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1	RW	32	0x000000A4	0x4A10 00A4
CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2	RW	32	0x000000A8	0x4A10 00A8
CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3	RW	32	0x000000AC	0x4A10 00AC
CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4	RW	32	0x000000B0	0x4A10 00B0
CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0	RW	32	0x000000B4	0x4A10 00B4
CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1	RW	32	0x000000B8	0x4A10 00B8
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE	RW	32	0x000000BC	0x4A10 00BC
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK	RW	32	0x000000C0	0x4A10 00C0
CONTROL_CORE_PAD0_USBB1_ULPI	RW	32	0x000000C4	0x4A10 00C4

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
TLL_STP_PAD1_USBB1_ULPITLL_DIR				
CONTROL_CORE_PAD0_USBB1_ULPITLL_NXT_PAD1_USBB1_ULPITLL_DAT0	RW	32	0x000000C8	0x4A10 00C8
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT1_PAD1_USBB1_ULPITLL_DAT2	RW	32	0x000000CC	0x4A10 00CC
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT3_PAD1_USBB1_ULPITLL_DAT4	RW	32	0x000000D0	0x4A10 00D0
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT5_PAD1_USBB1_ULPITLL_DAT6	RW	32	0x000000D4	0x4A10 00D4
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA	RW	32	0x000000D8	0x4A10 00D8
~~CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP~~ CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_GPIO_98	RW	32	0x000000DC	0x4A10 00DC
~~CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK~~ CONTROL_CORE_PAD0_GPIO_99_PAD1_SDMMC1_CLK	RW	32	0x000000E0	0x4A10 00E0
CONTROL_CORE_PAD0_SDMMC1_CMD_PAD1_SDMMC1_DAT0	RW	32	0x000000E4	0x4A10 00E4
CONTROL_CORE_PAD0_SDMMC1_DAT1_PAD1_SDMMC1_DAT2	RW	32	0x000000E8	0x4A10 00E8
CONTROL_CORE_PAD0_SDMMC1_DAT3_PAD1_SDMMC1_DAT4	RW	32	0x000000EC	0x4A10 00EC
CONTROL_CORE_PAD0_SDMMC1_DAT5_PAD1_SDMMC1_DAT6	RW	32	0x000000F0	0x4A10 00F0
CONTROL_CORE_PAD0_SDMMC1_DAT7_PAD1_ABE_MCB-SP2_CLKX	RW	32	0x000000F4	0x4A10 00F4
CONTROL_CORE_PAD0_ABE_MCBSP2_DR_PAD1_ABE_MCBSP2_DX	RW	32	0x000000F8	0x4A10 00F8

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_ABE_MCBSP2_FSX_PAD1_ABE_MCBSP1_CLKX	RW	32	0x000000FC	0x4A10 00FC
CONTROL_CORE_PAD0_ABE_MCBSP1_DR_PAD1_ABE_MCBSP1_DX	RW	32	0x00000100	0x4A10 0100
CONTROL_CORE_PAD0_ABE_MCBSP1_FSX_PAD1_ABE_PDM_UL_DATA	RW	32	0x00000104	0x4A10 0104
CONTROL_CORE_PAD0_ABE_PDM_DL_DATA_PAD1_ABE_PDM_FRAME	RW	32	0x00000108	0x4A10 0108
CONTROL_CORE_PAD0_ABE_PDM_LB_CLK_PAD1_ABE_CLKS	RW	32	0x0000010C	0x4A10 010C
CONTROL_CORE_PAD0_ABE_DMIC_CLK1_PAD1_ABE_DMIC_DIN1	RW	32	0x00000110	0x4A10 0110
CONTROL_CORE_PAD0_ABE_DMIC_DIN2_PAD1_ABE_DMIC_DIN3	RW	32	0x00000114	0x4A10 0114
CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS	RW	32	0x00000118	0x4A10 0118
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX	RW	32	0x0000011C	0x4A10 011C
CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL	RW	32	0x00000120	0x4A10 0120
CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL	RW	32	0x00000124	0x4A10 0124
CONTROL_CORE_PAD0_I2C2_SDA_PAD1_I2C3_SCL	RW	32	0x00000128	0x4A10 0128
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_I2C4_SCL	RW	32	0x0000012C	0x4A10 012C
CONTROL_CORE_PAD0_I2C4_SDA_PAD1_MCSPI1_CLK	RW	32	0x00000130	0x4A10 0130
CONTROL_CORE_PAD0_MCSPI1_SOMI_PAD1_MCSPI1_SIMO	RW	32	0x00000134	0x4A10 0134

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_MCSPI1_CS0_PAD1_MCSPI1_CS1	RW	32	0x00000138	0x4A10 0138
CONTROL_CORE_PAD0_MCSPI1_CS2_PAD1_MCSPI1_CS3	RW	32	0x0000013C	0x4A10 013C
CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD	RW	32	0x00000140	0x4A10 0140
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX	RW	32	0x00000144	0x4A10 0144
CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD	RW	32	0x00000148	0x4A10 0148
CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1	RW	32	0x0000014C	0x4A10 014C
CONTROL_CORE_PAD0_SDMMC5_DAT2_PAD1_SDMMC5_DAT3	RW	32	0x00000150	0x4A10 0150
CONTROL_CORE_PAD0_MCSPI4_CLK_PAD1_MCSPI4_SIMO	RW	32	0x00000154	0x4A10 0154
CONTROL_CORE_PAD0_MCSPI4_SOMI_PAD1_MCSPI4_CS0	RW	32	0x00000158	0x4A10 0158
CONTROL_CORE_PAD0_UART4_RX_PAD1_UART4_TX	RW	32	0x0000015C	0x4A10 015C
CONTROL_CORE_PAD0_USBB2_ULPITLL_CLK_PAD1_USBB2_ULPITLL_STP	RW	32	0x00000160	0x4A10 0160
CONTROL_CORE_PAD0_USBB2_ULPITLL_DIR_PAD1_USBB2_ULPITLL_NXT	RW	32	0x00000164	0x4A10 0164
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT0_PAD1_USBB2_ULPITLL_DAT1	RW	32	0x00000168	0x4A10 0168
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT2_PAD1_USBB2_ULPITLL_DAT3	RW	32	0x0000016C	0x4A10 016C
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT4_PAD1_USBB2_ULPITLL_DAT5	RW	32	0x00000170	0x4A10 0170
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1_USBB2_ULPITLL_DAT7	RW	32	0x00000174	0x4A10 0174
CONTROL_CORE_PAD0_USBB2_HSIC	RW	32	0x00000178	0x4A10 0178

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
_DATA_PAD1_USBB2_HSIC_STROBE				
CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4	RW	32	0x0000017C	0x4A10 017C
CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0	RW	32	0x00000180	0x4A10 0180
CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2	RW	32	0x00000184	0x4A10 0184
CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4	RW	32	0x00000188	0x4A10 0188
CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0	RW	32	0x0000018C	0x4A10 018C
CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2	RW	32	0x00000190	0x4A10 0190
CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP	RW	32	0x00000194	0x4A10 0194
CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT	RW	32	0x00000198	0x4A10 0198
CONTROL_CORE_PAD0_FREF_CLK2_OUT_PAD1_SYS_NIRQ1	RW	32	0x0000019C	0x4A10 019C
CONTROL_CORE_PAD0_SYS_NIRQ2_PAD1_SYS_BOOT0	RW	32	0x000001A0	0x4A10 01A0
CONTROL_CORE_PAD0_SYS_BOOT1_PAD1_SYS_BOOT2	RW	32	0x000001A4	0x4A10 01A4
CONTROL_CORE_PAD0_SYS_BOOT3_PAD1_SYS_BOOT4	RW	32	0x000001A8	0x4A10 01A8
CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0	RW	32	0x000001AC	0x4A10 01AC
CONTROL_CORE_PAD0_DPM_EMU1_PAD1_DPM_EMU2	RW	32	0x000001B0	0x4A10 01B0
CONTROL_CORE_PAD0_DPM_EMU3_PAD1_DPM_EMU4	RW	32	0x000001B4	0x4A10 01B4
CONTROL_CORE_PAD0_DPM_EMU5_PAD1_DPM_EMU6	RW	32	0x000001B8	0x4A10 01B8
CONTROL_CORE_PAD0_DPM_EMU7_PAD1_DPM_EMU8	RW	32	0x000001BC	0x4A10 01BC

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_DPM_EMU9_PAD1_DPM_EMU10	RW	32	0x000001C0	0x4A10 01C0
CONTROL_CORE_PAD0_DPM_EMU11_PAD1_DPM_EMU12	RW	32	0x000001C4	0x4A10 01C4
CONTROL_CORE_PAD0_DPM_EMU13_PAD1_DPM_EMU14	RW	32	0x000001C8	0x4A10 01C8
CONTROL_CORE_PAD0_DPM_EMU15_PAD1_DPM_EMU16	RW	32	0x000001CC	0x4A10 01CC
CONTROL_CORE_PAD0_DPM_EMU17_PAD1_DPM_EMU18	RW	32	0x000001D0	0x4A10 01D0
CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2	RW	32	0x000001D4	0x4A10 01D4
CONTROL_PADCONF_WAKEUPEVENT_0	R	32	0x000001D8	0x4A10 01D8
CONTROL_PADCONF_WAKEUPEVENT_1	R	32	0x000001DC	0x4A10 01DC
CONTROL_PADCONF_WAKEUPEVENT_2	R	32	0x000001E0	0x4A10 01E0
CONTROL_PADCONF_WAKEUPEVENT_3	R	32	0x000001E4	0x4A10 01E4
CONTROL_PADCONF_WAKEUPEVENT_4	R	32	0x000001E8	0x4A10 01E8
CONTROL_PADCONF_WAKEUPEVENT_5	R	32	0x000001EC	0x4A10 01EC
CONTROL_PADCONF_WAKEUPEVENT_6	R	32	0x000001F0	0x4A10 01F0
CONTROL_CORE_PAD0_CSI22_DY2	RW	32	0x000001F4	0x4A10 01F4
CONTROL_PADCONF_GLOBAL	RW	32	0x000005A0	0x4A10 05A0
CONTROL_CORE_PADCONF_MODE	RW	32	0x000005A4	0x4A10 05A4
CONTROL_SMART1IO_PADCONF_0	RW	32	0x000005A8	0x4A10 05A8
CONTROL_SMART1IO_PADCONF_1	RW	32	0x000005AC	0x4A10 05AC
CONTROL_SMART2IO_PADCONF_0	RW	32	0x000005B0	0x4A10 05B0
CONTROL_SMART2IO_PADCONF_1	RW	32	0x000005B4	0x4A10 05B4
CONTROL_SMART3IO_PADCONF_0	RW	32	0x000005B8	0x4A10 05B8
CONTROL_SMART3IO_PADCONF_1	RW	32	0x000005BC	0x4A10 05BC
CONTROL_SMART3IO_PADCONF_2	RW	32	0x000005C0	0x4A10 05C0
CONTROL_USBB_HSIC	RW	32	0x000005C4	0x4A10 05C4
CONTROL_SMART3IO_PADCONF_3	RW	32	0x000005C8	0x4A10 05C8

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_SMART2IO_PADCONF_2	RW	32	0x000005CC	0x4A10 05CC
CONTROL_SMART1IO_PADCONF_2	RW	32	0x000005D0	0x4A10 05D0
CONTROL_SMART1IO_PADCONF_3	RW	32	0x000005D4	0x4A10 05D4
CONTROL_C2CIO_PADCONF_0	RW	32	0x000005D8	0x4A10 05D8
CONTROL_PBIASLITE	RW	32	0x00000600	0x4A10 0600
CONTROL_I2C_0	RW	32	0x00000604	0x4A10 0604
CONTROL_CAMERA_RX	RW	32	0x00000608	0x4A10 0608
~~CONTROL_AV-DAC~~RESERVED	RW	32	0x0000060C	0x4A10 060C
RESERVED	RW	32	0x00000610	0x4A10 0610
CONTROL_MMC2	RW	32	0x00000614	0x4A10 0614
CONTROL_DSIPHY	RW	32	0x00000618	0x4A10 0618
CONTROL_MCBSPLP	RW	32	0x0000061C	0x4A10 061C
CONTROL_USB2PHYCORE	RW	32	0x00000620	0x4A10 0620
CONTROL_I2C_1	RW	32	0x00000624	0x4A10 0624
CONTROL_MMC1	RW	32	0x00000628	0x4A10 0628
CONTROL_HSI	RW	32	0x0000062C	0x4A10 062C
CONTROL_USB	RW	32	0x00000630	0x4A10 0630
CONTROL_HDQ	RW	32	0x00000634	0x4A10 0634
CONTROL_LPDDR2IO1_0	RW	32	0x00000638	0x4A10 0638
CONTROL_LPDDR2IO1_1	RW	32	0x0000063C	0x4A10 063C
CONTROL_LPDDR2IO1_2	RW	32	0x00000640	0x4A10 0640
CONTROL_LPDDR2IO1_3	RW	32	0x00000644	0x4A10 0644
CONTROL_LPDDR2IO2_0	RW	32	0x00000648	0x4A10 0648
CONTROL_LPDDR2IO2_1	RW	32	0x0000064C	0x4A10 064C
CONTROL_LPDDR2IO2_2	RW	32	0x00000650	0x4A10 0650
CONTROL_LPDDR2IO2_3	RW	32	0x00000654	0x4A10 0654
CONTROL_BUS_HOLD	RW	32	0x00000658	0x4A10 0658
CONTROL_C2C	RW	32	0x0000065C	0x4A10 065C
CONTROL_CORE_CONTROL_SPARE_RW	RW	32	0x00000660	0x4A10 0660
CONTROL_CORE_CONTROL_SPARE_R	R	32	0x00000664	0x4A10 0664
CONTROL_CORE_CONTROL_SPARE_R_C0	RW	32	0x00000668	0x4A10 0668
CONTROL_CORE_CONTROL_SPARE_RW1	RW	32	0x0000066C	0x4A10 066C

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_CONTROL_SPARE_RW2	RW	32	0x00000670	0x4A10 0670
CONTROL_CORE_CONTROL_SPARE_RW3	RW	32	0x00000674	0x4A10 0674
CONTROL_CORE_CONTROL_SPARE_RW4	RW	32	0x00000678	0x4A10 0678
CONTROL_CORE_CONTROL_SPARE_RW5	RW	32	0x0000067C	0x4A10 067C
CONTROL_CORE_CONTROL_SPARE_RW6	RW	32	0x00000680	0x4A10 0680
CONTROL_CORE_CONTROL_SPARE_RW7	RW	32	0x00000684	0x4A10 0684
CONTROL_CORE_CONTROL_SPARE_RW8	RW	32	0x00000688	0x4A10 0688
CONTROL_CORE_CONTROL_SPARE_RW9	RW	32	0x0000068C	0x4A10 068C
CONTROL_CORE_CONTROL_SPARE_R1	R	32	0x0000068C	0x4A10 068C
RESERVED	RW	32	0x00000694	0x4A10 0694
~~CONTROL_EFUSE_1~~ RESERVED	RW	32	0x00000700	0x4A10 0700
CONTROL_EFUSE_2	RW	32	0x00000704	0x4A10 0704
CONTROL_EFUSE_3	R	32	0x00000708	0x4A10 0708
CONTROL_EFUSE_4	RW	32	0x0000070C	0x4A10 070C

19.6.7. SYSCTRL_PADCONF_CORE Register Description

Note

This section contains only modified registers.

Table 19.43. CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17

Address Offset	0x0000 0060		
Physical Address	Please refer to Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a16 and gpmc_a17 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_A17_WAKEUPEVENT	GPMC_A17_WAKEUPENABLE	GPMC_A17_OFFMODEPULLTYPESELECT	GPMC_A17_OFFMODEPULLUDENABLE	GPMC_A17_OFFMODEOUTVALUE	GPMC_A17_OFFMODEOUTENABLE	GPMC_A17_OFFMODEENABLE	GPMC_A17_INPUTENABLE	RESERVED			GPMC_A17_PULLTYPESELECT	GPMC_A17_PULLUDENABLE	GPMC_A17_MUXMODE			GPMC_A16_WAKEUPEVENT	GPMC_A16_WAKEUPENABLE	GPMC_A16_OFFMODEPULLTYPESELECT	GPMC_A16_OFFMODEPULLUDENABLE	GPMC_A16_OFFMODEOUTVALUE	GPMC_A16_OFFMODEOUTENABLE	GPMC_A16_OFFMODEENABLE	GPMC_A16_INPUTENABLE	RESERVED			GPMC_A16_PULLTYPESELECT	GPMC_A16_PULLUDENABLE	GPMC_A16_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_A17_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPMC_A17_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	GPMC_A17_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_a17 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	GPMC_A17_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_a17 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	GPMC_A17_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a17 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A17_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a17. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A17_OFFMODEENABLE	OffMode mode override control for pad gpmc_a17 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A17_INPUTENABLE	Input enable value for pad gpmc_a17 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_A17_PULLTYPESELECT	Pull-Up/Down selection for pad gpmc_a17 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19		Pull-Up/Down enable for pad gpmc_a17	RW	1

Bits	Field Name	Description	Type	Reset
	GPMC_A17_PULLUDENABLE	0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled		
18:16	GPMC_A17_MUXMODE	Functional multiplexing selection for pad gpmc_a17 0x1: Select kpd_row5 0x7: Select safe_mode 0x0: Select gpmc_a17 ~~0x4: Select venc_656_data1~~ 0x2: Select c2c_datain1 0x3: Select gpio_41	RW	0x7
15	GPMC_A16_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPMC_A16_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13	GPMC_A16_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_a16 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	GPMC_A16_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_a16 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	GPMC_A16_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a16 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A16_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a16. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A16_OFFMODEENABLE	OffMode mode override control for pad gpmc_a16 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A16_INPUTENABLE	Input enable value for pad gpmc_a16 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A16_PULLTYPESELECT	Pull-Up/Down selection for pad gpmc_a16 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPMC_A16_PULLUDENABLE	Pull-Up/Down enable for pad gpmc_a16 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPMC_A16_MUXMODE	Functional multiplexing selection for pad gpmc_a16 0x1: Select kpd_row4 0x7: Select safe_mode 0x0: Select gpmc_a16	RW	0x7

Bits	Field Name	Description	Type	Reset
		~~0x4: Select venc_656_data0~~ 0x2: Select c2c_datain0 0x3: Select gpio_40		

Table 19.44. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.45. CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19

Address Offset	0x0000 0064		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a18 and gpmc_a19 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	GPMC_A19_WAKEUPEVENT
30	GPMC_A19_WAKEUPENABLE
29	GPMC_A19_OFFMODEPULLTYPESELECT
28	GPMC_A19_OFFMODEPULLUDENABLE
27	GPMC_A19_OFFMODEOUTVALUE
26	GPMC_A19_OFFMODEOUTENABLE
25	GPMC_A19_OFFMODEENABLE
24	GPMC_A19_INPUTENABLE
23–21	RESERVED
20	GPMC_A19_PULLTYPESELECT
19	GPMC_A19_PULLUDENABLE
18–16	GPMC_A19_MUXMODE
15	GPMC_A18_WAKEUPEVENT
14	GPMC_A18_WAKEUPENABLE
13	GPMC_A18_OFFMODEPULLTYPESELECT
12	GPMC_A18_OFFMODEPULLUDENABLE
11	GPMC_A18_OFFMODEOUTVALUE
10	GPMC_A18_OFFMODEOUTENABLE
9	GPMC_A18_OFFMODEENABLE
8	GPMC_A18_INPUTENABLE
7–5	RESERVED
4	GPMC_A18_PULLTYPESELECT
3	GPMC_A18_PULLUDENABLE
2–0	GPMC_A18_MUXMODE

Bits	Field Name	Description	Type	Reset
31	GPMC_A19_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPMC_A19_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	GPMC_A19_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_a19 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	GPMC_A19_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_a19 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	GPMC_A19_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a19 0x0: Set value at 0 0x1: Set value at 1	RW	0

Bits	Field Name	Description	Type	Reset
26	GPMC_A19_OFFMODE OUTENABLE	OffMode mode output enable value for pad gpm c_a19. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A19_OFFMODE ENABLE	OffMode mode override control for pad gpmc_a19 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
24	GPMC_A19_INPUTENABLE	Input enable value for pad gpmc_a19 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_A19_PULLTYPES-ELECT	Pull-Up/Down selection for pad gpmc_a19 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPMC_A19_PULLUDENABL E	Pull-Up/Down enable for pad gpmc_a19 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPMC_A19_MUXMODE	Functional multiplexing selection for pad gpmc_a19 0x1: Select kpd_row7 0x7: Select safe_mode 0x0: Select gpmc_a19 ~~0x4: Select venc_656_data3~~ 0x2: Select c2c_datain3 0x3: Select gpio_43	RW	0x7
15	GPMC_A18_WAKEUPE VENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPMC_A18_WAKEUPE NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13	GPMC_A18_OFFMODEPULLTYPESE LECT	OffMode mode Pull-Up/Down selection for pad gpmc_a18 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	GPMC_A18_OFFMODEPULL UDENABLE	OffMode mode Pull-Up/Down enable for pad gpm c_a18 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	GPMC_A18_OFFMODE OUTVALUE	OffMode mode output value for pad gpmc_a18 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A18_OFFMODE OUTENABLE	OffMode mode output enable value for pad gpm c_a18. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

Bits	Field Name	Description	Type	Reset
9	GPMC_A18_OFFMODE ENABLE	OffMode mode override control for pad gpmc_a18 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
8	GPMC_A18_INPUTENABLE	Input enable value for pad gpmc_a18 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A18_PULLTYPES-ELECT	Pull-Up/Down selection for pad gpmc_a18 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPMC_A18_PULLUDENABL E	Pull-Up/Down enable for pad gpmc_a18 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPMC_A18_MUXMODE	Functional multiplexing selection for pad gpmc_a18 0x1: Select kpd_row6 0x7: Select safe_mode 0x0: Select gpmc_a18 ~~0x4: Select venc_656_data2~~ 0x2: Select c2c_datain2 0x3: Select gpio_42	RW	0x7

Table 19.46. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.47. CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21

Address Offset	0x0000 0068		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Pads gpmc_a20 and gpmc_a21 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GPMC_A21_WAKEUPEVENT	GPMC_A21_WAKEUPENABLE	GPMC_A21_OFFMODEPULLTYPESELECT	GPMC_A21_OFFMODEPULLUDENABLE	GPMC_A21_OFFMODEOUTVALUE	GPMC_A21_OFFMODEOUTENABLE	GPMC_A21_OFFMODEENABLE	GPMC_A21_INPUTENABLE	RESERVED			GPMC_A21_PULLTYPESELECT	GPMC_A21_PULLUDENABLE	GPMC_A21_MUXMODE		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPMC_A20_WAKEUPEVENT	GPMC_A20_WAKEUPENABLE	GPMC_A20_OFFMODEPULLTYPESELECT	GPMC_A20_OFFMODEPULLUDENABLE	GPMC_A20_OFFMODEOUTVALUE	GPMC_A20_OFFMODEOUTENABLE	GPMC_A20_OFFMODEENABLE	GPMC_A20_INPUTENABLE	RESERVED			GPMC_A20_PULLTYPESELECT	GPMC_A20_PULLUDENABLE	GPMC_A20_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPMC_A21_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPMC_A21_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	GPMC_A21_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_a21 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	GPMC_A21_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_a21 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	GPMC_A21_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a21 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A21_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a21. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A21_OFFMODEENABLE	OffMode mode override control for pad gpmc_a21 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A21_INPUTENABLE	Input enable value for pad gpmc_a21 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_A21_PULLTYPESELECT	Pull-Up/Down selection for pad gpmc_a21 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPMC_A21_PULLUDENABLE	Pull-Up/Down enable for pad gpmc_a21 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPMC_A21_MUXMODE	Functional multiplexing selection for pad gpmc_a21 0x1: Select kpd_col5 0x7: Select safe_mode 0x0: Select gpmc_a21 ~~0x4: Select venc_656_data5~~ 0x2: Select c2c_datain5 0x3: Select gpio_45	RW	0x7
15	GPMC_A20_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPMC_A20_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: wake-up detection on high level		
13	GPMC_A20_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_a20 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	GPMC_A20_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_a20 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	GPMC_A20_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a20 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A20_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a20. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A20_OFFMODEENABLE	OffMode mode override control for pad gpmc_a20 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A20_INPUTENABLE	Input enable value for pad gpmc_a20 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A20_PULLTYPESELECT	Pull-Up/Down selection for pad gpmc_a20 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPMC_A20_PULLUDENABLE	Pull-Up/Down enable for pad gpmc_a20 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPMC_A20_MUXMODE	Functional multiplexing selection for pad gpmc_a20 0x1: Select kpd_col4 0x7: Select safe_mode 0x0: Select gpmc_a20 ~~0x4: Select venc_656_data4~~ 0x2: Select c2c_datain4 0x3: Select gpio_44	RW	0x7

Table 19.48. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.49. CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23

Address Offset	0x0000 006C		
Physical Address	Please refer to Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads gpmc_a22 and gpmc_a23 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	GPMC_A23_WAKEUPEVENT
30	GPMC_A23_WAKEUPENABLE
29	GPMC_A23_OFFMODEPULLTYPESELECT
28	GPMC_A23_OFFMODEPULLUDENABLE
27	GPMC_A23_OFFMODEOUTVALUE
26	GPMC_A23_OFFMODEOUTENABLE
25	GPMC_A23_OFFMODEENABLE
24	GPMC_A23_INPUTENABLE
23 22 21	RESERVED
20	GPMC_A23_PULLTYPESELECT
19	GPMC_A23_PULLUDENABLE
18 17 16	GPMC_A23_MUXMODE
15	GPMC_A22_WAKEUPEVENT
14	GPMC_A22_WAKEUPENABLE
13	GPMC_A22_OFFMODEPULLTYPESELECT
12	GPMC_A22_OFFMODEPULLUDENABLE
11	GPMC_A22_OFFMODEOUTVALUE
10	GPMC_A22_OFFMODEOUTENABLE
9	GPMC_A22_OFFMODEENABLE
8	GPMC_A22_INPUTENABLE
7 6 5	RESERVED
4	GPMC_A22_PULLTYPESELECT
3	GPMC_A22_PULLUDENABLE
2 1 0	GPMC_A22_MUXMODE

Bits	Field Name	Description	Type	Reset
31	GPMC_A23_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPMC_A23_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	GPMC_A23_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_a23 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	GPMC_A23_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_a23 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	GPMC_A23_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a23 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_A23_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a23. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_A23_OFFMODEENABLE	OffMode mode override control for pad gpmc_a23 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_A23_INPUTENABLE	Input enable value for pad gpmc_a23	RW	1

Bits	Field Name	Description	Type	Reset
		0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled		
23:21	RESERVED		R	0x0
20	GPMC_A23_PULLTYPESELECT	Pull-Up/Down selection for pad gpmc_a23 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPMC_A23_PULLUDENABLE	Pull-Up/Down enable for pad gpmc_a23 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPMC_A23_MUXMODE	Functional multiplexing selection for pad gpmc_a23 0x1: Select kpd_col7 0x7: Select safe_mode 0x0: Select gpmc_a23 ~~0x4: Select venc_656_data7~~ 0x2: Select c2c_datain7 0x3: Select gpio_47	RW	0x7
15	GPMC_A22_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPMC_A22_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13	GPMC_A22_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_a22 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	GPMC_A22_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_a22 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	GPMC_A22_OFFMODEOUTVALUE	OffMode mode output value for pad gpmc_a22 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_A22_OFFMODEOUTENABLE	OffMode mode output enable value for pad gpmc_a22. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_A22_OFFMODEENABLE	OffMode mode override control for pad gpmc_a22 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
8	GPMC_A22_INPUTENABLE	Input enable value for pad gpmc_a22 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_A22_PULLTYPESELECT	Pull-Up/Down selection for pad gpmc_a22 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0

Bits	Field Name	Description	Type	Reset
3	GPMC_A22_PULLUDENABLE	Pull-Up/Down enable for pad gpmc_a22 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPMC_A22_MUXMODE	Functional multiplexing selection for pad gpmc_a22 0x1: Select kpd_col6 0x7: Select safe_mode 0x0: Select gpmc_a22 ~~0x4: Select venc_656_data6~~ 0x2: Select c2c_datain6 0x3: Select gpio_46	RW	0x7

Table 19.50. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.51. CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2

Address Offset	0x0000 008C		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Pads gpmc_wait1 and gpmc_wait2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	GPMC_WAIT2_WAKEUPEVENT
30	GPMC_WAIT2_WAKEUPENABLE
29	GPMC_WAIT2_OFFMODEPULLTYPESELECT
28	GPMC_WAIT2_OFFMODEPULLUDENABLE
27	GPMC_WAIT2_OFFMODEOUTVALUE
26	GPMC_WAIT2_OFFMODEOUTENABLE
25	GPMC_WAIT2_OFFMODEENABLE
24	GPMC_WAIT2_INPUTENABLE
23 22 21	RESERVED
20	GPMC_WAIT2_PULLTYPESELECT
19	GPMC_WAIT2_PULLUDENABLE
18 17 16	GPMC_WAIT2_MUXMODE
15	GPMC_WAIT1_WAKEUPEVENT
14	GPMC_WAIT1_WAKEUPENABLE
13	GPMC_WAIT1_OFFMODEPULLTYPESELECT
12	GPMC_WAIT1_OFFMODEPULLUDENABLE
11	GPMC_WAIT1_OFFMODEOUTVALUE
10	GPMC_WAIT1_OFFMODEOUTENABLE
9	GPMC_WAIT1_OFFMODEENABLE
8	GPMC_WAIT1_INPUTENABLE
7 6 5	RESERVED
4	GPMC_WAIT1_PULLTYPESELECT
3	GPMC_WAIT1_PULLUDENABLE
2 1 0	GPMC_WAIT1_MUXMODE

Bits	Field Name	Description	Type	Reset
31	GPMC_WAIT2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPMC_WAIT2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	GPMC_WAIT2_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_wait2 0x0: Offmode Pull-Down selected	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: Offmode Pull-Up selected		
28	GPMC_WAIT2_OFF-MODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_wait2 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	GPMC_WAIT2_OFFMODE-OUTVALUE	OffMode mode output value for pad gpmc_wait2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	GPMC_WAIT2_OFFMODE-OUTENABLE	OffMode mode output enable value for pad gpmc_wait2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	GPMC_WAIT2_OFF-MODEENABLE	OffMode mode override control for pad gpmc_wait2 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	GPMC_WAIT2_INPUTENABLE	Input enable value for pad gpmc_wait2 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPMC_WAIT2_PULLTYPESELECT	Pull-Up/Down selection for pad gpmc_wait2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	GPMC_WAIT2_PULLUDE-NABLE	Pull-Up/Down enable for pad gpmc_wait2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPMC_WAIT2_MUXMODE	Functional multiplexing selection for pad gpmc_wait2 0x1:~~Select usbc1_icusb_txen~~Reserved 0x7: Select safe_mode 0x0: Select gpmc_wait2 0x4: Select sys_ndmareq0 0x2: Select c2c_dataout3 0x3: Select gpio_100	RW	0x7
15	GPMC_WAIT1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPMC_WAIT1_WAKEUPE-NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13	GPMC_WAIT1_OFF-MODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad gpmc_wait1 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	GPMC_WAIT1_OFF-MODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad gpmc_wait1 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0

Bits	Field Name	Description	Type	Reset
11	GPMC_WAIT1_OFFMODE-OUTVALUE	OffMode mode output value for pad gpmc_wait1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	GPMC_WAIT1_OFFMODE-OUTENABLE	OffMode mode output enable value for pad gpmc_wait1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	GPMC_WAIT1_OFF-MODEENABLE	OffMode mode override control for pad gpmc_wait1 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
8	GPMC_WAIT1_INPUTENAB LE	Input enable value for pad gpmc_wait1 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPMC_WAIT1_PULLTYPES ELECT	Pull-Up/Down selection for pad gpmc_wait1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	GPMC_WAIT1_PULLUDE-NABLE	Pull-Up/Down enable for pad gpmc_wait1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPMC_WAIT1_MUXMODE	Functional multiplexing selection for pad gpmc_wait1 0x0: Select gpmc_wait1 0x3: Select gpio_62 0x7: Select safe_mode 0x2: Select c2c_dataout2	RW	0x7

Table 19.52. Register Call Summary for Register CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.53. CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_GPIO_98

Address Offset	0x0000 00DC		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Pads usbb1_hsic_strobe and~~usbc1_icusb_dp~~gpio_98 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	USBC1_ICUSB_DP_WAKEUPEVENT GPIO_98_WAKEUPEVENT
30	USBC1_ICUSB_DP_WAKEUPENABLE GPIO_98_WAKEUPENABLE
29	USBC1_ICUSB_DP_OFFMODEPULLTYPESELECT GPIO_98_OFFMODEPULLTYPESELECT
28	USBC1_ICUSB_DP_OFFMODEPULLUDENABLE GPIO_98_OFFMODEPULLUDENABLE
27	USBC1_ICUSB_DP_OFFMODEOUTVALUE GPIO_98_OFFMODEOUTVALUE
26	USBC1_ICUSB_DP_OFFMODEOUTENABLE GPIO_98_OFFMODEOUTENABLE
25	USBC1_ICUSB_DP_OFFMODEENABLE GPIO_98_OFFMODEENABLE
24	USBC1_ICUSB_DP_INPUTENABLE GPIO_98_INPUTENABLE
23-21	RESERVED
20	USBC1_ICUSB_DP_PULLTYPESELECT GPIO_98_PULLTYPESELECT
19	USBC1_ICUSB_DP_PULLUDENABLE GPIO_98_PULLUDENABLE
18-16	USBC1_ICUSB_DP_MUXMODE GPIO_98_MUXMODE
15	USBB1_HSIC_STROBE_WAKEUPEVENT
14	USBB1_HSIC_STROBE_WAKEUPENABLE
13-12	RESERVED
11	USBB1_HSIC_STROBE_OFFMODEOUTVALUE
10	USBB1_HSIC_STROBE_OFFMODEOUTENABLE
9	USBB1_HSIC_STROBE_OFFMODEENABLE
8-3	RESERVED
2-0	USBB1_HSIC_STROBE_MUXMODE

Bits	Field Name	Description	Type	Reset
31	~~USBC1_ICUSB_DP_WAKEUPEVENT~~ GPIO_98_WAKEUPEVENT	Pad wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	~~USBC1_ICUSB_DP_WAKEUPENABLE~~ GPIO_98_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	~~USBC1_ICUSB_DP_OFFMODEPULLTYPESELECT~~ GPIO_98_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad~~usbc1_icusb_dp~~gpio_98 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28			RW	0

Bits	Field Name	Description	Type	Reset
	~~USBC1_ICUSB_DP_OFFMODEPULLUDENABLE~~ GPIO_98_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad ~~usbc1_icusb_dp~~gpio_98 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled		
27	~~USBC1_ICUSB_DP_OFFMODEOUTVALUE~~ GPIO_98_OFFMODEOUTVALUE	OffMode mode output value for pad ~~usbc1_icusb_dp~~gpio_98 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	~~USBC1_ICUSB_DP_OFFMODEOUTENABLE~~ GPIO_98_OFFMODEOUTENABLE	OffMode mode output enable value for pad ~~usbc1_icusb_dp~~gpio_98. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	~~USBC1_ICUSB_DP_OFFMODEENABLE~~ GPIO_98_OFFMODEENABLE	OffMode mode override control for pad ~~usbc1_icusb_dp~~gpio_98 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	~~USBC1_ICUSB_DP_INPUTENABLE~~ GPIO_98_INPUTENABLE	Input enable value for pad ~~usbc1_icusb_dp~~gpio_98 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	~~USBC1_ICUSB_DP_PULLTYPESELECT~~ GPIO_98_PULLTYPESELECT	Pull-Up/Down selection for pad ~~usbc1_icusb_dp~~gpio_98 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	~~USBC1_ICUSB_DP_PULLUDENABLE~~ GPIO_98_PULLUDENABLE	Pull-Up/Down enable for pad ~~usbc1_icusb_dp~~gpio_98 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	~~USBC1_ICUSB_DP_MUXMODE~~ GPIO_98_MUXMODE	Functional multiplexing selection for pad ~~usbc1_icusb_dp~~gpio_98 ~~0x0: Select usbc1_icusb_dp~~ 0x0,0x3: Select gpio_98 0x7: Select safe_mode	RW	0x7
15	USBB1_HSIC_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	USBB1_HSIC_STROBE_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13:12	RESERVED		R	0x0
11	USBB1_HSIC_STROBE_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_hsic_strobe 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	USBB1_HSIC_STROBE_OFFMODEOUTENABLE	OffMode mode output enable value for pad usbb1_hsic_strobe. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

Bits	Field Name	Description	Type	Reset
9	USBB1_HSIC_STROBE_OFFMODEENABLE	Off mode override control for pad usbb1_hsic_strobe 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
8:3	RESERVED		R	0x00
2:0	USBB1_HSIC_STROBE_MUXMODE	Functional multiplexing selection for pad usbb1_hsic_strobe 0x0: Select usbb1_hsic_strobe 0x3: Select gpio_97 0x7: Select safe_mode	RW	0x7

Table 19.54. Register Call Summary for Register CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_GPIO_98

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.55. CONTROL_CORE_PAD0_GPIO_99_PAD1_SDMMC1_CLK

Address Offset	0x0000 00E0		
Physical Address	Please refer to Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads ~~usbc1_icusb_dm~~ gpio_99 and sdmmc1_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	SDMMC1_CLK_WAKEUPEVENT
30	SDMMC1_CLK_WAKEUPENABLE
29	SDMMC1_CLK_OFFMODEPULLTYPESELECT
28	SDMMC1_CLK_OFFMODEPULLUDENABLE
27	SDMMC1_CLK_OFFMODEOUTVALUE
26	SDMMC1_CLK_OFFMODEOUTENABLE
25	SDMMC1_CLK_OFFMODEENABLE
24	SDMMC1_CLK_INPUTENABLE
23 22 21	RESERVED
20	SDMMC1_CLK_PULLTYPESELECT
19	SDMMC1_CLK_PULLUDENABLE
18 17 16	SDMMC1_CLK_MUXMODE
15	USBC1_ICUSB_DM_WAKEUPEVENT GPIO_99_WAKEUPEVENT
14	USBC1_ICUSB_DM_WAKEUPENABLE GPIO_99_WAKEUPENABLE
13	USBC1_ICUSB_DM_OFFMODEPULLTYPESELECT GPIO_99_OFFMODEPULLTYPESELECT
12	USBC1_ICUSB_DM_OFFMODEPULLUDENABLE GPIO_99_OFFMODEPULLUDENABLE
11	USBC1_ICUSB_DM_OFFMODEOUTVALUE GPIO_99_OFFMODEOUTVALUE
10	USBC1_ICUSB_DM_OFFMODEOUTENABLE GPIO_99_OFFMODEOUTENABLE
9	USBC1_ICUSB_DM_OFFMODEENABLE GPIO_99_OFFMODEENABLE
8	USBC1_ICUSB_DM_INPUTENABLE GPIO_99_INPUTENABLE
7 6 5	RESERVED
4	USBC1_ICUSB_DM_PULLTYPESELECT GPIO_99_PULLTYPESELECT
3	USBC1_ICUSB_DM_PULLUDENABLE GPIO_99_PULLUDENABLE
2 1 0	USBC1_ICUSB_DM_MUXMODE GPIO_99_MUXMODE

Bits	Field Name	Description	Type	Reset
31	SDMMC1_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SDMMC1_CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	SDMMC1_CLK_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad sdmmc1_clk 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28			RW	0

Bits	Field Name	Description	Type	Reset
	SDMMC1_CLK_OFF-MODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad sdmmc1_clk 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled		
27	SDMMC1_CLK_OFFMODE-OUTVALUE	OffMode mode output value for pad sdmmc1_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC1_CLK_OFFMODE-OUTENABLE	OffMode mode output enable value for pad sdmmc1_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC1_CLK_OFF-MODEENABLE	OffMode mode override control for pad sdmmc1_clk 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	SD-MMC1_CLK_INPUTENABLE	Input enable value for pad sdmmc1_clk 0x0: Input buffer of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC1_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad sdmmc1_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SDMMC1_CLK_PULLUDE-NABLE	Pull-Up/Down enable for pad sdmmc1_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SDMMC1_CLK_MUXMODE	Functional multiplexing selection for pad sdmmc1_clk 0x0: Select sdmmc1_clk 0x3: Select gpio_100 0x7: Select safe_mode 0x2: Select dpm_emu19	RW	0x7
15	~~USBC1_ICUSB_DM_WAKEUPEVENT~~ GPIO_99_WAKEUPEVENT	Pad wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	~~US-BC1_ICUSB_DM_WAKEUPE-NABLE~~ GPIO_99_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13	~~USBC1_ICUSB_DM_OFF-MODEPULLTYPESELECT~~ GPIO_99_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad ~~usbc1_icusb_dm~~gpio_99 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	~~USBC1_ICUSB_DM_OFF-MODEPULLUDENABLE~~ GPIO_99_OFFMODEPUL-LUDENABLE	OffMode mode Pull-Up/Down enable for pad ~~usbc1_icusb_dm~~gpio_99 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	~~USBC1_ICUSB_DM_OFF-MODEOUTVALUE~~	OffMode mode output value for pad ~~usbc1_icusb_dm~~gpio_99 0x0: Set value at 0	RW	0

Bits	Field Name	Description	Type	Reset
	GPIO_99_OFFMODEOUTVALUE	0x1: Set value at 1		
10	~~USBC1_ICUSB_DM_OFFMODEOUTENABLE~~ GPIO_99_OFFMODEOUTENABLE	OffMode mode output enable value for pad~~usbc1_icusb_dm~~gpio_99. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	~~USBC1_ICUSB_DM_OFFMODEENABLE~~ GPIO_99_OFFMODEENABLE	OffMode mode override control for pad~~usbc1_icusb_dm~~gpio_99 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
8	~~USBC1_ICUSB_DM_INPUTENABLE~~ GPIO_99_INPUTENABLE	Input enable value for pad~~usbc1_icusb_dm~~gpio_99 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	~~USBC1_ICUSB_DM_PULLTYPESELECT~~ GPIO_99_PULLTYPESELECT	Pull-Up/Down selection for pad~~usbc1_icusb_dm~~gpio_99 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	~~USBC1_ICUSB_DM_PULLUDENABLE~~ GPIO_99_PULLUDENABLE	Pull-Up/Down enable for pad~~usbc1_icusb_dm~~gpio_99 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	~~USBC1_ICUSB_DM_MUXMODE~~ GPIO_99_MUXMODE	Functional multiplexing selection for pad~~usbc1_icusb_dm~~gpio_99 ~~0x0: Select usbc1_icusb_dm~~ 0x0,0x3: Select gpio_99 0x7: Select safe_mode	RW	0x7

Table 19.56. Register Call Summary for Register CONTROL_CORE_PAD0_GPIO_99_PAD1_SDMMC1_CLK

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.57. CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL

Address Offset	0x0000 0124		
Physical Address	See Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads i2c1_sda and i2c2_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C2_SCL_WAKEUPEVENT	I2C2_SCL_WAKEUPENABLE	I2C2_SCL_OFFMODEPULLTYPESELECT	I2C2_SCL_OFFMODEPULLUDENABLE	I2C2_SCL_OFFMODEOUTVALUE	I2C2_SCL_OFFMODEOUTENABLE	I2C2_SCL_OFFMODEENABLE	I2C2_SCL_INPUTENABLE	RESERVED			I2C2_SCL_PULLTYPESELECT	I2C2_SCL_PULLUDENABLE	I2C2_SCL_MUXMODE			I2C1_SDA_WAKEUPEVENT	I2C1_SDA_WAKEUPENABLE	RESERVED					I2C1_SDA_INPUTENABLE	RESERVED			I2C1_SDA_PULLTYPESELECT	I2C1_SDA_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31	I2C2_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	I2C2_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	I2C2_SCL_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad i2c2_scl 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	I2C2_SCL_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad i2c2_scl 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	I2C2_SCL_OFFMODEOUTVALUE	OffMode mode output value for pad i2c2_scl 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	I2C2_SCL_OFFMODEOUTENABLE	OffMode mode output enable value for pad i2c2_scl. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	I2C2_SCL_OFFMODEENABLE	OffMode mode override control for pad i2c2_scl 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	I2C2_SCL_INPUTENABLE	Input enable value for pad i2c2_scl 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	I2C2_SCL_PULLTYPES-ELECT	pullup/down selection for pad i2c2_scl 0x0: pulldown selected 0x1: pullup selected	RW	1
19	I2C2_SCL_PULLUDENABLE	pullup/down enable for pad i2c2_scl 0x0: pullup/down disabled	RW	1

Bits	Field Name	Description	Type	Reset
		0x1: pullup/down enabled		
18:16	I2C2_SCL_MUXMODE	Functional multiplexing selection for pad i2c2_scl 0x0: Select i2c2_scl 0x1: Select uart1_rx 0x3: Select gpio_128 0x7: Select safe_mode	RW	0x7
15	I2C1_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	I2C1_SDA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	I2C1_SDA_INPUTENABLE	Input enable value for pad i2c1_sda 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	I2C1_SDA_PULLTYPESELECT	pullup/down selection for pad i2c1_sda 0x0: pulldown selected 0x1: pullup selected	RW	~~1~~0
3	I2C1_SDA_PULLUDENABLE	pullup/down enable for pad i2c1_sda 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	~~1~~0
2:0	RESERVED		R	0x0

Table 19.58. Register Call Summary for Register CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.59. CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD

Address Offset	0x0000 0148		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc5_clk and sdmmc5_cmd Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC5_CMD_WAKEUPEVENT	SDMMC5_CMD_WAKEUPENABLE	SDMMC5_CMD_OFFMODEPULLTYPESELECT	SDMMC5_CMD_OFFMODEPULLUDENABLE	SDMMC5_CMD_OFFMODEOUTVALUE	SDMMC5_CMD_OFFMODEOUTENABLE	SDMMC5_CMD_OFFMODEENABLE	SDMMC5_CMD_INPUTENABLE	RESERVED			SDMMC5_CMD_PULLTYPESELECT	SDMMC5_CMD_PULLUDENABLE	SDMMC5_CMD_MUXMODE			SDMMC5_CLK_WAKEUPEVENT	SDMMC5_CLK_WAKEUPENABLE	SDMMC5_CLK_OFFMODEPULLTYPESELECT	SDMMC5_CLK_OFFMODEPULLUDENABLE	SDMMC5_CLK_OFFMODEOUTVALUE	SDMMC5_CLK_OFFMODEOUTENABLE	SDMMC5_CLK_OFFMODEENABLE	SDMMC5_CLK_INPUTENABLE	RESERVED			SDMMC5_CLK_PULLTYPESELECT	SDMMC5_CLK_PULLUDENABLE	SDMMC5_CLK_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SDMMC5_CMD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SDMMC5_CMD_WAKEUPE-NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	SDMMC5_CMD_OFF-MODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad sd-mmc5_cmd 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	SDMMC5_CMD_OFF-MODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad sdm mc5_cmd 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	SDMMC5_CMD_OFFMODE-OUTVALUE	OffMode mode output value for pad sdmmc5_cmd 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC5_CMD_OFFMODE-OUTENABLE	OffMode mode output enable value for pad sdmmc5_cmd. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC5_CMD_OFF-MODEENABLE	OffMode mode override control for pad sdmmc5 _cmd 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
24	SD-MMC5_CMD_INPUTENABLE	Input enable value for pad sdmmc5_cmd 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC5_CMD_PULLTYPESELECT	Pull-Up/Down selection for pad sdmmc5_cmd 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1

Bits	Field Name	Description	Type	Reset
19	SDMMC5_CMD_PULLUDE-NABLE	Pull-Up/Down enable for pad sdmmc5_cmd 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SDMMC5_CMD_MUXMODE	Functional multiplexing selection for pad sdmmc5_cmd 0x1: Select mcspi2_simo 0x7: Select safe_mode 0x0: Select sdmmc5_cmd 0x2:~~Select usbc1_icusb_dm~~Reserved 0x5: Select sdmmc2_cmd 0x3: Select gpio_146	RW	0x7
15	SDMMC5_CLK_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	SDMMC5_CLK_WAKEUPE-NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13	SDMMC5_CLK_OFF-MODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad sd-mmc5_clk 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	SDMMC5_CLK_OFF-MODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad sdm mc5_clk 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	SDMMC5_CLK_OFFMODE-OUTVALUE	OffMode mode output value for pad sdmmc5_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC5_CLK_OFFMODE-OUTENABLE	OffMode mode output enable value for pad sdmmc5_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	SDMMC5_CLK_OFF-MODEENABLE	OffMode mode override control for pad sdmmc5 _clk 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
8	SD-MMC5_CLK_INPUTENABLE	Input enable value for pad sdmmc5_clk 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC5_CLK_PULLTYPESELECT	Pull-Up/Down selection for pad sdmmc5_clk 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	SDMMC5_CLK_PULLUDE-NABLE	Pull-Up/Down enable for pad sdmmc5_clk 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	SDMMC5_CLK_MUXMODE	Functional multiplexing selection for pad sdmmc5_clk	RW	0x7

Bits	Field Name	Description	Type	Reset
		0x1: Select mcspi2_clk		
		0x7: Select safe_mode		
		0x0: Select sdmmc5_clk		
		0x2:~~Select usbc1_icusb_dp~~Reserved		
		0x5: Select sdmmc2_clk		
		0x3: Select gpio_145		

Table 19.60. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.61. CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1

Address Offset	0x0000 014C		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads sdmmc5_dat0 and sdmmc5_dat1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	SDMMC5_DAT1_WAKEUPEVENT
30	SDMMC5_DAT1_WAKEUPENABLE
29	SDMMC5_DAT1_OFFMODEPULLTYPESELECT
28	SDMMC5_DAT1_OFFMODEPULLUDENABLE
27	SDMMC5_DAT1_OFFMODEOUTVALUE
26	SDMMC5_DAT1_OFFMODEOUTENABLE
25	SDMMC5_DAT1_OFFMODEENABLE
24	SDMMC5_DAT1_INPUTENABLE
23 22 21	RESERVED
20	SDMMC5_DAT1_PULLTYPESELECT
19	SDMMC5_DAT1_PULLUDENABLE
18 17 16	SDMMC5_DAT1_MUXMODE
15	SDMMC5_DAT0_WAKEUPEVENT
14	SDMMC5_DAT0_WAKEUPENABLE
13	SDMMC5_DAT0_OFFMODEPULLTYPESELECT
12	SDMMC5_DAT0_OFFMODEPULLUDENABLE
11	SDMMC5_DAT0_OFFMODEOUTVALUE
10	SDMMC5_DAT0_OFFMODEOUTENABLE
9	SDMMC5_DAT0_OFFMODEENABLE
8	SDMMC5_DAT0_INPUTENABLE
7 6 5	RESERVED
4	SDMMC5_DAT0_PULLTYPESELECT
3	SDMMC5_DAT0_PULLUDENABLE
2 1 0	SDMMC5_DAT0_MUXMODE

Bits	Field Name	Description	Type	Reset
31	SDMMC5_DAT1_WAKEUP-EVENT	Pad_x wake-up event status latched in the IO	R	0
		Read 0x1: A wake-up event occurred		
		Read 0x0: No wake-up event occurred		
30	SDMMC5_DAT1_WAKEUP-ENABLE	Input pad wake-up enable (and OFF mode input enable value)	RW	0
		0x0: wake-up detection on low level		
		0x1: wake-up detection on high level		
29	SDMMC5_DAT1_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad sd-mmc5_dat1	RW	0
		0x0: Offmode Pull-Down selected		
		0x1: Offmode Pull-Up selected		
28	SDMMC5_DAT1_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad sdm mc5_dat1	RW	0
		0x0: Offmode Pull-Up/Down disabled		

Bits	Field Name	Description	Type	Reset
		0x1: Offmode Pull-Up/Down enabled		
27	SDMMC5_DAT1_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_dat1 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	SDMMC5_DAT1_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_dat1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	SDMMC5_DAT1_OFFMODEENABLE	OffMode mode override control for pad sdmmc5_dat1 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	SDMMC5_DAT1_INPUTENABLE	Input enable value for pad sdmmc5_dat1 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SDMMC5_DAT1_PULLTYPESELECT	Pull-Up/Down selection for pad sdmmc5_dat1 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	SDMMC5_DAT1_PULLUDENABLE	Pull-Up/Down enable for pad sdmmc5_dat1 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	SDMMC5_DAT1_MUXMODE	Functional multiplexing selection for pad sdmmc5_dat1 0x0: Select sdmmc5_dat1 0x5: Select sdmmc2_dat1 0x3: Select gpio_148 0x7: Select safe_mode ~~0x2: Select usbc1_icusb_txen~~Reserved	RW	0x7
15	SDMMC5_DAT0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	SDMMC5_DAT0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13	SDMMC5_DAT0_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad sdmmc5_dat0 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	SDMMC5_DAT0_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad sdmmc5_dat0 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	SDMMC5_DAT0_OFFMODEOUTVALUE	OffMode mode output value for pad sdmmc5_dat0 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	SDMMC5_DAT0_OFFMODEOUTENABLE	OffMode mode output enable value for pad sdmmc5_dat0. This is an active low signal	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Output enable 0x1: Output disable		
9	SDMMC5_DAT0_OFFMODEENABLE	OffMode mode override control for pad sdmmc5_dat0 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
8	SDMMC5_DAT0_INPUTENABLE	Input enable value for pad sdmmc5_dat0 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SDMMC5_DAT0_PULLTYPESELECT	Pull-Up/Down selection for pad sdmmc5_dat0 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
3	SDMMC5_DAT0_PULLUDENABLE	Pull-Up/Down enable for pad sdmmc5_dat0 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	SDMMC5_DAT0_MUXMODE	Functional multiplexing selection for pad sdmmc5_dat0 0x1: Select mcspi2_somi 0x7: Select safe_mode 0x0: Select sdmmc5_dat0 ~~0x2: Select usbc1_icusb_rcv~~Reserved 0x5: Select sdmmc2_dat0 0x3: Select gpio_147	RW	0x7

Table 19.62. Register Call Summary for Register CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.63. CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP

Address Offset	0x0000 0194		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usba0_otg_ce and usba0_otg_dp Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29:21	20	19	18:16	15:5	4	3	2:0
USBA0_OTG_DP_WAKEUPEVENT	USBA0_OTG_DP_WAKEUPENABLE	RESERVED	USBA0_OTG_DP_PULLTYPESELECT	USBA0_OTG_DP_PULLUDENABLE	USBA0_OTG_DP_MUXMODE	RESERVED	USBA0_OTG_CE_PULLTYPESELECT	USBA0_OTG_CE_PULLUDENABLE	RESERVED

Bits	Field Name	Description	Type	Reset
31	USBA0_OTG_DP_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	USBA0_OTG_DP_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29:21	RESERVED		R	0x000
20	USBA0_OTG_DP_PULLTYPESELECT	Pull-Up/Down selection for pad usba0_otg_dp 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	USBA0_OTG_DP_PULLUDENABLE	Pull-Up/Down enable for pad usba0_otg_dp 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	USBA0_OTG_DP_MUXMODE	Functional multiplexing selection for pad usba0_otg_dp 0x0: Select usba0_otg_dp 0x1: Select uart3_rx_irrx 0x7: Select safe_mode 0x2: Select uart2_rx	RW	~~0x7~~0x0
15:5	RESERVED		R	0x000
4	USBA0_OTG_CE_PULLTYPESELECT	Pull-Up/Down selection for pad usba0_otg_ce 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	USBA0_OTG_CE_PULLUDENABLE	Pull-Up/Down enable for pad usba0_otg_ce 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	RESERVED		R	0x0

Table 19.64. Register Call Summary for Register CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.65. CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT

Address Offset	0x0000 0198		
Physical Address	Please refer to Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads usba0_otg_dm and fref_clk1_out Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	FREF_CLK1_OUT_WAKEUPEVENT
30	FREF_CLK1_OUT_WAKEUPENABLE
29	FREF_CLK1_OUT_OFFMODEPULLTYPESELECT
28	FREF_CLK1_OUT_OFFMODEPULLUDENABLE
27	FREF_CLK1_OUT_OFFMODEOUTVALUE
26	FREF_CLK1_OUT_OFFMODEOUTENABLE
25	FREF_CLK1_OUT_OFFMODEENABLE
24	FREF_CLK1_OUT_INPUTENABLE
23-21	RESERVED
20	FREF_CLK1_OUT_PULLTYPESELECT
19	FREF_CLK1_OUT_PULLUDENABLE
18-16	FREF_CLK1_OUT_MUXMODE
15-5	RESERVED
4	USBA0_OTG_DM_PULLTYPESELECT
3	USBA0_OTG_DM_PULLUDENABLE
2-0	USBA0_OTG_DM_MUXMODE

Bits	Field Name	Description	Type	Reset
31	FREF_CLK1_OUT_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	FREF_CLK1_OUT_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29	FREF_CLK1_OUT_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad fref_clk1_out 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	FREF_CLK1_OUT_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad fref_clk1_out 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	FREF_CLK1_OUT_OFFMODEOUTVALUE	OffMode mode output value for pad fref_clk1_out 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	FREF_CLK1_OUT_OFFMODEOUTENABLE	OffMode mode output enable value for pad fref_clk1_out. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	FREF_CLK1_OUT_OFFMODEENABLE	OffMode mode override control for pad fref_clk1_out 0x0: IO state keeps its previous state when OFF mode is active	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: IO state is forced to OFF mode value when OFF mode is active		
24	FREF_CLK1_OUT_INPUTENABLE	Input enable value for pad fref_clk1_out 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	FREF_CLK1_OUT_PULLTYPESELECT	Pull-Up/Down selection for pad fref_clk1_out 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	FREF_CLK1_OUT_PULLUDENABLE	Pull-Up/Down enable for pad fref_clk1_out 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	FREF_CLK1_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk1_out 0x0: Select fref_clk1_out 0x3: Select gpio_181 0x7: Select safe_mode	RW	0x7
15:5	RESERVED		R	0x000
4	USBA0_OTG_DM_PULLTYPESELECT	Pull-Up/Down selection for pad usba0_otg_dm 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	USBA0_OTG_DM_PULLUDENABLE	Pull-Up/Down enable for pad usba0_otg_dm 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	USBA0_OTG_DM_MUXMODE	Functional multiplexing selection for pad usba0_otg_dm 0x0: Select usba0_otg_dm 0x1: Select uart3_tx_irtx 0x7: Select safe_mode 0x2: Select uart2_tx	RW	~~0x7~~0x0

Table 19.66. Register Call Summary for Register CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.67. CONTROL_PADCONF_WAKEUPEVENT_2

Address Offset	0x0000 01E0		
Physical Address	See Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31	ABE_MCBSP1_CLKX_DUPLICATEWAKEUPEVENT
30	ABE_MCBSP2_FSX_DUPLICATEWAKEUPEVENT
29	ABE_MCBSP2_DX_DUPLICATEWAKEUPEVENT
28	ABE_MCBSP2_DR_DUPLICATEWAKEUPEVENT
27	ABE_MCBSP2_CLKX_DUPLICATEWAKEUPEVENT
26	SDMMC1_DAT7_DUPLICATEWAKEUPEVENT
25	SDMMC1_DAT6_DUPLICATEWAKEUPEVENT
24	SDMMC1_DAT5_DUPLICATEWAKEUPEVENT
23	SDMMC1_DAT4_DUPLICATEWAKEUPEVENT
22	SDMMC1_DAT3_DUPLICATEWAKEUPEVENT
21	SDMMC1_DAT2_DUPLICATEWAKEUPEVENT
20	SDMMC1_DAT1_DUPLICATEWAKEUPEVENT
19	SDMMC1_DAT0_DUPLICATEWAKEUPEVENT
18	SDMMC1_CMD_DUPLICATEWAKEUPEVENT
17	SDMMC1_CLK_DUPLICATEWAKEUPEVENT
16	USBC1_ICUSB_DM_DUPLICATEWAKEUPEVENTGPIO_99_DUPLICATEWAKEUPEVENT
15	USBC1_ICUSB_DP_DUPLICATEWAKEUPEVENTGPIO_98_DUPLICATEWAKEUPEVENT
14	USBB1_HSIC_STROBE_DUPLICATEWAKEUPEVENT
13	USBB1_HSIC_DATA_DUPLICATEWAKEUPEVENT
12	USBB1_ULPITLL_DAT7_DUPLICATEWAKEUPEVENT
11	USBB1_ULPITLL_DAT6_DUPLICATEWAKEUPEVENT
10	USBB1_ULPITLL_DAT5_DUPLICATEWAKEUPEVENT
9	USBB1_ULPITLL_DAT4_DUPLICATEWAKEUPEVENT
8	USBB1_ULPITLL_DAT3_DUPLICATEWAKEUPEVENT
7	USBB1_ULPITLL_DAT2_DUPLICATEWAKEUPEVENT
6	USBB1_ULPITLL_DAT1_DUPLICATEWAKEUPEVENT
5	USBB1_ULPITLL_DAT0_DUPLICATEWAKEUPEVENT
4	USBB1_ULPITLL_NXT_DUPLICATEWAKEUPEVENT
3	USBB1_ULPITLL_DIR_DUPLICATEWAKEUPEVENT
2	USBB1_ULPITLL_STP_DUPLICATEWAKEUPEVENT
1	USBB1_ULPITLL_CLK_DUPLICATEWAKEUPEVENT
0	CAM_GLOBALRESET_DUPLICATEWAKEUPEVENT

Bits	Field Name	Description	Type	Reset
31	ABE_MCBSP1_CLKX_DU-PLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp1_clkx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	ABE_MCBSP2_FSX_DUP-LICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_fsx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
29	ABE_MCBSP2_DX_DUPLIC ATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_dx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
28	ABE_MCBSP2_DR_DUPLIC ATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_dr Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
27	ABE_MCBSP2_CLKX_DU-PLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad abe_mcbsp2_clkx Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
26	SDMMC1_DAT7_DU-PLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sd-mmc1_dat7	R	0

Bits	Field Name	Description	Type	Reset
		Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred		
25	SDMMC1_DAT6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
24	SDMMC1_DAT5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
23	SDMMC1_DAT4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
22	SDMMC1_DAT3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
21	SDMMC1_DAT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
20	SDMMC1_DAT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
19	SDMMC1_DAT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_dat0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
18	SDMMC1_CMD_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_cmd Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
17	SDMMC1_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad sdmmc1_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
16	~~USBC1_ICUSB_DM_DUPLICATEWAKEUPEVENT~~ GPIO_99_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad ~~usbc1_icusb_dm~~gpio_99 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
15	~~USBC1_ICUSB_DP_DUPLICATEWAKEUPEVENT~~ GPIO_98_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad ~~usbc1_icusb_dp~~gpio_98 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	USBB1_HSIC_STROBE_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_hsic_strobe Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Bits	Field Name	Description	Type	Reset
13	USBB1_HSIC_DATA_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_hsic_data Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
12	USBB1_ULPITLL_DAT7_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat7 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
11	USBB1_ULPITLL_DAT6_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat6 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
10	USBB1_ULPITLL_DAT5_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat5 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
9	USBB1_ULPITLL_DAT4_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat4 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
8	USBB1_ULPITLL_DAT3_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat3 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
7	USBB1_ULPITLL_DAT2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat2 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	USBB1_ULPITLL_DAT1_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat1 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	USBB1_ULPITLL_DAT0_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dat0 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	USBB1_ULPITLL_NXT_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_nxt Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	USBB1_ULPITLL_DIR_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_dir Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	USBB1_ULPITLL_STP_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_stp Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
1	USBB1_ULPITLL_CLK_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad usbb1_ulpitll_clk Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Bits	Field Name	Description	Type	Reset
0	CAM_GLOBALRESET_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad cam_globalreset Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Table 19.68. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_2

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0][1][2][3][4]

Table 19.69. CONTROL_SMART1IO_PADCONF_2

Address Offset	0x0000 05D0		
Physical Address	Please refer to Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	SMART1 IO control 2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28	27 26	25 24	23 22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_DR0_SC	KPD_DR1_SC	KPD_DR2_SC	KPD_DR3_SC	HDQ_DR0_SC																						

Bits	Field Name	Description	Type	Reset
31:30	KPD_DR0_SC	Slew rate control for group kpd_dr0 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
29:28	KPD_DR1_SC	Slew rate control for group kpd_dr1 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
27:26	KPD_DR2_SC	Slew rate control for group kpd_dr2 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
25:24	KPD_DR3_SC	Slew rate control for group kpd_dr3 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
23:22	HDQ_DR0_SC	Slew rate control for group hdq_dr0 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
21:20	GPIO_DR12_SC	Slew rate control for group gpio_dr12 Refer to Section 19.4.12.11,section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
~~21~~19:0	RESERVED		R	0x000000

Table 19.70. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_2

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment:[0]

Table 19.71. CONTROL_SMART1IO_PADCONF_3

Address Offset	0x0000 05D4		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_ CORE
Description	SMART1 IO control 3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_DR0_LB		KPD_DR1_LB		KPD_DR2_LB		KPD_DR3_LB		HDQ_DR0_LB																							

Bits	Field Name	Description	Type	Reset
31:30	KPD_DR0_LB	Load control for group kpd_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
29:28	KPD_DR1_LB	Load control for group kpd_dr1 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
27:26	KPD_DR2_LB	Load control for group kpd_dr2 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
25:24	KPD_DR3_LB	Load control for group kpd_dr3 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0

Bits	Field Name	Description	Type	Reset
23:22	HDQ_DR0_LB	Load control for group hdq_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
21:20	GPIO_DR12_LB	Load control for group gpio_dr12 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
~~21~~19:0	RESERVED		R	0x000000

Table 19.72. Register Call Summary for Register CONTROL_SMART1IO_PADCONF_3

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment:[0]

Table 19.73. CONTROL_PBIASLITE

Address Offset	0x0000 0600		
Physical Address	See Table 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	PBIASLITE control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					MMC1_PWRDNZ	MMC1_PBIASLITE_HIZ_MODE	MMC1_PBIASLITE_SUPPLY_HI_OUT	MMC1_PBIASLITE_VMODE_ERROR	MMC1_PBIASLITE_PWRDNZ	MMC1_PBIASLITE_VMODE																					

Bits	Field Name	Description	Type	Reset
~~31~~	~~PBIASLITE1_HIZ_MODE~~	~~HIZ MODE of the PBIASLITE1~~ ~~0x0: PBIAS1 is in normal operation mode.~~ ~~0x1: PBIAS1 output is in high-impedance state.~~	RW	~~0~~
~~30~~	~~PBIASLITE1_SUPPLY_HI_OUT~~	~~SUPPLY_HI_OUT from PBIASLITE1~~ ~~Read 0x0: SIM_VDDS = 1.8 V~~	R	~~0~~

Bits	Field Name	Description	Type	Reset
		~~Read 0x1: SIM_VDDS = 3 V~~		
~~29~~	~~PBIASLITE1_VMODE_ERROR~~	~~VMODE ERROR from PBIASLITE1~~ ~~Read 0x0: VMODE level is the same as SUPPLY_HI_OUT.~~ ~~Read 0x1: VMODE level is not the same as SUPPLY_HI_OUT.~~	R	0
28	~~PBIASLITE1_PWRDNZ~~	~~PWRDNZ control to PBIASLITE1~~ ~~This bit is used to protect the PBIAS1 cell (associated with the gpio_wk0-gpio_wk2 pads I/O cell) when SIM_VDDS is not stable.~~ ~~0x0: Software must clear this bit when SIM_VDDS changes.~~ ~~0x1: Software must set this bit only when SIM_VDDS is stable.~~	RW	0
~~27~~	~~PBIASLITE1_VMODE~~	~~VMODE control to PBIASLITE1~~ ~~0x0: SIM_VDDS = 1.8 V~~ ~~0x1: SIM_VDDS = 3 V~~	~~RW~~	~~1~~
31:27	RESERVED		R	0x00
26	MMC1_PWRDNZ	PWRDNZ control to MMC1 IO This bit is used to protect the MMC1 I/O cell when MMC1_VDDS is not stable. 0x0: Software must clear this bit when MMC1_VDDS changes. 0x1: Software must set this bit only when MMC1_VDDS is stable.	RW	0
25	MMC1_PBIASLITE_HIZ_MODE	HIZ_MODE from MMC1 PBIASLITE 0x0: PBIAS in normal operation mode 0x1: PBIAS output is in high impedance state	RW	0
24	MMC1_PBIASLITE_SUPPLY_HI_OUT	SUPPLY_HI_OUT from MMC1 PBIASLITE Read 0x0: MMC1_VDDS = 1.8V Read 0x1: MMC1_VDDS = 3V	R	0
23	MMC1_PBIASLITE_VMODE_ERROR	VMODE ERROR from MMC1 PBIASLITE Read 0x0: VMODE level is same as SUPPLY_HI_OUT Read 0x1: VMODE level is not same as SUPPLY_HI_OUT	R	0
22	MMC1_PBIASLITE_PWRDNZ	PWRDNZ control to MMC1 PBIASLITE This bit is used to protect the MMC1_PBIAS cell (MMC1 I/O cell associated) when MMC1_VDDS is not stable. 0x0: Software must clear this bit when MMC1_VDDS changes. 0x1: Software must set this bit only when MMC1_VDDS is stable.	RW	0
21	MMC1_PBIASLITE_VMODE	VMODE control to MMC1 PBIASLITE 0x0: MMC1_VDDS = 1.8V 0x1: MMC1_VDDS = 3V	RW	1
~~20~~	~~USBC1_ICUSB_PWRDNZ~~	~~PWRDNZ control to USBC1 IO~~ ~~This bit is used to protect the USBC1_ICUSB I/O cell when SIM_VDDS is not stable.~~ ~~0x0: Software must clear this bit when SIM_VDDS changes.~~ ~~0x1: Software must set this bit only when SIM_VDDS is stable.~~	~~RW~~	~~0~~
~~19~~20:0	RESERVED		R	0x00 0000

Table 19.74. Register Call Summary for Register CONTROL_PBIASLITE

Control Module Functional Description

- Extended-Drain I/O and PBIAS Cell:[0][1][2][3][4][5][6]

Table 19.75. CONTROL_I2C_0

Address Offset	0x0000 0604		
Physical Address	Please refer toTable 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	I2C pads control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30 29	28	27	26 25	24	23	22 21	20	19	18 17	16	15	14 13	12	11	10 9	8	7	6 5	4	3	2 1	0
I2C4_SDA_GLFENB	I2C4_SDA_LOAD_BITS	I2C4_SDA_PULLUPRESX	I2C3_SDA_GLFENB	I2C3_SDA_LOAD_BITS	I2C3_SDA_PULLUPRESX	I2C2_SDA_GLFENB	I2C2_SDA_LOAD_BITS	I2C2_SDA_PULLUPRESX	I2C1_SDA_GLFENB	I2C1_SDA_LOAD_BITS	I2C1_SDA_PULLUPRESX	I2C4_SCL_GLFENB	I2C4_SCL_LOAD_BITS	I2C4_SCL_PULLUPRESX	I2C3_SCL_GLFENB	I2C3_SCL_LOAD_BITS	I2C3_SCL_PULLUPRESX	I2C2_SCL_GLFENB	I2C2_SCL_LOAD_BITS	I2C2_SCL_PULLUPRESX	I2C1_SCL_GLFENB	I2C1_SCL_LOAD_BITS	I2C1_SCL_PULLUPRESX

Bits	Field Name	Description	Type	Reset
31	I2C4_SDA_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
30:29	I2C4_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c4 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	0x1
28	I2C4_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
27	I2C3_SDA_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
26:25	I2C3_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c3 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	0x1
24	I2C3_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
23	I2C2_SDA_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation		
22:21	I2C2_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c2 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	0x1
20	I2C2_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
19	I2C1_SDA_GLFENB	Active_high glitch free operation enable pin for i2c1 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
18:17	I2C1_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c1 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	~~0x2~~0x1
16	I2C1_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
15	I2C4_SCL_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
14:13	I2C4_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c4 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	0x1
12	I2C4_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
11	I2C3_SCL_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
10:9	I2C3_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c3 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	0x1
8	I2C3_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0

Bits	Field Name	Description	Type	Reset
7	I2C2_SCL_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
6:5	I2C2_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c2 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	0x1
4	I2C2_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
3	I2C1_SCL_GLFENB	Active_high glitch free operation enable pin for i2c1 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
2:1	I2C1_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c1 0x0: 4.5 kOhms (5-15 pF) / 1.66 kOhms (5-12 pF) 0x1: 2.1 kOhms (15-50 pF) / 920 Ohms (12-25 pF) 0x2: 860 Ohms (50-150 pF) / 500 Ohms (25-50 pF) 0x3: N.A / 300 Ohms (50-80 pF)	RW	~~0x2~~0x1
0	I2C1_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0

Table 19.76. Register Call Summary for Register CONTROL_I2C_0

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.77. CONTROL_MMC1

Address Offset	0x0000 0628		
Physical Address	SeeTable 19.42	**Instance**	SYSCTRL_PADCONF_CORE
Description	MMC1 control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDMMC1_PUSTRENGTH_GRP0	SDMMC1_PUSTRENGTH_GRP1	SDMMC1_PUSTRENGTH_GRP2	SDMMC1_PUSTRENGTH_GRP3	SDMMC1_DR0_SPEEDCTRL	SDMMC1_DR1_SPEEDCTRL	SDMMC1_DR2_SPEEDCTRL	RESERVED	USB_FD_CDEN																							

Bits	Field Name	Description	Type	Reset
31	SDMMC1_PUSTREN-GTH_GRP0	Pullstrengh control for sdmmc1_pustrength_grp0 0x0: Pull up with 50 to 110K ohms on MMC1 data pins 0x1: Pull up with 10 to 50K ohms on MMC1 data pins	RW	1
30	SDMMC1_PUSTREN-GTH_GRP1	Pullstrengh control for sdmmc1_pustrength_grp1 0x0: Pull up with 50 to 110K ohms on MMC1 data pins 0x1: Pull up with 10 to 50K ohms on MMC1 data pins	RW	0
29	SDMMC1_PUSTREN-GTH_GRP2	Pullstrengh control for sdmmc1_pustrength_grp2 0x0: Pull up with 50 to 110K ohms on MMC1 data pins 0x1: Pull up with 10 to 50K ohms on MMC1 data pins	RW	1
28	SDMMC1_PUSTREN-GTH_GRP3	Pullstrengh control for sdmmc1_pustrength_grp3 0x0: Pull up with 50 to 110K ohms on MMC1 data pins 0x1: Pull up with 10 to 50K ohms on MMC1 data pins	RW	1
27	SDMMC1_DR0_SPEEDCTRL	Speed control for group sdmmc1_dr0 0x0: FMAX = 26Mhz at 30pF 0x1: FMAX = 65Mhz at 30 pF	RW	0
26	SDMMC1_DR1_SPEEDCTRL	Speed control for group sdmmc1_dr1 0x0: FMAX = 26Mhz at 30pF 0x1: FMAX = 65Mhz at 30 pF	RW	0
25	SDMMC1_DR2_SPEEDCTRL	Speed control for group sdmmc1_dr2 0x0: FMAX = 26Mhz at 30pF 0x1: FMAX = 65Mhz at 30 pF	RW	0
~~24~~	~~USBC1_DR0_SPEEDCTRL~~	~~Speed control for group usbc1_dr0~~ ~~0x0: FMAX = 26Mhz at 30pF~~ ~~0x1: FMAX = 65Mhz at 30 pF~~	~~RW~~	~~0~~
24	RESERVED		R	0x0
23	USB_FD_CDEN	USB FD pull down select 0x0: select pull down from USB FD logic 0x1: select pull down from device control modules registers	RW	0
~~22~~	~~USBC1_ICUSB_DP_PDDIS~~	~~usbc1_icusb_dp pull down disable~~ ~~0x0: usbc1_icusb_dp pull down disabled~~ ~~0x1: usbc1_icusb_dp pull down enabled~~	~~RW~~	~~0~~
~~21~~	~~USBC1_ICUSB_DM_PDDIS~~	~~usbc1_icusb_dm pull dowm disable~~ ~~0x0: usbc1_icusb_dm pull down disabled~~ ~~0x1: usbc1_icusb_dm pull down enabled~~	~~RW~~	~~0~~
2022:0	RESERVED		R	0x000000

Table 19.78. Register Call Summary for Register CONTROL_MMC1

Control Module Functional Description

- Extended-Drain I/O and PBIAS Cell:[0][1][2][3]

19.6.8. SYSCTRL_PADCONF_WKUP Register Summary

Table 19.79. SYSCTRL_PADCONF_WKUP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_PADCONF_WKUP_REVISION	R	32	0x0000 0000	0x4A31 E000
CONTROL_PADCONF_WKUP_HWINFO	R	32	0x0000 0004	0x4A31 E004
CONTROL_PADCONF_WKUP_SYSCONFIG	RW	32	0x0000 0010	0x4A31 E010
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1	RW	32	0x0000 0040	0x4A31 E040
CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3	RW	32	0x0000 0044	0x4A31 E044
CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL	RW	32	0x0000 0048	0x4A31 E048
CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN	RW	32	0x0000 004C	0x4A31 E04C
CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ	RW	32	0x0000 0050	0x4A31 E050
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ	RW	32	0x0000 0054	0x4A31 E054
CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ	RW	32	0x0000 0058	0x4A31 E058
CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K	RW	32	0x0000 005C	0x4A31 E05C
CONTROL_WKUP_PAD0_SYS_NRES-PWRON_PAD1_SYS_NRESWARM	RW	32	0x0000 0060	0x4A31 E060
CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT	RW	32	0x0000 0064	0x4A31 E064
CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7	RW	32	0x0000 0068	0x4A31 E068
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK	RW	32	0x0000 006C	0x4A31 E06C
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC	RW	32	0x0000 0070	0x4A31 E070
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO	RW	32	0x0000 0074	0x4A31 E074
CONTROL_WKUP_PADCONF_WAKEUPEVENT_0	R	32	0x0000 007C	0x4A31 E07C

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_SMART1NOPMIO_PADCONF_0	RW	32	0x0000 05A0	0x4A31 E5A0
CONTROL_SMART1NOPMIO_PADCONF_1	RW	32	0x0000 05A4	0x4A31 E5A4
CONTROL_WKUP_PADCONF_MODE	RW	32	0x0000 05A8	0x4A31 E5A8
CONTROL_XTAL_OSCIL-LATOR	RW	32	0x0000 05AC	0x4A31 E5AC
CONTROL_SMART3NOPMIO_PADCONF_0	RW	32	0x0000 05B0	0x4A31 E5B0
CONTROL_SMART3NOPMIO_PADCONF_1	RW	32	0x0000 05B4	0x4A31 E5B4
~~CONTROL_GPIOWK~~ RESERVED	RW	32	0x0000 0600	0x4A31 E600
CONTROL_I2C_2	RW	32	0x0000 0604	0x4A31 E604
CONTROL_JTAG	RW	32	0x0000 0608	0x4A31 E608
CONTROL_SYS	RW	32	0x0000 060C	0x4A31 E60C
CONTROL_WKUP_CONTROL_SPARE_RW	RW	32	0x0000 0614	0x4A31 E614
CONTROL_WKUP_CONTROL_SPARE_R	R	32	0x0000 0618	0x4A31 E618
CONTROL_WKUP_CONTROL_SPARE_R_C0	RW	32	0x0000 061C	0x4A31 E61C
CONTROL_WKUP_CONTROL_SPARE_RW1	RW	32	0x0000 0620	0x4A31 E620
CONTROL_WKUP_CONTROL_SPARE_RW2	RW	32	0x0000 0624	0x4A31 E624
CONTROL_WKUP_CONTROL_SPARE_RW3	RW	32	0x0000 0628	0x4A31 E628
CONTROL_WKUP_CONTROL_SPARE_RW4	RW	32	0x0000 062C	0x4A31 E62C
CONTROL_WKUP_CONTROL_SPARE_RW5	RW	32	0x0000 0630	0x4A31 E630
CONTROL_WKUP_CONTROL_SPARE_RW6	RW	32	0x0000 0634	0x4A31 E634
CONTROL_WKUP_CONTROL_SPARE_RW7	RW	32	0x0000 0638	0x4A31 E638
CONTROL_WKUP_CONTROL_SPARE_RW8	RW	32	0x0000 063C	0x4A31 E63C
CONTROL_WKUP_CONTROL_SPARE_RW9	RW	32	0x0000 0640	0x4A31 E640

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_WKUP_CONTROL_SPARE_R1	R	32	0x0000 064C	0x4A31 E64C

19.6.9. SYSCTRL_PADCONF_WKUP Register Summary

Note

This section contains only modified registers.

Table 19.80. CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1

Address Offset	0x0000 0040		
Physical Address	See Table 19.79	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk0 and gpio_wk1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO_WK1_WAKEUPEVENT	GPIO_WK1_WAKEUPENABLE	RESERVED					GPIO_WK1_INPUTENABLE	RESERVED			GPIO_WK1_PULLTYPESELECT	GPIO_WK1_PULLUDENABLE				GPIO_WK0_WAKEUPEVENT	GPIO_WK0_WAKEUPENABLE	RESERVED					GPIO_WK0_INPUTENABLE	RESERVED			GPIO_WK0_PULLTYPESELECT	GPIO_WK0_PULLUDENABLE			

Bits	Field Name	Description	Type	Reset
31	GPIO_WK1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPIO_WK1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	GPIO_WK1_INPUTENABLE	Input enable value for pad gpio_wk1 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPIO_WK1_PULLTYPESELECT	pullup/down selection for pad gpio_wk1 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPIO_WK1_PULLUDENABLE	pullup/down enable for pad gpio_wk1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

Bits	Field Name	Description	Type	Reset
18:16	GPIO_WK1_MUXMODE	Functional multiplexing selection for pad gpio_wk1 ~~0x0: Reserved~~ 0x0,0x3: Select gpio_wk1 0x6: Select hw_dbg2 0x7: Select safe_mode	RW	0x7
15	GPIO_WK0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO_WK0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK0_INPUTENABLE	Input enable value for pad gpio_wk0 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK0_PULLTYPESELECT	pullup/down selection for pad gpio_wk0 0x0: pulldown selected 0x1: pullup selected	RW	0
3	GPIO_WK0_PULLUDENABLE	pullup/down enable for pad gpio_wk0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPIO_WK0_MUXMODE	Functional multiplexing selection for pad gpio_wk0 ~~0x0: Reserved~~ 0x0,0x3: Select gpio_wk0 0x4: Select c2c_pwkup 0x6: Select hw_dbg1 0x7: Select safe_mode	RW	0x7

Table 19.81. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.82. CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3

Address Offset	0x0000 0044		
Physical Address	Please refer toTable 19.79	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk2 and gpio_wk3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29:25	24	23:21	20	19	18:16	15	14	13:9	8	7:5	4	3	2:0
GPIO_WK3_WAKEUPEVENT	GPIO_WK3_WAKEUPENABLE	RESERVED	GPIO_WK3_INPUTENABLE	RESERVED	GPIO_WK3_PULLTYPESELECT	GPIO_WK3_PULLUDENABLE	GPIO_WK3_MUXMODE	GPIO_WK2_WAKEUPEVENT	GPIO_WK2_WAKEUPENABLE	RESERVED	GPIO_WK2_INPUTENABLE	RESERVED	GPIO_WK2_PULLTYPESELECT	GPIO_WK2_PULLUDENABLE	GPIO_WK2_MUXMODE

Bits	Field Name	Description	Type	Reset
31	GPIO_WK3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	GPIO_WK3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29:25	RESERVED		R	0x00
24	GPIO_WK3_INPUTENABLE	Input enable value for pad gpio_wk3 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPIO_WK3_PULLTYPES-ELECT	Pull-Up/Down selection for pad gpio_wk3 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	1
19	GPIO_WK3_PULLUDENABLE	Pull-Up/Down enable for pad gpio_wk3 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	GPIO_WK3_MUXMODE	Functional multiplexing selection for pad gpio_wk3 ~~0x0: Reserved~~ 0x0,0x3: Select gpio_wk3 0x7: Select safe_mode 0x6: Select hw_dbg4	RW	0x7
15	GPIO_WK2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPIO_WK2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK2_INPUTENABLE	Input enable value for pad gpio_wk2 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK2_PULLTYPES-ELECT	Pull-Up/Down selection for pad gpio_wk2	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Pull-Down selected 0x1: Pull-Up selected		
3	GPIO_WK2_PULLUDENABLE	Pull-Up/Down enable for pad gpio_wk2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPIO_WK2_MUXMODE	Functional multiplexing selection for pad gpio_wk2 ~~0x0: Reserved~~ 0x0,0x3: Select gpio_wk2 0x7: Select safe_mode 0x6: Select hw_dbg3	RW	0x7

Table 19.83. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.84. CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL

Address Offset	0x0000 0048		
Physical Address	Please refer toTable 19.79	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk4 and sr_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

Bits	Field
31	SR_SCL_WAKEUPEVENT
30	SR_SCL_WAKEUPENABLE
29:25	RESERVED
24	SR_SCL_INPUTENABLE
23:21	RESERVED
20	SR_SCL_PULLTYPESELECT
19	SR_SCL_PULLUDENABLE
18:16	RESERVED
15	GPIO_WK4_WAKEUPEVENT
14	GPIO_WK4_WAKEUPENABLE
13:9	RESERVED
8	GPIO_WK4_INPUTENABLE
7:5	RESERVED
4	GPIO_WK4_PULLTYPESELECT
3	GPIO_WK4_PULLUDENABLE
2:0	GPIO_WK4_MUXMODE

Bits	Field Name	Description	Type	Reset
31	SR_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SR_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29:25	RESERVED		R	0x00
24	SR_SCL_INPUTENABLE	Input enable value for pad sr_scl 0x0: Input buffere of IO cell is disabled 0x1: Input buffer of IO cell is enabled	RW	1

Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	SR_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad sr_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	SR_SCL_PULLUDENABLE	Pull-Up/Down enable for pad sr_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0
18:16	RESERVED		R	0x0
15	GPIO_WK4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPIO_WK4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK4_INPUTENABLE	Input enable value for pad gpio_wk4 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK4_PULLTYPES-ELECT	Pull-Up/Down selection for pad gpio_wk4 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPIO_WK4_PULLUDENABLE	Pull-Up/Down enable for pad gpio_wk4 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPIO_WK4_MUXMODE	Functional multiplexing selection for pad gpio_wk4 ~~0x0: Reserved~~ 0x0,0x3: Select gpio_wk4 0x6: Select hw_dbg5 0x7: Select safe_mode	RW	0x7

Table 19.85. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.86. CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K

Address Offset	0x0000 005C		
Physical Address	SeeTable 19.79	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads fref_clk4_out and sys_32k Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	SYS_32K_WAKEUPEVENT
30	SYS_32K_WAKEUPENABLE
29–25	RESERVED
24	SYS_32K_INPUTENABLE
23–21	RESERVED
20	SYS_32K_PULLTYPESELECT
19	SYS_32K_PULLUDENABLE
18–16	RESERVED
15	FREF_CLK4_OUT_WAKEUPEVENT
14	FREF_CLK4_OUT_WAKEUPENABLE
13–9	RESERVED
8	FREF_CLK4_OUT_INPUTENABLE
7–5	RESERVED
4	FREF_CLK4_OUT_PULLTYPESELECT
3	FREF_CLK4_OUT_PULLUDENABLE
2–0	FREF_CLK4_OUT_MUXMODE

Bits	Field Name	Description	Type	Reset
31	SYS_32K_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_32K_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SYS_32K_INPUTENABLE	Input enable value for pad sys_32k 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_32K_PULLTYPESE-LECT	pullup/down selection for pad sys_32k 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_32K_PULLUDENABLE	pullup/down enable for pad sys_32k 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	0
18:16	RESERVED		R	0x0
15	FREF_CLK4_OUT_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	FREF_CLK4_OUT_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	FREF_CLK4_OUT_INPUTE NABLE	Input enable value for pad fref_clk4_out 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	FREF_CLK4_OUT_PULL-TYPESELECT	pullup/down selection for pad fref_clk4_out 0x0: pulldown selected 0x1: pullup selected	RW	0

Bits	Field Name	Description	Type	Reset
3	FREF_CLK4_OUT_PULLUDENABLE	pullup/down enable for pad fref_clk4_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	~~1~~0
2:0	FREF_CLK4_OUT_MUXMODE	Functional multiplexing selection for pad fref_clk4_out 0x0: Select fref_clk4_out 0x3: Select gpio_wk8 0x6: Select hw_dbg10	RW	0x0

Table 19.87. Register Call Summary for Register CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.88. CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM

Address Offset	0x0000 0060		
Physical Address	See Table 19.79	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads sys_nrespwron and sys_nreswarm Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29–5	4	3	2–0
SYS_NRESWARM_WAKEUPEVENT	SYS_NRESWARM_WAKEUPENABLE	RESERVED	SYS_NRESPWRON_PULLTYPESELECT	SYS_NRESPWRON_PULLUDENABLE	RESERVED

Bits	Field Name	Description	Type	Reset
31	SYS_NRESWARM_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_NRESWARM_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:05	RESERVED		R	0x0000000
4	SYS_NRESPWRON_PULLTYPESELECT	pullup/down selection for pad sys_nrespwron 0x0: pulldown selected 0x1: pullup selected	RW	0
3	SYS_NRESPWRON_PULLUDENABLE	pullup/down enable for pad sys_nrespwron 0x0: pullup/down disabled	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: pullup/down enabled		
2:0	RESERVED		R	0x0

Table 19.89. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.90. CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC

Address Offset	0x0000 0070		
Physical Address	SeeTable 19.79	**Instance**	SYSCTRL_PADCONF_ WKUP
Description	Register control for Pads jtag_rtck and jtag_tms_tmsc Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29–25	24	23–19	18–16	15	14	13–5	4	3	2–0
JTAG_TMS_TMSC_WAKEUPEVENT	JTAG_TMS_TMSC_WAKEUPENABLE	RESERVED	JTAG_TMS_TMSC_INPUTENABLE	RESERVED	JTAG_TMS_TMSC_MUXMODE	JTAG_RTCK_WAKEUPEVENT	JTAG_RTCK_WAKEUPENABLE	RESERVED	JTAG_RTCK_PULLTYPESELECT	JTAG_RTCK_PULLUDENABLE	RESERVED

Bits	Field Name	Description	Type	Reset
31	JTAG_TMS_TMSC_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	JTAG_TMS_TMSC_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	JTAG_TMS_TMSC_INPUTE NABLE	Input enable value for pad jtag_tms_tmsc 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:19	RESERVED		R	0x00
18:16	JTAG_TMS_TMSC_MU XMODE	Functional multiplexing selection for pad jtag_tms_tmsc 0x0: Select jtag_tms_tmsc 0x7: Select safe_mode	RW	0x0
15	JTAG_RTCK_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Bits	Field Name	Description	Type	Reset
14	JTAG_RTCK_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:5	RESERVED		R	0x000
4	JTAG_RTCK_PULL-TYPESELECT	pullup/down selection for pad jtag_rtck 0x0: pulldown selected 0x1: pullup selected	RW	0
3	JTAG_RTCK_PULLUDENABLE	pullup/down enable for pad jtag_rtck 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	~~1~~0
2:0	RESERVED		R	0x0

Table 19.91. Register Call Summary for Register CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 19.92. CONTROL_SMART1NOPMIO_PADCONF_0

Address Offset	0x0000 05A0		
Physical Address	See Table 19.79	**Instance**	SYSCTRL_PADCONF_WKUP
Description	SMART1 NOPM I/O control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30	29 28 27 26 25 24 23 22 21 20	19 18	17 16	15 14	13 12	11 10	9	8	7	6	5	4	3	2	1	0
FREF_DR0_SC	RESERVED	GPIO_DR7_SC	RESERVED	DPM_DR0_SC	RESERVED	GPIO_DR11_SC										

Bits	Field Name	Description	Type	Reset
31:30	FREF_DR0_SC	Slew rate control for group fref_dr0 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
29:20	RESERVED		R	0x000
19:18	GPIO_DR7_SC	Slew rate control for group gpio_dr7 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
17:16	RESERVED		R	0x0
15:14	DPM_DR0_SC	Slew rate control for group dpm_dr0 Refer to Section 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
~~13:12~~	~~GPIOWK4_DR0_SC~~	~~Slew rate control for group gpiowk4_dr0~~ ~~Refer to Section 19.4.12.11, section~~	RW	0x0

Bits	Field Name	Description	Type	Reset
		~~Low Speed I/Os Combined~~ ~~Slew Rate vs TL Length and Load Settings~~ ~~for more details on SR settings.~~		
13:12	RESERVED		R	0x000
11:10	GPIO_DR11_SC	Slew rate control for group gpio_dr11 Refer toSection 19.4.12.11, section Low Speed I/Os Combined Slew Rate vs TL Length and Load Settings for more details on SR settings.	RW	0x0
~~11~~9:0	RESERVED		R	0x000

Table 19.93. Register Call Summary for Register CONTROL_SMART1NOPMIO_PADCONF_0

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment:[0]

Table 19.94. CONTROL_SMART1NOPMIO_PADCONF_1

Address Offset	0x0000 05A4		
Physical Address	SeeTable 19.79	**Instance**	SYSCTRL_PADCONF_ WKUP
Description	SMART1 NOPM I/O control 1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">FREF_DR0_LB</td><td colspan="10">RESERVED</td><td colspan="2">GPIO_DR7_LB</td><td colspan="2">RESERVED</td><td colspan="2">DPM_DR0_LB</td><td colspan="2">RESERVED</td><td colspan="2">GPIO_DR11_LB</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

Bits	Field Name	Description	Type	Reset
31:30	FREF_DR0_LB	Load control for group fref_dr0 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
29:20	RESERVED		R	0x000
19:18	GPIO_DR7_LB	Load control for group gpio_dr7 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
17:16	RESERVED		R	0x0
15:14	DPM_DR0_LB	Load control for group dpm_dr0 0x0: TL Length= [2cm-20cm] /	RW	0x0

Bits	Field Name	Description	Type	Reset
		Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]		
~~13:12~~	~~GPIOWK4_DR0_LB~~	~~Load control for group gpiowk4_dr0~~ ~~0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF]~~ ~~0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF]~~ ~~0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF]~~ ~~0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]~~	~~RW~~	~~0x0~~
13:12	RESERVED		R	0x000
11:10	GPIO_DR11_LB	Load control for group gpio_dr11 0x0: TL Length= [2cm-20cm] / Farend cap per TL= [1pF-10pF] 0x1: Dual TL Length= [20cm-40cm] / Farend cap per TL= [1pF-10pF] 0x2: TL Length = [2cm-20cm] / Farend cap per TL= [10pF-20pF] 0x3: Dual TL Length = [20cm-40cm] / Farend cap per TL= [10pF-20pF]	RW	0x0
~~11~~9:0	RESERVED		R	0x000

Table 19.95. Register Call Summary for Register CONTROL_SMART1NOPMIO_PADCONF_1

Control Module Functional Description

- Signal Integrity Parameter Control Registers With Pad Group Assignment:[0]

Chapter 20. Mailbox

This chapter describes the differences in the Mailbox between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 21. Memory Management Units

This chapter describes the differences in the Memory Management Units between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 22. Spinlock

This chapter describes the differences in the Spinlock between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 23. Timers

This chapter describes the differences in the Timers between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 24. Serial Communication Interface

This chapter describes the differences in the Serial Communication Interfaces between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

24.1. Multimaster High-Speed I2C Controller

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.2. HDQ/1-Wire

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.3. UART/IrDA/CIR

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.4. Multichannel Serial Port Interface (MCSPI)

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.5. Multichannel Buffered Serial Port (MCBSP)

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.6. Multichannel PDM Controller

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.7. Digital Microphone Module

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.8. Multichannel Audio Serial Port

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.9. Serial Low-Power Inter-Chip Media Bus Controller

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.10. MIPI High-Speed Synchronous Serial Interface

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.11. High-Speed Multiport USB Host Subsystem

Note

Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.12. High-Speed USB OTG Controller

Note

The High-Speed USB OTG Controller is an instantiation of the MUSBMHDRC from Mentor Graphics Corporation.

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Note

This section has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

24.13. Full-Speed USB Host Controller

Note

Note

The Full-Speed USB host controller is no longer available in OMAP4470 Silicon Revision 1.0.

Chapter 25. MMC/SD/SDIO

This chapter describes the differences in the MMC/SD/SDIO between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 26. General Purpose Interface

This chapter describes differences in General-Purpose Interface between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

26.1. General Purpose Interface Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.2. General Purpose Interface Environment

Caution

Because of buffer strength, an external serial resistor must be connected to the balls where gpio_10~~0~~6 through gpio_109 are muxed with MMC signals.

26.2.1. General - Purpose Interface as a Keyboard Interface

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.2.2. General - Purpose Interface Signals

Refer to OMAP4470 Silicon revision 1.0 TRM.

26.4. General-Purpose Interface Functional Description

26.4.1. General-Purpose Interface Block Diagram

Refer to OMAP 4470 Silicon Revision 1.0 TRM.

26.4.2. General-Purpose Interface Interrupt and Wake-Up Features

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.4.3. General-Purpose Interface Clock Configuration

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.4.4. General-Purpose Interface Hardware and Software Reset

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.4.5. General-Purpose Interface Power Management

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.4.6. General-Purpose Interface Interrupt and Wake-Up Requests

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.4.7. General-Purpose Interface Channel Description

Table 26.1. GPIO Channel Description

Channel Number	Type[1]	Mapping	Wake-Up Feature	Comments
GPIO1				
[31]	I/O	gpio_wk31	Yes[2]	Wake-up path
[30]	I/O	gpio_wk30	Yes[2]	Wake-up path
[29]	I/O	gpio_wk29	Yes[2]	Wake-up path
[28:11]	I/O	gpio_[28:11]	Yes[2]	GPIO
[10:6]	I/O	gpio_wk[10:6]	Yes[2]	Wake-up path
[5]	I	gpi_wk5	Yes[2]	Inputs only
[4]	I/O	gpio_wk4	Yes[2]	Wake-up path
[3]	I/O	gpio_wk3	Yes[2]	Wake-up path
	I/O	gpio_3	Yes[2]	GPIO
[2]	I/O	gpio_wk2	Yes[2]	Wake-up path
	I/O	gpio_2	Yes[2]	GPIO
[1:0]	I/O	gpio_[1:0]	Yes[2]	GPIO
	I/O	gpio_wk[1:0]	Yes[2]	Wake-up path
GPIO2				
[31:27]	I/O	gpio_[63:59]	Yes[2]	GPIO
[26][3]	I	~~TV_SHORT~~gpio_58	Yes[2]	~~Internal TV short signal from video DAC1~~Reserved for internal use only
[25][3]	I	~~TV_DETECT~~gpio_57	Yes[2]	~~Internal TV detection signal from video DAC1~~Reserved for internal use only
[24:0]	I/O	gpio_[56:32]	Yes[2]	GPIO
GPIO3				
[31:17]	I/O	gpio_[95:87]	Yes[2]	GPIO
[22][5]	I/O	gpio_86	Yes[2]	GPIO
	I	TSHUT	Yes[2]	Bandgap internal TSHUT
[21:17]	I/O	gpio_[85:81]	Yes[2]	GPIO
[16:3]	I	gpi_[80:67]	Yes[2]	GPIO inputs only
[2:0]	I/O	gpio_[66:64]	Yes[2]	GPIO
GPIO4				
[31:0]	I/O	gpio_[127:96]	Yes[2]	GPIO
GPIO5				
[31:0]	I/O	gpio_[159:128]	Yes[2]	GPIO
GPIO6				
[31:21]	I/O	gpio_[191:181]	Yes[2]	GPIO
[20][3]	I	DPDM5VSHORT	Yes[2]	USB OTG PHY short detect (DPDM5VSHORT)
[19][3]	I	CHGDETECT	Yes[2]	USB OTG PHY charge detect (CHGDETECT)
[18:15]	I/O	gpio_[178:175]	Yes[2]	GPIO
[14:0]	I/O	gpio_[174:160]		GPIO

Channel Number	Type[1]	Mapping	Wake-Up Feature	Comments
			Yes[2]	

1. I = Input; O = Output
2. Only when the PER power domain is active
3. The GPIO channel is not available on device pads. Reserved for internal use only (see the Comments column).
4. The video DAC (VDAC) function is not supported.
5. The GPIO channel provides additional internal functionality (see the Comments column), besides its GPIO capabilities, when it is not connected to a pad of the device. That is, the corresponding pad is configured in a mode different from multiplexing mode 3. For more information about pad configuration and multiplexing, see , Pad Functional Multiplexing and Configuration, in , Control Module.

26.4.8. General-Purpose Interface Data Input/Output Capabilities

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.4.9. General-Purpose Interface Set-and-Clear Protocol

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.5. General-Purpose Interface Programming Guide

Refer to OMAP4470 Silicon Revision 1.0 TRM.

26.6. General-Purpose Interface Register Manual

Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 27. Keyboard Controller

This chapter describes the differences in the Keyboard Controller between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

Note

This chapter has not changed. Refer to OMAP4470 Silicon Revision 1.0 TRM.

Chapter 28. Initialization

This chapter describes differences in initialization between the OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0 multimedia devices.

28.1. Initialization Overview

Refer to OMAP4470 Silicon Revision 1.0 TRM

28.2. Preinitialization

- The TPS62361 auxiliary power-supply device is not used to supply the MPU PD
- TWL6032 replaces the TWL6030 power-management device
- TWL6041 replaces the TWL6040 audio device
- TPS62234 is used for 2.1-V pre-regulation of TWL6041, and LDO6 and LDOLN of TWL6032
- A new booting option is introduced: MMC2_BOOT (MMC2 interface), which is the same as MMC2(1) booting option but supports the boot partition feature of the eMMC standard.
- Tables *Memory Preferred Booting* and *Peripheral Preferred Booting* are updated with sys_boot[4:0] booting options:
  - 0b00100
  - 0b01100

28.3. Power, Clocks, and Reset Power-Up Sequence

Refer to OMAP4470 Silicon Revision 1.0 TRM

28.4. Device Initialization by ROM Code

- ASIC-ID descriptor has been updated to discriminate OMAP4470 from other devices. Device identifier is 0x4470.
- USB Device Descriptor's field Product ID has been updated to discriminate OMAP4470 from other devices during USB boot. Product ID String Descriptor is OMAP4470.
- Tracing vector 3 is updated as follows:

Table 28.1. Tracing Vector 3

Bit	Group	Meaning
0	Memory boot	Memory booting device NULL
1	Memory boot	Memory booting device XIP
2	Memory boot	Memory booting device XIPWAIT
3	Memory boot	Memory booting device NAND
4	Memory boot	Memory booting device OneNAND
5	Memory boot	Memory booting device MMC1
6	~~Reserved~~Memory boot	Memory booting device MMC2(1)
7	Memory boot	~~Memory booting device MMC2(1)~~Memory booting device MMC2(2)
8	~~Reserved~~Memory boot	Memory booting device MMC2_BOOT
9	Reserved	
10	Reserved	
11	~~Memory boot~~Reserved	~~Memory booting device MMC2(2)~~
12	Reserved	
13	Reserved	
14	Reserved	
15	Reserved	
16	Reserved	

Bit	Group	Meaning
17	Reserved	
18	Peripheral boot	Peripheral booting device UART3
19	Reserved	
20	Peripheral boot	Peripheral booting device USB(1)
21	Peripheral boot	Peripheral booting device USB-ULPI
22	Peripheral boot	Peripheral booting device USB(2)
23	Peripheral boot	Peripheral booting device NULL
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Reserved	
29	Reserved	
30	Reserved	
31	Reserved	

28.5. Services for HLOS Support

Refer to OMAP4470 Silicon Revision 1.0 TRM

Chapter 29. On-Chip Debug Support

This chapter describes the differences in the On-Chip Debug Support between OMAP4460 Silicon Revision 1.x and OMAP4470 Silicon Revision 1.0.

29.1. Introduction

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.2. Debug Ports

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.3. Debugger Connection

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.4. Primary Debug Support

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.5. Power, Reset, and Clock Management Debug Support

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.6. Performance Monitoring

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.7. Processor Trace

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.8. System Instrumentation

29.8.1. MIPI STM

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.8.2. Software Instrumentation

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.8.3. OCP Watch-Point

The Full-Speed USB host controller (FSUSB / USBHOSTFS) is removed and thus, it is no longer available as L3 master. Tables ***ConnID Mapping (Debug View)*** and **Statistics Collector Master Address Mapping** are updated in accordance.

29.8.4. IVA-HD Pipeline

Refer to OMAP4470 Silicon Revision 1.0 TRM.

29.8.5. NoC Statistics Collector

L3 NoC statistics collectors have the following functional changes:

- 2D blitter accelerator (BB2D) with two master ports and one slave port is now connected to the L3 interconnect. Also, SGX now has two master ports to L3. As a consequence, performance probes mapping (and related port mapping) is updated as follows:
  - SC_LAT0 instance:
    - ~~Six~~Eight probe inputs:
      - Probe 0: Cortex-A9 MPU subsystem
      - Probe 1: DSP subsystem
      - Probe 2: SDMA_RD
      - Probe 3: SDMA_WR
      - Probe 4: DSS
      - Probe 5: ISS
      - Probe 6: SGX_M1
        - NTTP REQ link mapped to port #12
        - NTTP RSP link mapped to port #13
      - Probe 7: BB2D_M1
        - NTTP REQ link mapped to port #14
        - NTTP RSP link mapped to port #15
  - SC_LAT1 instance:
    - ~~Five~~Six probe inputs:
      - Probe 0: IVA-HD
      - Probe 1: Cortex-A9 MPU subsystem
      - Probe 2: SDMA_WR
      - Probe 3: ~~SGX~~SGX_M2
      - Probe 4: Dual Cortex-M3 MPU subsystem
      - Probe 5: BB2D_M2
        - NTTP REQ link mapped to port #10
        - NTTP RSP link mapped to port #11
- SGX_M2, BB2D_M1, and BB2D_M2 added as initiators in ConnID Mapping (Debug View) table;
- Size of data counters (of all 3 statistics collector instances) doubled from 16- to 32-bits;
- Size of collecting window counter (of all 3 statistics collector instances) doubled from 16- to 32-bits;
- Counters 6 and 7 of SC_SDRAM now have 1 filter implemented
- L3 "Master Address" parameter changed from 8- to 10-bits
- Statistics collectors now support alarm and suspend modes (added sections Statistics Collector Alarm Mode and Statistics Collector Suspend Mode)

29.8.6. PM Instrumentation (PMI)

Refer to OMAP4470 Silicon Revision 1.x TRM.

29.8.7. CM Instrumentation (CMI)

Refer to OMAP4470 Silicon Revision 1.x TRM.

29.9. Concurrent Debug Modes

Refer to OMAP4470 Silicon Revision 1.x TRM.

29.10. Memory Mapping

Refer to OMAP4470 Silicon Revision 1.x TRM.