Texas Instruments

TRF4903 Design Guide

User's Guide

2005

High Speed and RF

SWRU011

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Read This First

About This Manual

This document briefly describes the TRF4903 single-chip RF transmitter and the major RF design techniques and system considerations involved in establishing a wireless transmit link. Many of the topics covered also apply to designing a wireless system using other products in the TRF49xx family.

How to Use This Manual

The first two chapters focus on the initial system design considerations. Transmit system design consideration is discussed in Chapter 3. Chapter 4 reviews the overal system design using Texas Instruments EasyRF™ software.

This document contains the following chapters:

- Chapter 1 — Introduction
- Chapter 2 — Initial Design
- Chapter 3 — Setting Up the PLL and Transmit Section
- Chapter 4 — Software Overview
- Chapter 5 — Operation and Troubleshooting
- Chapter 6 — References

Related Documentation From Texas Instruments

Other related Texas Instruments documents that may be helpful are:

- TRF4903 data sheet − (SWRS023)
- MSP430F449 data sheet − http://focus.ti.com/lit/ds/symlink/msp430f449.pdf
- TRF6901 FAQ − http://focus.ti.com/lit/misc/slad008/slad008.pdf

Product Websites

For design and product information related to the TRF4903, MSP430, and similar products, go to:

- http://www.ti.com/ismrf
- http://www.msp430.com

PDF documents and zip files may be located on Texas Instruments' website by typing in the literature number in the *Search* text box; for example, typing in SWRS023 will locate the TRF4903 data sheet.

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Chapter 1

Introduction

The Texas Instruments TRF4903 is a low cost RF transmitter that is intended for use to establish a frequency-programmable, unidirectional wireless RF link in the European or North American industrial, scientific, and medical (ISM) bands (315, 433, 868, 915 MHz bands). It supports binary frequency-shift keying (2 FSK) and on-off keying (OOK) modulation. A terminal location diagram of the TRF4903 is shown in Figure 1−1. See the *TRF4903 Single-Chip Multiband RF Transmitter* data sheet (SRWS023) for additional information.

This document covers some of the basic design considerations and techniques in using the TRF4903 as a wireless transmitter system. This document has to be used along with the TRF6903 Design Guide (*SWRU009*) to fully understand the receive section to design a unidirectional wireless system. Figure 1−2 is a block diagram of the TRF4903 device.

Although every effort is made to provide accurate information, actual performance may vary from application to application. The designer is encouraged to review the latest documentation, available on the Texas Instruments Web site (http://www.ti.com/ismrf), and to do the necessary development testing to obtain the best results from the product.

Figure 1−1. TRF4903 PW Package

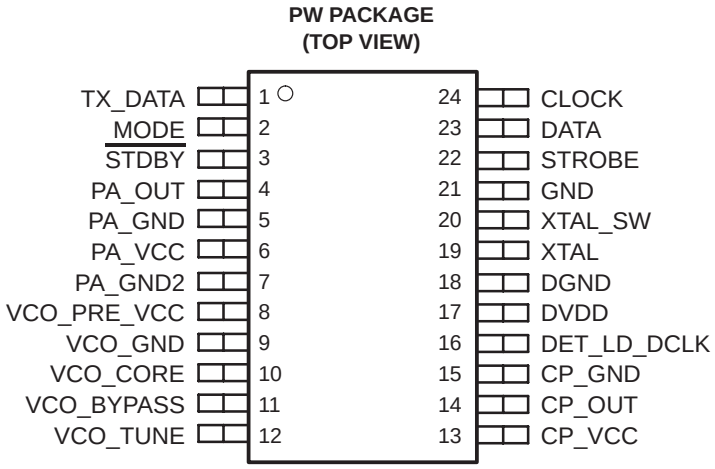
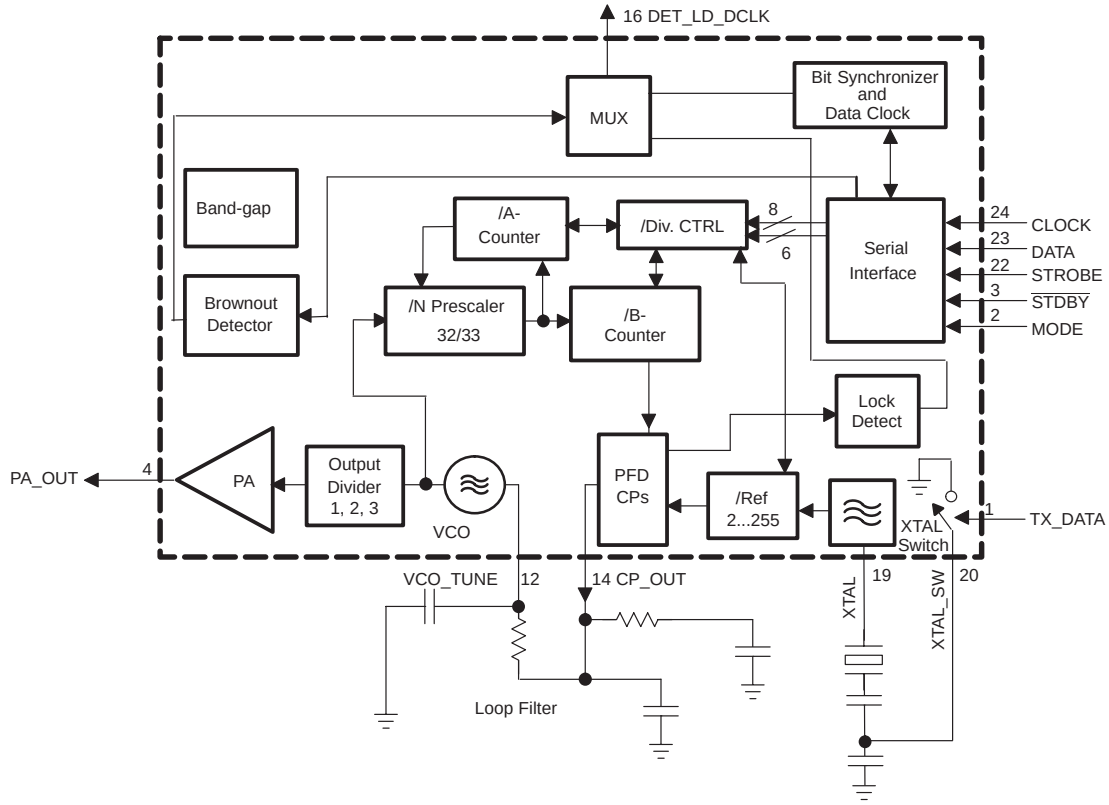


Figure 1−2. Functional Block Diagram



Chapter 2

Initial Design

This chapter discusses the initial design.

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2.1 Design Flow

- ❑ Initial system design involves selecting the data rate, coding scheme, modulation, frequency deviation, and frequency planning. Considerations include design complexity, performance, and cost tradeoffs.
- ❑ Set up and test transmit section.
- ❑ Make modifications to produce a layout based on engineering test, characterization data, production yield, and centering and process requirements.

2.2 Design Complexity

The designer first determines the design complexity necessary to implement the system, chooses a data rate and coding scheme, and determines the number of required frequency channels.

Wireless transmitter designs can be loosely classified into three groups according to performance and design complexity. Simple designs are often characterized by low data rates (10 kbps), low cost targets, and short transmission ranges (under 100 m). Cost can be the primary driver in making design choices for a simple design.

Complex designs have higher performance goals that may include higher data rates or longer transmission ranges (over 100 m). Performance largely determines design choices for complex design.

Intermediate designs fall between the two extremes where additional system costs are carefully traded against the benefits of increased performance.

2.3 Data Coding

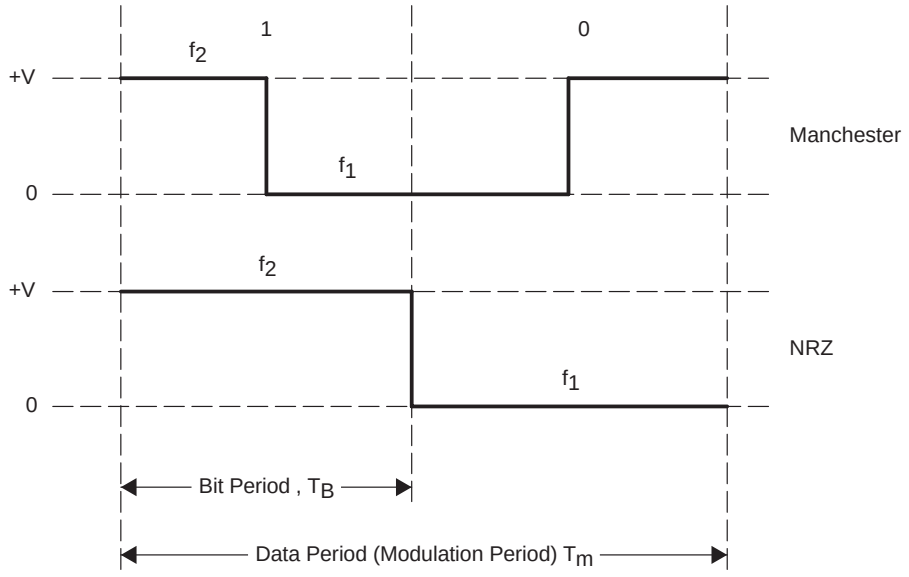
The choice of coding scheme has important implications for several parts of the transceiver design, including loop filter bandwidth and frequency deviation.

Systems with low data rates (2.4 kbps to around 30 kbps) can be implemented with Manchester coding, in which a 1 is signified by a voltage transition from high to low, and a 0 is signified by a transition from low to high. There is a voltage change every bit (or symbol) period, hence the dc content of the data is zero or constant. In FSK systems, this means that the bit rate is the same as the rate at which the transmitter toggles between frequencies (symbol rate, data rate, or frequency modulation rate).

Systems with data rates higher than 30 kbps are often implemented with unipolar nonreturn-to-zero (NRZ) coding, in which a 1 is represented by a voltage high and 0 by a voltage low or 0 V. There is a voltage change only when the data changes from one to zero or vice versa, hence the voltage content of the bit stream and the frequency modulation rate depends on the data content. In FSK systems, this means that the bit rate is about twice the maximum frequency modulation rate.

There are other coding schemes in use, but many designers choose either Manchester or NRZ. Manchester- and NRZ-coding waveforms are shown in Figure 2−1.

Figure 2−1. Manchester and Nonreturn-to-Zero Coding



2.4 FSK Coding Equations

For 2-FSK, we define:

$f_B \equiv$ bit rate (bps) $\equiv 1 / T_B$

$T_B \equiv$ bit period

$T_m \equiv$ Data period (Modulation period)

$f_M \equiv 1/ T_m \equiv$ frequency modulation rate, symbol rate, or maximum rate at which FSK frequencies are toggled, also sometimes called the data rate (Hz)

For *Manchester* coding with alternate 1's and 0's:

$T_m = 2T_b$

$f_M = 1/2 \times f_B$ (Modulation rate is half the bit rate)

For Manchester coding with all 1's or all 0's:

$T_m = T_b$

$f_M = f_B$ (Modulation rate is equal to the bit rate)

The modulation rate for a Manchester encoded data stream varies between the bit rate (highest) and half the bit rate (lowest).

For NRZ coding, with alternate 1's and 0's:

$T_m = 2T_b$

$f_M = 1/2 \times f_B$ (Modulation rate is half the bit rate)

For NRZ coding, with alternate n consecutive 1's and 0's:

$T_m = 2nT_b$

$f_M = 1/2n \times f_B$ (Modulation rate is bit rate divided by 2n)

The modulation rate for a NRZ encoded data stream with alternate n consecutive 1's and 0's varies between the half the bit rate (highest) and bit rate divided by 2n (lowest). Where n is number of consecutive 1's and 0's.

2.5 Initial System Design Specifications

The goal of this document is to guide the designer to develop a wireless data link using the TRF4903 single-chip RF transmitter. We start out with a set of initial system design parameters† and explain the calculation of all the components needed to satisfy these design parameters in the subsequent sections. The system design specifications are tabulated in Table 2−1.

Table 2−1. Initial System Design† Specifications

Operating band	915 MHz
Operating frequency	915.0464 MHz
Crystal frequency	19.6608 MHz
Reference divider	48
PLL reference frequency	409.6 kHz
Charge pump current	0.5 mA
Modulation	FSK
Coding scheme	NRZ
Peak-to-peak frequency deviation	80 kHz (±40 kHz)
Data rate	38.4 kbps

† The system design parameters shown above are used as an example. The designer needs to choose parameters that are specific to their application.

The TRF4903 RF VCO is controlled by an integer-N phase-locked loop (PLL) (see the Texas Instruments technical brief SWRA029 for an overview of Integer-N and fractional-N PLL). This means that the TRF4903 generates RF frequencies at integer multiples of the PLL reference frequency. Therefore, the RF channel spacing must be an integer multiple of the PLL reference frequency.

For the example system defined in Table 2−1, the operating frequency closest to 915 MHz and is a multiple of the PLL reference frequency (409.6 kHz) is 915.0464 MHz. This is the CW frequency when *TXDATA* is low (f_0). If *TXDATA* is high, the CW frequency is 915.0464 MHz + peak-to-peak frequency deviation. In this example this frequency is 915.1264 MHz (f_1).

The carrier frequency $f_c = \frac{f_0 + f_1}{2} = 915.0864$ MHz

The design involves calculating the loop filter values, crystal switch capacitor values, and PA matching values at the transmit side. The design of these components is discussed extensively in the following chapters.

Chapter 3

Setting Up the PLL and Transmit Section

The voltage controlled oscillator (VCO) is the RF frequency source for the transmit amplifier. Setting up the PLL and transmit section is a key step in configuring the TRF4903 for use.

Figure 3−1 is a PLL block diagram. The capacitors loading the crystal are shown in series-shunt configuration and may produce less frequency overshoot during FSK operation.

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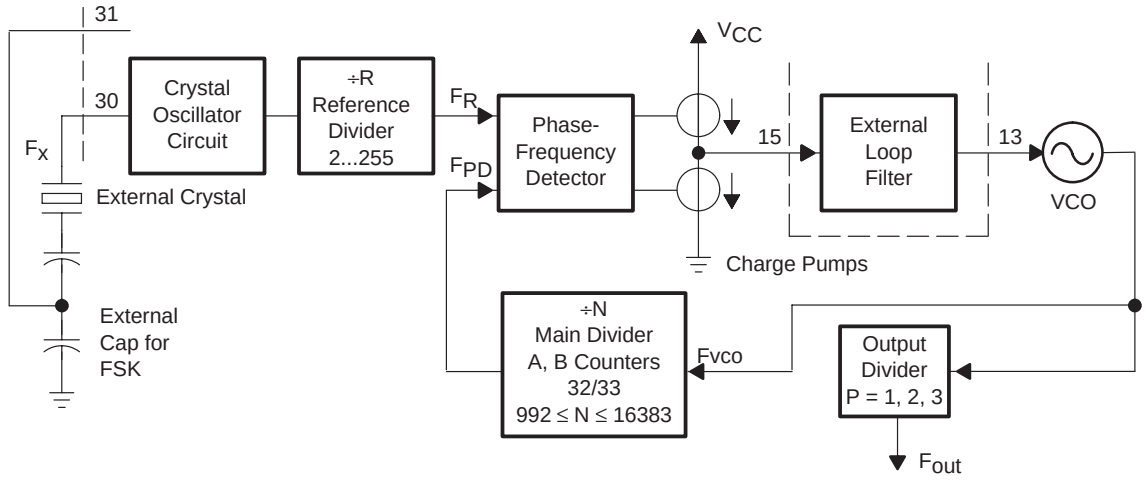
Figure 3−1. Integer-N Phase-Locked Loop Block Diagram



3.1 Frequency Deviation

The amount of frequency shift during binary FSK, termed the frequency deviation, can be expressed either as a total deviation (difference between the two frequencies) or as a plus/minus deviation (amount of deviation from the arithmetic mean of the two frequencies). The amount of deviation required for a given application depends on the data (modulation) rate, and, to a lesser degree, on the frequency jitter of the transmit/receive VCOs and on the linearity/sensitivity of the receiver data slicer. The mean of the two down-converted FSK transmitter frequencies, often referred to as the carrier frequency, must be centered as much as possible in the 10.7-MHz IF bandwidth.

The modulation index is a measure of the total deviation as a fraction of the FSK center frequency and is calculated by dividing the frequency deviation by the modulating data rate.

Digital Modulation Index = h = Δf / DR

Where: DR = Modulating Data rate (kHz); Δf is the peak frequency deviation.

Depending on the modulation index of the signal, an FSK spectrum can appear (with pseudorandom data) anywhere between a single peak at the carrier and two peaks separated from the carrier. The separation of the peaks is not necessarily the frequency deviation. The distance between the peaks is a function of both the modulation index h and the frequency deviation. The modulation index h should be between 0.5 and 1 or 2 maximum to conserve bandwidth and minimize BER.

Figure 3−2. Power Spectral Density of FSK for Pseudorandom Data

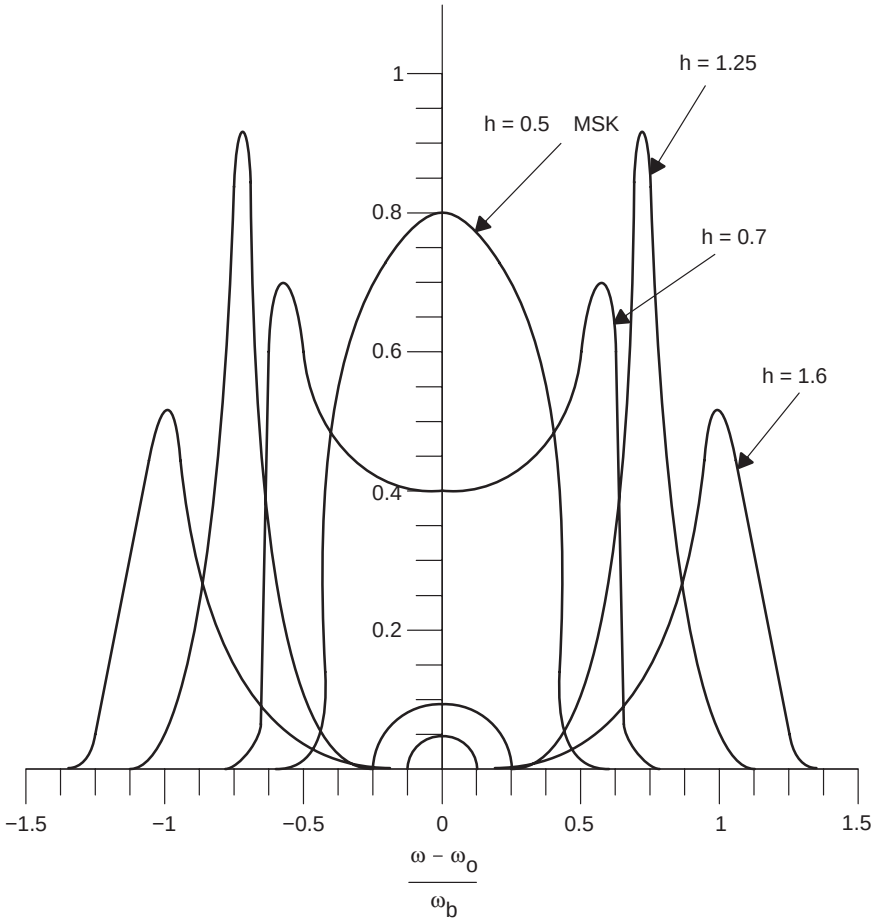


Table 3−1. Modulation Index (h) vs Power Spectra

Modulation Index h	Power Spectra Effects
h < 0.5	FSK signals are less orthogonal and BER increases (do not use).
h = 0.5	Minimum shift keying. MSK equals the narrowest spectrum for orthogonality.
h = 0.6	Spectrum is smooth and single-peaked at carrier frequency.
0.6<h<1	Spectrum is smooth and well confined; spectrum moves from a single peak at carrier frequency to peaks at two frequencies (as h −> 1, spectra begins to peak at two frequencies).
h = 1	Impulses occur at two frequencies.
h >1	Spectrum is broadest, peaks outside carrier frequency ±bit rate/2, decreases in sharpness and amplitude.

The power spectral density of the FSK for pseudorandom data is illustrated in Figure 3−2. As a general rule and according to communications theory, the modulation index should be about one. If the deviation is too small, the signal-to-noise ratio deteriorates and the data slicer may have trouble delivering accurate decisions, driving up bit error rate. If the deviation is too large, the FSK frequencies may not fit into the IF filter bandwidth. Excessive IF bandwidth allows more noise into the demodulated signal. Large deviations incur longer lock times, which may not be fast enough for high data rates. In practice, the total static frequency deviation that the designer chooses should be typically between 80 kHz and 100 kHz. For modulation rates up to 30 kHz,

80−100 kHz of static deviation is sufficient. For higher data rates, more frequency deviation is required to satisfy communication theory. During modulation, effective deviation may vary due to frequency overshoot as the PLL retunes.

3.2 Switch Capacitor and Crystal Oscillator Circuit

Frequency deviation during FSK operation is accomplished by pulling the crystal off-frequency. The configuration of the crystal oscillator of the TRF4903 multi-band RF transmitter is discussed in the following section.

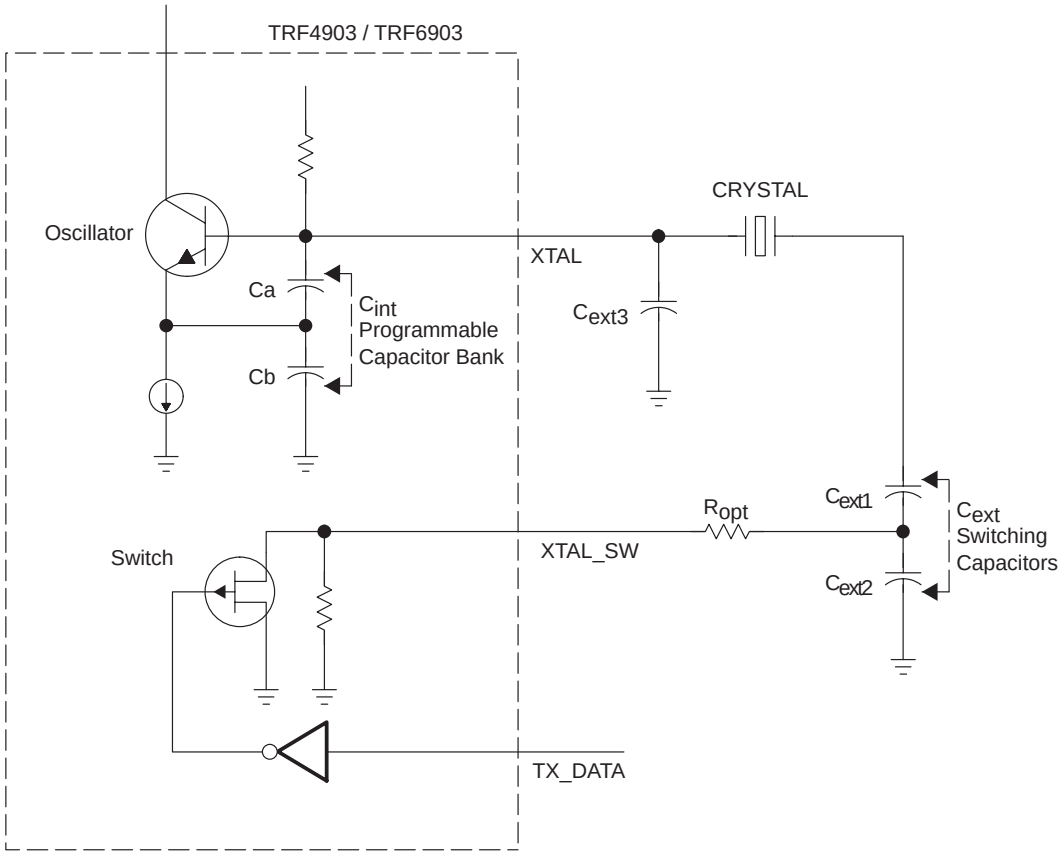
The crystal oscillator circuit of the TRF4903 is comprised of the internal programmable capacitor bank, the internal oscillator, the external crystal, and the external switching capacitors as described in the Figure 3−3. The crystal used in the circuit is specified to operate at fundamental frequency − parallel resonance. The specification of the crystal needs to also include the loading capacitor CL and in some cases, the spurious response per Table 3−2 to ensure that the data being sent will not be overly distorted.

Table 3−2. Specification of the Spurious Response

FREQUENCY OFFSET RELATIVE TO FUNDAMENTAL CRYSTAL RESPONSE	MAXIMUM SPURIOUS LEVEL
Frequency Offset<= 30 kHz	−40 dBc
30 kHz < Frequency Offset <= 100 kHz	−35 dBc
100 kHz < Frequency Offset <= 200 kHz	−30 dBc
200 kHz < Frequency Offset <= 500 kHz	−25 dBc
500 kHz < Frequency Offset <= 1 MHz	−15 dBc
1 MHz < Frequency Offset	−10 dBc

For many low-cost simple applications, the spurious response may be relaxed and need not be as tight as specified in Table 3−2. In these instances simple low-cost crystals without any spurious response specification may be considered for use.

Figure 3−3. TRF4903 Crystal Oscillator Circuit Configuration



In Figure 3−3, the crystal oscillator operates at the specified frequency of the crystal if Equation 3−1 is satisfied.

Equation 3−1.

$$C_L = \frac{C_{int} \times C_{ext}}{C_{int} + C_{ext}} + C_{STRAY}$$

Where:

C_L: specified value of the crystal load capacitance

C_{int}: value of the internal programmable capacitor bank

C_{ext}: value of the external loading capacitor

C_{STRAY}: value of the PCB stray capacitance

Now assume that all capacitors in Equation 3−1 are fixed values, except C_{ext}. The operating frequency of the oscillator will be lower than the specified frequency of the crystal if the value of the capacitor C_{ext} is increased and the operating frequency of the oscillator will be higher than the specified frequency of the crystal if the value of the capacitor C_{ext} is decreased.

The mechanism to vary the value of the capacitor C_{ext} is by using the TX_DATA line. The XTAL_SW terminal will be set to low for the TX_DATA input low state; thus, the capacitor C_{ext2} will be excluded from the circuit. The value of capacitor C_{ext1}, that is equal to the value of the capacitor C_{ext}, defines the

frequency of the crystal oscillator to represent the low data bit. If the TX_DATA input is a high state, the XTAL_SW terminal will be set to high; the value of capacitor C_{ext} will be the result of the series combination of the capacitors C_{ext1} and C_{ext2} and defines the frequency of the crystal oscillator to represent the high data bit.

The following example is to assist in obtaining the value of the capacitor C_{ext1} and C_{ext2}.

1) Require that the transmit center frequency of the TRF4903 will be 915.0464 MHz and the frequency deviation is ±40 kHz. These required conditions can be simply stated as:
   - Frequency of $Freq_{TX0}$ = 915.0864 MHz – 40 kHz = 915.0464 MHz represents the low data bit and
   - Frequency of $Freq_{TX1}$ = 915.0864 MHz + 40 kHz = 915.1264 MHz will be the high data bit.
2) The recommended crystal (Crystek PN 017119) has a precise load resonant frequency of 19.6608 MHz with the following specifications:
   - Loading capacitor, C_L = 12 pF
   - Motional capacitance, C_1 = 7.5 pF
   - Motional inductance, L_1 = 8.7418 mH
   - Shunt capacitance, C_0 = 2.2 pF
   - Series resistance, R = 6.8 Ω
   - The spurious response satisfies the requirements as per Table 2−1.
3) The reference frequency of the phase−locked loop (PLL) of the TRF4903 or the TRF4903 is chosen as 409.6 kHz.
4) From (2) and (3) above, the reference divider is:

$$\text{Ref\_Div} = \frac{19.6608\ \text{MHz}}{409.6\ \text{kHz}} = 48$$

5) The Main divider of the TRF4903 is calculated as:

$$\text{Main\_Div} = \frac{915.0464\ \text{MHz}}{409.6\ \text{kHz}} = 2234$$

6) Assume that the internal programmable capacitor of the TRF4903 is set mid-way to C_{int} = 20.23 pF.
7) Since the PCB stray capacitance is an uncertain value, assume that C_{STRAY} = 1.95 pF for the first trial.
8) From steps (1), (4), and (5), the required crystal oscillator frequencies that represent the low data bit and the high data bit are:

$$Freq_{XTAL0} = Freq_{TX0} \times \frac{\text{Ref\_Div}}{\text{Main\_Div}} = 915.0464\ \text{MHz} \times \frac{48}{2234} = 19.6608\ \text{MHz}$$

$$Freq_{XTAL1} = Freq_{TX1} \times \frac{\text{Ref\_Div}}{\text{Main\_Div}} = 915.1264\ \text{MHz} \times \frac{48}{2234} = 19.66251889\ \text{MHz}$$

9) The capacitor C_{ext1} can be calculated as:

$$C_{ext1} = \frac{C_{int} \times \left\{ \left[\left[\frac{C_1}{\left(\left[\left\{ 2 \times \pi \times Freq_{XTAL0} \right\}^2 \times L_1 \times C_1 \right]^{-1} \right)} \right] - C_0 \right] - C_{STRAY} \right\}}{C_{int} - \left\{ \left[\left[\frac{C_1}{\left(\left[\left\{ 2 \times \pi \times Freq_{XTAL0} \right\}^2 \times L_1 \times C_1 \right]^{-1} \right)} \right] - C_0 \right] - C_{STRAY} \right\}}$$

$$C_{ext1} = \frac{(20.23e-12) \times \left\{ \left[\left[\frac{(7.5e-15)}{\left(\left[\left\{ 2 \times \pi \times (19.6608e+6) \right\}^2 \times (8.7418e-3) \times (7.5e-15) \right]^{-1} \right)} \right] - (2.2e-12) \right] - (1.95e-12) \right\}}{(20.23e-12) \times \left\{ \left[\left[\frac{(7.5e-15)}{\left(\left[\left\{ 2 - \pi \times (19.6608e+6) \right\}^2 \times (8.7418e-3) \times (7.5e-15) \right]^{-1} \right)} \right] - (2.2e-12) \right] - (1.95e-12) \right\}}$$

C_{ext1} = 21.28 pF− Choose C_{ext1} = 22 pF as standard value

Note:

The value of C_{ext1} may result in a negative value for very large deviations and different crystal specifications. This negative value indicates that the circuit cannot meet the low-side deviation as specified. An additional shunt capacitor C_{ext3} as shown in Figure 3−3 is needed. Since the capacitor C_{ext3} is in parallel with the capacitor C_{int}, simply add the value of C_{ext3} to the value of C_{int} in the above equation and recalculate the value of C_{ext1}.

Adding capacitor C_{ext3} to the circuit causes mismatch to the input of the internal oscillator and results into a slow start-up time. The larger in value of the C_{ext3}, the slower the start-up time will be. It is highly recommended to avoid using C_{ext3}.

10) Similarly, the capacitor C_{ext2} can be calculated as:

$$C_{ext20} = \frac{C_{int} \times \left\{ \left[\left[\frac{C_1}{\left(\left[\left\{ 2 \times \pi \times Freq_{XTAL1} \right\}^2 \times L_1 \times C_1 \right]^{-1} \right)} \right] - C_0 \right] - C_{STRAY} \right\}}{C_{int} - \left\{ \left[\left[\frac{C_1}{\left(\left[\left\{ 2 \times \pi \times Freq_{XTAL1} \right\}^2 \times L_1 \times C_1 \right]^{-1} \right)} \right] - C_0 \right] - C_{STRAY} \right\}}$$

$$C_{ext20} = \frac{(20.23e-12) \times \left\{\left\{\left[\frac{(7.5e-15)}{\left(\left[\{2 \times \pi \times (19.6625e+6)\}^2 \times (8.7418e-3) \times (7.5e-15)\right] - 1\right)}\right] - (2.2e-12)\right\} - (1.95e-12)\right\}}{(20.23e-12) \times \left\{\left\{\left[\frac{(7.5e-15)}{\left(\left[\{2 - \pi \times (19.6625e+6)\}^2 \times (8.7418e-3) \times (7.5e-15)\right] - 1\right)}\right] - (2.2e-12)\right\} - (1.95e-12)\right\}}$$

C_{ext20} = 13.98 pF

$$C_{ext2} = \frac{C_{ext1} \times C_{ext20}}{C_{ext1} - C_{ext20}} = \frac{(21.3e-12) \times (13.98e-12)}{(21.3e-12) - (13.98e-12)} = 18.90 \text{ pF}$$

− Choose C_{ext2} = 18 pF as standard value

Note:

The value of C_{ext2} may result in a negative value for different crystal specifications. This negative value indicates that the circuit cannot meet the high-side deviation as specified. It is suggested to reduce the deviation requirement or select a different crystal.

11) Choose C_{ext1} = 22 pF as standard value. Set TX_DATA to low state and verify that the transmit signal is at 915.0464 MHz. Adjusting the value of C_{ext1} may be needed to obtain the wanted transmit frequency of 915.0464 MHz.

12) Repeat step (11) with the capacitor C_{ext2} = 18 pF. Set TX_DATA to high state and verify that the transmit signal is at 915.126 4 MHz. Adjusting the value of C_{ext1} may be needed to obtain the wanted transmit frequency of 915.1264 MHz.

■ For convenience, Table 3−3 is a summary of values of C_{ext1} and C_{ext2} for different frequency deviations for the crystal specification mentioned above.

Table 3−3. Values of C_{ext1} and C_{ext2} for Different Frequency Deviations

Frequency Deviation	C_{ext1}	C_{ext2}
±10 kHz	22 pF	85 pF
±20 kHz	22 pF	41 pF
±30 kHz	22 pF	26 pF
±40 kHz	22 pF	18 pF
±50 kHz	22 pF	15 pF
±60 kHz	22 pF	12 pF
±70 kHz	22 pF	10 pF
±80 kHz	22 pF	8 pF
±90 kHz	22 pF	7 pF
±100 kHz	22 pF	6 pF

Note:

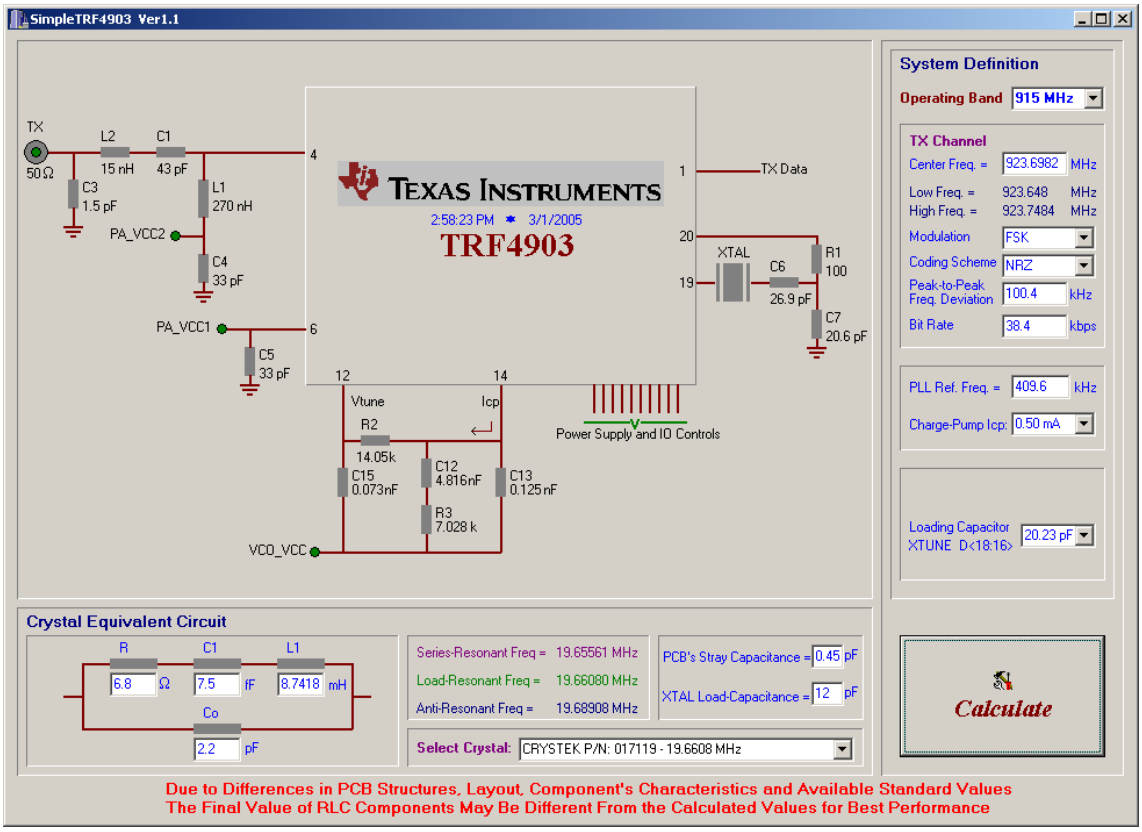
Figure 3−3 shows an optional resistor at the XTAL_SW output. This resistor can be used to smooth out the transition states of the data, especially when the TRF4903 operates in the 315-MHz band and 433-MHz band. The value of this optional resistor should be approximately 100 Ω. For the 868-MHz and 915-MHz bands, the resistor is not needed.

In conclusion, the switching mechanism of the crystal oscillator and the calculation process to obtain the value of the switching capacitors was discussed. For convenience, a summary table of switching capacitors for different frequency deviation was also presented. Due to a different PCB layout, the stray capacitance of the PCB may result in different value of switching capacitors; also, the calculation values may be different from the standard values, empirical results from the bench are required to meet the final design requirements.

Texas Instruments has developed the EasyRF™ software to ease the system development process.

The switching capacitor calculator software has been integrated in the EasyRF™. It is available on the www.ti.com.ismrf webpage. A screen shot of the software is shown in Figure 3−4.

Figure 3−4. Switching Capacitor Calculator Software

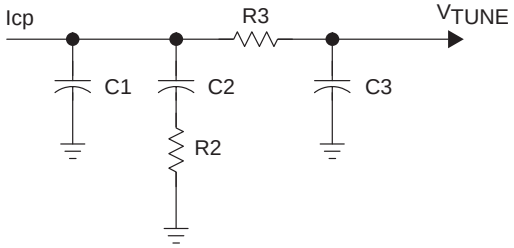


3.3 Loop Filter

The calculation of the components of loop filter for the TRF4903 multi-band RF transmitter is discussed in the following section.

The local oscillator of the TRF4903 is a phase-locked loop (PLL) that consists of an internal voltage-controlled oscillator (VCO), an internal frequency synthesizer and an external passive loop filter. The internal VCO has a sensitivity level of Kvco ≈ 100 MHz/V and the internal frequency synthesizer has a selectable charge-pump current of Icp = (0.25 mA, 0.5 mA, and 1 mA). The external loop filter (with I_{cp} = 0.5 mA) is typically designed with a third-order passive low-pass filter as shown in Figure 3−5.

Figure 3−5. Typical External Third-Order Passive Low-Pass Filter for the TRF4903



Because the modulation is done within the loop bandwidth, the design of the loop filter requires:

1) As flat a gain response as possible across the pass-band to avoid a variation in amplitude of the base-band signal. This requirement implies that the damping ratio of the loop must be about 2 or, equivalently, exhibit a phase margin of about 67 degrees.

2) The response of the loop must be as fast as the VCO changing frequency from the frequency that represents a 1 to the frequency that represents a 0 and vice-versa. This requirement avoids over-distortion of the base-band signal. An empirical result suggests that the required response time of the loop, as the VCO changing frequency from the frequency that represents a 1 to the frequency that represents a 0 and vice-versa, can be defined based on the transmit data rate as:

$$\text{response time} = 0.8 \times \frac{1}{\text{DataRate(Hz)}}$$

Where, *DataRate*: the fundamental frequency (in Hz) of the base band waveform Equivalently, the –3 dB bandwidth of the loop needs to be about 1.25 x *DataRate*. Thorough analysis of the loop filter design is rather complicated; however, the calculation of the components of the loop filter can be summarized as:

$$C_1 = 2.08e-3 \times \frac{K_{PD}K_{VCO}}{N \times (\text{DataRate})^2} \text{ ; Farad}$$

$$C_2 = 38.5 \times C_1 \text{ ; Farad}$$

$$R_2 = 0.65 \times \frac{1}{C_2 \times \text{DataRate}} \text{ ; Ohms}$$

$$R_3 \cong 2 \times R_2 \text{ ; Ohms}$$

$$C_3 = \frac{1}{50.5 \times \text{DataRate} \times R_3} \text{ ; Farad}$$

Where:

$$K_{PD} \text{ : phase−detector gain, } \frac{I_{CP}}{2\pi} \text{ ; A/rad}$$

$$K_{VCO} \text{ : VCO gain, } 2\pi \frac{\Delta f}{\text{Volt}} \text{ ; rad/V}$$

$$N = \frac{\text{Operating\_Frequency}}{\text{reference\_Frequency}} \text{ : main divider constant}$$

DataRate: The fundamental frequency (in Hz) of the base band waveform.

For example: given a system with a transmit frequency of 915.0464 MHz, a reference frequency of 409.6 kHz, a data rate of 19.2 kHz (38.4 kbps NRZ) and a charge-pump current set to Icp = 0.5 mA, the components of the loop filter are calculated as:

K_{VCO} = 100 MHz/V

$$\text{Main divider } N = \frac{915.0464 \text{ MHz}}{409.6 \text{ kHz}} = 2234$$

$$C1 = 2.08e-3 \times \frac{100 \times 500}{2234 \times (19.2e3)^2} = 126 \text{ pF} \quad - \text{ select 120 pF}$$

$$C2 = 38.5 \times 126.28e-12 = 4861 \text{ pF} - \text{ select } 4700 \text{ pF}$$

$$R2 = 0.65 \times \frac{1}{4861e-12 \times 19.2e3} - 6.963 \text{ k}\Omega - \text{ select } 7.5k$$

$$R3 = 2 \times 6.963 = 13.93 \text{ k}\Omega - \text{ select } 15k$$

$$C3 = \frac{1}{50.5 \times 19.2e3 \times 13.93e3} = 74 \text{ pF} \quad - \text{ select 68 pF}$$

Figure 3−6 shows the loop gain based on the calculation and a −3-dB bandwidth of about 40 kHz as needed. The 0-dB crossing and the phase margin of the open-loop response based on the calculation are also shown in Figure 3−6.

Figure 3−6. Phase Noise Plot for the Loop Filter

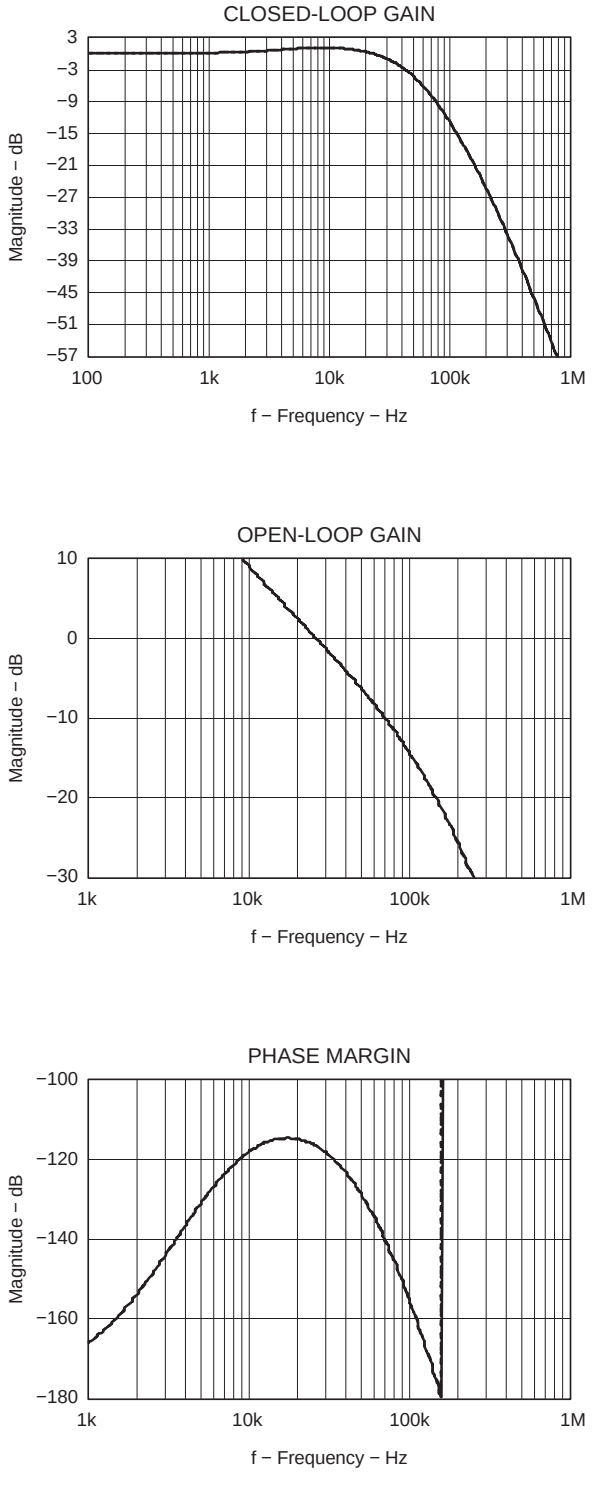


Table 3−4 summarizes loop filter components and typical performance for various data rate at:

- ❏ Carrier frequency of 915.0464 MHz
- ❏ Reference frequency of 409.6 kHz
- ❏ Charge-pump current is 0.5 mA
- ❏ VCO gain = 100 MHz / V

Table 3−4. Loop Filter Components and Typical Performance for Various Data Rates at a Carrier Frequency of 915.0464 MHz and a Reference Frequency of 409.6 kHz

Bit rate − kbps	Manchester coding	4.8	9.6	19.2	32
	NRZ coding	9.6	19.2	38.4	64
Data rate − kHz	Fundamental freq of BB	4.8	9.6	19.2	32
Loop filter component (selected to nearest standard value)	C1, pF	2200	470	120	47
	C2, nF	82	18	5.1	1.8
	C3, pF	1200	330	75	27
	R2, kΩ	1.8	3.3	6.8	12
	R3, kΩ	3.3	6.8	15	22
−3-dB bandwidth, kHz (approximate)		9.6	19.2	38.4	64
Response time, µs	Standby to Tx (lock time)	850	650	634	650
	Step of 1.2 MHz (lock time)	515	230	170	110
Reference spur, dBc		−66	−60	−55	−24
Phase noise, dBc/Hz	50-kHz offset	−76	−76	−75	−74
	200-kHz offset	−90	−90	−90	−89

It can be observed that the Lock−Time reduces and reference spur suppression degrades as the loop bandwidth is widened. As a rule of thumb, it is advisable to choose a reference frequency that is at least 10 times the –3-dB bandwidth of the loop to ensure that reference spurs are minimized. Note that the last entry in Table 6 violates this rule of thumb and a new reference frequency of 1.2288 MHz is chosen to recalculate the loop filter components. Table 3−6 summarizes loop filter components and typical performance for the last entry of Table 3−5 at:

- ❏ Carrier frequency of 915.0464 MHz
- ❏ Reference frequency of 1228.8 kHz
- ❏ Charge-pump current is 0.5 mA
- ❏ VCO gain = 100 MHz / V

Table 3−5. Loop Filter Components and Typical Performance for Various Data Rates at a Carrier Frequency of 915.0464 MHz and a Reference Frequency of 1228.8 kHz

Bit rate − kbps	Manchester coding	32
	NRZ coding	64
Data rate − kHz	Fundamental freq of BB	32
Loop filter component (selected to nearest standard value)	C1, pF	120
	C2, pF	5600
	C3, pF	82
	R2, kΩ	3.9
	R3, kΩ	7.5
−3-dB bandwidth, kHz (approximate)		64
Response time, μs	Standby to Tx (lock time)	611
	Step of 1.2 MHz (lock time)	113
Reference spur, dBc		−59
Phase noise, dBc/Hz	50-kHz offset	−72
	200-kHz offset	−89

The design of the loop filter for PLL of the TRF4903 was presented. To avoid distortion and variation in amplitude of the base-band signal during transmit, the design of the loop needs to consider the data rate of the system as well as the response of the loop filter.

EasyRF™ software can be used to design the third order loop filter for user-defined system parameters. This eases the system development process condisderably.

3.4 Frequency Correction With Crystal Tuning

Incremental corrections of the RF output frequency are done with the TRF4903 crystal tune feature. An internal user-selectable capacitor can be placed in shunt with the external reference crystal under the control of three bits in the serial word. This is normally done at assembly or production test and the correct value stored as part of the programming information for the unit. Frequency correction can also be done in hardware by adjusting a variable capacitor installed on the circuit board in shunt with the crystal. This is usually manually tuned during production. If using the series-shunt crystal capacitor arrangement, the caps should be calculated to give the correct frequency with the internal capacitor bank set to the middle of the adjustment range.

The frequency adjustment obtained using the Crystal tuning feature is shown in Table 3−6. A Crystek 19.6608 MHz (PN 017119) is used. The intended frequency of operation is 915.0464 MHz (409.6-kHz reference frequency).

Table 3−6. Frequency Correction With Crystal Tuning

Capacitor Value (pF)	Observed Frequency (MHz)	Frequency Error (kHz)
13.23	915.09987	+52.47
15.56	915.07417	+28.57
17.9	915.05637	+9.97
20.23	915.04153	−4.87
22.57	915.02983	−16.5
24.9	915.01943	−26.97
27.24	915.01087	−35.53
29.57	915.0034	−43

It can be seen that using a 20.23-pF Crystal tuning capacitor, the observed frequency is within about 5 kHz of the actual frequency.

3.5 Using Lock Detect, Data Clock, and Brownout Detect

The TRF4903 pin 16 is a multiplexed output capable of generating one of the following signals:

- ❑ Lock Detect (Active High)
- ❑ Brownout Detect (Active High)
- ❑ Data Clock (At the specified baud rate)

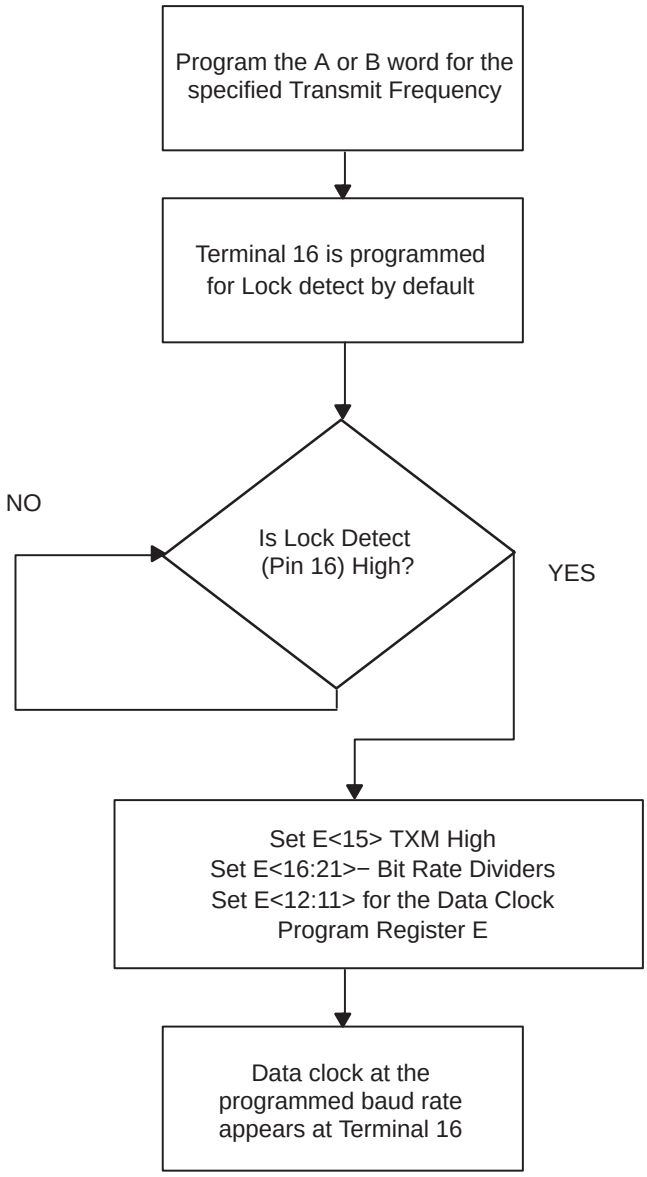
The output at terminal 16 is programmable using 2 bits in the E register E<12:11> as shown in Table 3−7.

Table 3−7. Multiplexed Output (Terminal 16) Function

E<12:11>	Terminal 16, DET_LD_DCLK, Function
00	PLL lock detect output (default)
01	Data clock output
10	Brownout detect output
11	Not used

By default, the multiplexed output is programmed for the lock detect output. If the designer chooses to use the data clock for transmit, the application needs to wait for lock detect and then program the E register for data clock output (the transmit capture mode E<15> needs to be set) to enable the DCLK signal. This is shown in Figure 3−7.

Figure 3−7. Using the Multiplexed Output (Terminal 16)



3.6 Regulations for Unlicensed Transmitters

In the US, low date rate transmitters are governed by Federal Communications Commission (FCC). FCC regulations focus exclusively on the emissions of devices. Receiver performance is not regulated. Telecommunications rules in the US are codified in Title 47 of the Code of Federal Regulations (CFR). The FCC rules on low date rate devices are covered in Part 15 of Title 47.

The first part of the regulations on unlicensed transmitters is a list of restricted bands in which only low-level spurious emissions are allowed (§15.205). These restricted bands apply to the harmonics and sub-harmonics of transmitter outputs as well as the fundamental. The restricted frequencies from 30 MHz to 10 GHz are listed in Table 3−8.

Table 3−8. FCC Restricted Frequencies from 30 MHz to 10 GHz

MHz	MHz	MHz	GHz
37.5 – 38.25	167.72 – 173.2	1660 – 1710	3.6 – 4.4
73 – 74.6	240 – 285	1718.8 – 1722.2	4.5 – 5.15
74.8 – 75.2	322 – 335.4	2200 – 2300	5.35 – 5.46
108 – 121.94	399.9 – 410	2310 – 2390	7.25 – 7.75
123 – 138	608 – 614	2483.5 – 2500	8.025 – 8.5
149.9 – 150.05	960 – 1240	2655 – 2900	9 – 9.2
156.52475 – 156.52525	1300 – 1427	3260 – 3267	9.3 – 9.5
156.7 – 156.9	1435 – 1626.5	3332 – 3339	
162.0125 – 167.17	1645.5 – 1646.5	3345.8 − 3358	

There is also a general limitation on the level of spurious emissions (§15.209). These levels depend on frequency and are summarized in Table 3−9. Usually, the requirements on harmonics of the transmit frequency are relaxed, but if the harmonic falls in one of the restricted bands, it must meet the spurious limits in Table 3−9.

Table 3−9. US General Spurious Limitations

Frequency Range (MHz)	Maximum Spurious Emission (dBm)
30−88	−55.25
88−216	−51.75
216−960	−49.25
Above 960	−41.25

If the harmonics of the transmitted frequency does not fall in one of the restricted bands outlined in Table 3−8, the harmonic suppression limit is only 20 dBc.

General purpose data devices with frequency hopping, or hoppers, do not have any restriction on the type of data or the duty cycle of the transmission. However a spreading of the transmission spectrum through frequency hopping (§15.247) is required. The allowed UHF band for hoppers is 902 – 928 MHz. Frequency hopping systems (15.247a1) must use at least 50 hopping frequencies if the 20-dB bandwidth is <250 kHz, having a duration of <0.4 s of a 20 s period and maximum 1-W output power. For bandwidths >250 kHz, at least 25 channels must be used, having a duration of <0.4 s of a 10 s period and maximum 0.25-W output power.

The maximum output power for a hopper is +30 dBm, with an allowed antenna gain of up to 6 dBi. Spurious emissions in a hopper need only be 20 dB below the fundamental, with the exception, of course, of the restricted bands. It is important to note that the 3rd, 4th, and 5th harmonics of the 902 – 928 MHz band do fall within restricted bands, so their emission is limited to –41.25 dBm.

Single-channel general purpose data devices share the same 902 – 928 MHz frequency band as hoppers, just at a reduced power level. There is no hopping requirement. The maximum output power is approximately –1.25 dBm, and the maximum harmonic power is approximately –41.25 dBm. Spurious output other than harmonics must be either 50 dB below the fundamental, or meet the requirements in Table 3−9, whichever is the least restrictive.

The TRF4903 is capable of operating in the 315-MHz, 433-MHz, 868-MHz, and 915-MHz ISM bands. Table 3−10 summarizes the location of the harmonics of these bands. Harmonics up to 5^{th} order are considered. Of particular importance are the 2^{nd} and the 3^{rd} order harmonics.

Table 3−10. ISM Band Frequencies With Harmonic Locations

Frequency Range (MHz)	Harmonics Falling in the Restricted Band	Harmonics Falling in the Non-Restricted Band
315	5^{th}	2^{nd}, 3^{rd}, 4^{th}
430−440	3^{rd}, 4^{th}	2^{nd}, 5^{th}
868−870	5^{th}	2^{nd}, 3^{rd}, 4^{th}
902−928	3^{rd}, 4^{th}, 5^{th}	2^{nd}

NOTE: The designer assumes all responsibility for compliance with applicable European, North American, or other governmental regulations in the use of the TRF4903 and other products made by Texas Instruments. Texas Instruments assumes no responsibility or liability for summarizing or interpreting regulations governing the use of wireless transmitters or receivers.

3.7 Amplifier Harmonic Suppression Using Discrete LC Filters

The RF output of the power amp may contain reference spurs at levels determined by the loop filter bandwidth. The RF signal also contains harmonics, at multiples of the fundamental RF frequency that are produced by the nonlinear nature of the amplifier. The second and third harmonics generated by the TRF4903 power amplifier are typically −25 dBc and −30 dBc respectively (see the TRF4903 data sheet Texas Instruments literature number SWRS023). If higher suppression is needed, the second and third harmonics can be attenuated (to meet governmental regulations) through the use of a discrete LC filter or a SAW filter. However, for most applications an external SAW filter or discrete LC filter may not be necessary. A discrete LC filter, if needed, is the preferred method to gain additional suppression. The design of a discrete LC filter is explained in this section. The filter must have low insertion loss in the RF pass band to avoid excessive loss of signal.

A three element T-type (two series inductors and an I-shunt capacitor) design and a three element PI-type (two shunt capacitors, one series inductor) filter are shown in Figure 3−8 and Figure 3−9. These filters are a 1-dB ripple Chebychev low-pass LC filter. The filters are designed for 50-Ω source and termination impedance. The PI- and T-filter design values along with the S21 plots for 315, 433, 868, and 915 MHz bands are shown below. Harmonic distortion values are illustrated on the plots for reference. The exact LC filter values may vary slightly from board to board due to board parasitics.

Figure 3−8. Three Element T-Type Filter

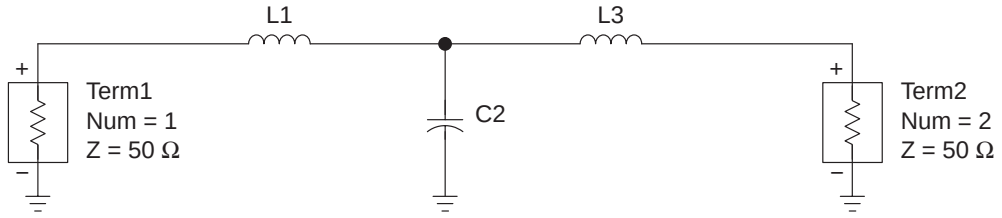
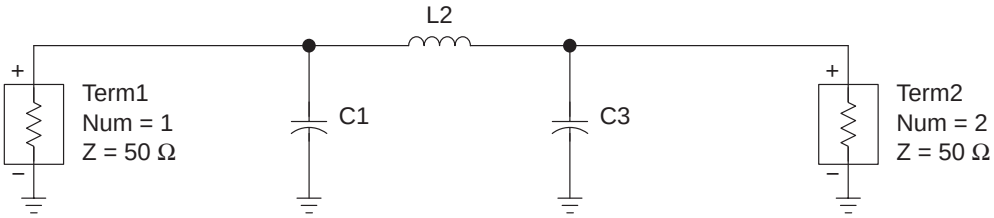


Figure 3−9. Three Element PI-Type Filter



It is recommended that high-Q inductors be used for the PI- and T-type filter design. Murata LQW1608A series wire-wound inductors were used for the PI- and T-type filters.

The T- and PI-type filter design values used on the board for various frequency bands are tabulated in Table 3−11. The component values may vary for different boards due to board stray capacitances and have to be fine tuned for the specific board used.

Table 3−11. T- and PI-Type Filter Values

Frequency Range (MHz)	T-Type Filter			PI-Type Filter		
	L1 (nH)	C1 (pF)	L3 (nH)	C1(pF)	L2(nH)	C3 (pF)
315	56	7.5	56	13	27	13
430−440	39	5.6	39	10	20	10
868−870	20	2.2	20	5.1	9.1	5.1
902−928	18	2	18	4.7	8.2	4.7

The harmonic attenuation achieved by these filters are tabulated in Table 3−12.

Table 3−12. Harmonic Attenuation Achieved by PI- and T-Type Filters

Frequency Range (MHz)	T-Type Filter		PI-Type Filter	
	2nd Harmonic (dBc)	3rd Harmonic (dBc)	2nd Harmonic (dBc)	3rd Harmonic (dBc)
315	22.61	36.32	17.03	29.94
430−440	22.32	36.71	19.3	31.48
868−870	24.93	41.98	24.77	28.84
902−928	24.33	42.51	22.02	29.85

The insertion losses achieved by these filters are tabulated in Table 3−13.

Table 3−13. Insertion Loss introduced by PI- and T-Type Filters

Frequency Range (MHz)	T-Type Filter	PI-Type Filter
	Insertion Loss (dB)	Insertion Loss (dB)
315	0.85	0.67
430−440	0.97	0.69
868−870	1	0.96
902−928	1	0.97

The frequency response of both PI- and T-type filters for different bands are shown in Figure 3−10 through Figure 3−17.

Figure 3−10. Harmonic Suppression Using PI-Type Filter at 915 MHz

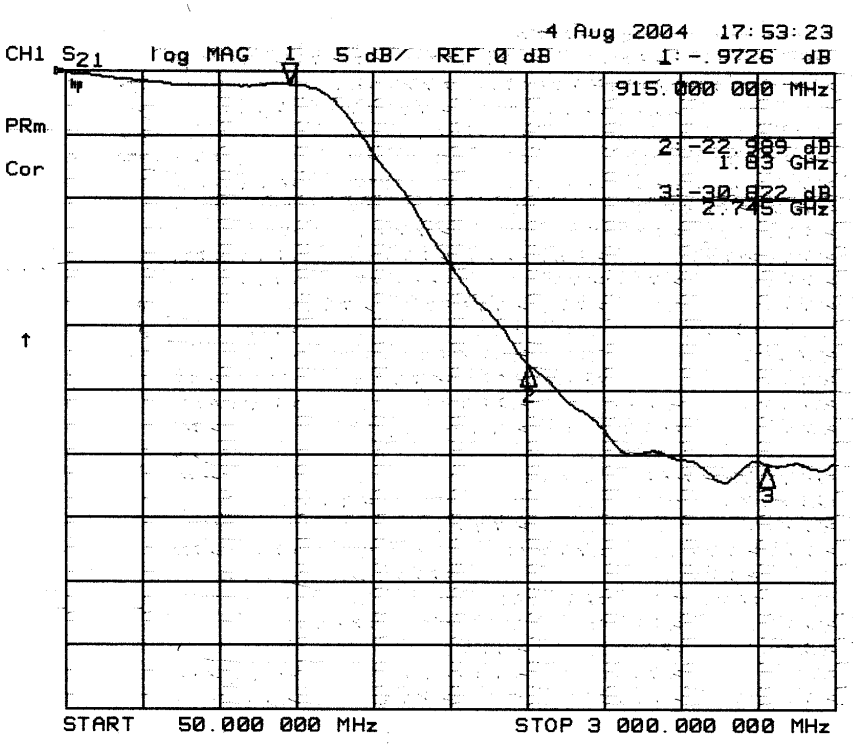


Figure 3−11. Harmonic Suppression Using T-Type Filter at 915 MHz

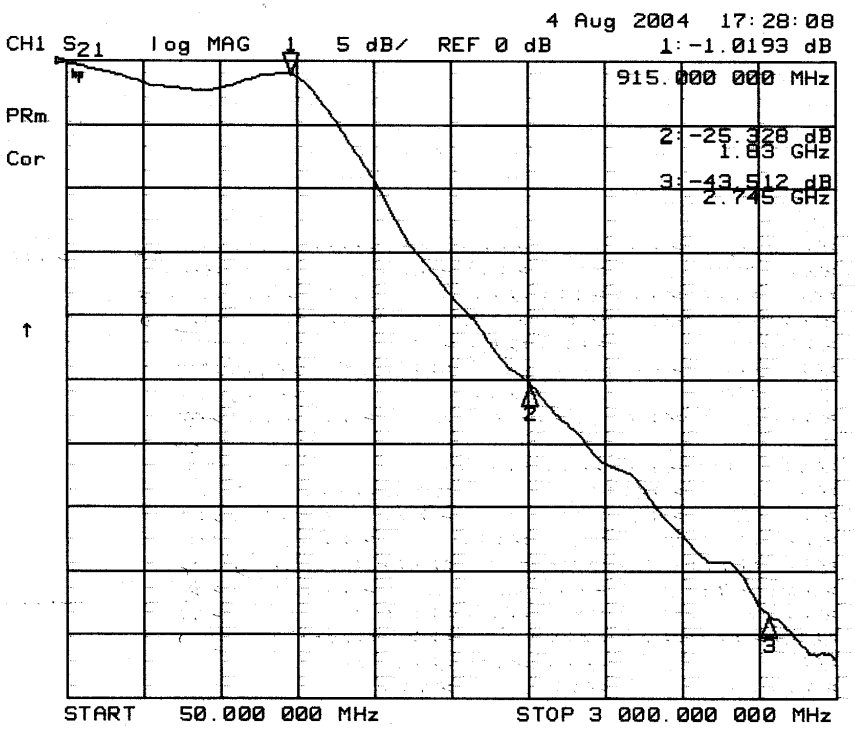


Figure 3−12. Harmonic Suppression Using PI-Type Filter at 868 MHz

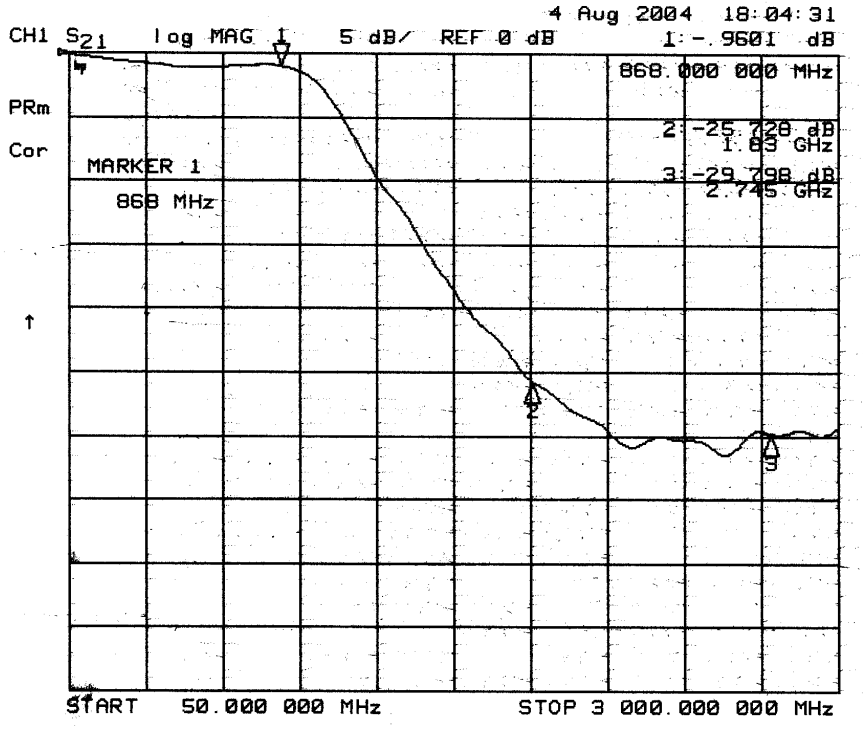


Figure 3−13. Harmonic Suppression Using T-Type Filter at 868 MHz

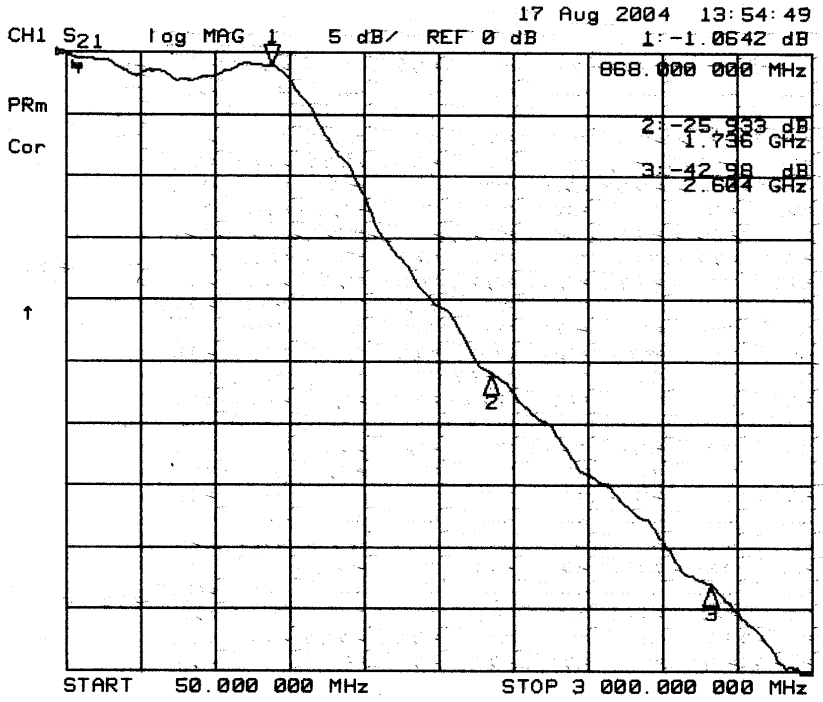


Figure 3−14. Harmonic Suppression Using PI-Type Filter at 433 MHz

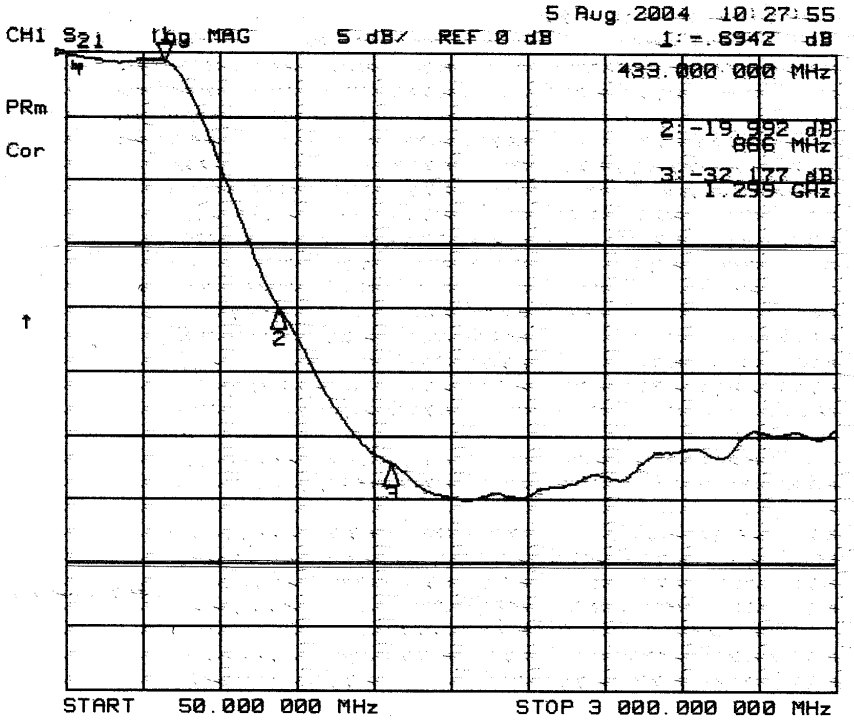


Figure 3−15. Harmonic Suppression Using T-Type Filter at 433 MHz

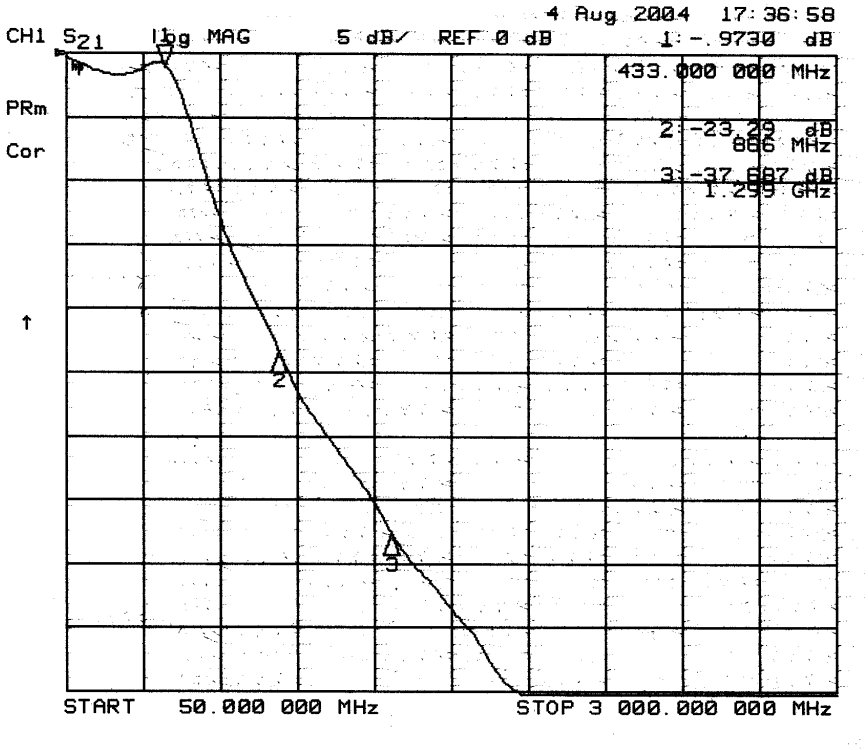


Figure 3−16. Harmonic Suppression Using PI-Type Filter at 315 MHz

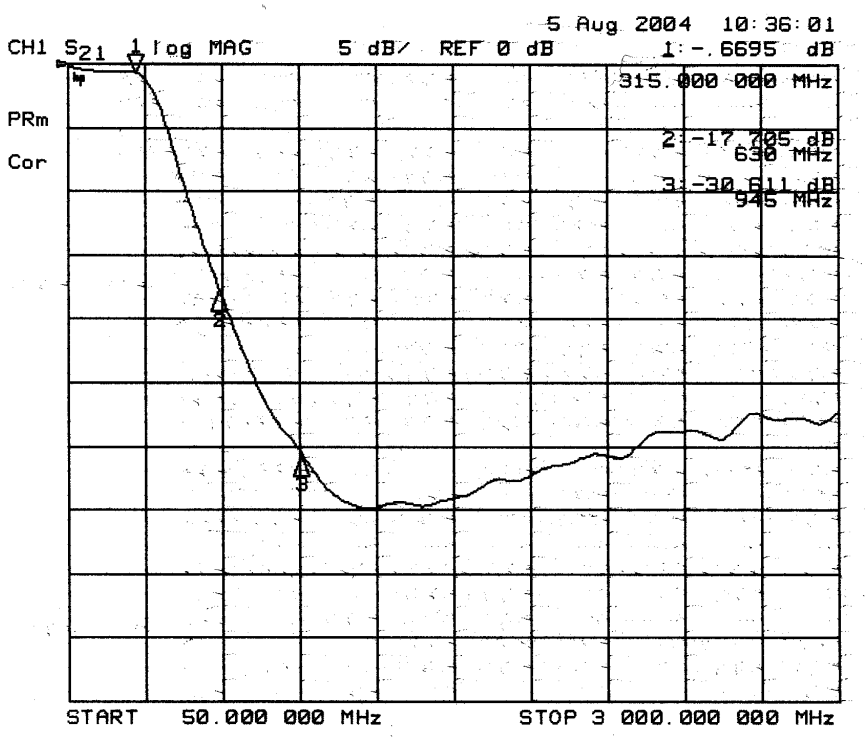
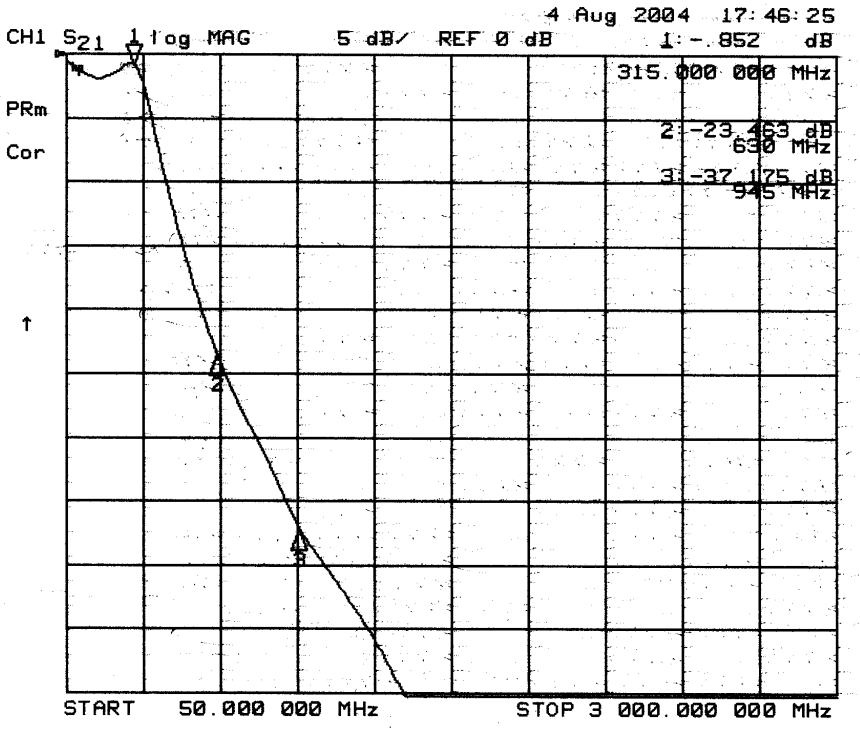


Figure 3−17. Harmonic Suppression Using T-Type Filter at 315 MHz



It can be observed that PI-type filter response flattens out at high frequencies due to the coupling effect. This can be avoided by using T-type filters. If higher harmonic attenuation is desired it is recommended that T-type filters be used at the expense of cost (due to an additional inductor).

Chapter 4

Design Example Using EasyRF™ Software

This chapter shows a design example using EasyRF™ software.

Topic **Page**

4.1 Design Example Using EasyRF™ Software

Most of the TRF4903 design has been implemented in software called EasyRF™. The software package is available from the Texas Instruments website http://www.ti.com/ismrf. This section discusses the system using the EasyRF™ software. To invoke the system design software, select the RF system design software from the EasyRF™ software main screen and press *Open*. The designer can use this software to design the following components for the TRF4903.

- ❑ PA matching
- ❑ Loop filter
- ❑ Crystal switching capacitors

It is recommended to verify the design values obtained from software with the mathematical design values given in earlier sections. *The design values obtained using software are initial estimates only. These values need to be fine tuned to obtain an accurate value for the desired application*.

The user needs to choose to the operating frequency band, operating frequency, modulation scheme, Coding scheme, peak-to-peak frequency deviation, bit rate, and PLL reference frequency. Press the C*alculate* button and the software populates the screen with the calculated recommended design values.

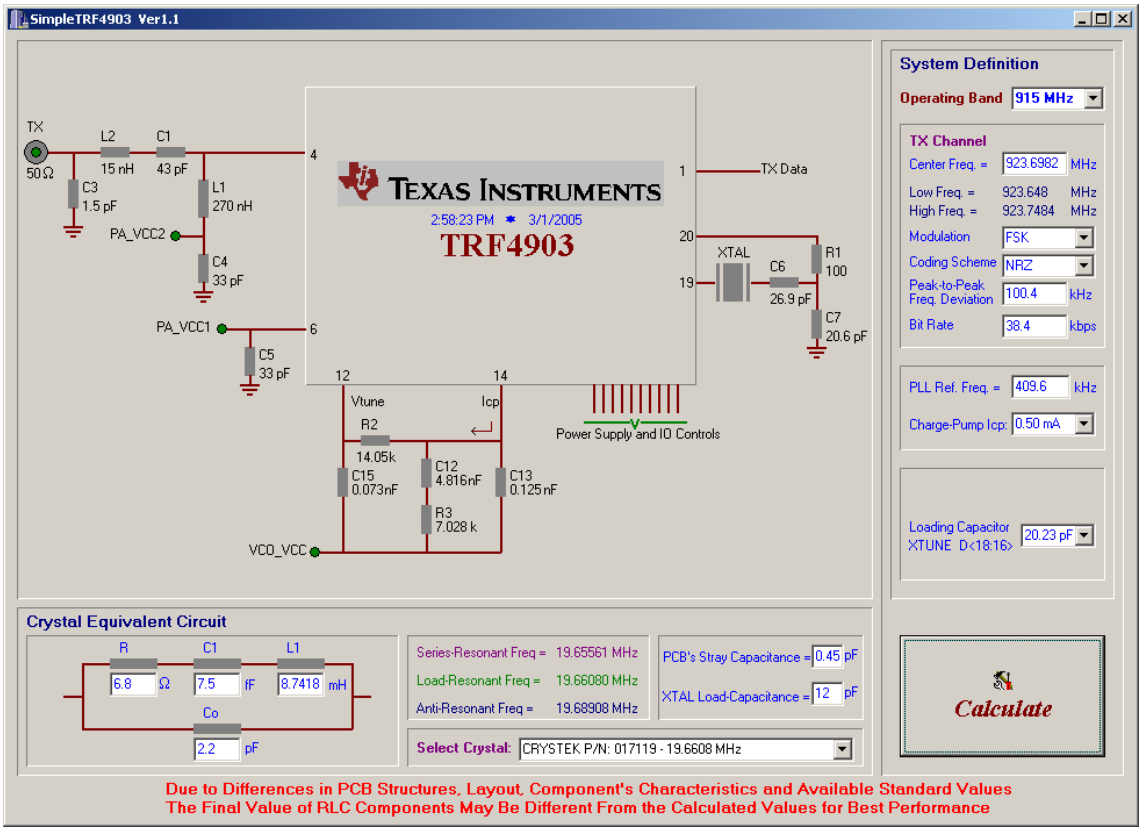
Figure 4−1 shows a screen shot of the software that has been developed to calculate the above design values.

In this example, we review the TRF4903 setup for the following parameters.

Table 4−1. TRF4903 Parameter Setup

Operating band	915 MHz
Operating frequency	915.0464 MHz
PLL reference frequency	409.6 kHz
Charge pump current	0.5 mA
Modulation	FSK
Coding scheme	NRZ
Peak-to-peak frequency deviation	80 kHz
Data rate	38.4 kbps

Figure 4−1. Design Using EasyRF ™ Software



Designers typically regard data rate as the amount of information to be transmitted, so here we use the term *modulation rate* rather than the term *data rate*.

NRZ coding at 38.4 kbps means the maximum FSK modulation rate through the loop filter will be 19.2 kHz. Choose a somewhat wider loop filter bandwidth. The −3-dB bandwidth of the loop filter in approximately to be 2 × modulation rate = 38.4 kHz. See the *loop filter* section. The components obtained from the software for a third-order loop filter with 409.6-kHz reference frequency, 0.5-mA charge pump current are C1 = 126 pF, R2 = 6.963 kΩ, C2 = 4.861 nF, R3 = 13.92 kΩ, and C3 = 74 pF.

Choosing a Crystek 19.6608-MHz crystal (PN 017119) and the series-shunt capacitor configuration, the calculated capacitor values are 26.9-pF series and 26.4-pF shunt for 80-kHz peak-to-peak frequency deviation.

When the TX_DATA terminal is set low, the RF transmit frequency is 915.0464 MHz. When it is high, the transmit frequency is 915.1264 MHz (80 kHz higher).

4.2 Transmit Section Evaluation

The RF output signal of the transmit amplifier in continuous wave (CW) mode should have only a single peak. There may be very small spurs present, spaced at a frequency interval equal to the PLL reference frequency. The principal harmonics from the power amp are at two and three times the fundamental frequency.

Examine the FSK signal on a spectrum analyzer by putting a 0-V to 1.5-V square wave into the TX_DATA terminal of the TRF4903 at the expected RF modulation frequency. The analyzer video bandwidth should be greater than the RF modulation rate in order to see the modulation envelope; there are two visible frequency peaks. The separation depends on the modulation index, the spectrum analyzer settings, the PLL lock time, and the loop filter damping.

The frequency shift observed when setting the TX_DATA terminal high or low differs depending on the rate at which TX_DATA changes. The static deviation (TX_DATA changing slowly) may be lower or higher than the dynamic deviation (TX_DATA changing rapidly). There are several reasons for this: the spectrum analyzer display is affected by the resolution settings and sweep/sampling rate, the spectral content of the signal changes with the frequency modulation rate, and PLL overshoot/undershoot. The two FSK frequencies may shift (or skew) together up or down slightly in comparison with their static values. Using the series-shunt capacitor configuration for the crystal loading helps make frequency overshoot vs modulation rate more consistent if it is needed to improve the modulated RF output spectrum.

Figure 4−2. FSK Spectrum – No Modulation (CW)

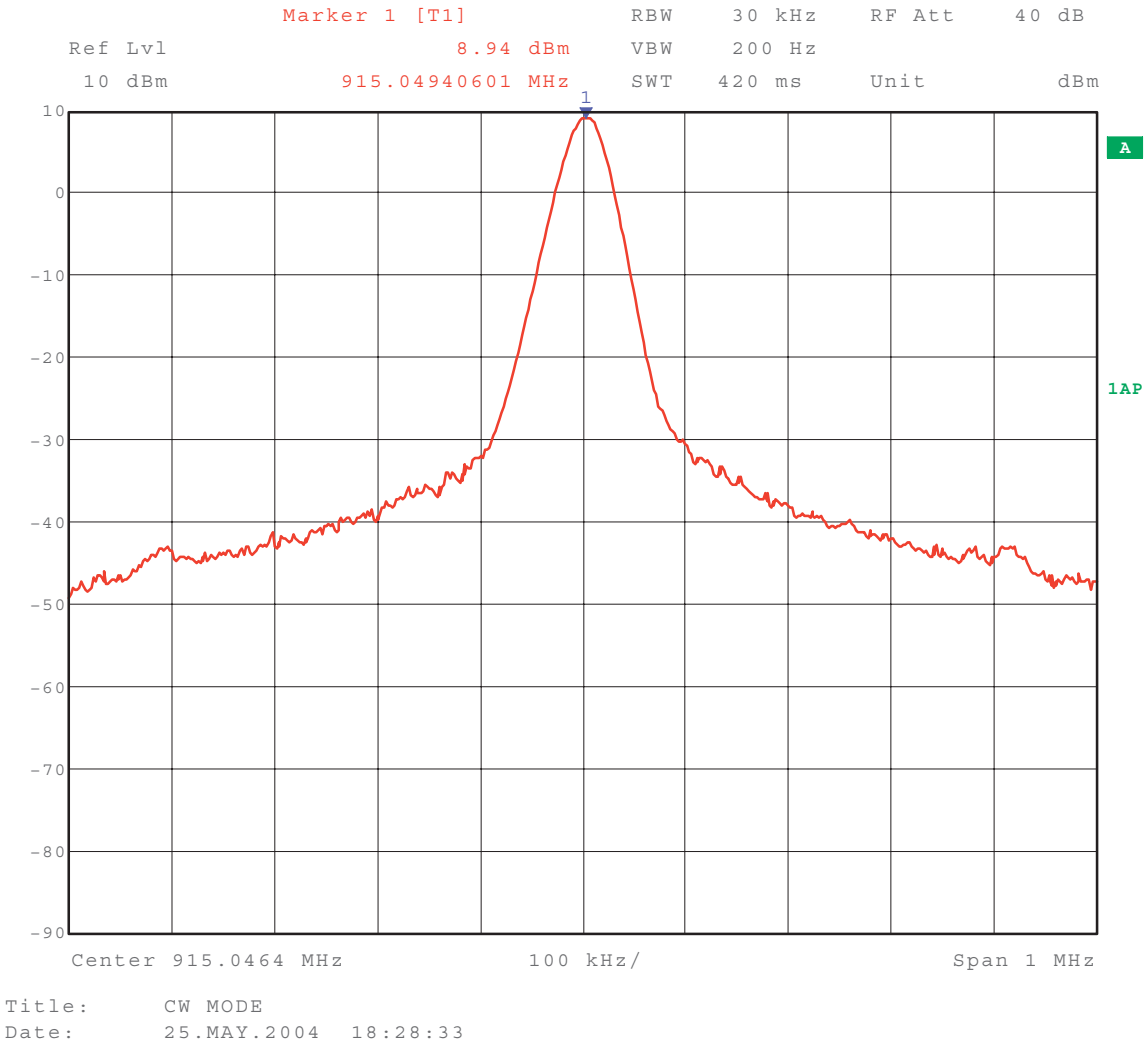


Figure 4−3. Second and Third Harmonics

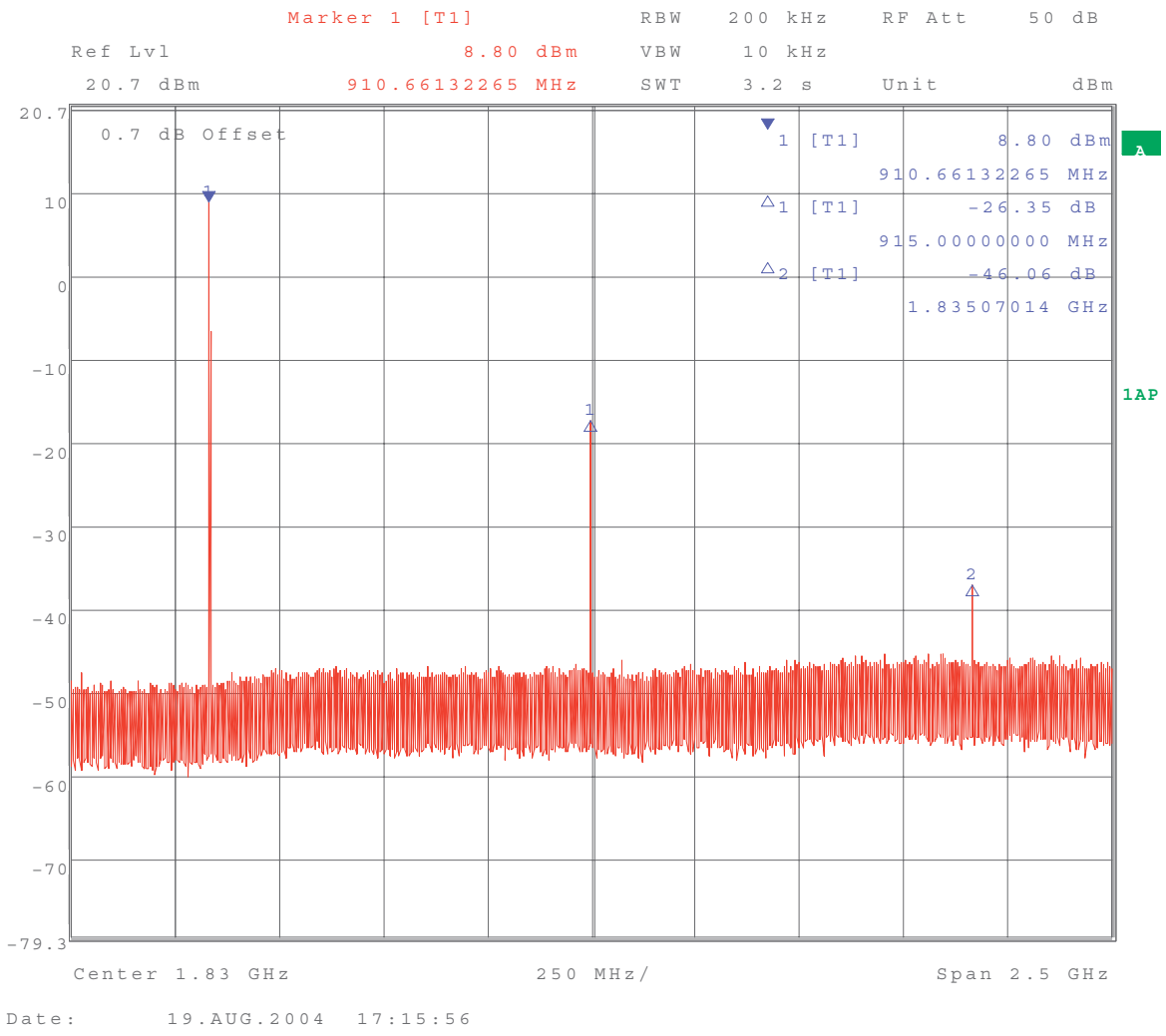
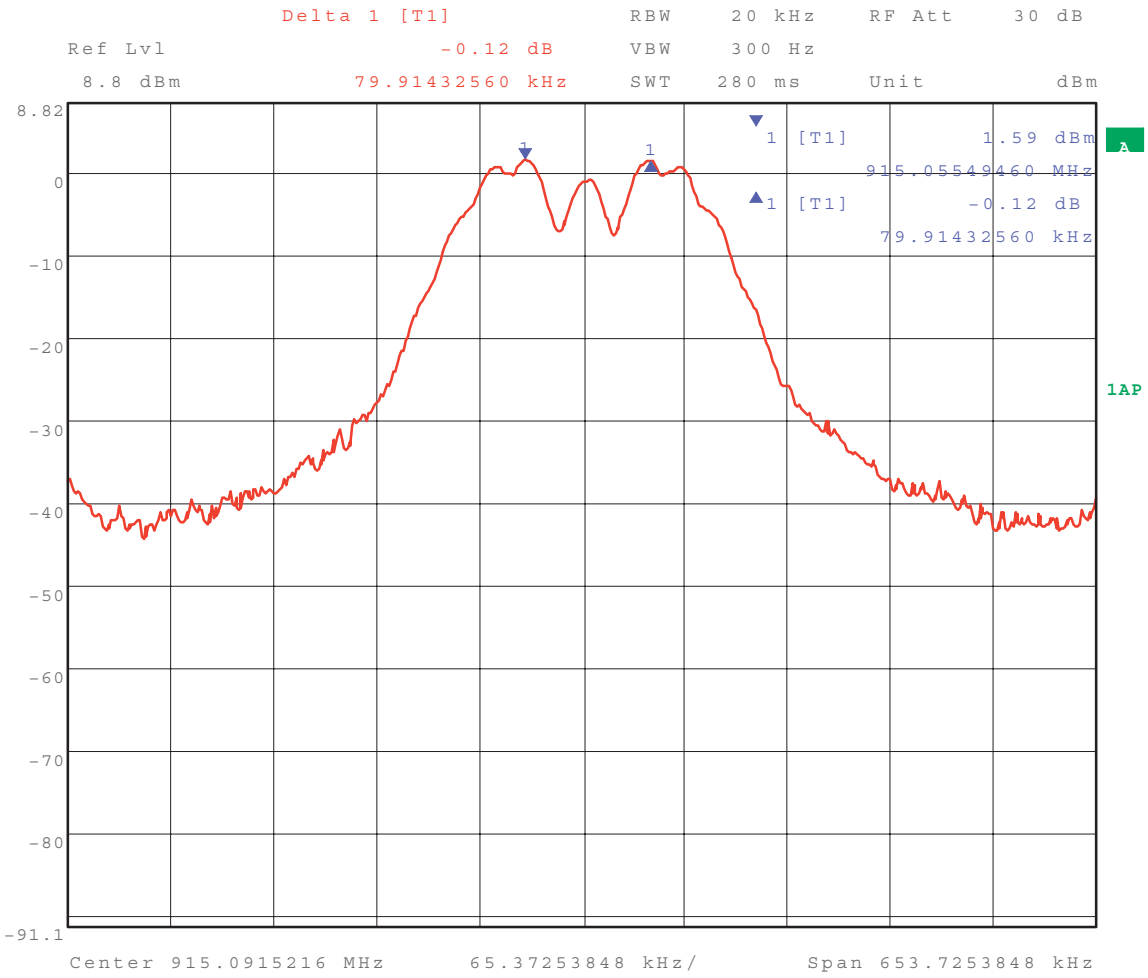
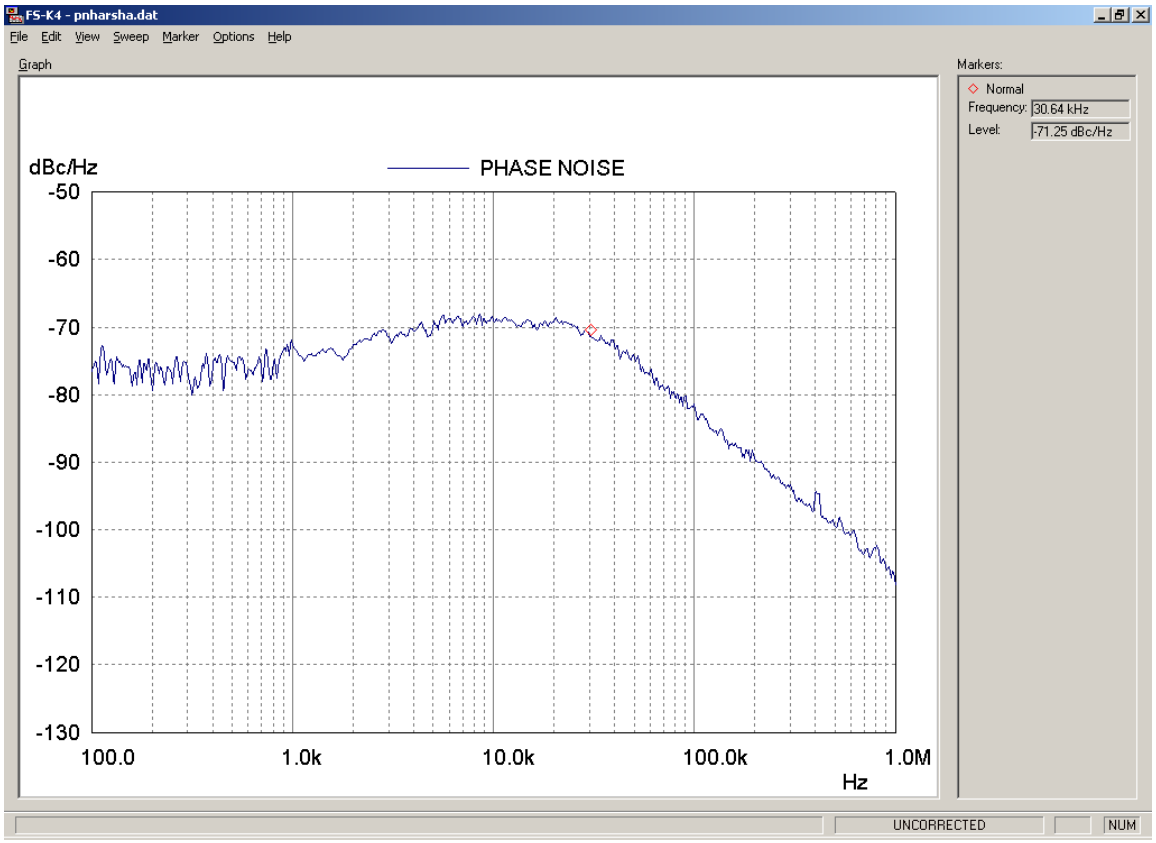


Figure 4−4. FSK Spectrum With Total Deviation Around 80 kHz and a 19.2-kHz Data Rate



Title: MODULATED SPECTRUM 915 MHz
Comment A: 19.2 KHz DATA RATE
Date: 24.MAY.2004 18:38:45

Figure 4−5. Phase Noise Plot



Note: 20-kHz loop filter with 915-MHz carrier, 0.5 mA Icp, 409.6-kHz reference frequency

4.3 Mode Switching and Lock Times

Standby to transmit has been measured at 650 μs, typical, triggering on the standby line and determining the time to a stable power amplifier output signal.

Frequency step time is influenced by the size of the frequency step and the PLL setup, including the reference frequency, loop filter bandwidth, and the charge pump current.

Determining lock time for transmit frequency modulation is somewhat subjective and there is some variance in the data. The effective lock time for the transceiver is the time to achieve a frequency shift that causes a reliable change of state in the receive data slicer. Frequency overshoot and ringing are not necessarily detrimental if the tuned frequency does not go near or back across the data slicer decision threshold. At high FSK data rates, the PLL may not have a chance to fully settle before the next symbol change, so the effective frequency deviation may be higher than a static measurement (measuring just one state change) would indicate. The minimum lock time for data transmission is often stated to be half of the symbol period, but there is some latitude in this requirement.

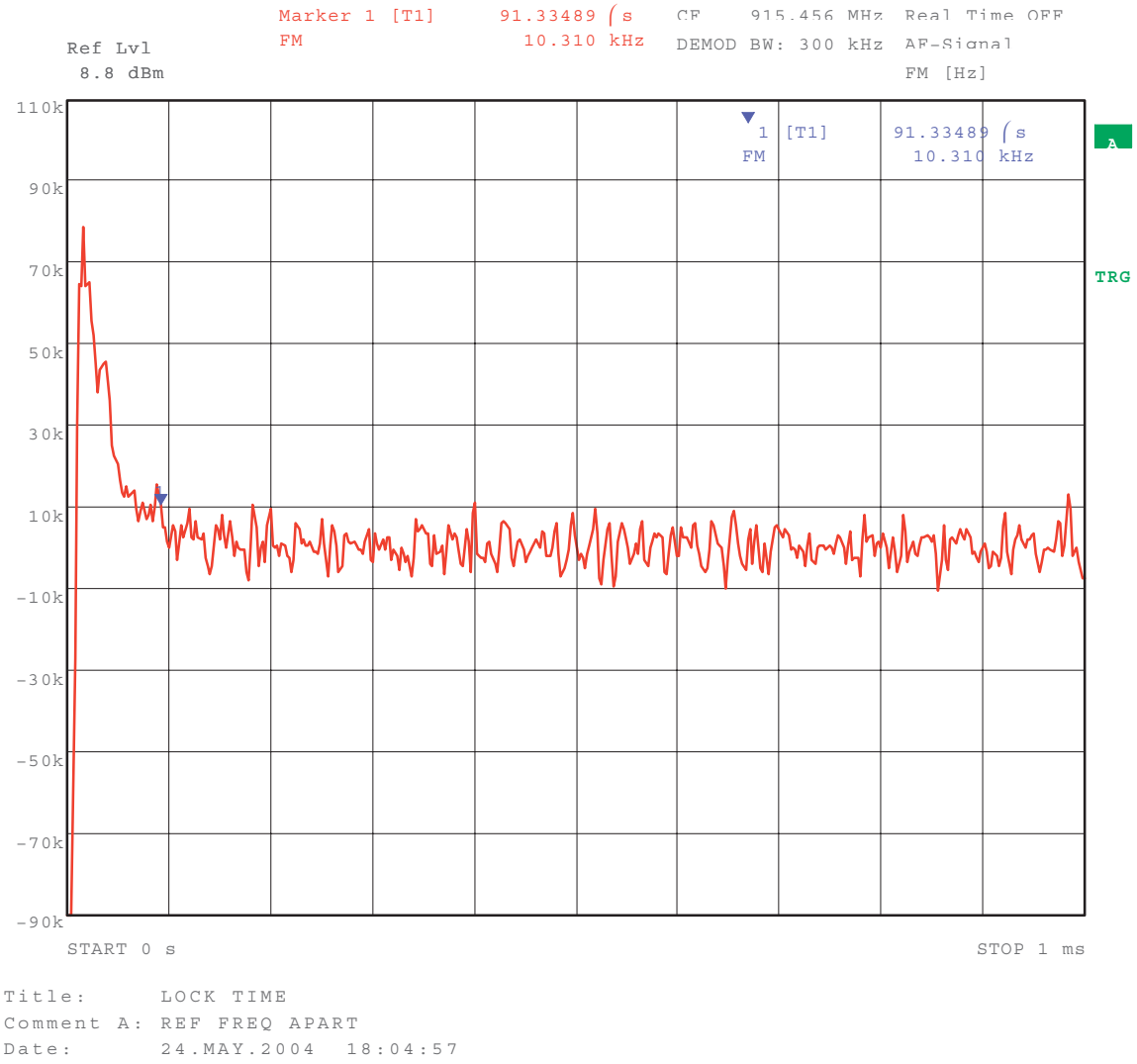
Some example lock time measurements are shown in Table 4−2 and Figure 4−6. Here the lock times are measured when the VCO settles to within 10 kHz of the designed value.

Table 4−2. Measured Lock Times for Frequency Step

FREQUENCY STEP	TYPICAL LOCK TIME, µs
409.6 kHz	91
14 MHz	180
26 MHz	206

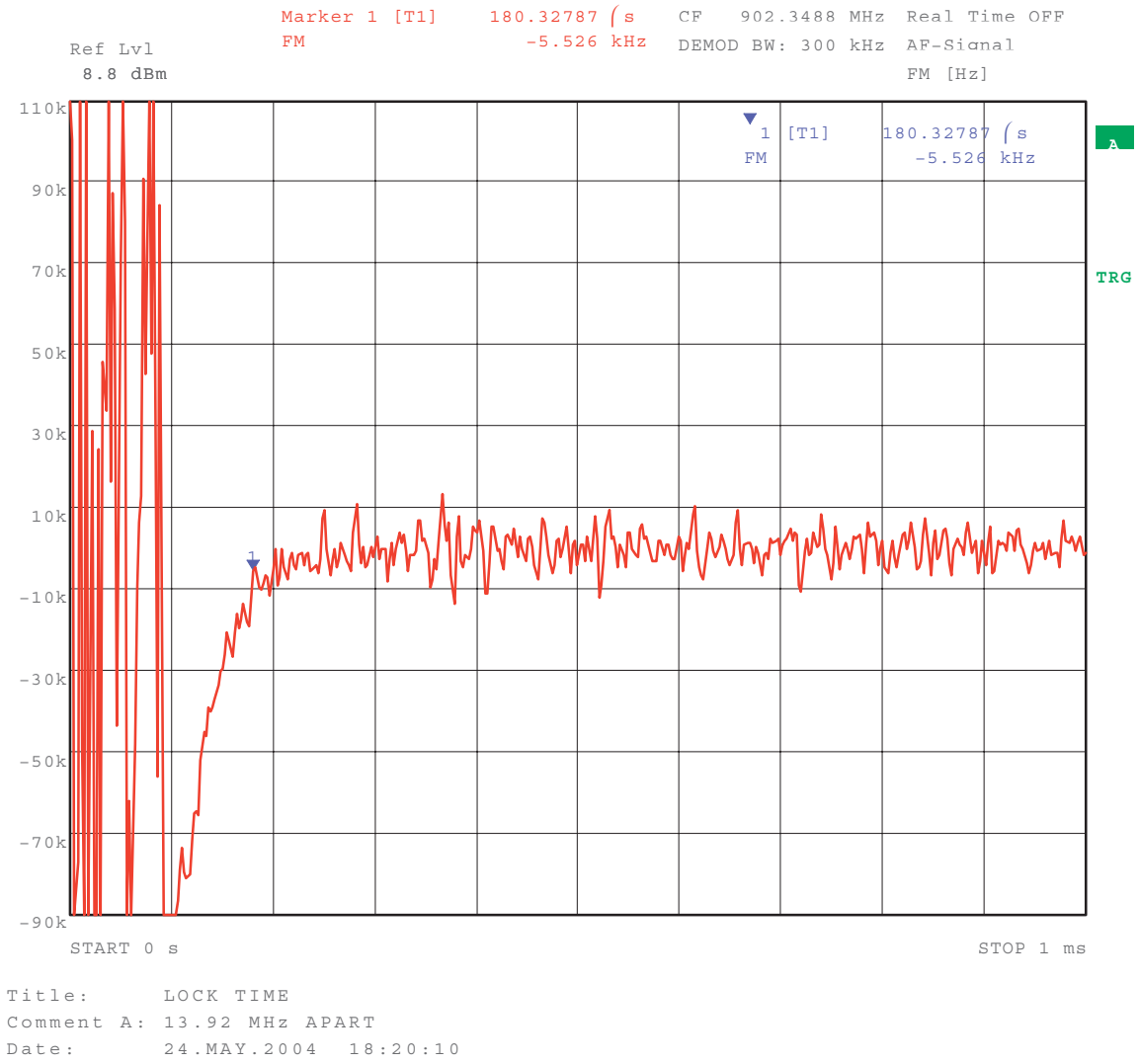
Note: NOTE: 20-kHz loop filter, Icp = 0.5 mA, 409.6-kHz reference frequency. Trigger on Strobe.

Figure 4−6. Lock Time Measurement With a 409.6-kHz (Reference Frequency) Shift



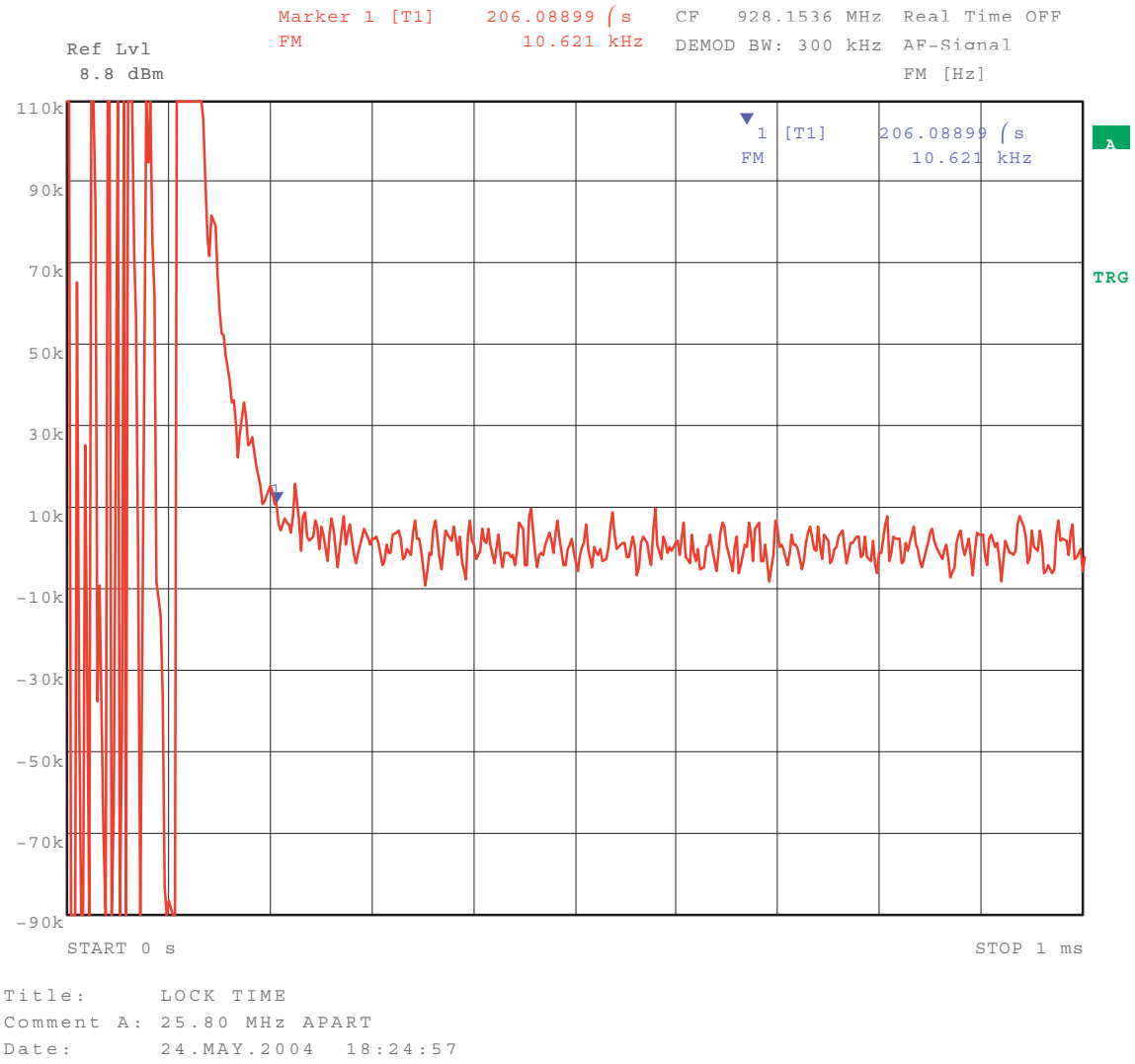
Note: Lock time is measured with a frequency shift from 915.0464 MHz to 915.456 MHz.

Figure 4−7. Lock Time Measurement With a 14-MHz Frequency Shift



Note: Lock time is measured with a frequency shift from 916.2752 MHz to 902.3488 MHz.

Figure 4−8. Lock Time Measurement With a 26-MHz Frequency Shift



Note: Lock time is measured with a frequency shift from 902.3488 MHz to 928.1536 MHz.

Chapter 5

Operation and Troubleshooting

This chapter discusses the operation and troubleshooting of the TRF4903.

Topic **Page**

5.1 Low-Power Operation With Batteries

At low battery voltage, the power output of the transmitter amplifier diminishes. On-off (amplitude shift) keying is often chosen for low data rates, low-power applications in the lower frequency band of 315 MHz and 433 MHz. Use the power amp attenuator to lower current consumption even further for short-range applications. This may require rematch of PA for optimal output power, current consumption, and harmonics.

5.2 Using the Brown-Out Detector

The brown-out detector has four user-selectable voltage thresholds. A brown-out signal is used at the system level to issue warning messages or to make performance degradation or shutdown more graceful. A multinode network might reroute data or instructions to units that have more robust connections.

5.3 Lock Detect

The lock detect circuit is an approximate indicator; when it is high, the PLL output frequency may still be settling, depending on the time in operation, loop filter bandwidth and damping, reference frequency, etc. The output will be low if the PLL is not locked. One method of using lock detect to avoid out-of-band transmission is to wait for lock detect (pin 21 lock detect high), wait an additional length of time (dependent upon loop filter, BW, etc.) and then enable the PA. The additional length of time needs to be measured by designers for their particular application, since it depends on PLL loop filter, BW, distance from one frequency to the next, etc.

5.4 Common Problems

VCO does not lock. Some causes are incorrect loop filter component values, improper loop filter design, or the charge pump current too low. One troubleshooting technique is to run the VCO open loop, where the loop filter is removed and a stable dc voltage source is connected to terminal 13. The VCO operates from around 750 MHz to 1 GHz in the high band setting. With the loop closed (loop filter reinstalled), the tuning voltage into terminal 13 should be steady.

High reference spurs. Causes are: too wide of a loop filter bandwidth, low reference frequency, or high charge pump current.

Noise in RF output. Many causes; they include switching transients from any system switching regulator, inadequate power supply bypassing, RF leakage from other RF components or assemblies, coupling from digital signals into sensitive RF circuits on the system PCB, large unshielded inductors on the system PCB. Harmonics are not common noise; they are normal products of the nature of the power amplifier, and often may be attenuated with a discrete LC filter, if required.

Low output power. Causes are inadequate power supply to the output stage of the transmit amplifier (in-line resistance or current limiting), or poor impedance matching with a filter, RF switch, or antenna. Using a common RF port with no switch degrades output power by perhaps 3 dB to 5 dB.

5.5 Subtle Problems

Slow PLL lock time. Symptoms include low effective frequency deviation and high FSK bit error rate. See the section on loop filter design.

Timing issues in baseband software also can cause high bit error rates.

5.6 Circuit Boards

Separate the traces for V_{CC}, logic, RF, and the VCO (loop filter). Reduce the potential crosstalk between major subcircuits. The loop filter and receive circuits are especially vulnerable to signal contamination.

Use adequate grounding, both for dc return, and to separate signal networks through the use of low-inductance ground planes and ground vias.

Use adequate bypassing on power supplies. Designers often use capacitors of varying values to bypass noise signals at varying frequencies. Capacitors have a resonant frequency above which they appear as an inductor and do not provide an adequate RF short to ground.

A circuit board with four metallization layers typically has a layer for topside components and RF traces, a layer for RF ground, a power plane layer, and the fourth layer for analog components and some digital signals. Having four layers helps to achieve a more compact layout which may offset the potential higher fabrication cost. A two-layer board is sometimes the only option for low-cost systems.

Use 50-Ω traces for RF signals. Low-loss propagation of RF signals over distance depends on transmission line structures such as microstrip, stripline, or coplanar waveguide. When using FR4 as a board material, a 50-Ω microstrip line can be achieved with approximately 12 mils of substrate thickness and 14 mils of conductor width. Dimensions for a 50-Ω line vary by PCB manufacturer. Ground shields on the RF conductor layer should be kept away from RF lines by at least three substrate heights unless ground vias are used to prevent voltage discontinuities.

Use separable subcircuits to facilitate characterization and troubleshooting. There should be board access to circuits for data in, data out, RF transmit out, RF receive in, mixer out, IF filter out, and VCO tuning voltage. Separate power supply networks for the TRF4903 from supply networks for other components such as LEDs, input buffers, etc. This layout approach is at odds with the compact, no-frills designs preferred for production. One approach is to have separate board layouts for engineering development and for production.

Use composite footprints wherever possible for components that are vendor dependent or may become hard to get, such as clock crystals, band-pass filters, ceramic capacitors, etc.

Minimize solder defects, particularly in circuits susceptible to small changes in dc values, such as the loop filter.

Use high-Q inductors in RF matching circuits for the LNA, PA, and in any discrete demodulation tank circuit. Consider putting shunt caps (100 pF to 1000 pF) on digital lines that change slowly, like RSSI or DET_OUT, in order to snub stray RF signals.

Use close-tolerance capacitors in RF matching circuits.

The dc bias circuits shown in some of the EVMs, design examples, and reference designs are aggressively bypassed. Some simplification may be done with little or no loss of performance, but the designer should test the circuit board to make sure that combining bias circuits together will not introduce noise, feedback. Bias circuits that might be combined are PA_VCC with LNA_VCC and perhaps MIX_VCC, VCO_VCC and CP_VCC, XTAL_VCC, and DVDD. DEM_VCC powers the bandgap reference and high-gain IF strip. PA_VCC2 feeds the amplifier output stage; a 10-Ω series resistor in this bias circuit increases isolation but may reduce output power by a few tenths of a dB.

5.7 External Parts: Crystal and PA

The crystal should be the fundamental type rather than an overtone type. The default crystal for the TRF4903 EVM is Crystek 017119, 19.6608 MHz. The TRF4903 works with other crystal frequencies from 9.5 MHz to 20 MHz. Other crystals include Citizen CS10, HCM49 and HC49US, ECS-196.6-20-5P, SMI 97SMX, and ICM HC45U.

Table 5−1. Example Crystal Information: Crystek 017119

Characteristic	Value
Overall tolerance	±45 ppm
Operating temperature	−40 to +80°C
Load capacitance	12 pF
Shunt capacitance	2 pF
Drive level	100 μW

An example high power amplifier is the RF2172 from RF Micro Devices.

5.8 Commonly Used Test Equipment

The following is a list of test equipment used for ISM wireless applications, although one could get by with equivalent instruments or fewer instruments. Producing a successful design without using an oscilloscope, a spectrum analyzer, and a function generator would be difficult.

1) Spectrum analyzer, HP 8560E, 30 Hz to 2.9 GHz, with phase noise option. Used to examine RF transmit and IF signals, spurs, harmonics, loop filter bandwidth and phase noise, etc.

2) High-frequency probe, HP 85024A, 300 kHz to 3 GHz. Use to examine RF signals on circuits not equipped with SMA connectors, such as MIX_OUT, the IF filter output, etc. The HF probe cannot be used to make accurate or repeatable RF power measurements, but it can be used to trace large amounts of gain or loss in RF circuits or to look for spurious signals within its measurement bandwidth.

3) Oscilloscope, Tektronix 2465B, 400 MHz, or Tektronix digital storage oscilloscope TDS 3054, 500 MHz, 5 GS/s. Use to examine the TX_DATA

and RX_DATA terminals, post-detect signal, sample-and-hold capacitor, noise on power supplies, etc.

4) Oscilloscope probes, Tektronix P6137 or P6139A. Two probes are useful for measuring input and output waveforms.

5) Frequency counter, HP 5347A, 10 Hz to 20 GHz, or Agilent 53131A, 200 MHz to 5 GHz. Use to measure the output frequency precisely, determine frequency corrections, and to check for large harmonic signal components.

6) Function generator, HP 8116A, 50 MHz, or Agilent 33250A, 80 MHz. Use to generate square-wave TX_DATA signal.

7) Signal generator, Rohde & Schwarz SMT03, 5 kHz to 3 GHz. Use to generate FSK test signals at RF frequencies with known modulation and deviation to test the receiver function.

8) Vector network analyzer, HP 8753D, 30 kHz to 6 GHz. Used to measure complex input, output impedances, and harmonics. Calibration standards should be included.

9) Power supplies, HP E3610A, 15 V, 2 A, or Agilent E3610A, 15 V, 2 A.

10) Multimeter for current and voltage measurements.

5.9 Advanced Topics

For advanced topics see Chapter 8 of the TRF6903 design guide (SWRU009).

Chapter 6

References

Product information, design information, evaluation circuit boards, and design examples for low data rate applications are located at www.ti.com/ismrf.

For information on data coding, see the *Designing With the TRF6900 Single-Chip RF Transceiver* application note (SWRA033).

For information on baseband code and designing a data link, see the *Implementing a Bidirectional, Wireless UART Application with TRF6903 and MSP430* application report (SWRA039).

For information on receiver sensitivity, see the *Understanding and Enhancing Sensitivity in Receivers for Wireless Applications* application report (SWRA030).

For information on phase-locked loops, see the *Fractional/Integer-N PLL Basics* application report (SWRA029).

TRF4903 Single-Chip Multiband RF Transmitter data sheet, (SWRS023)

TRF6903 design guide, (SWRU009)

TRF6901 Single-Chip RF Transceiver data manual, (SLWS110)

TRF6901 902 MHz to 928 MHz RF Tool Kit, (SWRU005)

TRF6901 868 MHz to 970 MHz RF Tool Kit, (SWRU006)

Phase-Lock Basics, William F. Egan, J. Wiley & Sons, 1998

PLL Performance, Simulation, and Design, Dean Banerjee

RF/Microwave Circuit Design for Wireless Applications, Ulrich L. Rohde, David P. Newkirk, John Wiley & Sons, 2000

Wireless Communications, 2nd Ed., Theodore S. Rappaport, Prentice Hall, 2002