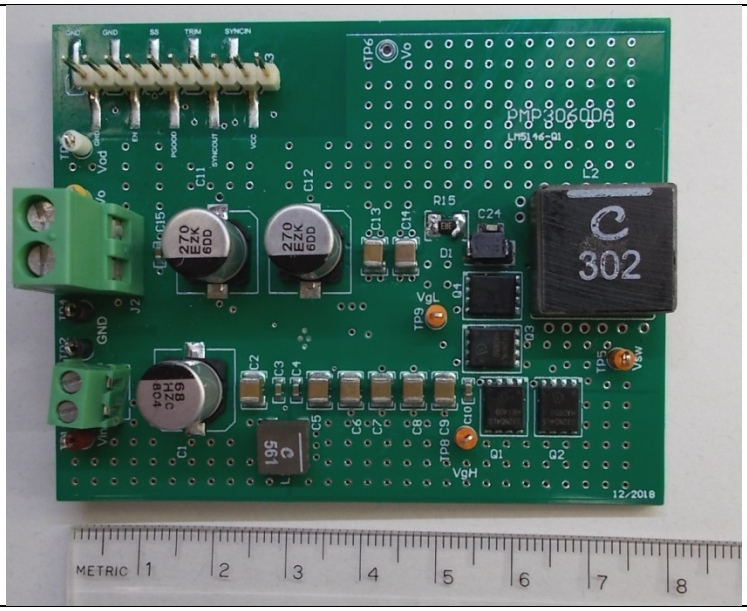
Test Report: PMP30600-AH
20-A Automotive Pre-Regulator Reference Design

Description

This reference design is a 100W synchronous buck converter primarily to supply automotive loads. The IC is LM5146-Q1 in fixed frequency operation at 250 kHz to ensure low noise operation. To minimize conducted emissions an input filter prevents from reflected ripple. Furthermore a RC snubber attenuates noise in the RF band to reduce radiated emissions. To reduce system EMI the design is prepared either to synchronize other converters (output) or just to be externally synchronized (input). The power stage itself withstands surge voltages up to 36Vpk.



1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	6 V to 18 V
Output Voltage	5 V
Maximum Output Current	20 A
Calculated Switching Frequency	250 kHz

*1.2 Considerations**

This circuit is realized on PCB PMP30600RevA

2 Testing and Results

2.1 Efficiency Graphs

The efficiency is shown in the Figure 1 below. The input voltage was set to 14V

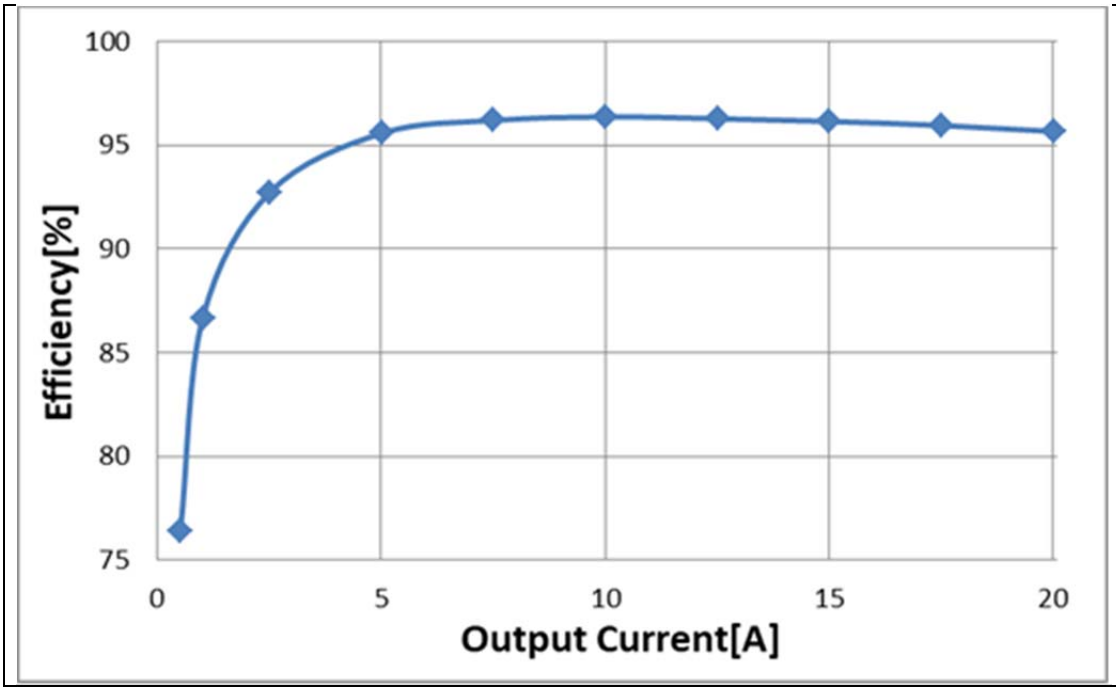
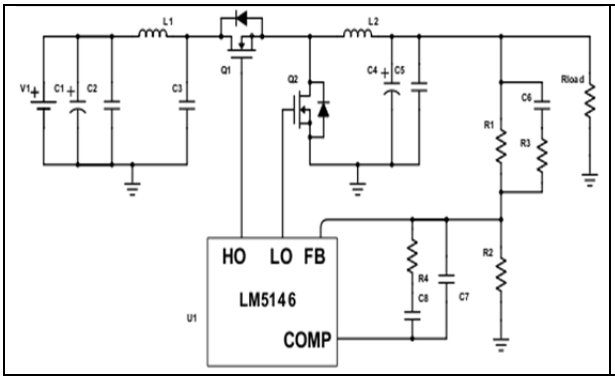


Figure 1

Full load efficiency 95.65%, calculated 95.9%;
Deviation by self heating of inductor and switching losses

Maximum efficiency 96.36% at 10A.

Efficiency ≥95% in a range 5A to 20A, so 25% load to 100% load



Power stage as calculated before:

Cin 5x 22uF/50V/X7R/1210

NFET Infineon BSC032N04LS

Inductor 3uF/3mOhm/43Asat

Cout 2x 270uF/25V

2.2 Load Regulation

The load regulation of the output is shown in the Figure 2 below. The input voltage was set to 14V.

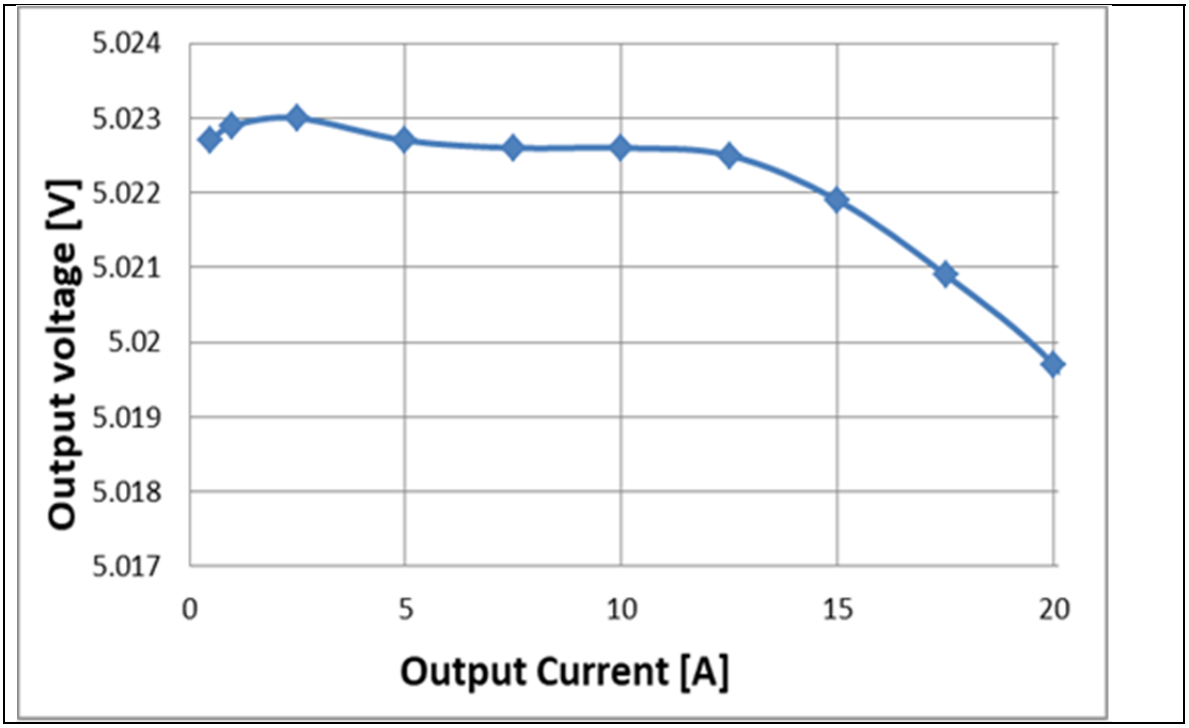


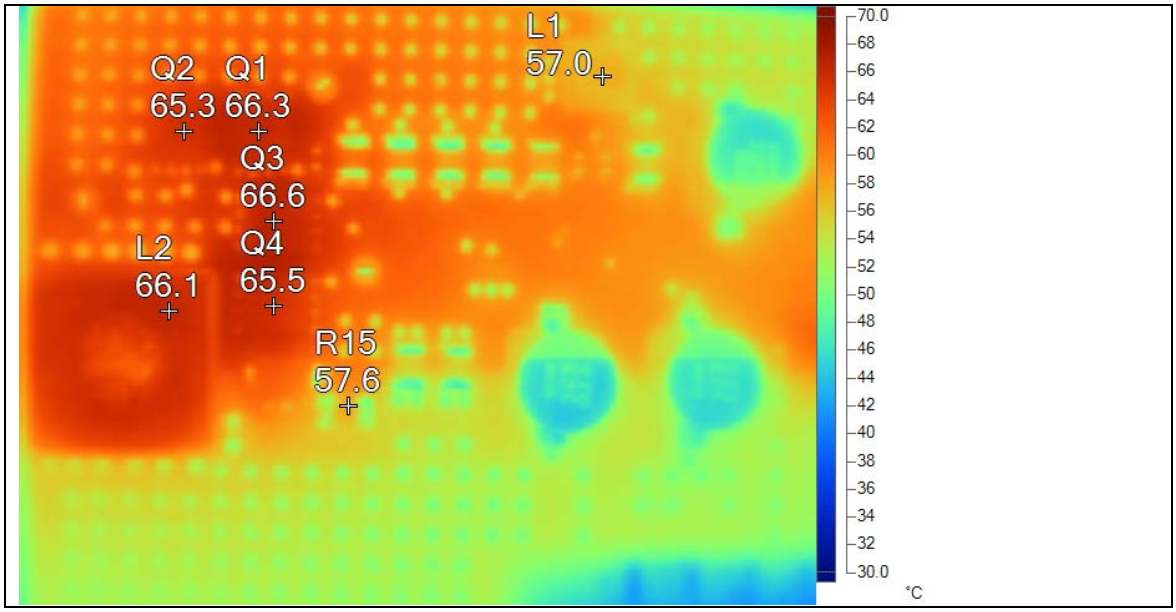
Figure 2

Min. Vout 5.0179V, max Vout 5.0229V,

Output voltage variation 5.0mV, so 0.1%, negligible.

2.3 Thermal Images

Thermal image at 14V input and full load 20Amp after 20 minutes continuous operation [Rt = 23c]:



Name	Temperature
Q1	66.3°C
Q2	65.3°C
Q3	66.6°C
Q4	65.5°C
L1	57.0°C
L2	66.1°C
R15	57.6°C

Temperature rise is below 50K, a proper design of the power stage with maximum efficiency results in relaxed thermal stress because inductor and MOSFETs are almost same temperature; good balance.

2.4 Dimensions

The extensions of the board are 79 mm x 62 mm

3 Waveforms

3.1 Switching

3.1.1 Low Side FET

With input voltage set to 14V and 20A Iout results in the waveform shown in Figure 3

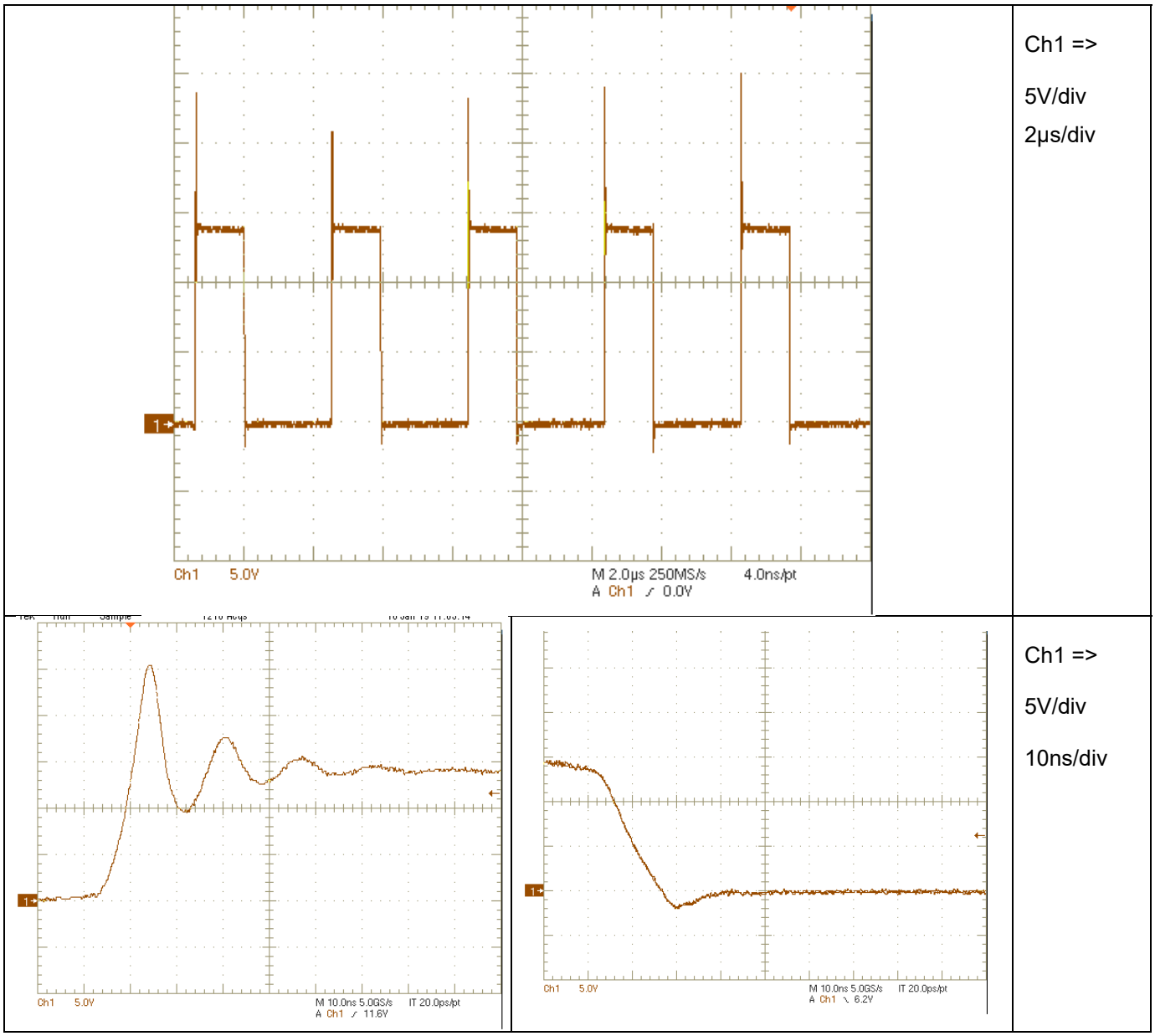
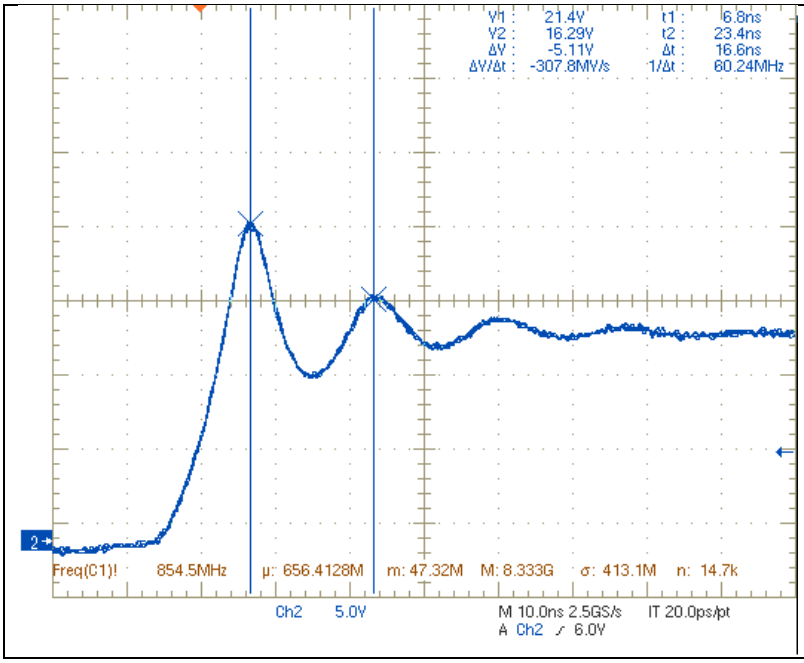


Figure 3

Maximum input voltage is 26V and the overshoot is around 12V.
Vds rating of BSC032N04LS is 40V – enough margins.
RC snubber circuit was implemented to demonstrate RF suppression:

Measure ringing frequency at switch node w/ RF probe (no GND leads, use GND clip),
here 60MHz – could cause trouble , radiated emissions:



Ch2=>

switch node

no snubber

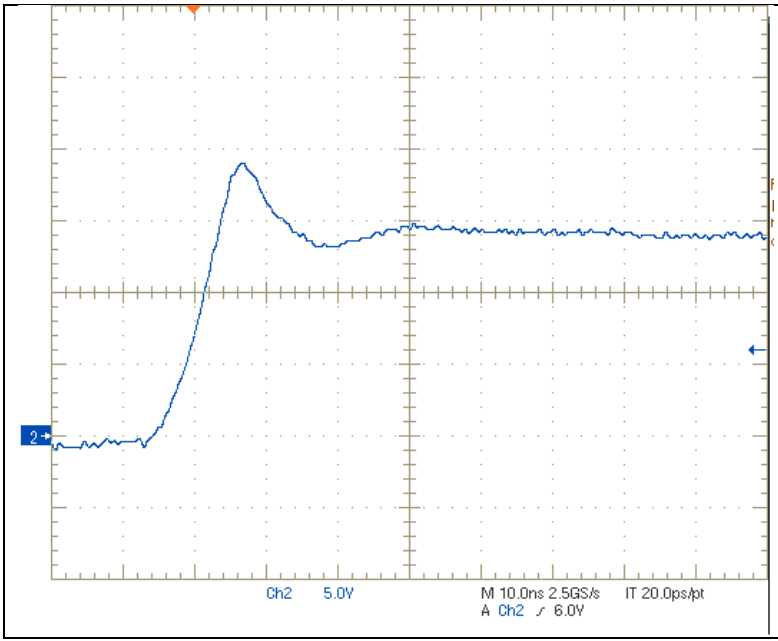
5V/div

full BW

10ns/div

1) **add capacitor from switch node to GND to achieve half of the prior frequency**,
here 1nF

2) **add resistor in series to achieve half of the prior overshoot**,
here 3.3Ω reduced overshoot from 7V to 4V:



Ch2=>

switch node

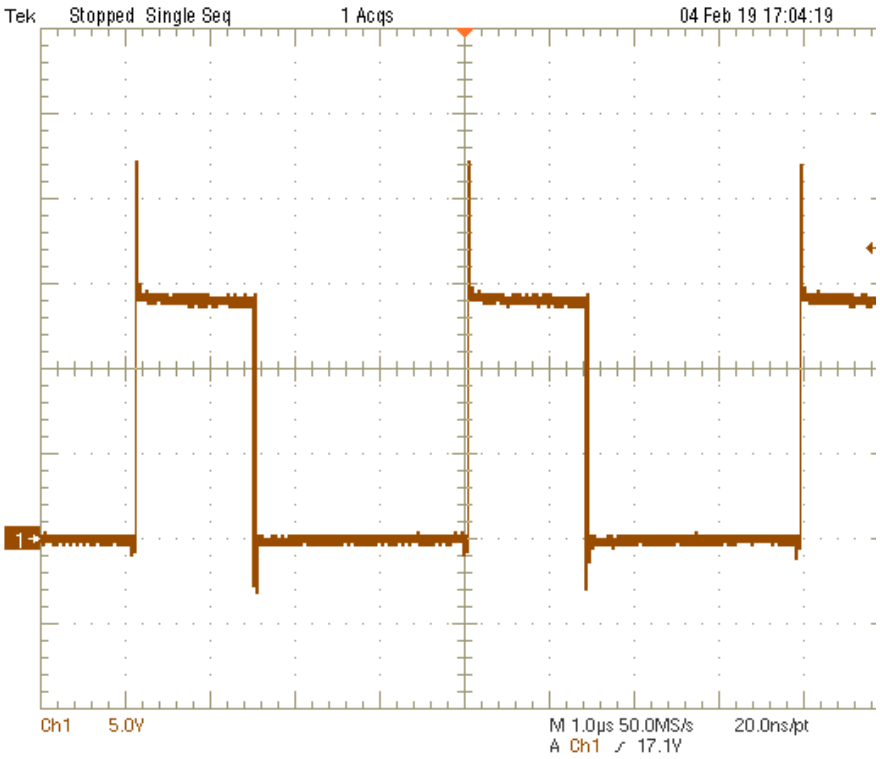
1nF+3.3Ω
RC snubber

5V/div

full BW

10ns/div

Clamping network 1nF / 3.3 Ohm reduces RF content at the switch node, less EMI !



Ch1=>

switch node

1nF+3.3Ω RC snubber

5V/div

full BW

1us/div

By experience could be said that a drop in efficiency from 0.2% to 0.5% is typically caused by adding the RC snubber circuit. For a medium power design like PMP30600 geometry 1206 or 1210 might fit, but for high power designs be aware of losses up to 500mW:

- 0603 <100mW
- 0805 <150mW
- 1206 <200mW
- 1210 <250mW
- 1812 <500mW
- 2010 <750mW
- 2512 <1W

3.1.2 High-Side FET referenced to Vin

With input voltage set to 12V and 20A Iout results in the waveform shown in Figure 3

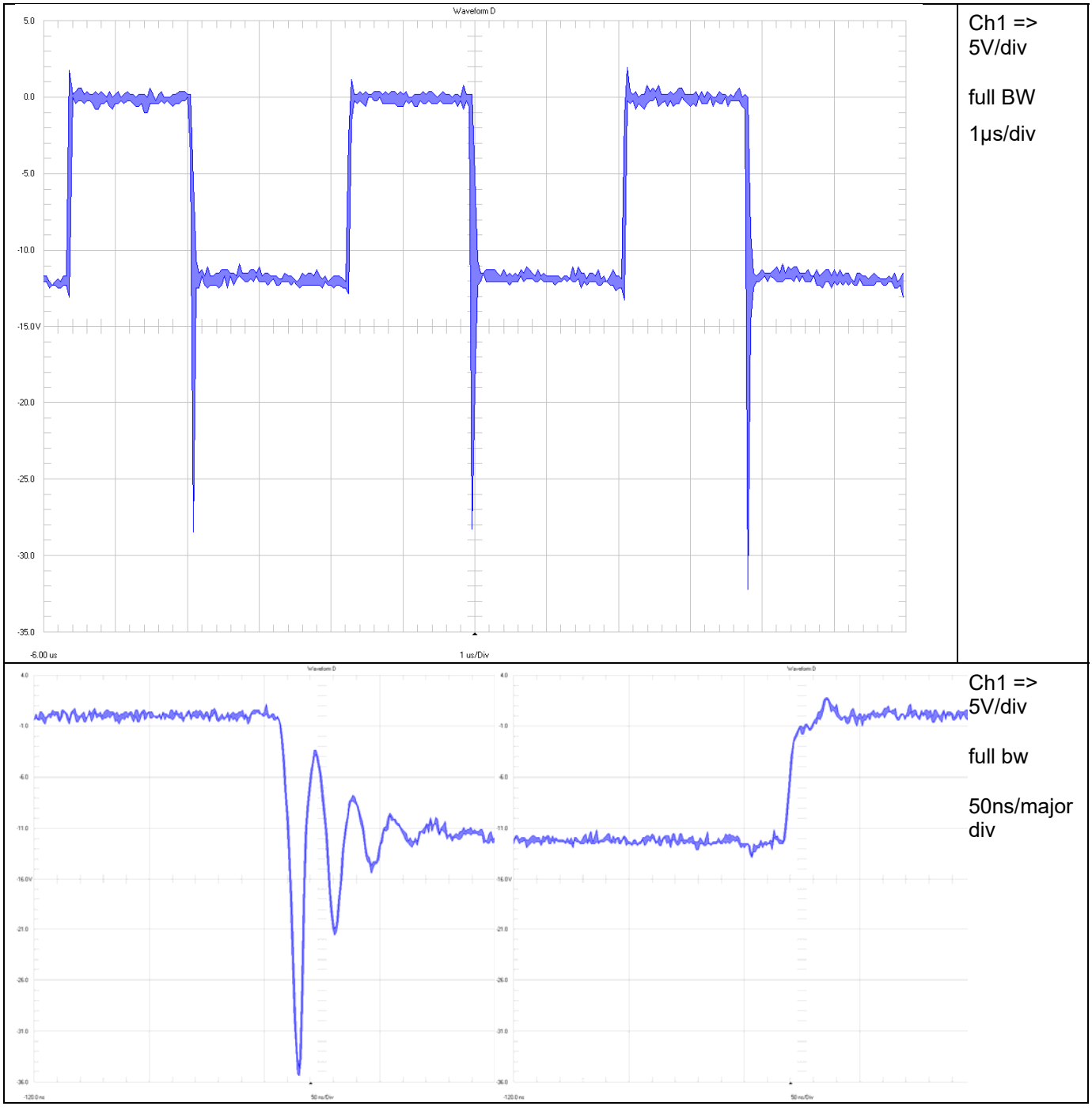


Figure 4

3.1.3 Gate-Source of High-Side FET

With input voltage set to 14V and 20A Iout results in the waveform shown in Figure 3.

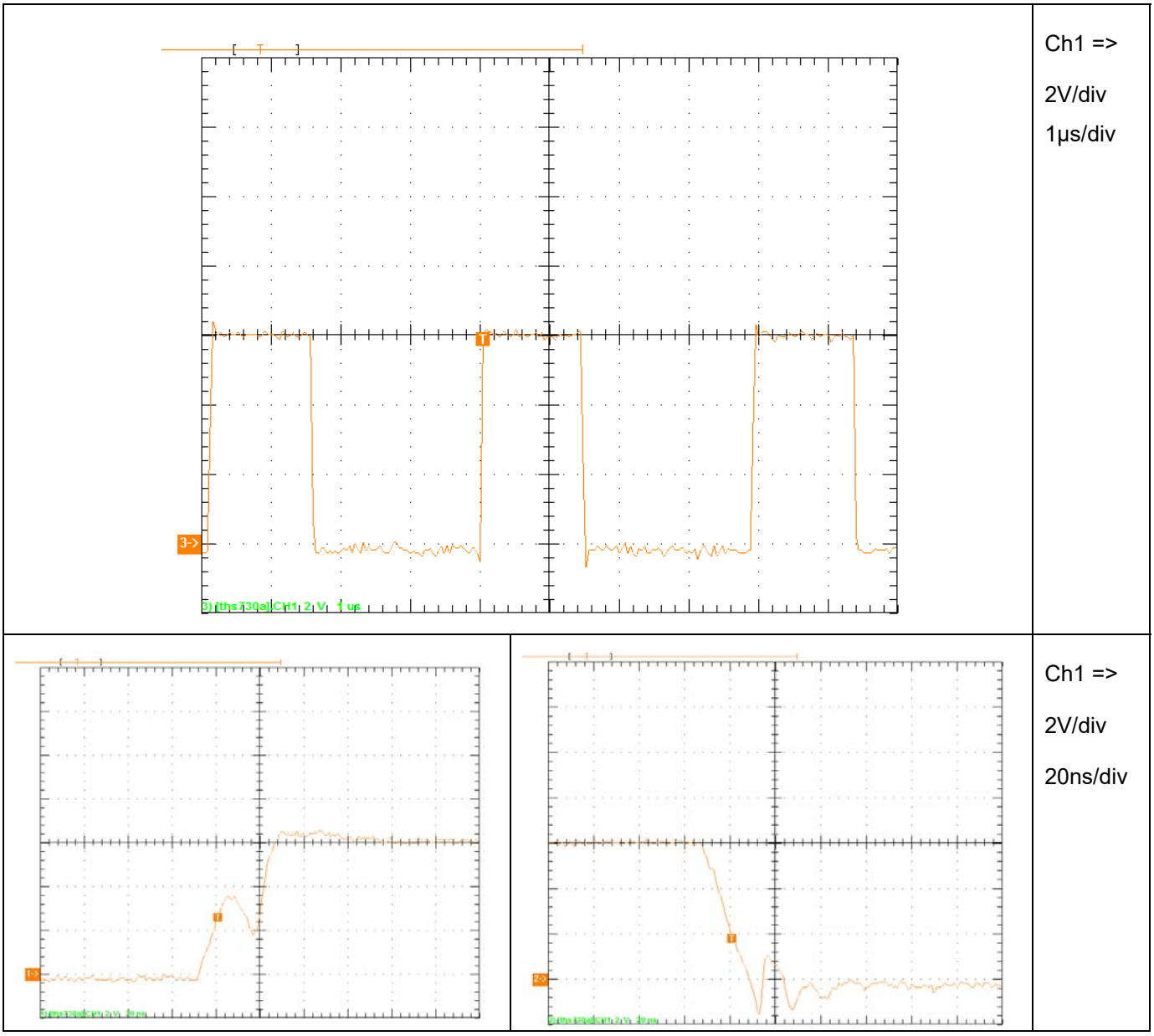


Figure 5 High side

3.1.4 Gate Source of Low-Side FET

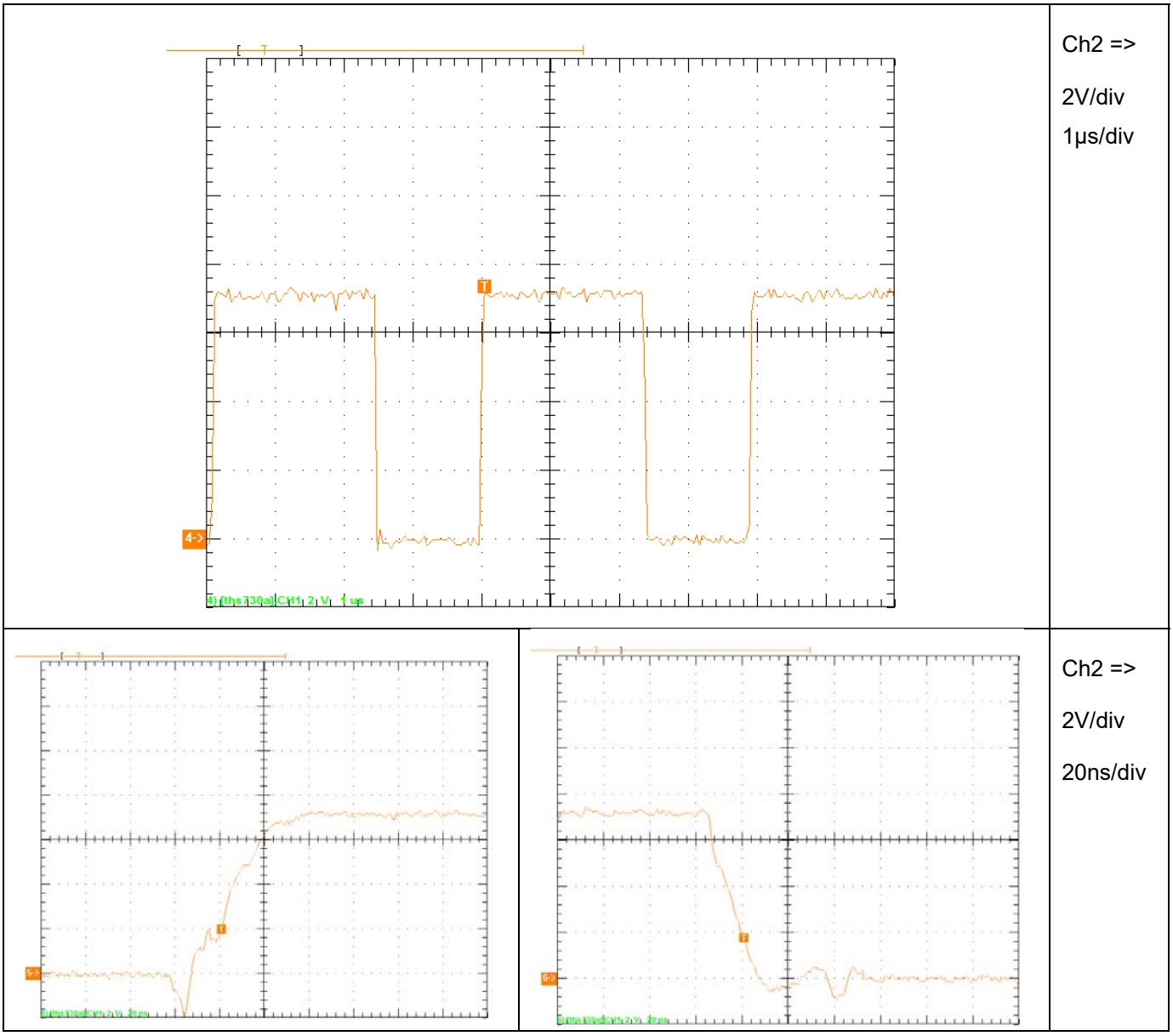


Figure 6 Low side

3.2 Output Voltage Ripple

The output ripple voltage is shown in Figure 7. The image was taken with 20A load 12V at the input. The output ripple voltage is less than 50mV except noise.

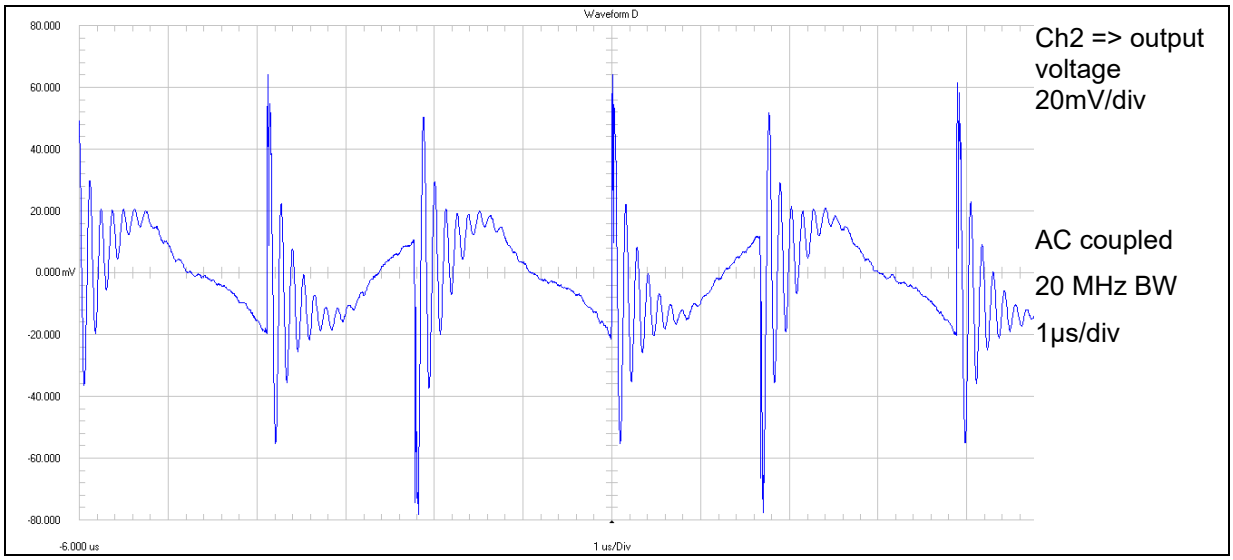


Figure 7

3.3 Input Voltage Ripple

The input ripple voltage is shown in **Error! Reference source not found.**. This was taken with 20A full load 14V at the input.

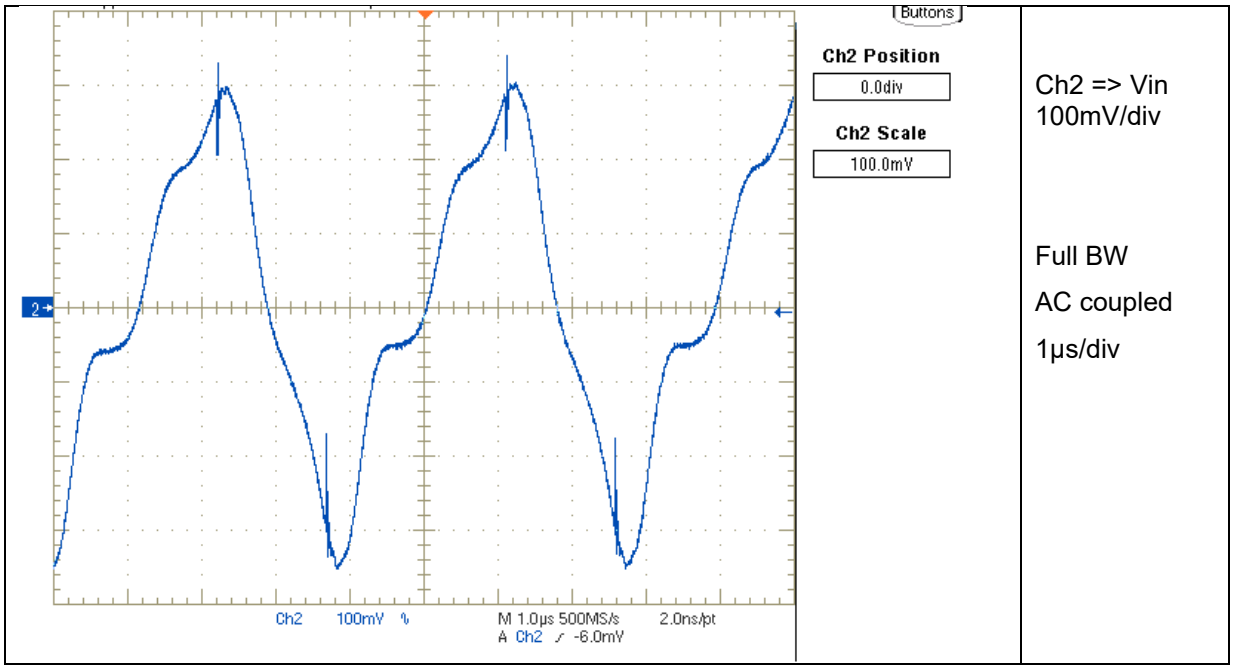
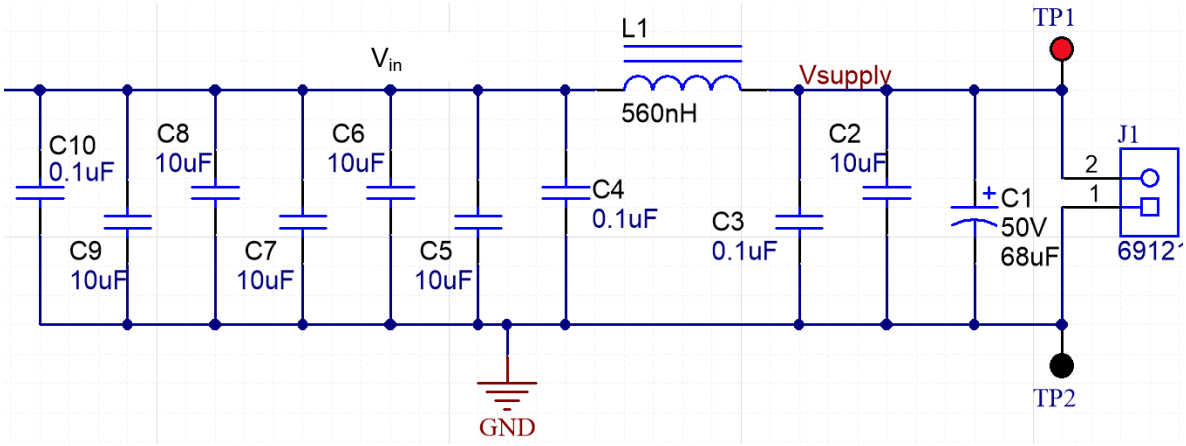


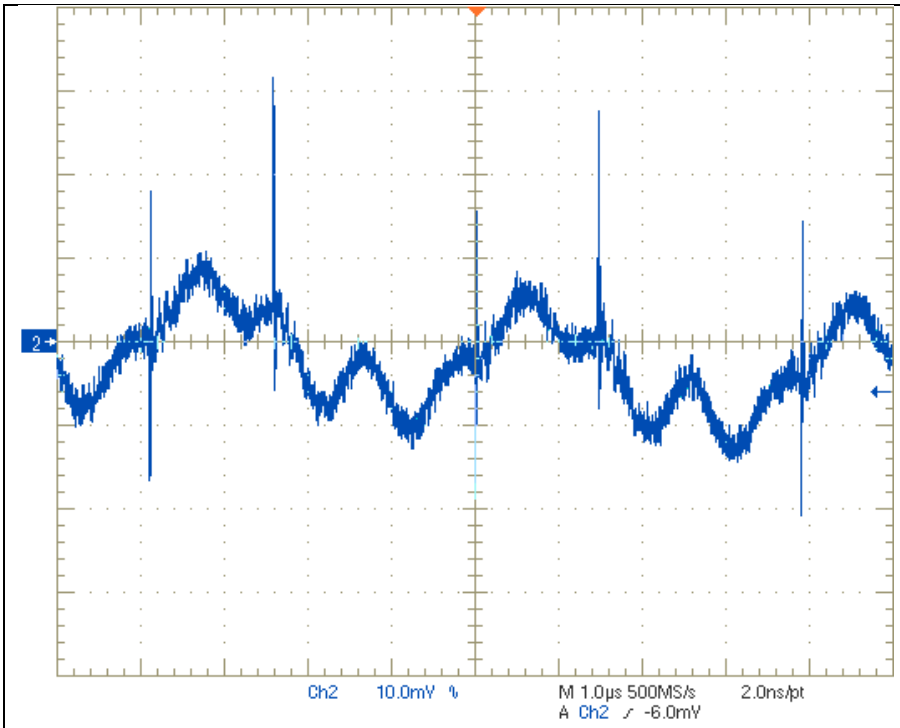
Figure 8

Input voltage ripple is around 650mV

Reflected ripple = conducted emissions, EMI

Finally the input voltage by using PI filter 68uF – 0.56uH – 5x 10uF;
A small ceramic capacitor 100nF was added to the electrolytic to suppress glitches:





Ch2=> Vsupply
10mV/div

full BW

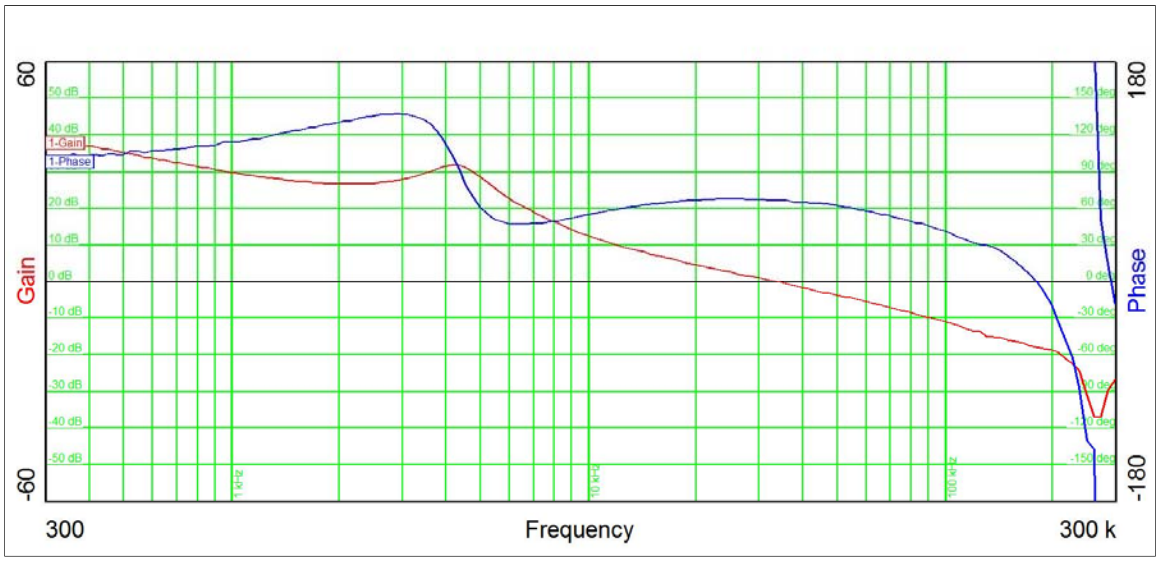
AC coupled

1µs/div

Input voltage is reduced to 20mV; reduction rate is 1/30.
A tremendous reduction of reflected ripple resulted in better EMI behavior !
The inductor prevents the source from seeing the pulse currents – less conducted emissions.

3.4 Bode Plot

Figures below shows the loop response with 20A load and 14V input – fco=32kHz



The crossover frequency 32kHz fits exactly to the first calculation by hand, the phase margin is more than 60 degrees. Slope at crossover is close to -1.

REMEMBER:

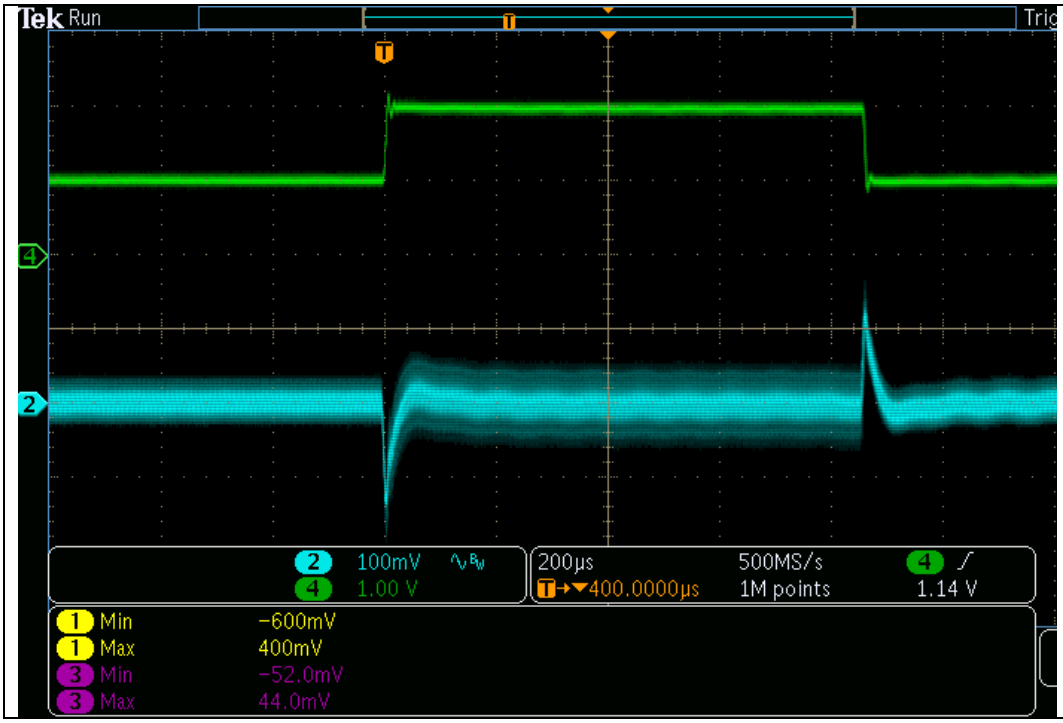
This analysis is a small signal analysis, shows the small signal behavior of the power supply.

The only true analysis is a large signal analysis, the system response on a load transient!

3.5 Load Transients

4 Load Transients

The Figure 9 shows the response to load transients. The load is switching from 10A to 20A. The input voltage was set to 14V



Ch2 => output voltage 100mV/div

20MHz BW

Ch4 => output current 10A/div

200µs/div

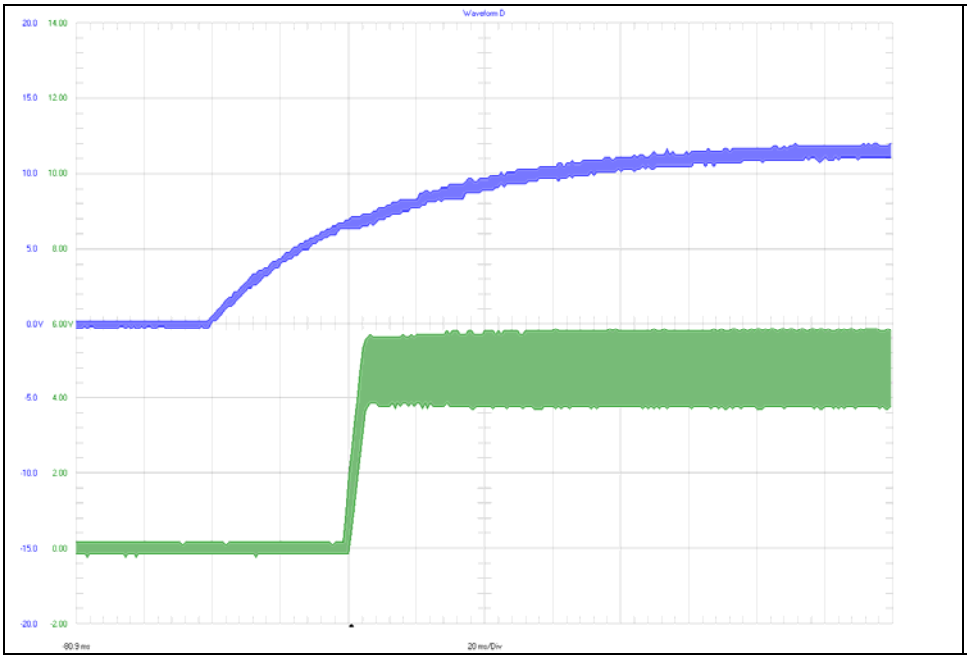
Figure 9

The voltage drop caused by 10A is around 150mV, so around 3% of the output voltage 5V;
The combination output capacitor to loop bandwidth matches.

A proper calculation of the error amplifier compensation results in a stable design. For series production a phase margin >60 degrees and a gain margin <-15dB is recommended.

4.1 Start-up Sequence

The startup waveform is shown in the Figure 10. The input voltage was set at 12V, with 20A load at the output. The power supply was enabled



Ch1=> input voltage 5V/div

Ch3=> output voltage 2V/div

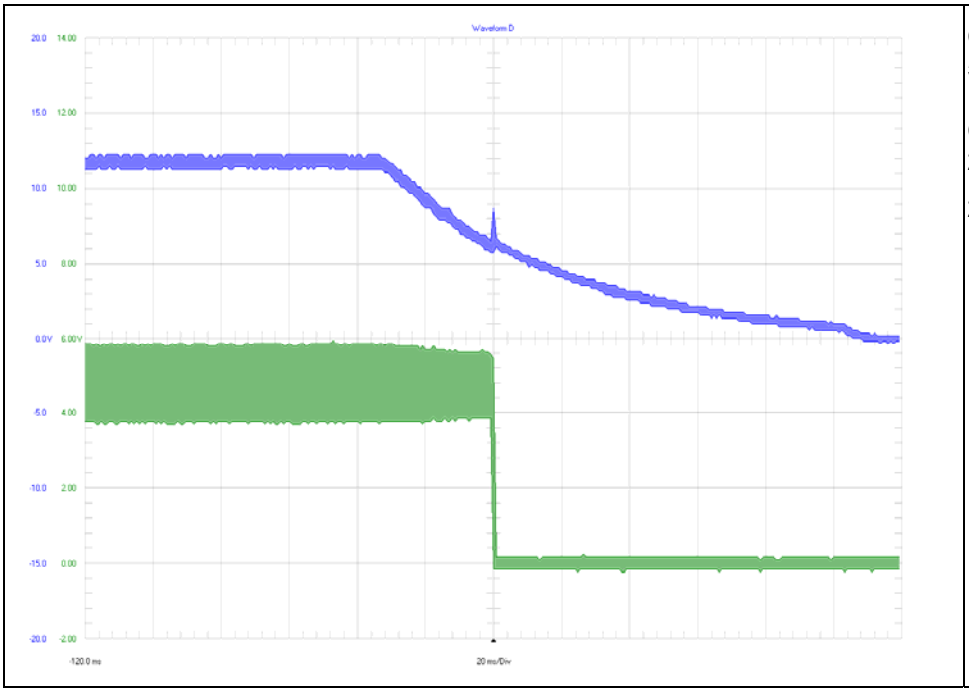
20ms/div

20 MHz bandwith

Figure 10

4.2 Shutdown Sequence

The shutdown waveform is shown in the Figure 11. The input voltage was set at 12V, with 20A load at the output. The power supply was disabled.



Ch1=> input voltage 5V/div

Ch3=> output voltage 2V/div

20ms/div

Figure 11

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