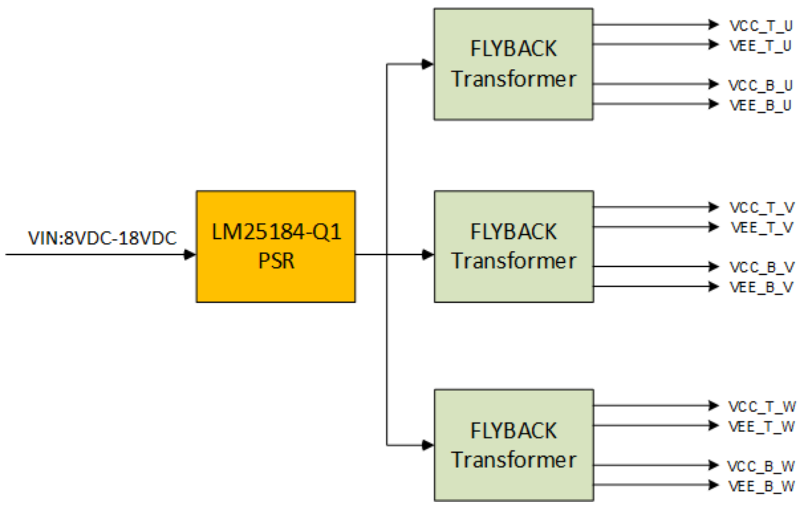
Test Report: PMP40747

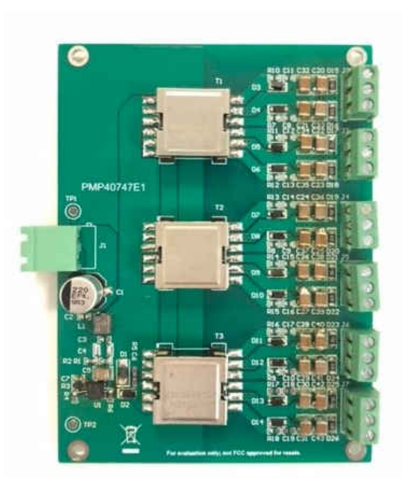
Multi-Output Primary-Side Regulated Flyback Reference Design for Automotive IGBT Gate Driver Applications

1 Description

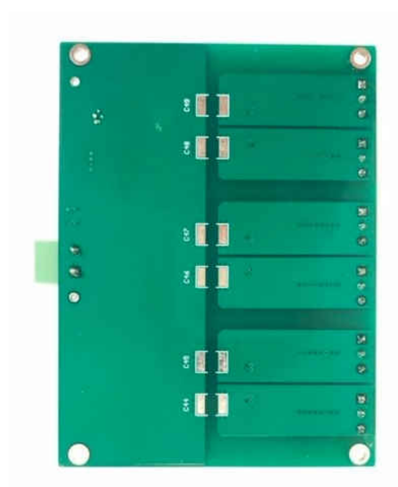
This reference design provides an isolated power supply for an automotive IGBT gate driver. The primary-side regulated flyback controller LM25184-Q1 is used to avoid an optocoupler and improve system reliability. Three transformers are used to achieve multiple outputs and facilitate flexible system layout.



Block Diagram



Top Photo



Bottom Photo

2 Test Prerequisites

2.1 Voltage and Current Requirements

Table 2-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage	8 V–18 VDC (12 V nom)
Output Voltage	6 × (+15 V, –8.2 V)
Maximum Output Current	100 mA

2.2 Required Equipment

- Multimeter (voltage): Fluke 287C
- Multimeter (current): Fluke 287C
- DC Source: Chroma 62012P-100-50
- E-Load: Chroma 63105A module
- Oscilloscope: Tektronix DPO3054
- Electrical Thermography: Fluke TiS55

2.3 Considerations

For better cross regulation, all outputs have a fixed 1-mA dummy load. According to inverter gate driver applications, only 3 × (+15 V, –8.2 V) outputs are loaded, and the other 3 × (+15 V, –8.2 V) outputs work at no load (with 1-mA dummy load).

2.4 Dimensions

The board dimensions are 100 mm (length) × 75 mm (width) × 10mm (height).

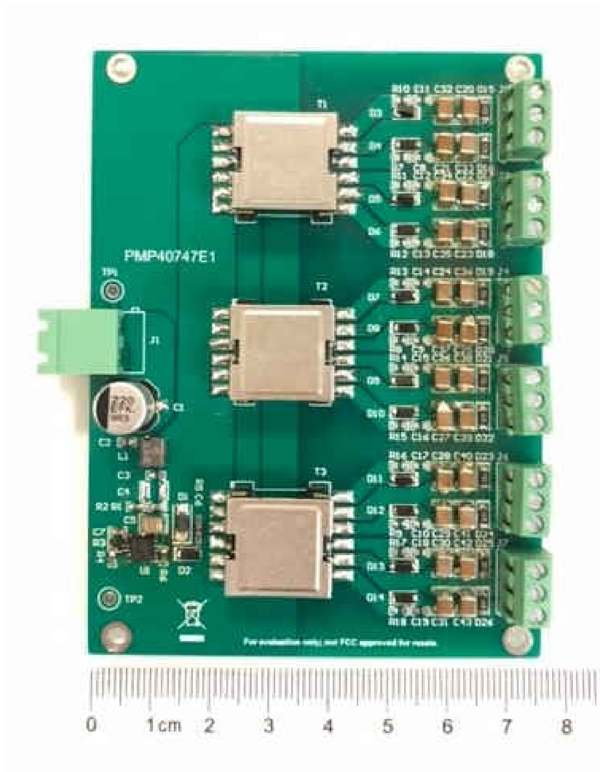


Figure 2-1. Dimension

3 Testing and Results

3.1 Efficiency Graphs

The following figure shows the efficiency graph.

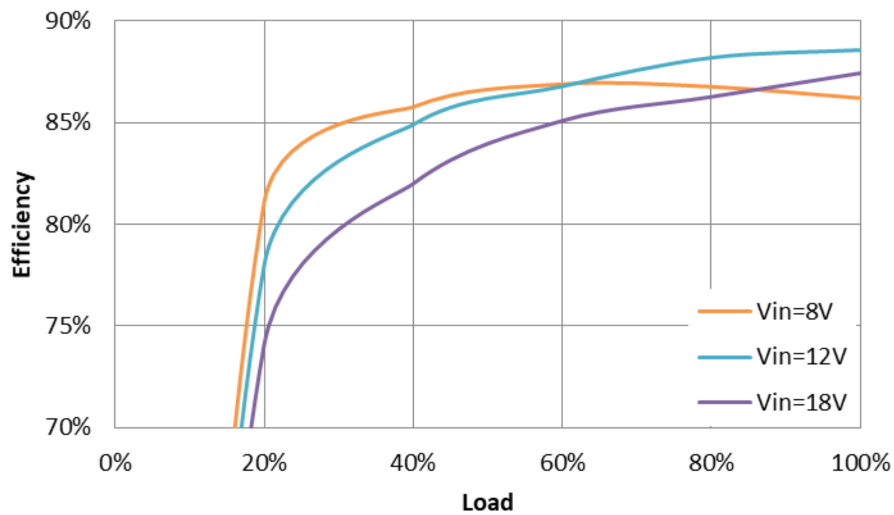


Figure 3-1. Efficiency Graph

3.2 Cross Regulation

The cross regulation is tested by adjusting the six loaded outputs (VCC_T and VEE_B), and the other six outputs (VCC_B and VEE_T) work at no load.

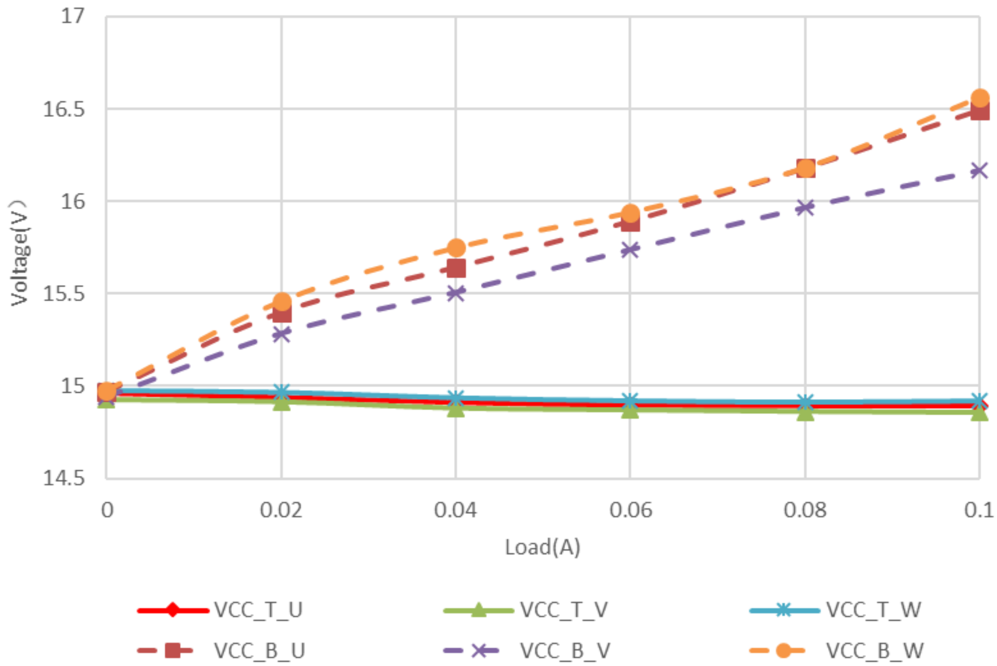


Figure 3-2. Cross Regulation of VCC_T and VCC_B

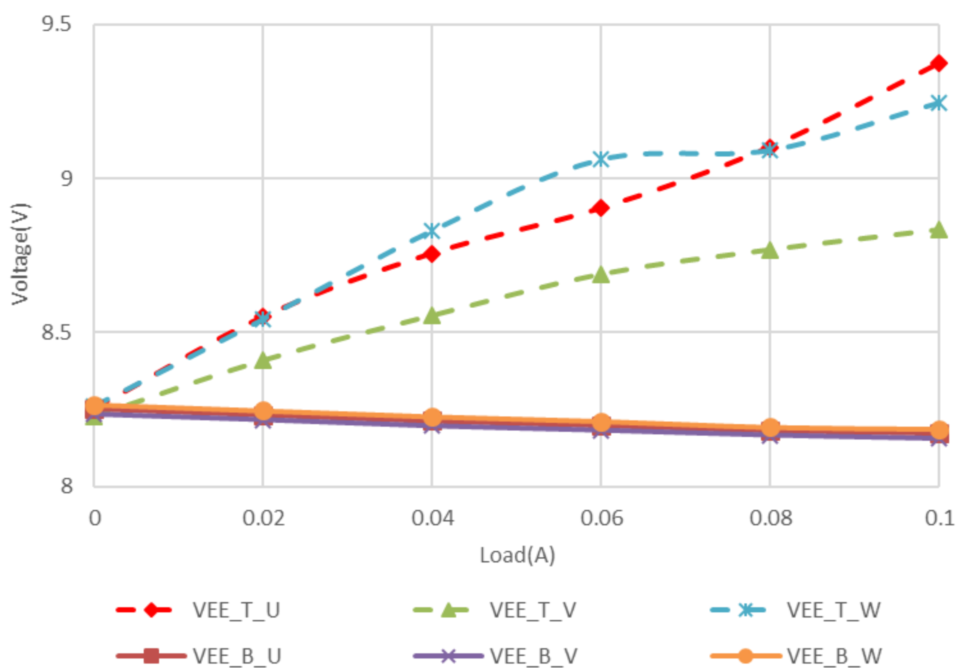


Figure 3-3. Cross Regulation of VEE_T and VEE_B

3.3 Thermal Images

The following photos show the thermal images.

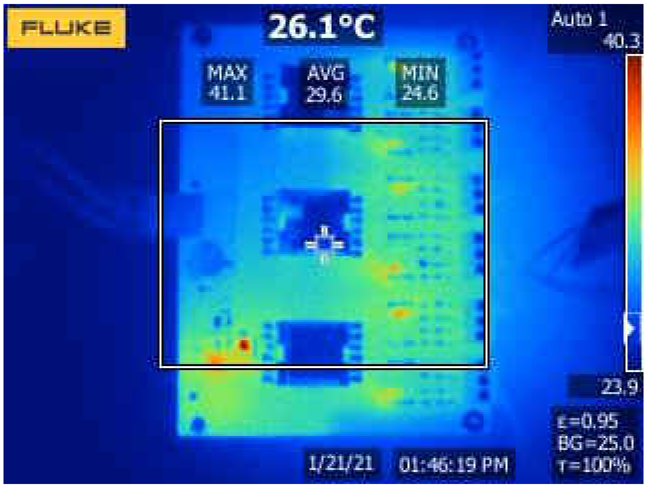


Figure 3-4. Thermal Top

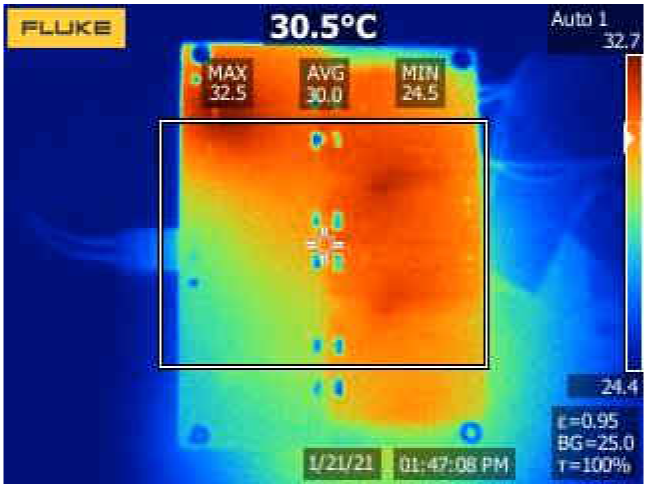


Figure 3-5. Thermal Bottom

4 Waveforms

4.1 Switching

Switching behavior is shown in the following figures.

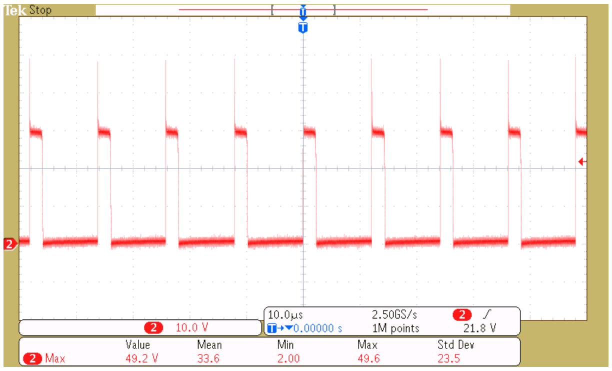


Figure 4-1. 8-V Input, no Load

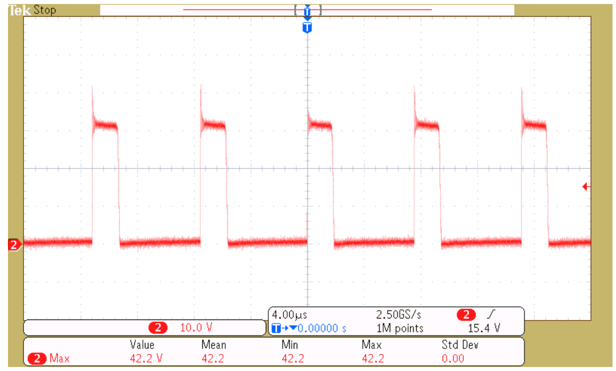


Figure 4-2. 8-V Input, VCC_T and VEE_B With 100-mA Load

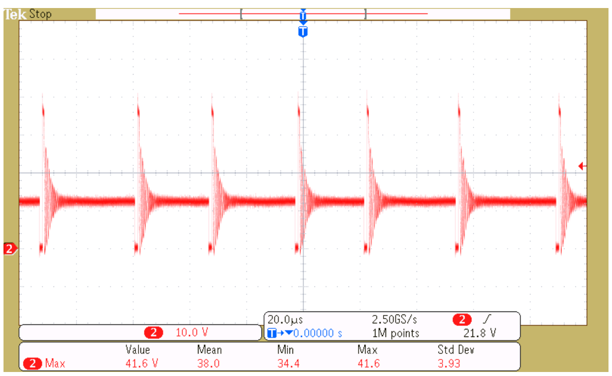


Figure 4-3. 12-V Input, no Load

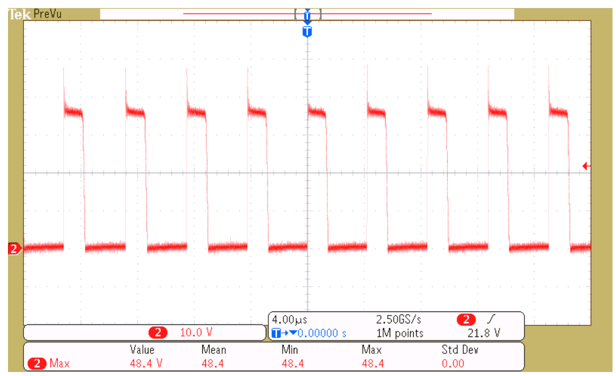


Figure 4-4. 12-V Input, VCC_T and VEE_B With 100-mA Load

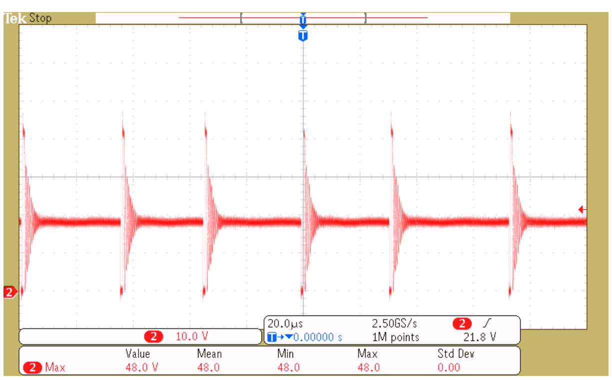


Figure 4-5. 18-V Input, no Load

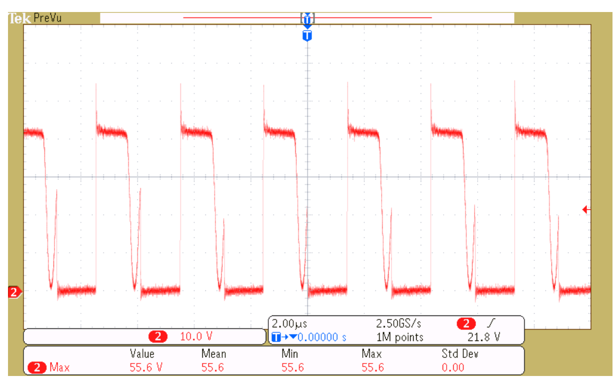
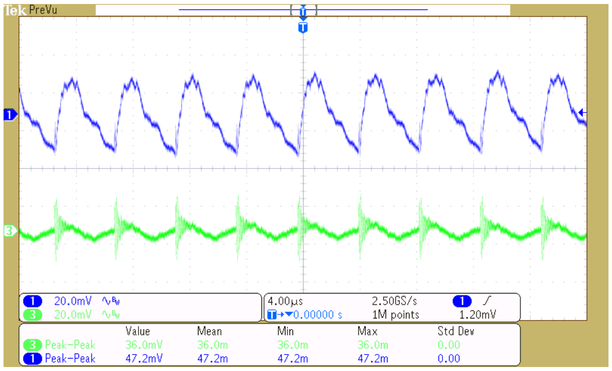


Figure 4-6. 18-V Input, VCC_T and VEE_B With 100-mA Load

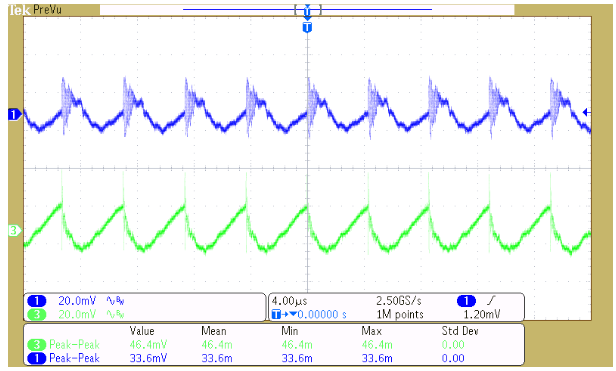
4.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures. The input voltage is set to 12 V.



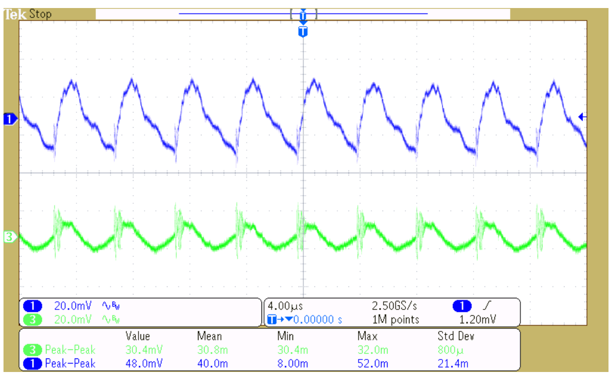
CH2: $V_{VCC\_T\_U}$ CH3: $V_{VEE\_T\_U}$

Figure 4-7. 12-V Input, VCC_T_U at Full Load, VEE_T_U at No Load



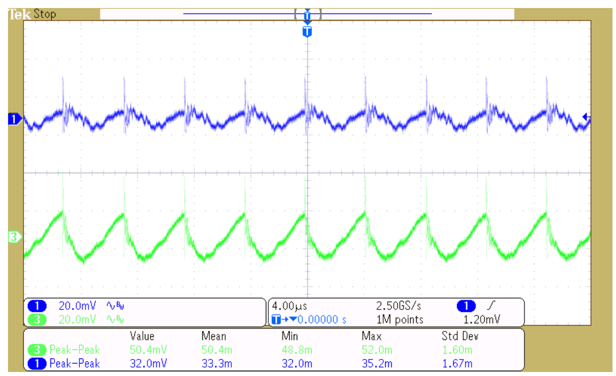
CH2: $V_{VCC\_B\_U}$ CH3: $V_{VEE\_B\_U}$

Figure 4-8. 12-V Input, VCC_B_U at no Load, VEE_B_U at Full Load



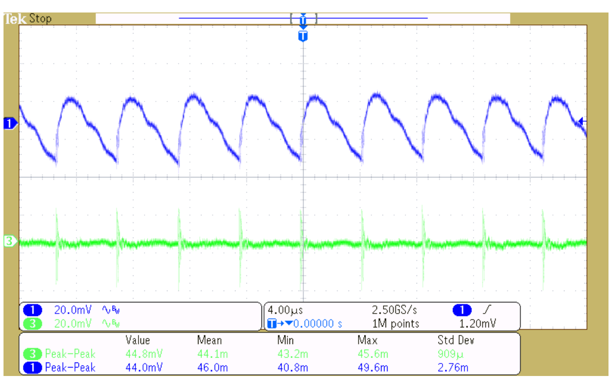
CH2: $V_{VCC\_T\_V}$ CH3: $V_{VEE\_T\_V}$

Figure 4-9. 12-V Input, VCC_T_V at Full Load, VEE_T_V at No Load



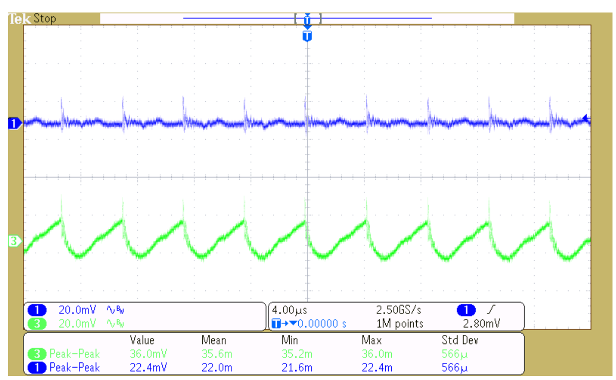
CH2: $V_{VCC\_B\_V}$ CH3: $V_{VEE\_B\_V}$

Figure 4-10. 12-V Input, VCC_B_V at No Load, VEE_B_V at Full Load



CH2: $V_{VCC\_T\_W}$ CH3: $V_{VEE\_T\_W}$

Figure 4-11. 12-V Input, VCC_T_W at Full Load, VEE_T_W at No Load

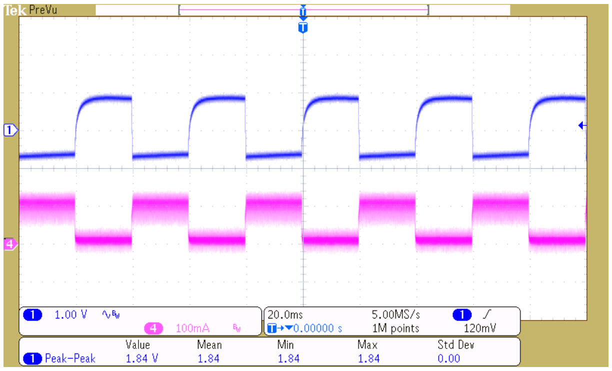


CH2: $V_{VCC\_B\_W}$ CH3: $V_{VEE\_B\_W}$

Figure 4-12. 12-V Input, VCC_B_W at No Load, VEE_B_W at Full Load

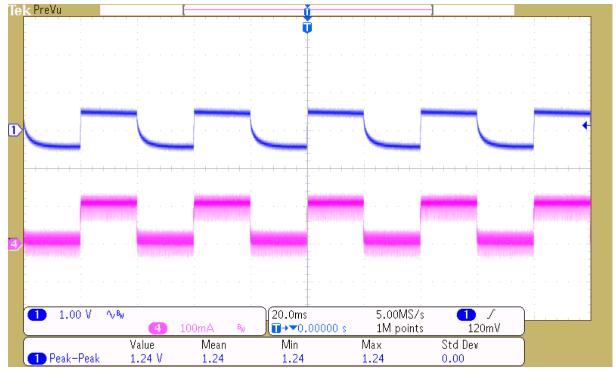
4.3 Load Transients

Load transient response is shown in the following figures. The slew rate is set to 0.1 A/µs.



CH1: $V_{VCC\_T\_U}$ CH4: $I_{VCC\_T\_U}$

Figure 4-13. 12-V Input, VCC Output 0 A → 0.1 A

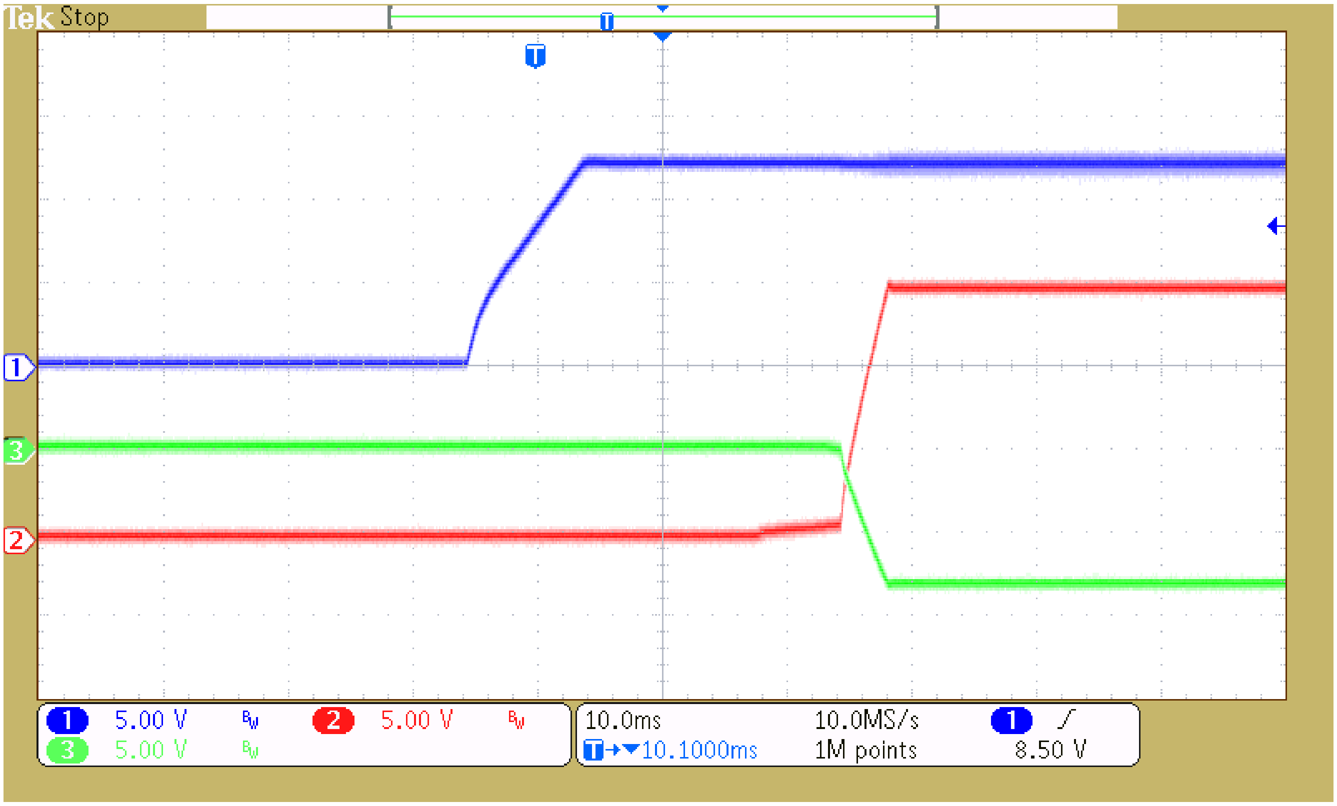


CH1: $V_{VEE\_B\_U}$ CH4: $I_{VEE\_B\_U}$

Figure 4-14. 12-V Input, VEE Output 0.1 A → 0 A

4.4 Start-up Sequence

Start-up shows the start-up behavior.

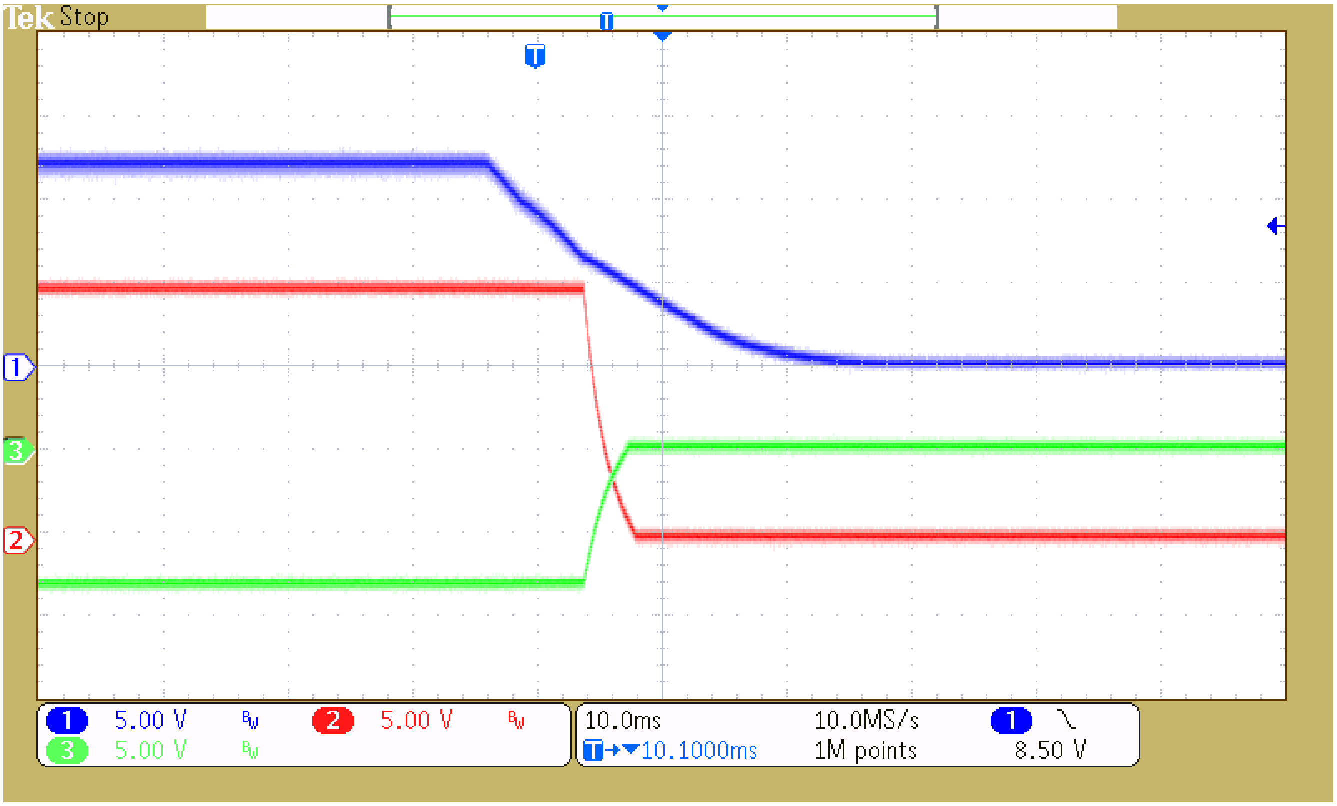


CH1: V_{IN} CH2: $V_{VCC\_T\_U}$ CH3: $V_{VEE\_B\_U}$

Figure 4-15. Start-up

4.5 Undervoltage Protection

Undervoltage shows the undervoltage protection.



CH1: V_{IN} CH2: $V_{VCC\_T\_U}$ CH3: $V_{VEE\_B\_U}$

Figure 4-16. Undervoltage