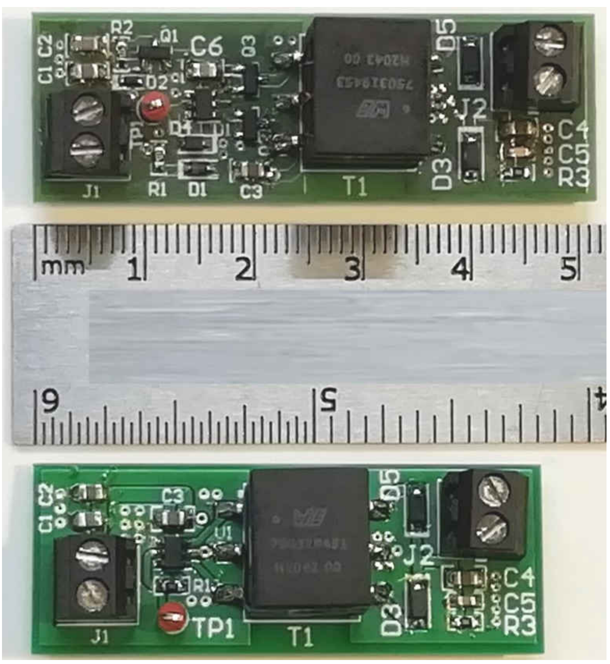
Test Report: PMP30911

3.8 V, 24 V to 6 V and 12 V, 1.8-W Isolated Push-Pull Reference Design

TEXAS INSTRUMENTS

Description

This reference design is an isolated push-pull, where *cascode* SOT-23 FETs are added for the 24-V version. This *cascode* connection extends input voltage range to 24-V_{IN} ±4% into 6 V or 12 V unregulated (open loop). With a selection of four different transformers, it is possible to get 6 V (at 300 mA) or 12 V (at 150 mA) from a 3.8-V or 24-V source.



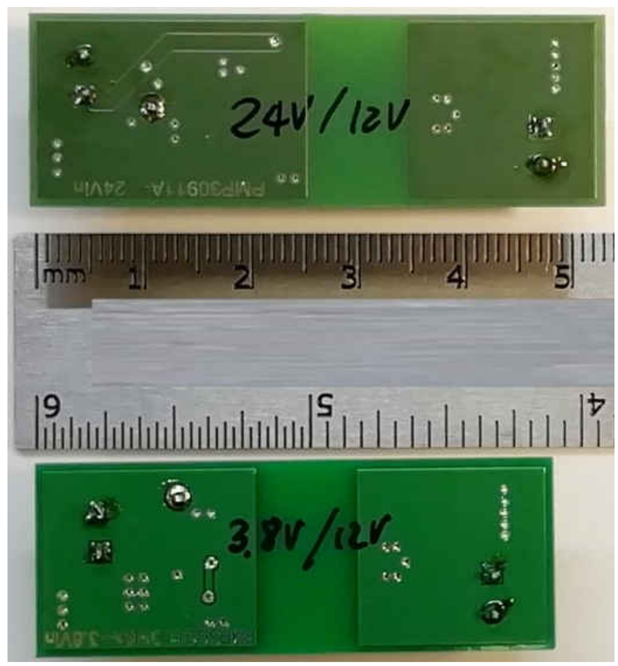
Top Photo

Features

- 3.8-V or 24-V input voltage versions
- 6-V or 12-V output voltage
- Rated for 150 mA or 300 mA according to the version selected

Applications

- Electricity meter



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage	3.8 V or 24 V ± 4 % (DC)
Output Voltage	6 V or 12 V ± 10 % (DC)
Output Current	150 mA or 300 mA

Table 1-2. Voltage Variants

V_{IN}, V_{OUT} Variants	Transformer Manufacturer	Transformer Part Number
3.8 V_{IN}, 12 V_{OUT} at 150 mA	Würth Elektronik	750319451
3.8 V_{IN}, 6 V_{OUT} at 300 mA	Würth Elektronik	750319452
24 V_{IN}, 12 V_{OUT} at 150 mA	Würth Elektronik	750319453
24 V_{IN}, 6 V_{OUT} at 300 mA	Würth Elektronik	750319454

1.2 Required Equipment

- 0 to 30 V, (min. 500 mA), constant voltage source (VS1)
- 0 to 15 V, (0 to 300 mA), constant-current electronic load
- Oscilloscope (minimum 100-MHz bandwidth)
- Current probe (minimum 100-kHz bandwidth)

1.3 Considerations

Connect the source VS1 to J1, pin 1 and 2.

Connect the load to J2, pin 1 and 2, set to CC mode.

Connect oscilloscope probes to Q2-drain and primary ground, as well as the anode of D5 and secondary ground.

1.4 Dimensions

The board dimensions are:

1. **3.8-V version**: 46.23 mm × 17.27 mm, height 11.9 mm
2. **24-V version**: 51.56 mm × 17.27 mm, height 11.9 mm

2 Testing and Results

2.1 Efficiency Graphs

The efficiency graphs, versus output current, are shown in Figure 2-1 through Figure 2-4. Four different versions were built: (1) 24 V_{IN} to 12 V_{OUT}, (2) 24 V_{IN} to 6 V_{OUT}, (3) 3.8 V_{IN} to 12 V_{OUT}, (4) 3.8 V_{IN} to 6 V_{OUT}.

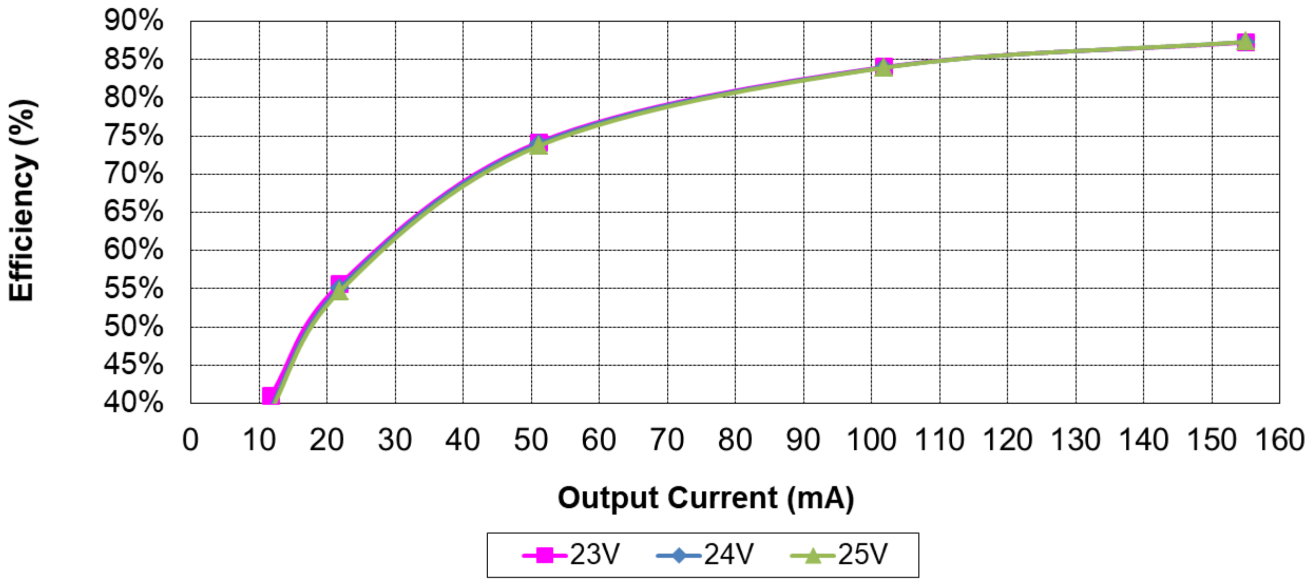


Figure 2-1. 24 V_{IN} to 12 V_{OUT} Version

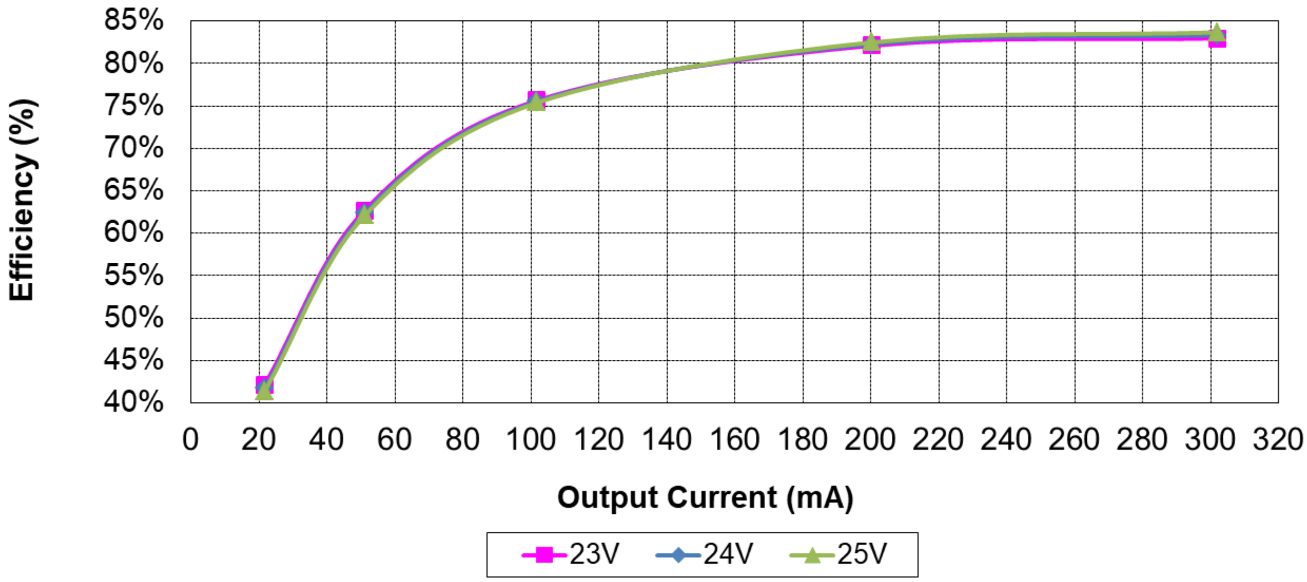


Figure 2-2. 24 V_{IN} to 6 V_{OUT} Version

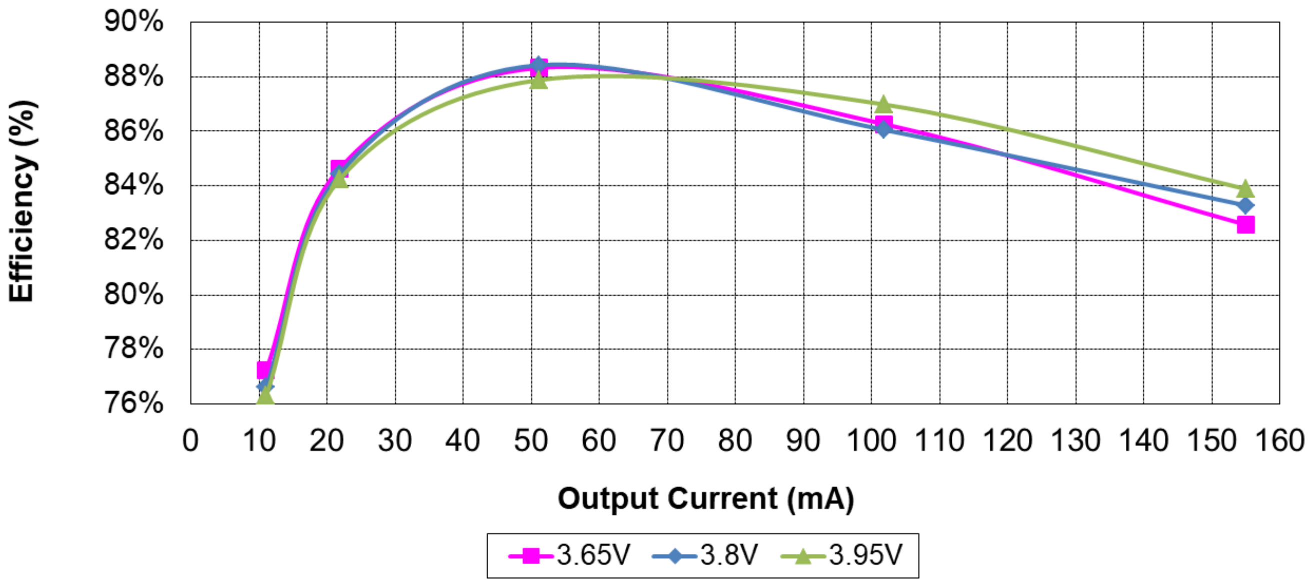


Figure 2-3. 3.8 V_{IN} to 12 V_{OUT} Version

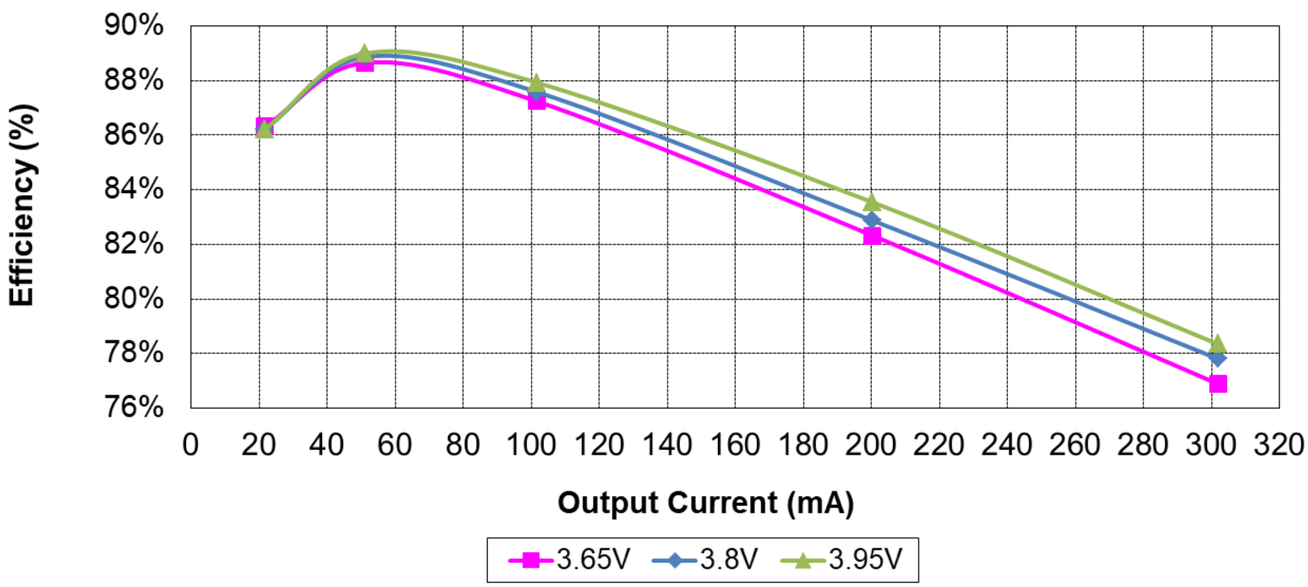


Figure 2-4. 3.8 V_{IN} to 6 V_{OUT} Version

2.2 Efficiency Data

The tables in this section detail the PMP30911 reference design efficiency data.

Table 2-1. 23 V_{IN} to 12 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
23.01	8.7	0.201	11.610	0	0.000	0.0%
23.00	14.3	0.328	11.500	11.7	0.135	40.97%
23.01	19.6	0.451	11.470	21.8	0.250	55.54%
23.01	34.1	0.784	11.380	51.1	0.582	74.19%
23.01	59.3	1.364	11.260	101.8	1.146	84.04%
23.00	86.0	1.977	11.130	155.0	1.725	87.26%

Table 2-2. 24 V_{IN} to 12 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
24.02	9.0	0.216	12.130	0	0.000	0.0%
24.01	14.5	0.348	12.030	11.1	0.134	38.41%
24.01	19.8	0.475	11.980	21.9	0.262	55.08%
24.02	34.3	0.823	11.900	51.2	0.609	74.02%
24.01	59.5	1.428	11.770	101.9	1.199	83.98%
24.00	86.2	2.068	11.650	155.0	1.806	87.32%

Table 2-3. 25 V_{IN} to 12 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
25.02	9.2	0.229	12.660	0	0.000	0.0%
25.01	14.7	0.368	12.550	11.1	0.140	38.00%
25.00	20.0	0.500	12.500	21.9	0.274	54.68%
25.01	34.5	0.862	12.420	51.2	0.636	73.74%
25.00	59.7	1.492	12.290	101.9	1.252	83.95%
25.01	86.4	2.160	12.170	155.0	1.886	87.33%

Table 2-4. 23 V_{IN} to 6 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
23.02	7.9	0.181	6.182	0	0.000	0.0%
23.02	13.4	0.309	6.006	21.6	0.130	42.06%
23.01	21.0	0.483	5.937	51.0	0.303	62.64%
23.00	34.2	0.786	5.842	101.8	0.595	75.63%
23.02	60.2	1.385	5.673	200.4	1.137	82.10%
23.00	87.4	2.010	5.522	301.9	1.667	82.96%

Table 2-5. 24 V_{IN} to 6 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
24.01	8.0	0.193	6.457	0	0.000	0.0%
24.00	13.6	0.327	6.278	21.7	0.136	41.73%
24.00	21.2	0.509	6.213	51.1	0.317	62.40%
24.01	34.4	0.825	6.121	101.8	0.623	75.51%
24.00	60.3	1.448	5.945	200.4	1.191	82.30%
24.00	87.5	2.101	5.799	301.9	1.751	83.33%

Table 2-6. 25 V_{IN} to 6 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
25.00	8.2	0.205	6.736	0	0.000	0.0%
25.00	13.8	0.345	6.560	21.8	0.143	41.42%
25.00	21.4	0.534	6.492	51.1	0.332	62.09%
25.02	34.5	0.864	6.398	101.8	0.651	75.38%
25.00	60.5	1.512	6.223	200.4	1.247	82.48%
25.01	87.7	2.193	6.078	301.9	1.835	83.66%

Table 2-7. 3.65 V_{IN} to 12 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
3.65	9.1	0.033	11.850	0	0.000	0.0%
3.67	45.7	0.168	11.740	11.1	0.130	77.23%
3.65	81.4	0.297	11.550	21.8	0.252	84.62%
3.63	178.9	0.650	11.230	51.1	0.574	88.33%
3.64	347.7	1.266	10.714	101.9	1.092	86.27%
3.65	523.1	1.911	10.183	155.0	1.578	82.58%

Table 2-8. 3.8 V_{IN} to 12 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
3.81	9.6	0.037	12.380	0	0.000	0.0%
3.80	46.1	0.175	12.160	11.0	0.134	76.60%
3.81	81.9	0.312	12.060	21.8	0.263	84.43%
3.81	179.4	0.683	11.818	51.1	0.604	88.43%
3.80	348.1	1.324	11.180	101.9	1.139	86.05%
3.81	523.0	1.993	10.707	155.0	1.660	83.29%

Table 2-9. 3.95 V_{IN} to 12 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
3.94	9.9	0.039	12.810	0	0.000	0.0%
3.94	46.4	0.183	12.640	11.1	0.140	76.30%
3.96	82.2	0.325	12.560	21.8	0.274	84.23%
3.95	179.8	0.709	12.200	51.1	0.623	87.88%
3.95	348.5	1.377	11.751	101.9	1.197	86.99%
3.95	523.1	2.068	11.194	155.0	1.735	83.89%

Table 2-10. 3.65 V_{IN} to 6 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
3.656	3.5	0.013	6.277	0	0.000	0.0%
3.648	42.0	0.153	6.091	21.7	0.132	86.32%
3.646	94.2	0.344	5.960	51.1	0.305	88.66%
3.650	184.4	0.673	5.768	101.8	0.587	87.24%
3.658	359.8	1.316	5.407	200.4	1.084	82.32%
3.653	538.5	1.967	5.010	301.9	1.513	76.89%

Table 2-11. 3.8 V_{IN} to 6 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
3.809	3.6	0.014	6.556	0	0.000	0.0%
3.802	42.2	0.161	6.367	21.7	0.138	86.23%
3.813	94.4	0.360	6.259	51.1	0.320	88.87%
3.801	184.6	0.702	6.037	101.8	0.615	87.58%
3.800	360.0	1.368	5.657	200.4	1.134	82.88%
3.808	538.5	2.051	5.285	301.9	1.596	77.81%

Table 2-12. 3.95 V_{IN} to 6 V_{OUT}

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)
3.948	3.8	0.015	6.805	0	0.000	0.0%
3.956	42.3	0.167	6.643	21.7	0.144	86.22%
3.957	94.6	0.374	6.516	51.1	0.333	89.00%
3.960	184.8	0.732	6.320	101.8	0.643	87.93%
3.969	360.1	1.429	5.958	200.4	1.194	83.54%
3.949	539.7	2.131	5.531	301.9	1.670	78.35%

2.3 Output Voltage Regulation

Figure 2-5 through Figure 2-8 show the PMP30911 output voltage regulation waveforms.

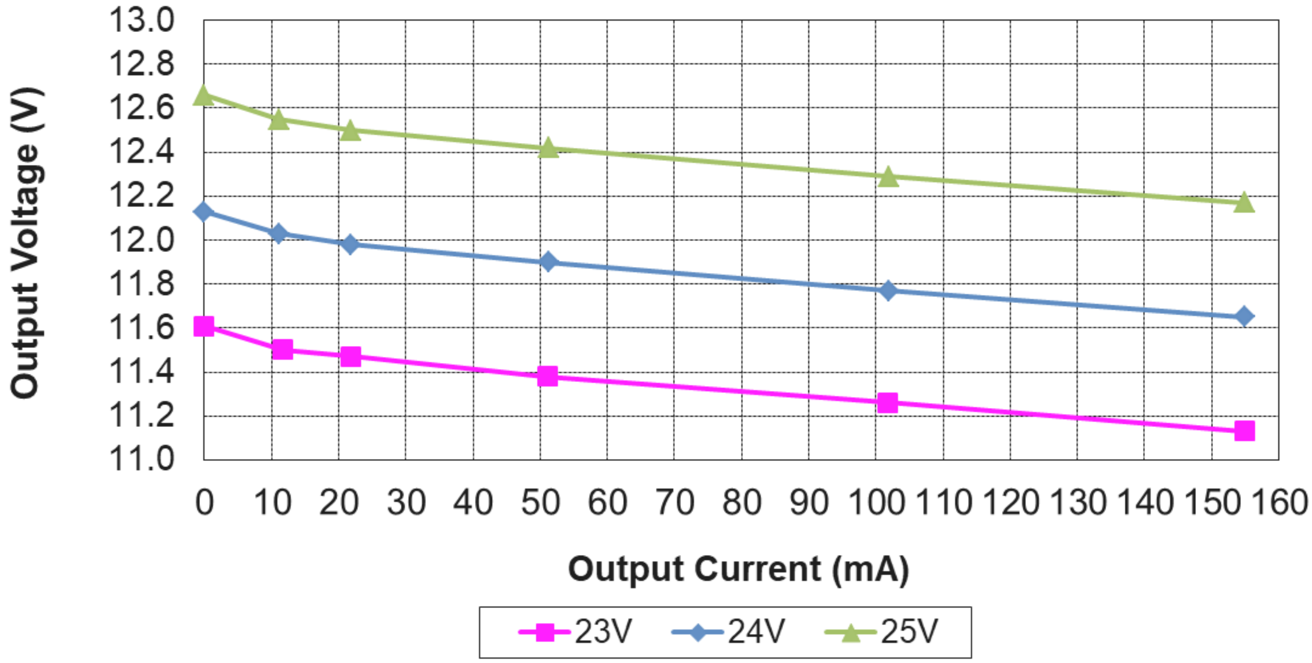


Figure 2-5. 24 V_{IN} to 12 V_{OUT} Version

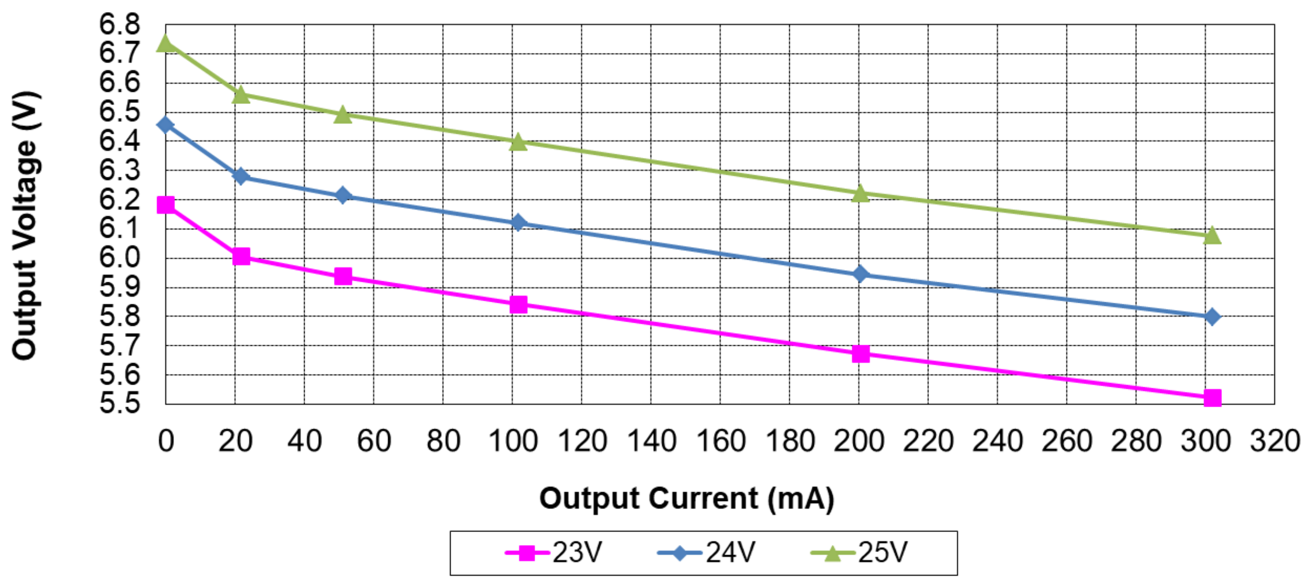


Figure 2-6. 24 V_{IN} to 6 V_{OUT} Version

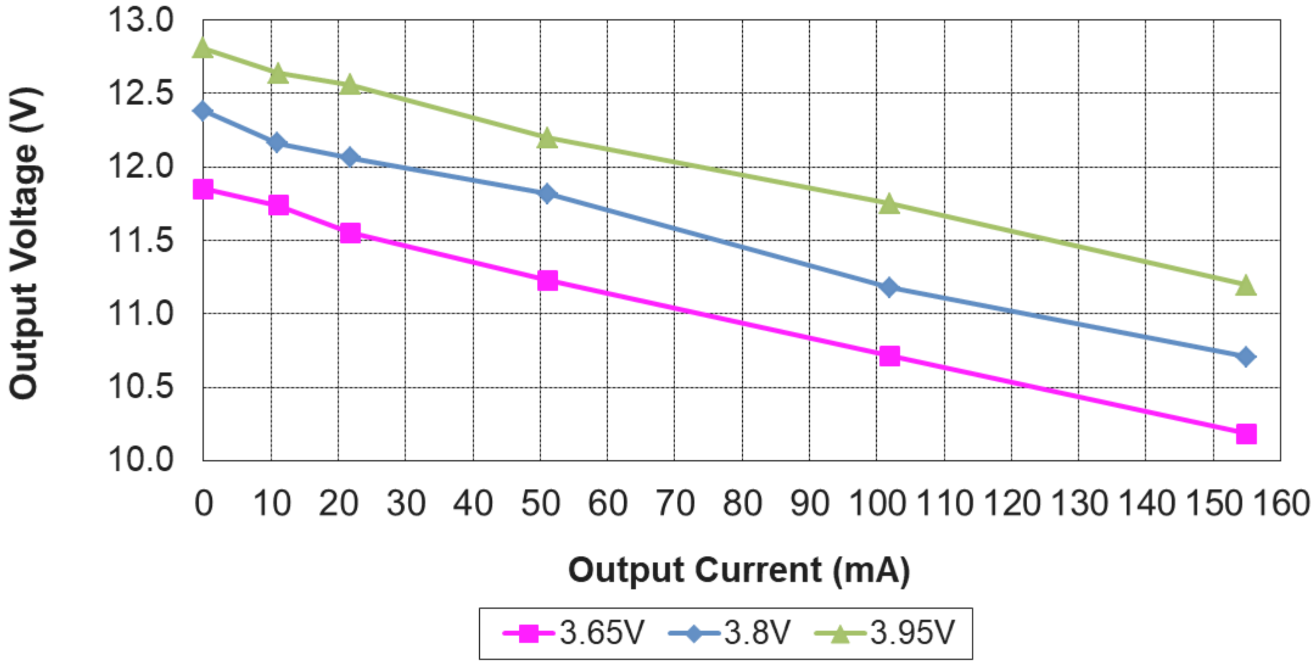


Figure 2-7. 3.8 V_{IN} to 12 V_{OUT}

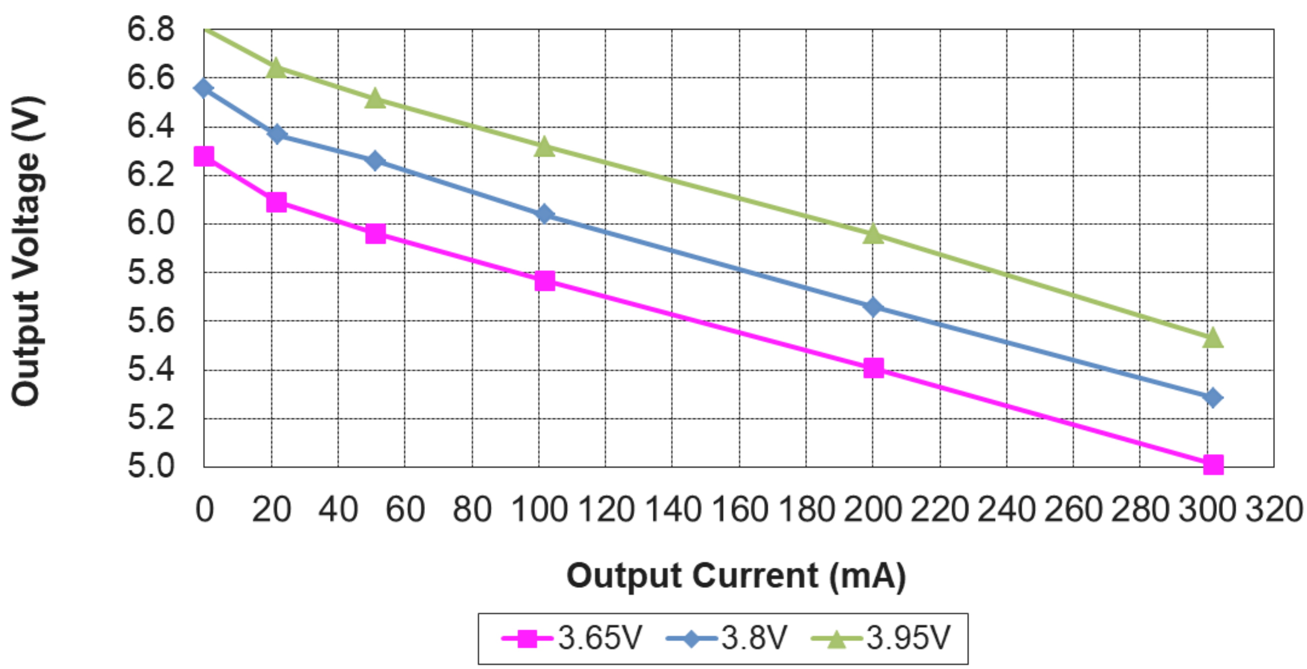
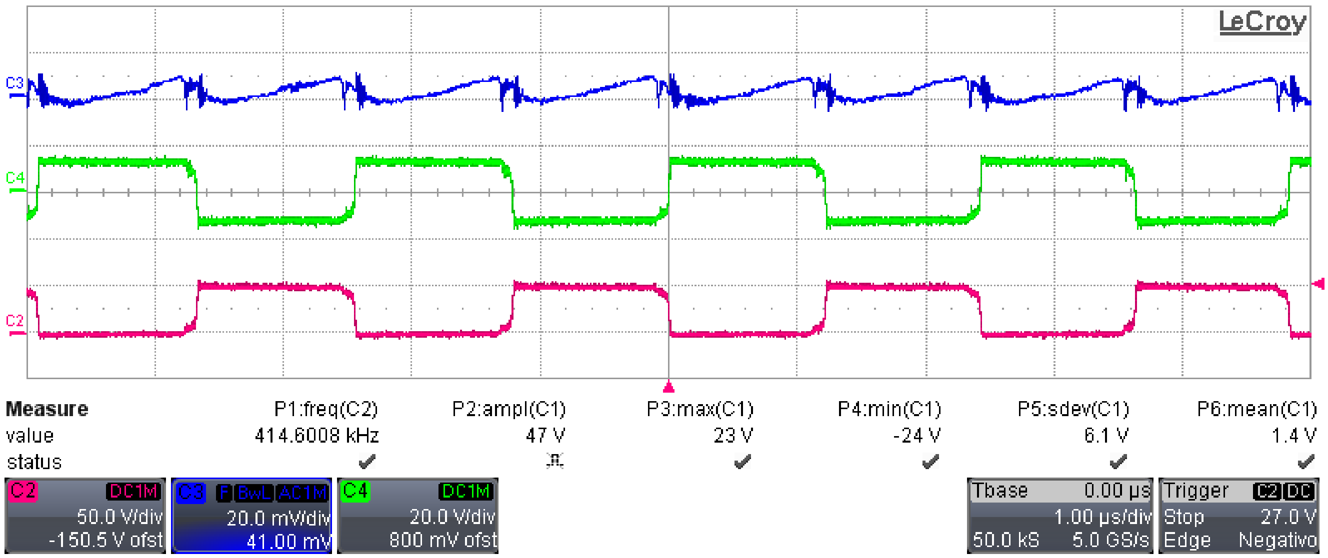


Figure 2-8. 3.8 V_{IN} to 6 V_{OUT}

3 Waveforms

3.1 Switching and Output Voltage Ripple

The switching waveforms in Figure 3-1 through Figure 3-4 were measured by supplying the converters respectively at 3.8 V and 24 V in full load condition (300 mA and 150 mA).

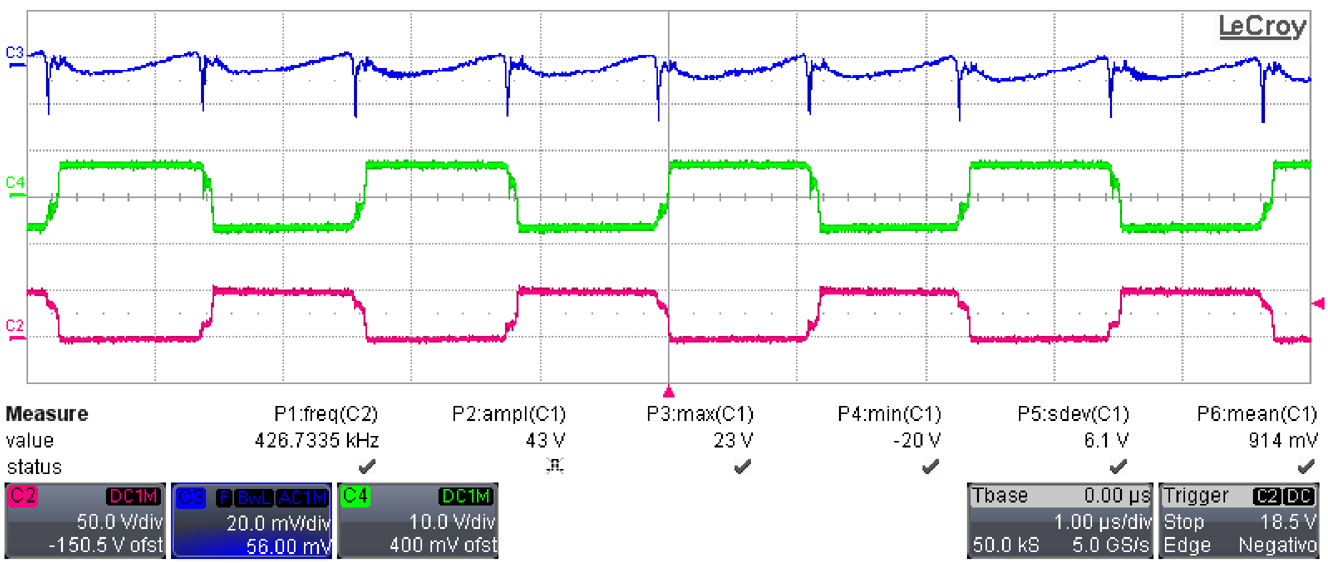


C2: VDS voltage of Q2 (50 V/div, 1 µs/div, no BWL)

C3: Output voltage (20 mV/div, 20-MHz BWL, AC coupling)

C4: Voltage on D5 anode (20 V/div, no BWL)

Figure 3-1. 24 V_{IN} to 12 V_{OUT} Version

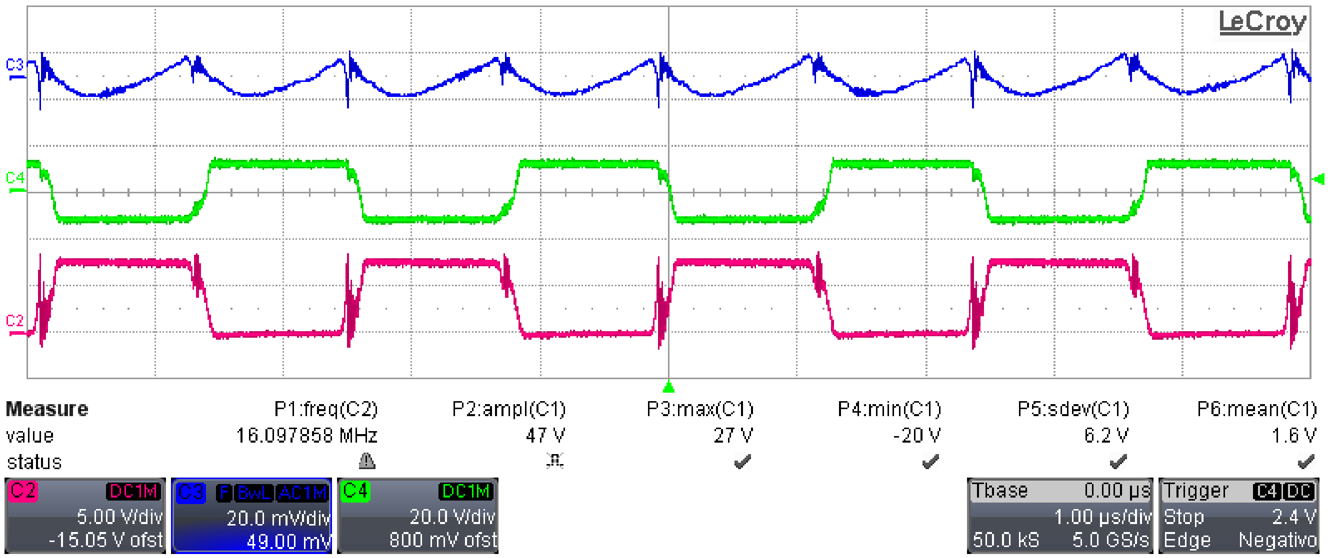


C2: VDS voltage of Q2 (50 V/div, 1 µs/div, no BWL)

C3: Output voltage (20 mV/div, 20-MHz BWL, AC coupling)

C4: Voltage on D5 anode (10 V/div, no BWL)

Figure 3-2. 24 V_{IN} to 6 V_{OUT} Version

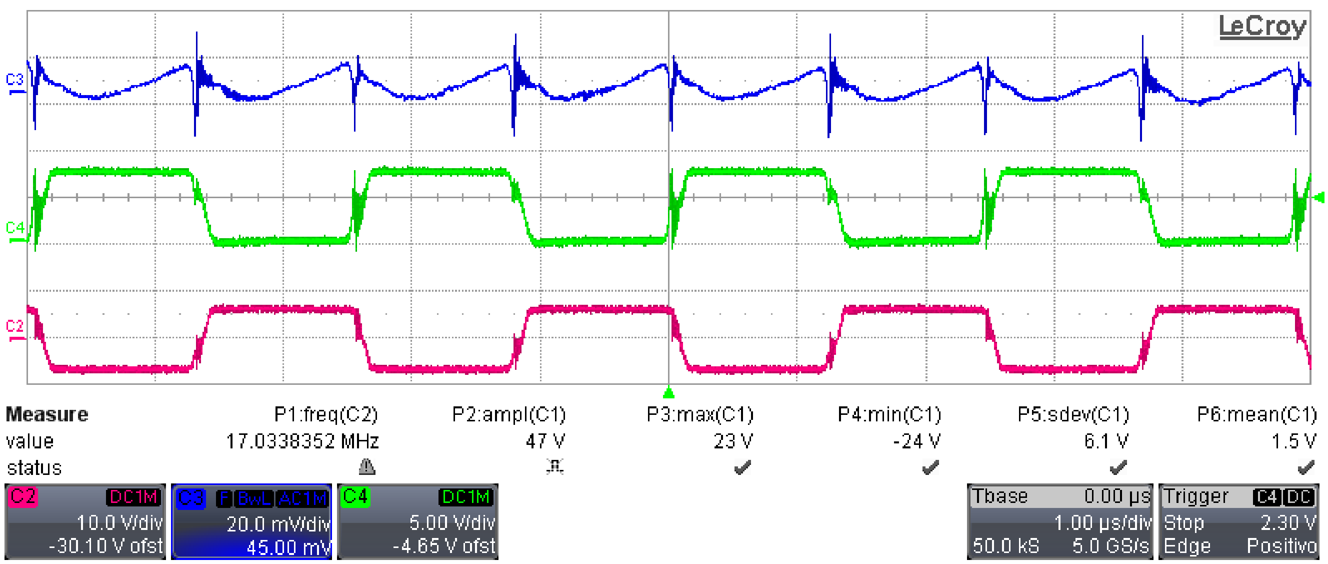


C2: VDS voltage of Q2 (5 V/div, 1 µs/div, no BWL)

C3: Output voltage (20 mV/div, 20-MHz BWL, AC coupling)

C4: Voltage on D5 anode (20 V/div, no BWL)

Figure 3-3. 3.8 V_{IN} to 12 V_{OUT}



C2: Voltage on D5 anode (10 V/div, 1 µs/div, no BWL)

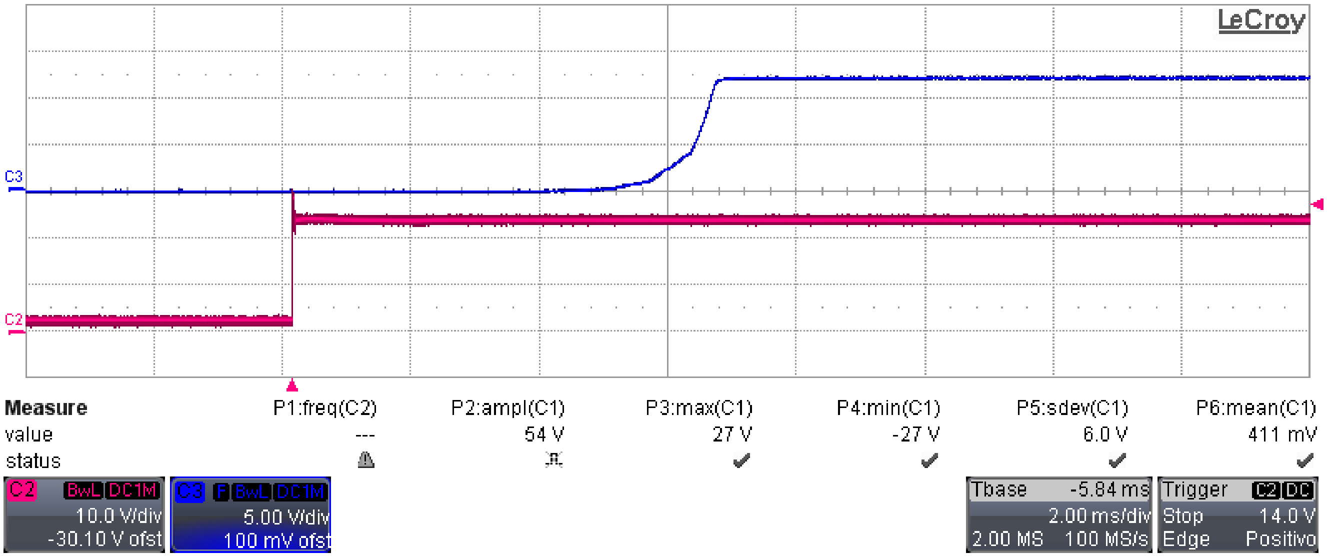
C3: Output voltage (20 mV/div, 20-MHz BWL, AC coupling)

C4: VDS voltage of Q2 (5 V/div, no BWL)

Figure 3-4. 3.8 V_{IN} to 6 V_{OUT}

3.2 Start-Up

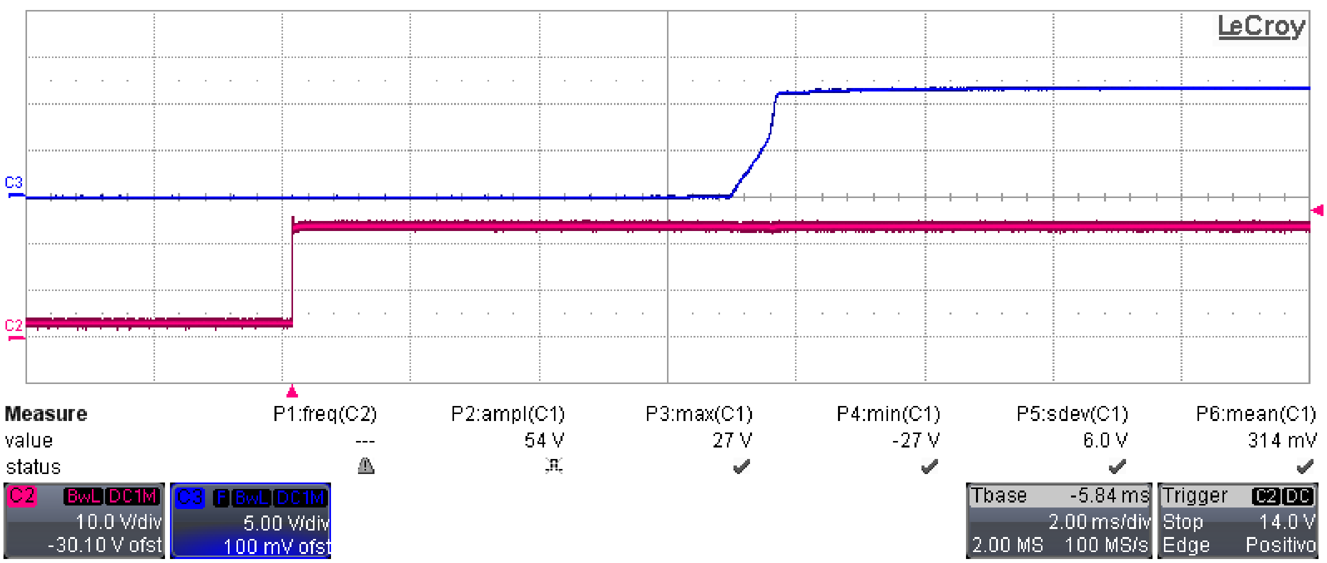
The output voltage versus input voltage behavior was measured and is shown in Figure 3-12 through Figure 3-12.



C2: Input voltage (10 V/div, 2 ms/div, 20-MHz BWL)

C3: Output voltage (5 V/div, 20-MHz BW)

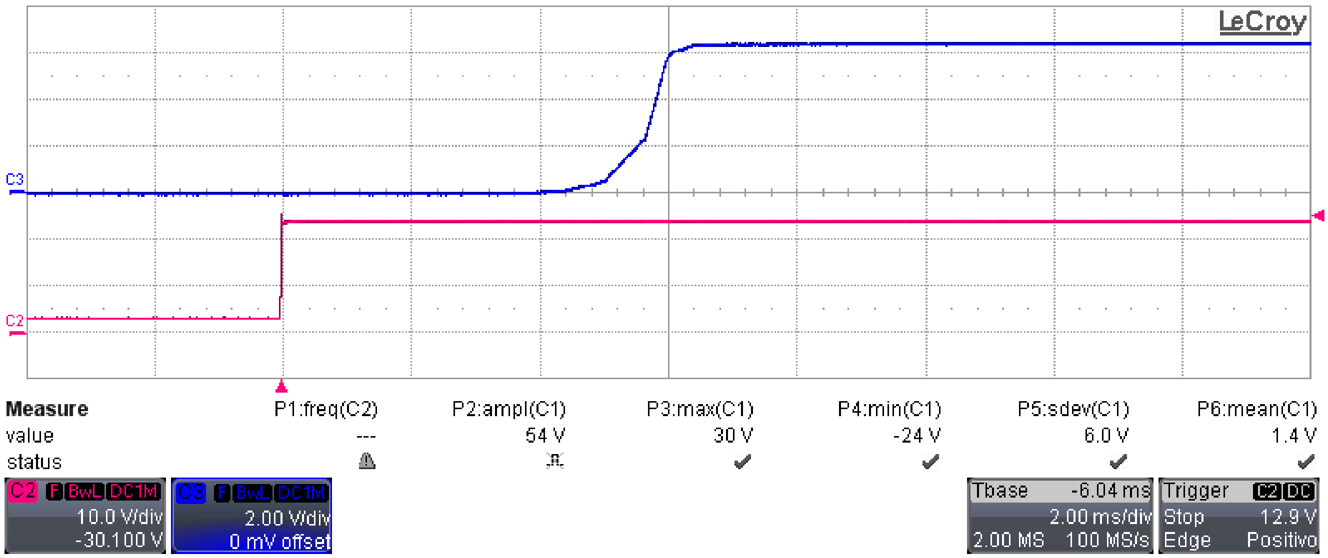
Figure 3-5. 24 V_{IN} to 12 V_{OUT} Version, No Load Applied



C2: Input voltage (10 V/div, 2 ms/div, 20-MHz BWL)

C3: Output voltage (5 V/div, 20-MHz BW)

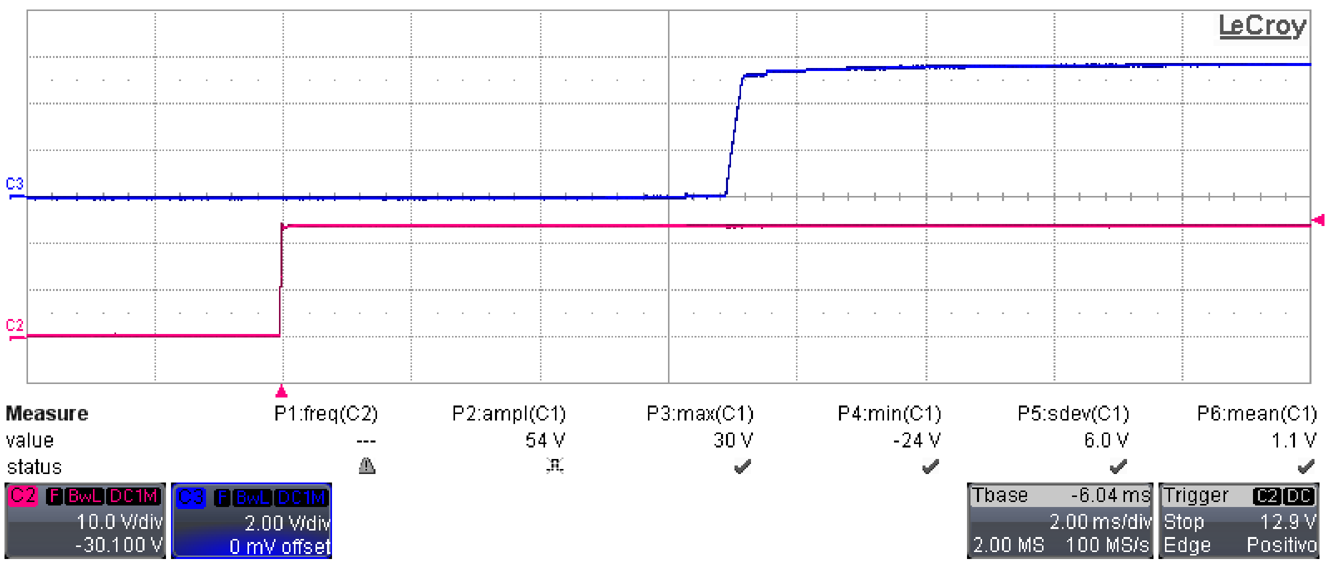
Figure 3-6. 24 V_{IN} to 12 V_{OUT} Version, Full Load Condition



C2: Input voltage (10 V/div, 2 ms/div, 20-MHz BWL)

C3: Output voltage (2 V/div, 20-MHz BW)

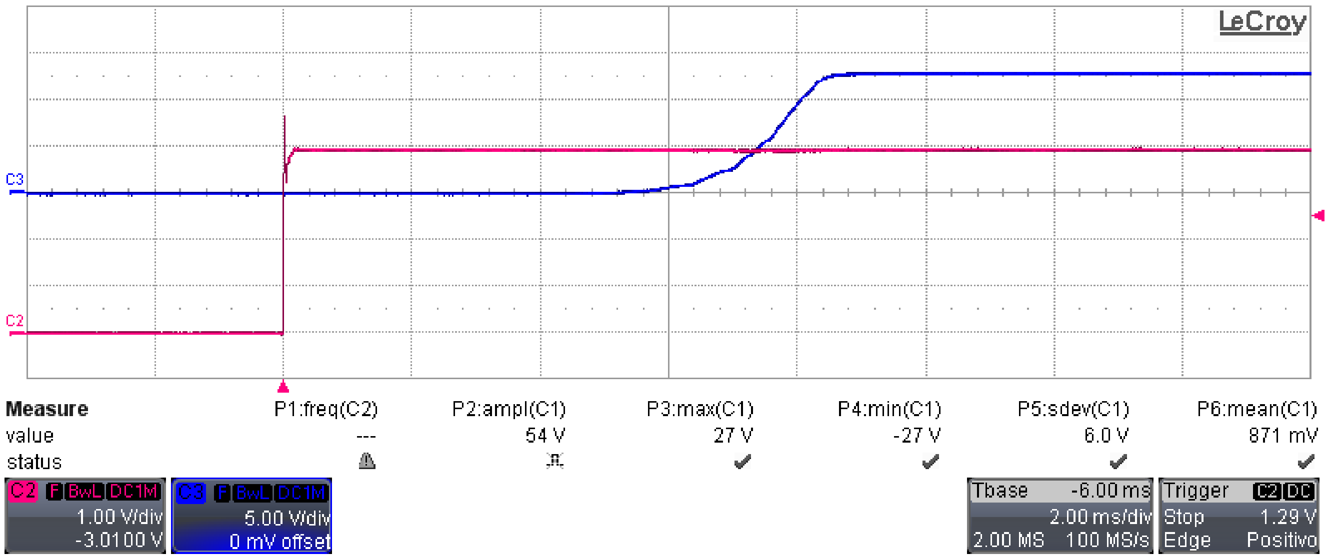
Figure 3-7. 24 V_{IN} to 6 V_{OUT}, No Load Applied



C2: Input voltage (10 V/div, 2 ms/div, 20-MHz BWL)

C3: Output voltage (2 V/div, 20-MHz BW)

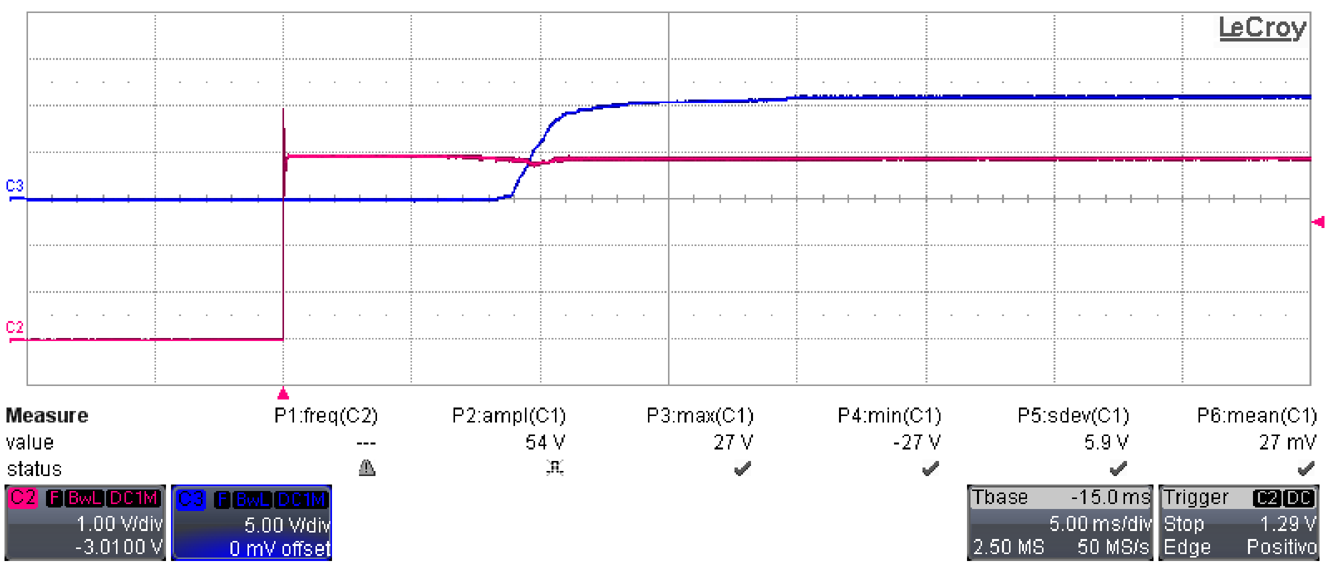
Figure 3-8. 24 V_{IN} to 6 V_{OUT}, Full Load Condition



C2: Input voltage (1 V/div, 2 ms/div, 20 - BWL)

C3: Output voltage (5 V/div, 20-MHz BW)

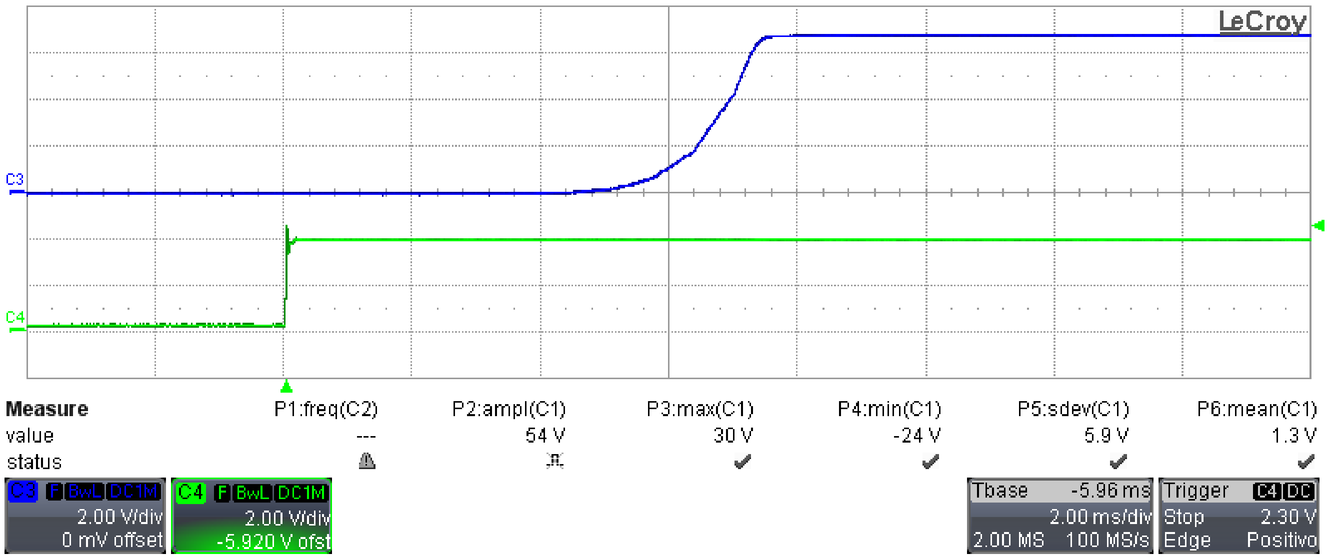
Figure 3-9. 3.8 V_{IN} to 12 V_{OUT} Version, No Load Applied



C2: Input voltage (1 V/div, 5 ms/div, 20-MHz BWL)

C3: Output voltage (5 V/div, 20-MHz BW)

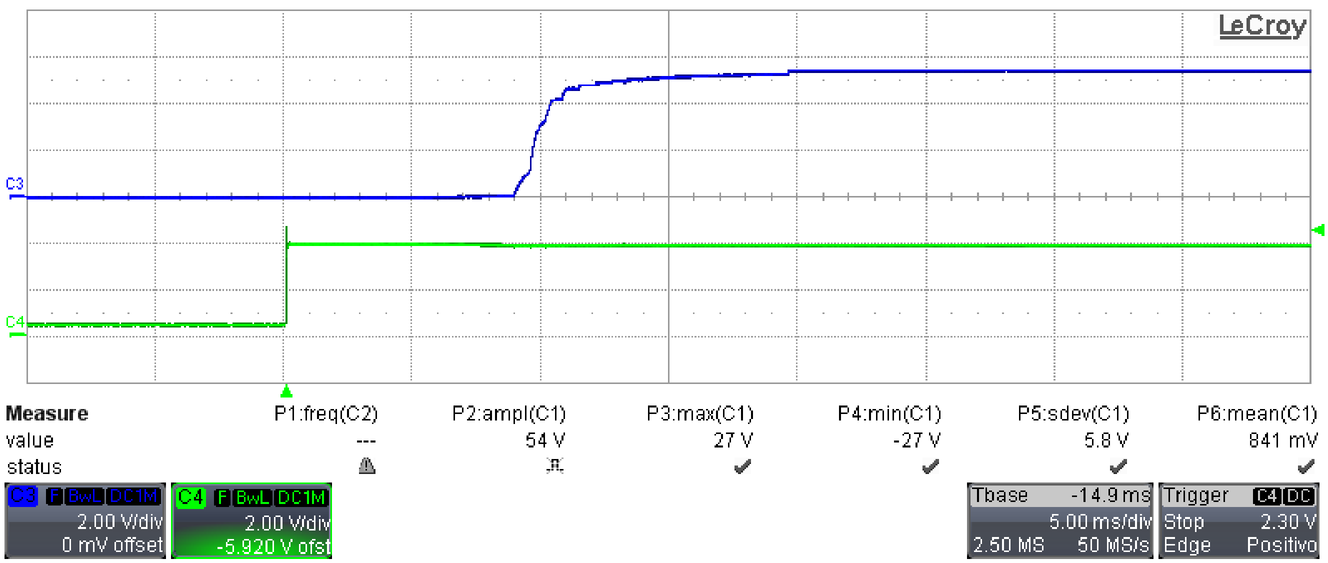
Figure 3-10. 3.8 V_{IN} to 12 V_{OUT} Version, Full Load Condition



C3: Output voltage (2 V/div, 2 ms/div, 20-MHz BW)

C4: Input voltage (2 V/div, 20-MHz BWL)

Figure 3-11. 3.8 V_{IN} to 6 V_{OUT} Version, No Load Applied



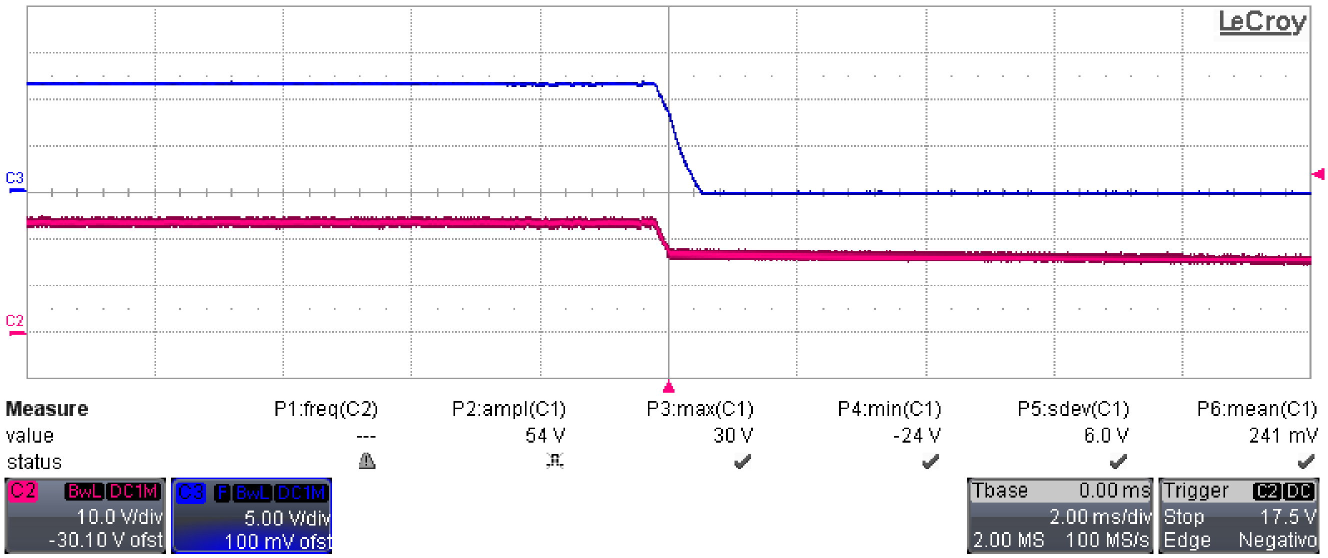
C3: Output voltage (2 V/div, 5 ms/div, 20-MHz BW)

C4: Input voltage (2 V/div, 20-MHz BWL)

Figure 3-12. 3.8 V_{IN} to 6 V_{OUT}, Full Load Condition

3.3 Shutdown

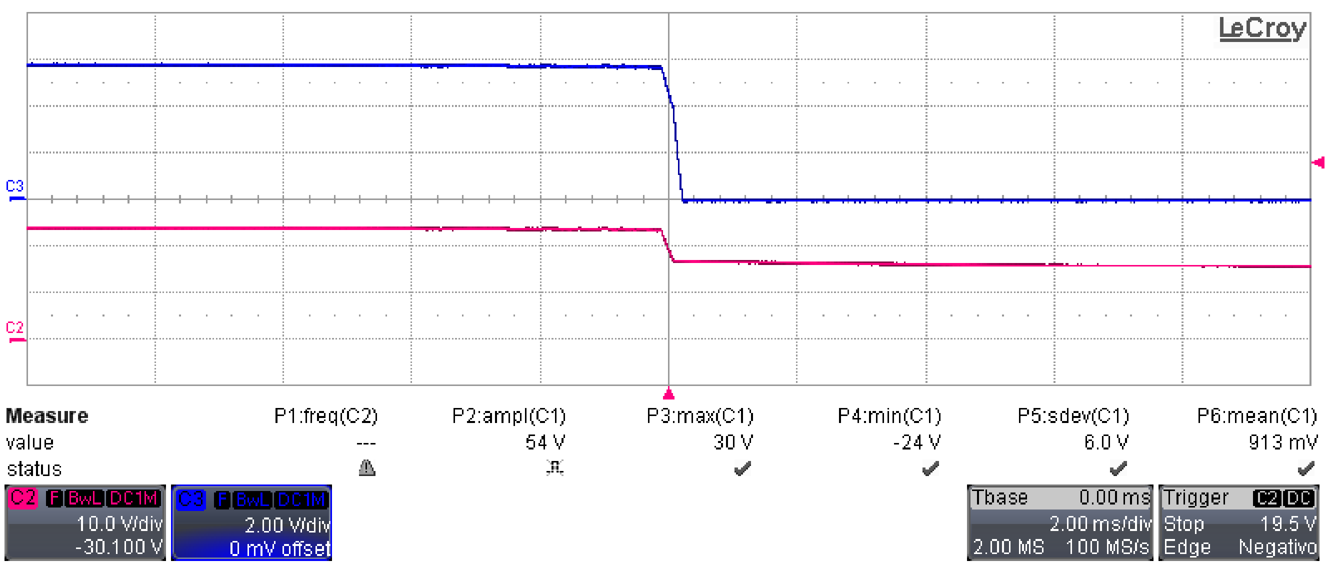
The output voltage versus input voltage behavior, during shut down and always full load, was measured and shown in Figure 3-13 through Figure 3-16.



C2: Input voltage (10 V/div, 2 ms/div, 20-MHz BWL)

C3: Output voltage (5 V/div, 20-MHz BW)

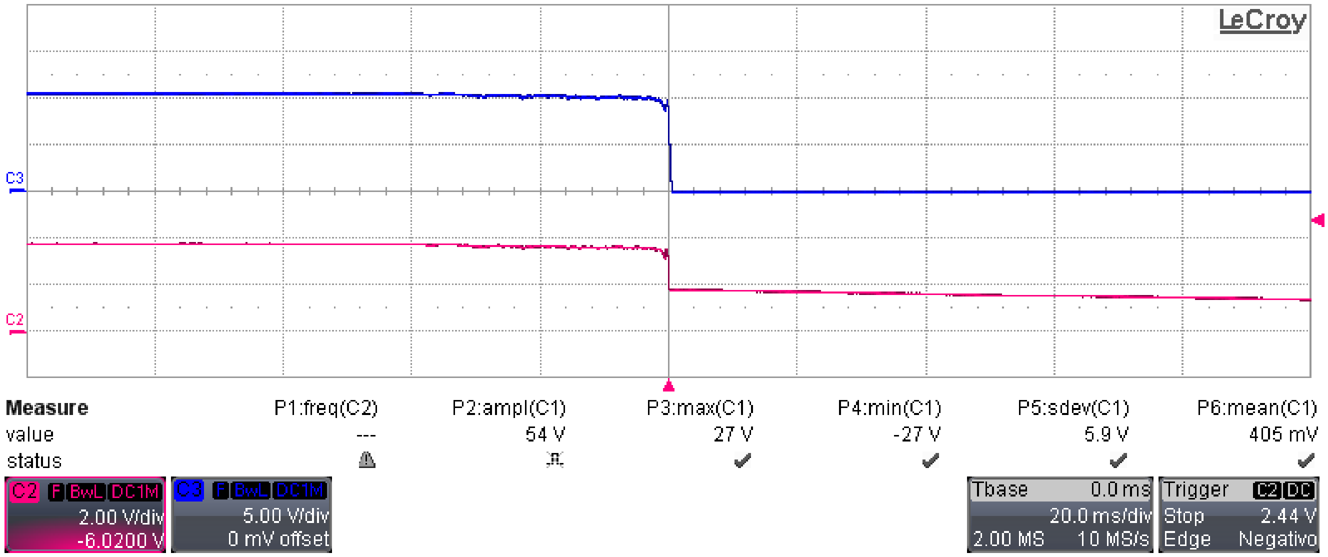
Figure 3-13. 24 V_{IN} to 12 V_{OUT} Version



C2: Input voltage (10 V/div, 2 ms/div, 20-MHz BWL)

C3: Output voltage (2 V/div, 20-MHz BW)

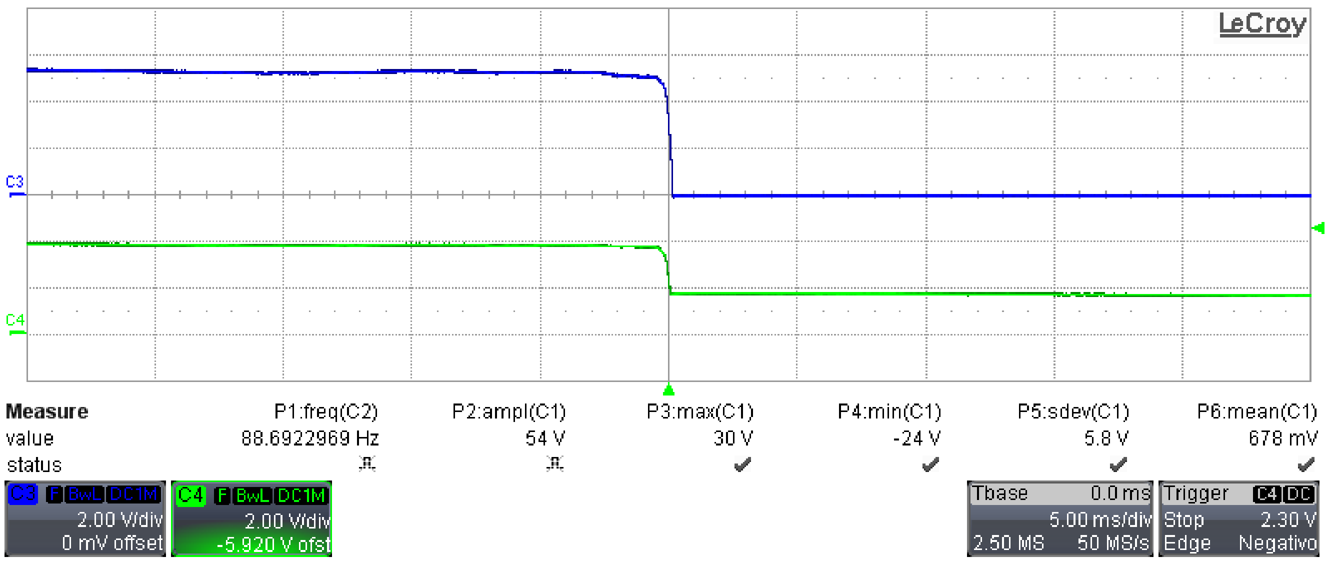
Figure 3-14. 24 V_{IN} to 6 V_{OUT} Version



C2: Input voltage (2 V/div, 20 ms/div, 20-MHz BWL)

C3: Output voltage (5 V/div, 20-MHz BW)

Figure 3-15. 3.8 V_{IN} to 12 V_{OUT} Version



C3: Output voltage (2 V/div, 5 ms/div, 20-MHz BW)

C4: Input voltage (2 V/div, 20-MHz BWL)

Figure 3-16. 3.8 V_{IN} to 6 V_{OUT} Version

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265