Test Report: PMP23240

3-W, Dual 18-V Output Bias Supply Reference Design

Description

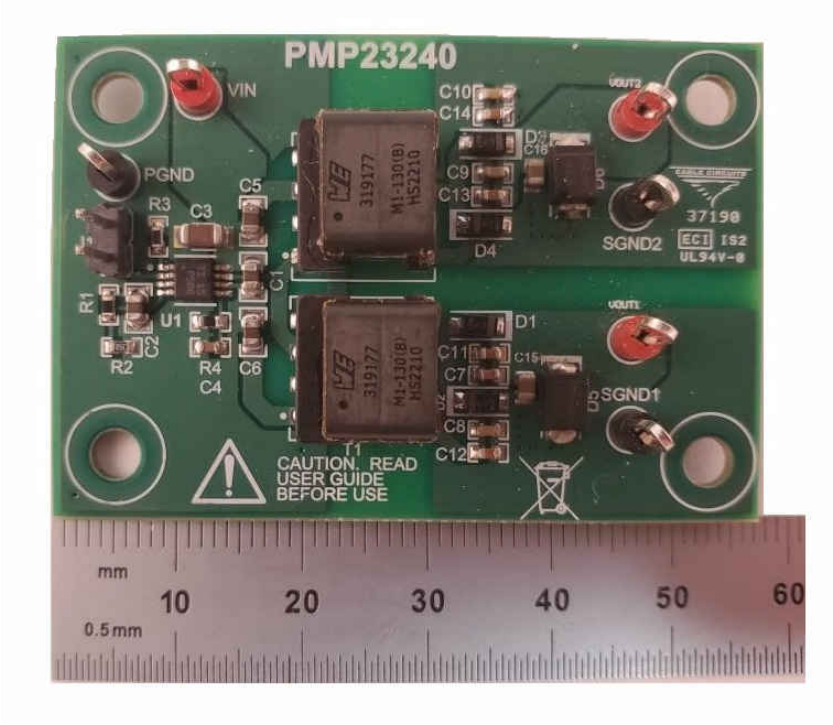
This reference design uses a single UCC25800-Q1 device to drive two LLC transformers with 600-kHz switching frequency. This design uses the 750319177 transformer. The 750319177 is an off-the-shelf, catalog transformer featuring a low interwinding capacitance of 0.68 pF (typical) which is beneficial for minimizing common-mode current in gate driver bias applications with high slew rates. This design generates two isolated 18-V rails. Each output can be loaded to 1.5 W.

Features

- 78.8% peak efficiency
- Catalog transformer with low interwinding capacitance of 0.68 pF
- Input power limiting
- Converters can be paralleled for increased power

Applications

- Single phase online UPS



Top Photo

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage	+12-V input, ±5%
Output Voltage	+18 V, +18 V
Max Current	85 mA per output

1.2 Required Equipment

- AC power supply
- Electronic load
- Digital multimeter
- Oscilloscope

1.3 Considerations

- Unless noted, all waveforms were captured at full load with a 12-V_{DC} input

1.4 Dimensions

The PCB is a two-layer, 1-oz per layer design. The dimensions are 1.5 in × 2.21 in, with a maximum component height of 0.47 in.

1.5 Test Setup

- DC source capable of 25 V, 1 A
- Resistive loads rated for at least 1 W

2 Testing and Results

2.1 Load Regulation Graph

Figure 2-1 shows the respective positive and negative voltage regulation graphs.

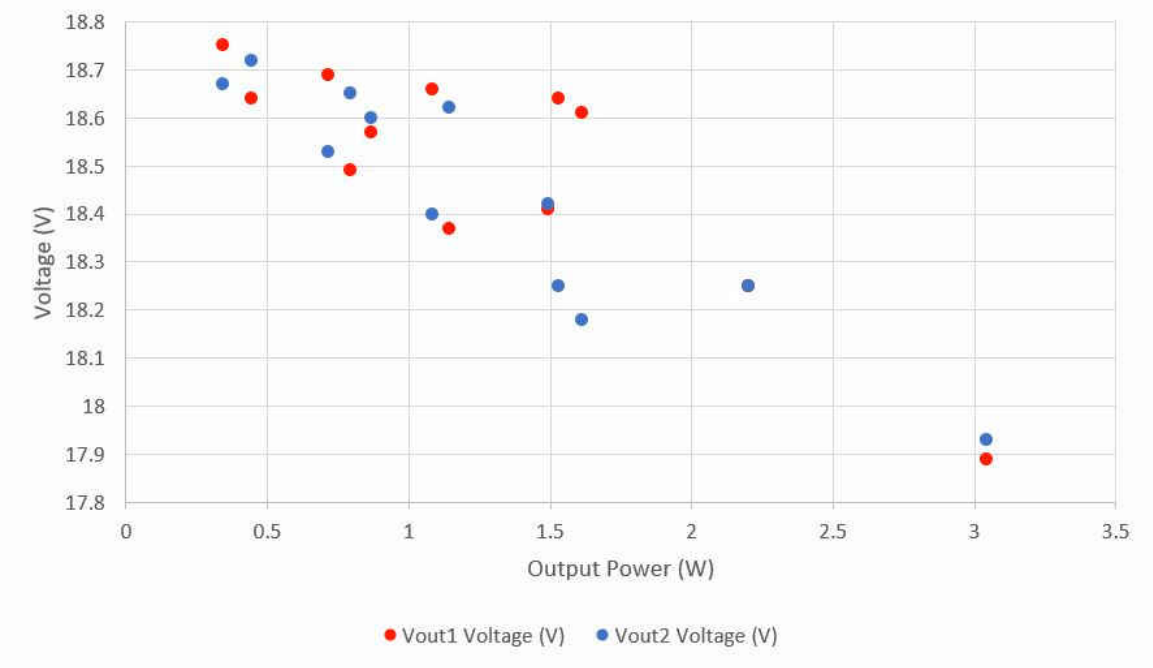


Figure 2-1. Voltage Regulation

2.2 Efficiency Graphs

Figure 2-2 shows the efficiency graph.

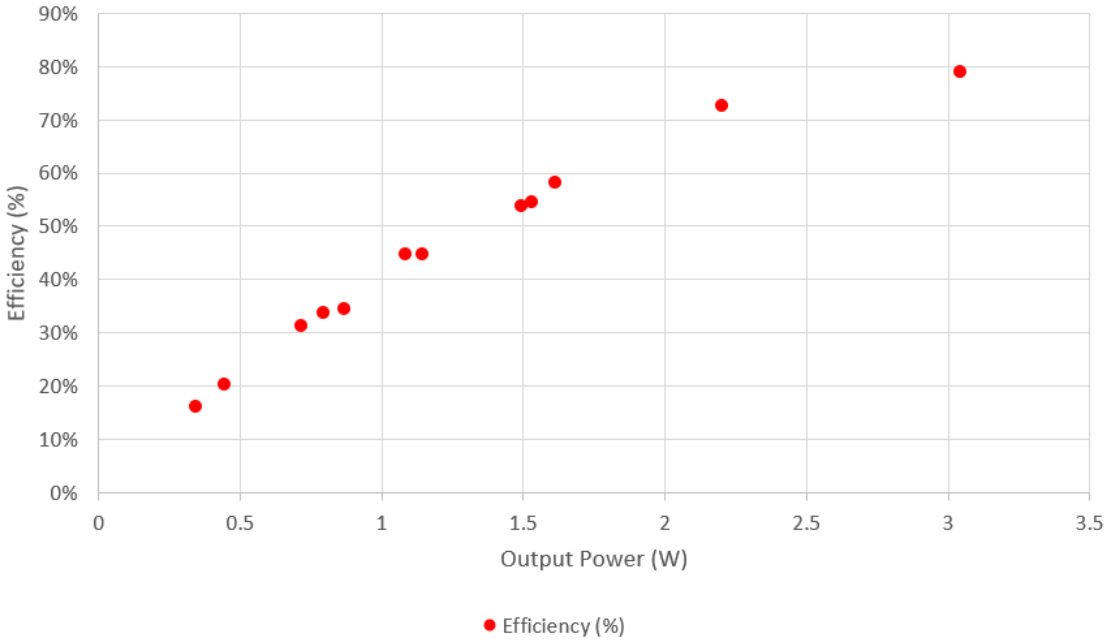


Figure 2-2. Efficiency Graph

2.3 Efficiency Data

Efficiency data is shown in the following table.

Table 2-1. Efficiency Data

Input Voltage Setting	Input Current (mA)	V_{OUT1} Voltage (V)	V_{OUT1} Current (mA)	V_{OUT2} Voltage (V)	V_{OUT2} Current (mA)	Total Input Power (W)	Total Output Power (W)	Efficiency (%)	Power Loss (W)
12 V_{DC}	183.3	18.64	23.79	18.72	0.075	2.1996	0.4448	20.22	1.7548
	196.5	18.49	42.93	18.65	0.075	2.3580	0.7952	33.72	1.5628
	213.3	18.37	62.16	18.62	0.075	2.5596	1.1433	44.67	1.4163
	231	18.61	86.55	18.18	0.08	2.7720	1.6121	58.16	1.1599
	178	18.75	0.016	18.67	18.47	2.1360	0.3440	16.11	1.7920
	191.1	18.69	0.017	18.53	38.7	2.2932	0.7174	31.29	1.5758
	202	18.66	0.015	18.4	58.8	2.424	1.0822	44.65	1.3418
	233.4	18.64	0.015	18.25	83.84	2.8008	1.5304	54.64	1.2704
	210.5	18.57	23.54	18.6	23.24	2.5260	0.8694	34.42	1.6566
	232	18.41	42.68	18.42	38.5	2.7840	1.4949	53.70	1.2891
	252.3	18.25	61.9	18.25	58.68	3.0276	2.201	72.68	0.8270
	321.8	17.89	86.3	17.93	83.68	3.8616	3.0443	78.83	0.8173

2.4 Thermal Images

The following images show the thermal performance of the board after 15-min soak.

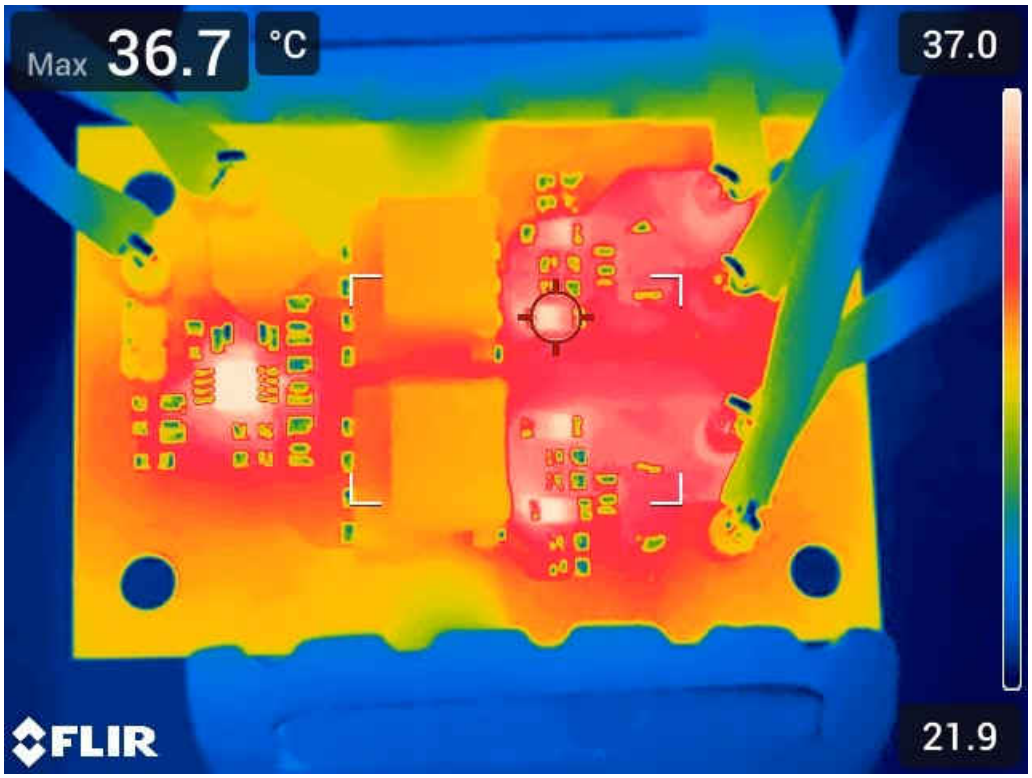


Figure 2-3. Thermal Image Full Load

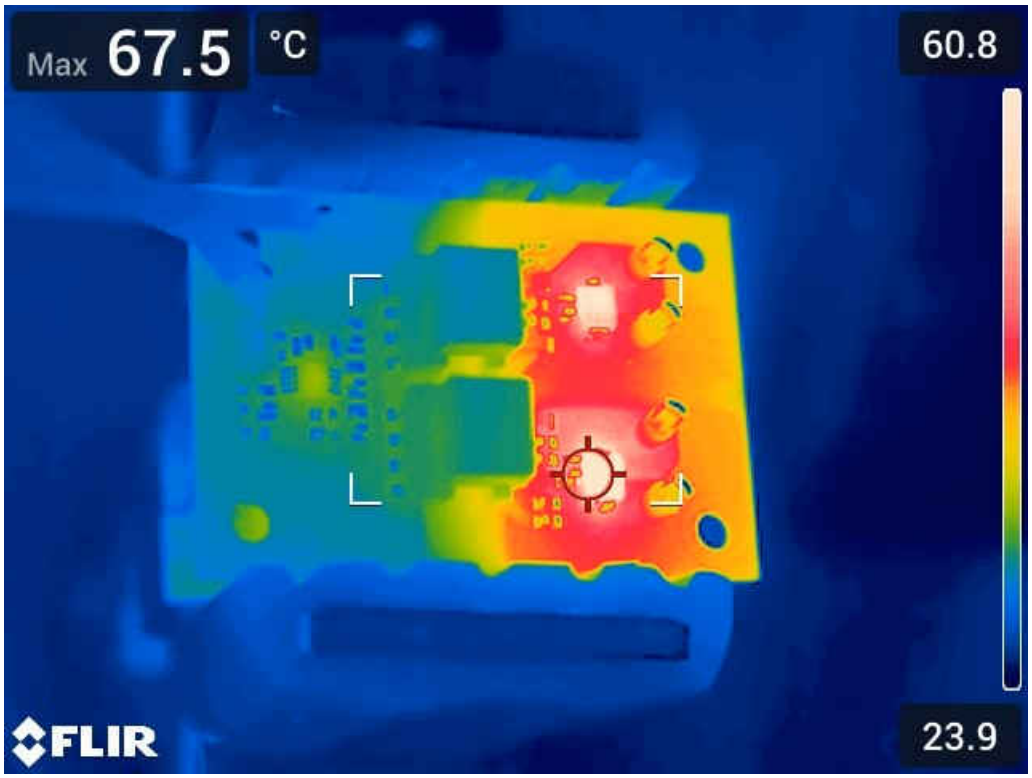


Figure 2-4. Thermal Image No Load

3 Waveforms

Unless noted, all waveforms were captured at full load with a 12-V_{DC} input.

3.1 Switching

Figure 3-1 shows the primary switch node with full load.

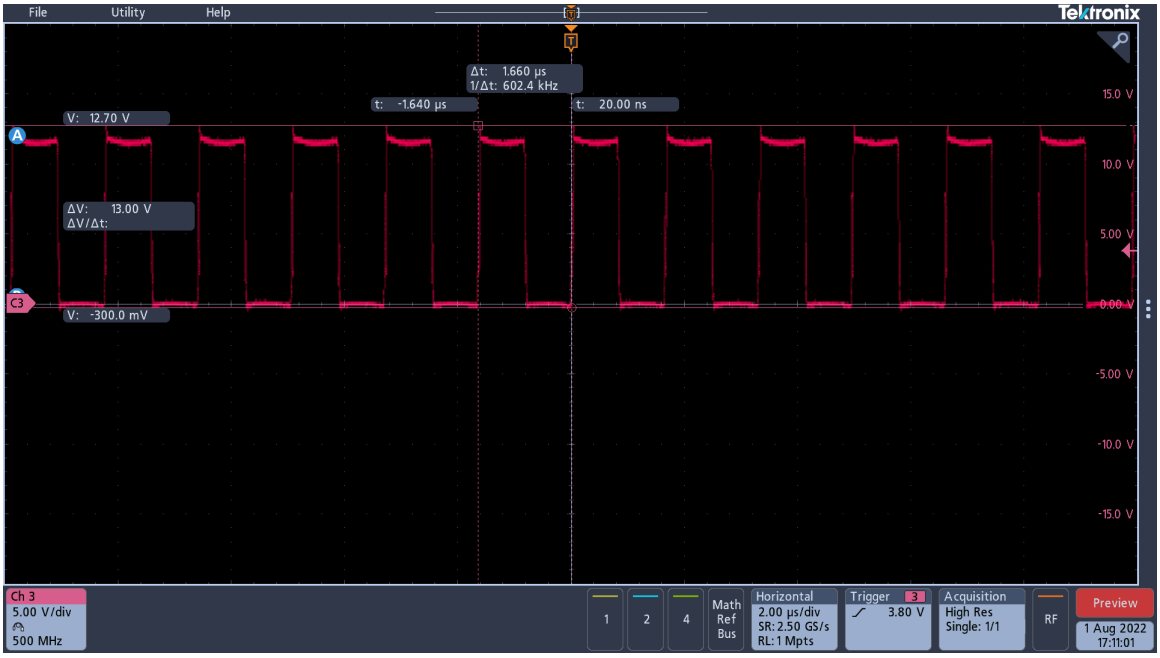


Figure 3-1. Switch Node Full Load

Figure 3-2 shows the primary switch node at no load.

Figure 3-2. Switch Node No Load

3.2 Output Voltage Ripple

The following waveforms shows the PMP23240 output voltage ripple of V_{OUT1} and V_{OUT2}.

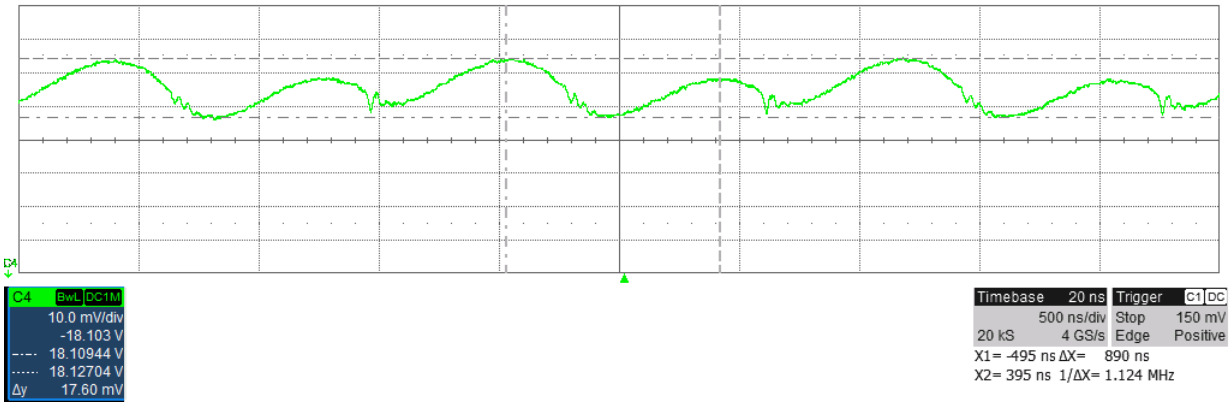


Figure 3-3. V_{OUT1} Output Ripple

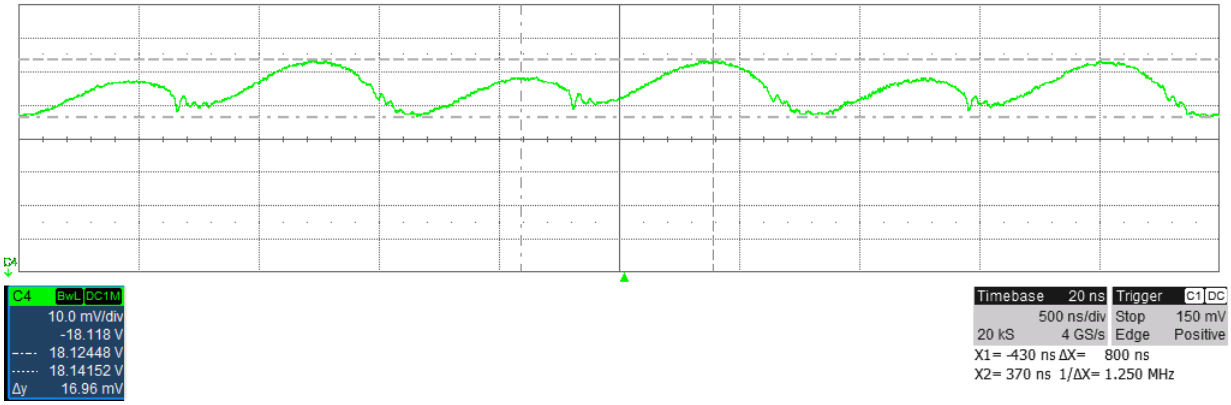
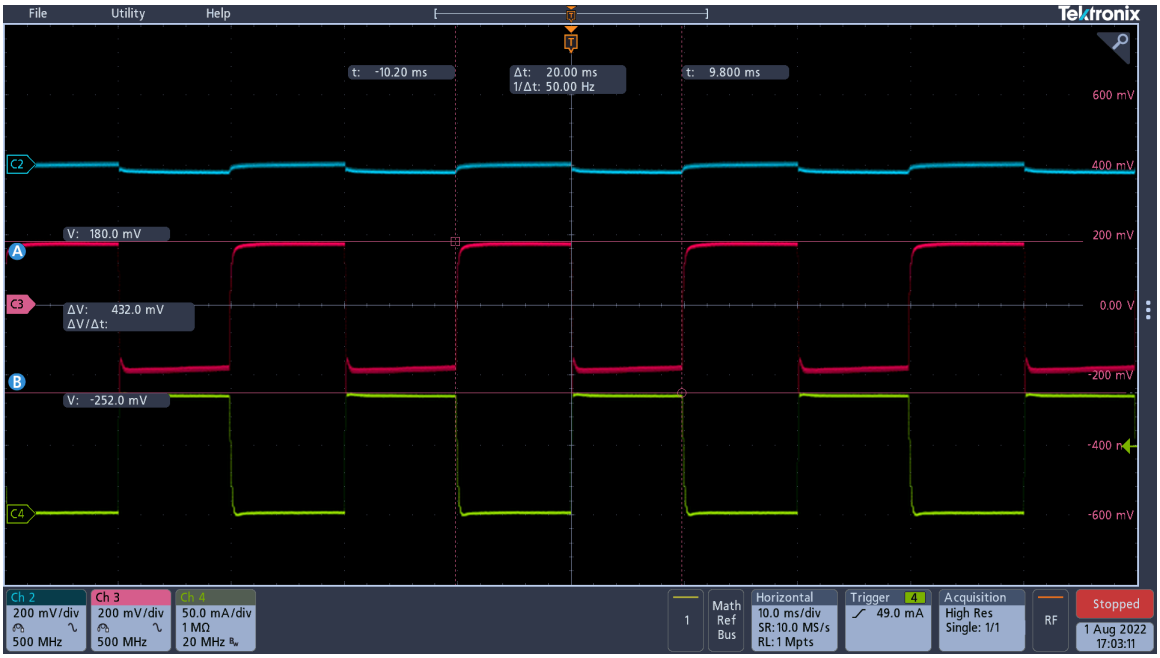


Figure 3-4. V_{OUT2} Output Ripple

3.3 Load Transients

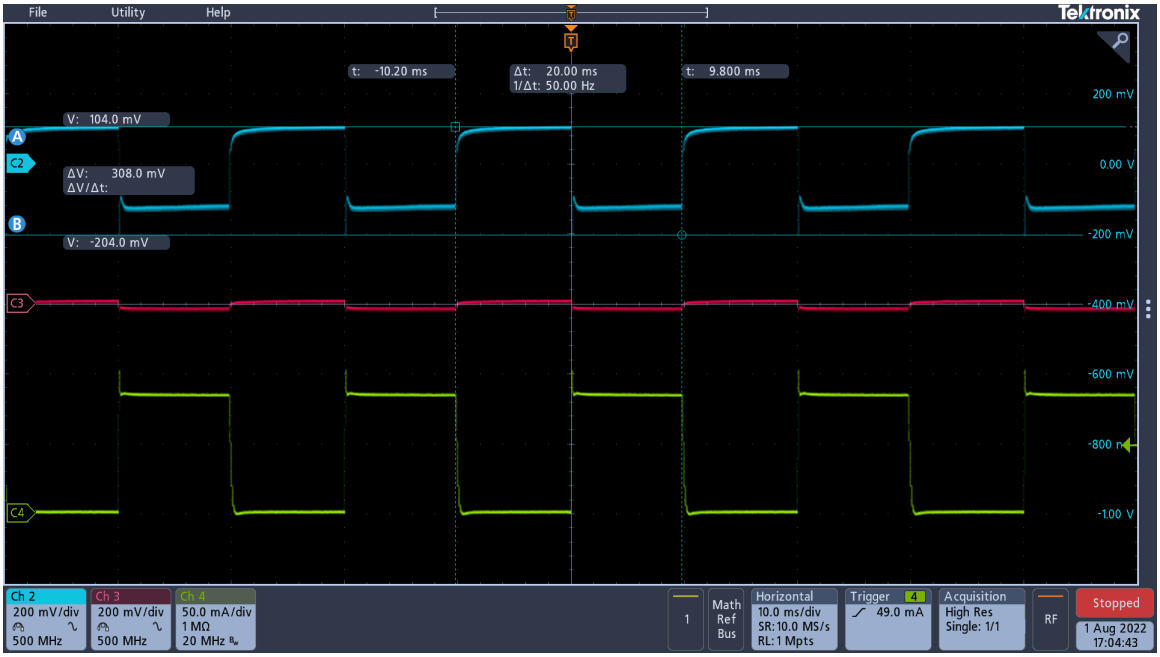
Figure 3-5 illustrates the no-load to full-load transient response of V_{OUT1}. V_{OUT2} is loaded with 40 mA during the test.



Channel 2 (blue) = V_{OUT2} AC coupled, Channel 3 (red) = V_{OUT1} AC coupled, Channel 4 (green) = load current of V_{OUT1}

Figure 3-5. V_{OUT1} Load Transient

Figure 3-6 illustrates the no-load to full-load transient response of V_{OUT1}. V_{OUT1} is loaded with 40 mA during the test.

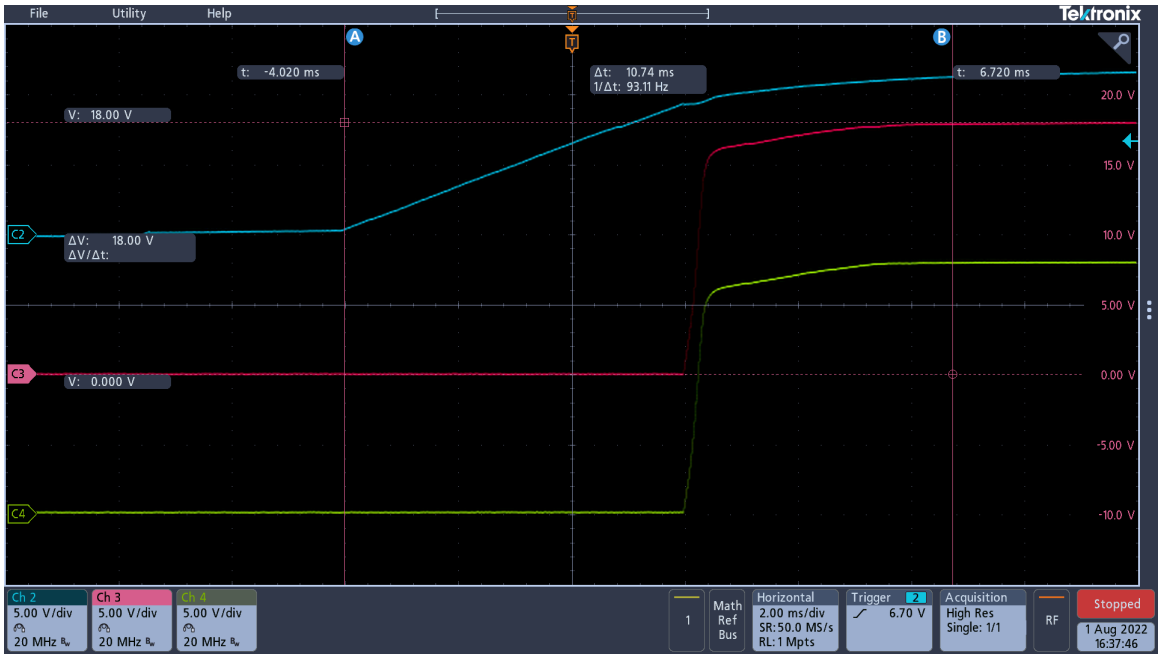


Channel 2 (blue) = V_{OUT2} AC coupled, Channel 3 (red) = V_{OUT1} AC coupled, Channel 4 (green) = load current of V_{OUT2}

Figure 3-6. V_{OUT2} Load Transient

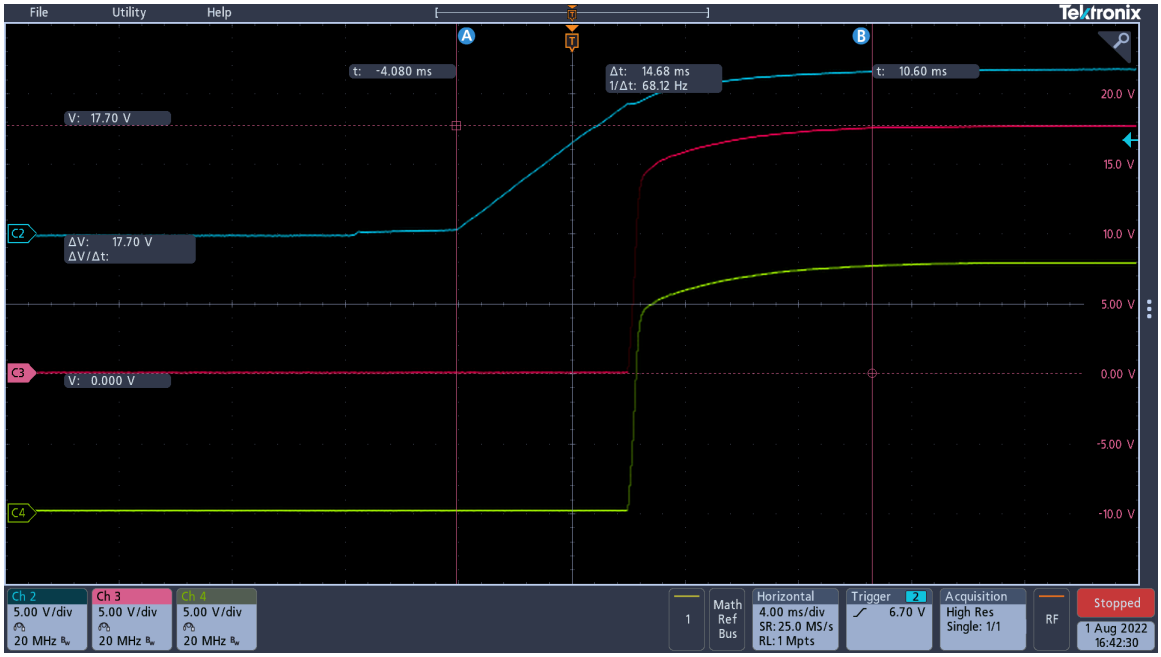
3.4 Start-up Sequence

Figure 3-7 shows the start-up with no load. Figure 3-8 shows the start-up with full load.



Channel 2 (blue) = Input voltage, Channel 3 (red) = V_{OUT1}, Channel 4 (green) = V_{OUT2}

Figure 3-7. Start-up No Load



Channel 2 (blue) = Input voltage, Channel 3 (red) = V_{OUT1}, Channel 4 (green) = V_{OUT2}

Figure 3-8. Start-Up With V_{IN}

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265