Description
This 26.54 mm × 11.68 mm × 5.6-mm height board is optimized to leverage the performance of the LM5181 PSR Flyback converter. The board operates over an input voltage range of 18 V to 32 V to deliver a 24-V and 3.3-V outputs at currents up to 40 mA and 15 mA, respectively. Operating without an auxiliary winding or optocoupler, the LM5181 provides very tight output voltage regulation. The LM5181 offers several protection features, like undervoltage lockout to provide proper operation during voltage-sag conditions, programmable soft-start to reduce inrush current, hiccup-mode overcurrent protection, and thermal shutdown.

Features
- 18-V to 32-V input voltage range
- 24-V and 3.3-V output voltages
- Up to 1-W total output power
- High-voltage isolation
- Fully assembled and tested PCB layout with small footprint and low profile

Applications
- Mixed module (AI,AO,DI,DO)
1 Test Prerequisites

1.1 Voltage and Current Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>18 V&lt;sub&gt;DC&lt;/sub&gt; – 32 V&lt;sub&gt;DC&lt;/sub&gt;</td>
</tr>
<tr>
<td>Output-1 Voltage</td>
<td>24 V&lt;sub&gt;DC&lt;/sub&gt;</td>
</tr>
<tr>
<td>Output-1, Current</td>
<td>40 mA</td>
</tr>
<tr>
<td>Output-2, Voltage</td>
<td>3.3 V&lt;sub&gt;DC&lt;/sub&gt;</td>
</tr>
<tr>
<td>Output-2, Current</td>
<td>15 mA</td>
</tr>
</tbody>
</table>

1.2 Required Equipment

- 0…35 V<sub>DC</sub> constant voltage source (VS1)
- Two electronic loads, (constant current range 0…100 mA minimum)
- Oscilloscope (minimum 100-MHz bandwidth)
- Current probe (minimum 100-kHz bandwidth)

1.3 Considerations

The reference design PMP31177 Rev_B was built on the PMP31177 Rev_A PCB.

1.4 Dimensions

The net PCB (containing all components) board dimensions are 26.54 mm × 11.68 mm, height 5.6 mm (T1).

1.5 Test Setup

1. Connect the source VS1 to TP1 (positive) and TP3 (negative)
2. Connect the first load to terminals TP2 (positive) and TP4 (negative)
3. Connect the second load to terminals TP6 (positive) and TP4 (negative)
4. Turn on VS1 (accepted range: 18 V<sub>DC</sub> – 32 V<sub>DC</sub>)
5. Increase the load on each output
2 Testing and Results

2.1 Efficiency Graph

The efficiency graph in Figure 2-1 shows the converter efficiency, versus total output power. The input voltage has been set to 18 V\textsubscript{DC}, 24 V\textsubscript{DC}, and 32 V\textsubscript{DC}, while the load on each output has been increased at the same ratio.

![Efficiency Graph](image)

**Figure 2-1. Efficiency Graph**

2.2 Efficiency Data

The efficiency graph in Figure 2-1 reports the data, taken from the following tables.

<table>
<thead>
<tr>
<th>Table 2-1. Efficiency Data for 24-V Input Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V\textsubscript{IN} )</td>
</tr>
<tr>
<td>24.00</td>
</tr>
<tr>
<td>23.99</td>
</tr>
<tr>
<td>23.99</td>
</tr>
<tr>
<td>23.97</td>
</tr>
<tr>
<td>24.05</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 2-2. Efficiency Data for 18-V Input Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V\textsubscript{IN} )</td>
</tr>
<tr>
<td>18.03</td>
</tr>
<tr>
<td>18.03</td>
</tr>
<tr>
<td>18.02</td>
</tr>
<tr>
<td>18.00</td>
</tr>
<tr>
<td>17.96</td>
</tr>
</tbody>
</table>
2.3 Static Output Voltage Variation vs Load Current and $V_{IN}$

2.3.1 24-V Output Voltage

![Figure 2-2. Static Output Voltage Variation of the 24-V Output](image)

2.3.2 3.3-V Output Voltage

![Figure 2-3. Static Output Voltage Variation of the 3.3-V Output](image)

2.3.3 U2 Input Voltage

![Figure 2-4. Static Output Voltage Variation of the U2 Input](image)

Table 2-3. Efficiency Data for 32-V Input Voltage

<table>
<thead>
<tr>
<th>$V_{IN}$ (V)</th>
<th>$I_{IN}$ (mA)</th>
<th>$P_{IN}$ (W)</th>
<th>24 V-$V_{OUT}$ (V)</th>
<th>24 V-$I_{OUT}$ (mA)</th>
<th>4 V-$V_{OUT}$ (V)</th>
<th>3.3 V-$V_{OUT}$ (V)</th>
<th>3.3 V-$I_{OUT}$ (mA)</th>
<th>$P_{OUT}$ (W)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32.19</td>
<td>1.28</td>
<td>0.041</td>
<td>23.71</td>
<td>0.0</td>
<td>4.592</td>
<td>3.307</td>
<td>0.0</td>
<td>0.000</td>
<td>0.00%</td>
</tr>
<tr>
<td>32.19</td>
<td>6.92</td>
<td>0.223</td>
<td>23.71</td>
<td>5.4</td>
<td>4.603</td>
<td>3.300</td>
<td>2.7</td>
<td>0.137</td>
<td>61.48%</td>
</tr>
<tr>
<td>32.18</td>
<td>12.16</td>
<td>0.391</td>
<td>23.70</td>
<td>10.7</td>
<td>4.618</td>
<td>3.299</td>
<td>5.1</td>
<td>0.270</td>
<td>69.11%</td>
</tr>
<tr>
<td>32.17</td>
<td>21.6</td>
<td>0.695</td>
<td>23.87</td>
<td>21.5</td>
<td>4.618</td>
<td>3.299</td>
<td>9.9</td>
<td>0.542</td>
<td>77.97%</td>
</tr>
<tr>
<td>32.15</td>
<td>38.1</td>
<td>1.225</td>
<td>23.66</td>
<td>40.2</td>
<td>4.628</td>
<td>3.298</td>
<td>15.3</td>
<td>1.002</td>
<td>81.77%</td>
</tr>
</tbody>
</table>
3 Waveforms

3.1 Switching Waveforms on Pin 1 of U1 (SW), Anodes of D1 and D4, at Full Load

The switching waveforms were measured by supplying the converter at 96 V<sub>AC</sub>, 400 Hz at full load. For all switch-node waveforms the bandwidth limit has been removed.

### 3.1.1 18-V Input Voltage

- **C1:** D1 Anode (50 V / div)
- **C2:** SW (20 V / div)
- **C4:** D4 Anode (10 V / div)

1 µs / div

**Figure 3-1. Switching Waveforms at 18-V Input Voltage**

### 3.1.2 24-V Input Voltage

- **C1:** D1 Anode (50 V / div)
- **C2:** SW (20 V / div)
- **C4:** D4 Anode (10 V / div)

1 µs / div

**Figure 3-2. Switching Waveforms at 24-V Input Voltage**

### 3.1.3 32-V Input Voltage

- **C1:** D1 Anode (50 V / div)
- **C2:** SW (20 V / div)
- **C4:** D4 Anode (10 V / div)

1 µs / div

**Figure 3-3. Switching Waveforms at 32-V Input Voltage**
3.2 Output Voltage Ripple

The 3.3-V and 24-V outputs, as well as input voltage and ripple were measured by supplying the converter at 24 V\textsubscript{DC} with both outputs loaded at nominal current. The bandwidth limit of the scope was set to 20 MHz, and the coupling to AC.

![Waveform Image](image-url)

**Figure 3-4. Output Voltage Ripple With 5 µs / div**

*Figure 3-5* is the same waveform as in *Figure 3-4* but with longer time division for showing details about low-frequency ripple.

![Waveform Image](image-url)

**Figure 3-5. Output Voltage Ripple With 100 µs / div**
3.3 Load Transients

During load transients, the outputs of the board were measured by supplying the converter at 24 V\textsubscript{DC} while the load on 24 V\textsubscript{OUT} was switched between 20 mA and 60 mA; the load on 3.3 V\textsubscript{OUT} was constant at 15 mA. For all waveforms the bandwidth limit of the oscilloscope was set to 20 MHz.

![Figure 3-6. Load Transient](image)

3.4 Start-Up Sequence

The start-up phase of the converter has been analyzed by supplying the circuit with 24 V\textsubscript{DC} at zero load and full-load conditions. All waveforms were taken at 20 MHz bandwidth limit and DC coupling.

3.4.1 No Load

![Figure 3-7. Start-Up With No Load](image)
3.4.2 Full Load

Figure 3-8. Start-Up With Full Load (at Both Outputs)

3.5 Shutdown Sequence

The shutdown phase of the converter was analyzed by supplying the circuit with 24 \( V_{DC} \) but only at full-load condition. All waveforms were taken at 20-MHz bandwidth limit and DC coupling.

Figure 3-9. Shutdown with Full Load (at both Outputs)
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