Test Report: PMP41042

Bidirectional CLLLC Resonant Converter Reference Design for Energy Storage System

Description

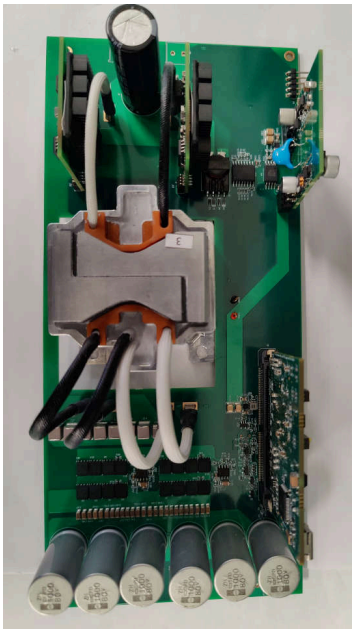
The capacitor-inductor-inductor-inductor-capacitor (CLLLC) resonant converter with a symmetric tank, soft switching characteristics, and ability to switch at higher frequencies is a good choice for energy storage systems. This design illustrates control of this power topology using a C2000® MCU in closed voltage and closed current-loop mode. The hardware and software available with this design help accelerate time to market.

Features

- Vprim: 380–410 V DC; Vsec: 40–60 V DC
- Power Maximum: 3.6 kW, 97.6% peak efficiency
- Soft switching with Zero Voltage Switching (ZVS) on the primary, Zero Current Switching (ZCS), and ZVS on the secondary enable higher efficiency
- Active synchronous rectification scheme implementation using Rogowski coil sensor enables higher efficiency
- Software Frequency Response Analyzer (SFRA) and Compensation Designer for ease of tuning of control loops
- Software support for the TMS320F28004x device with the Control Law Accelerator (CLA), which enables integrated power conversion system design with AC-DC and DC-DC controlled using a single C2000 MCU

Applications

- Battery energy storage system
- Power conversion system (PCS)
- Portable power station



Top View of Board

Bottom View of Board

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	380 VDC to 410 VDC (400 VDC typical)
Output Voltage Range	40 VDC to 60 VDC (48VDC typical)
Output Current	75 A MAX
Output Power	3.6 kW MAX

1.2 Required Equipment

- DC Voltage Source
- Electronic load
- Multimeters
- Oscilloscope
- Power meter

1.3 Test Setup

1.3.1 Hardware Setup

Figure 1-1 shows the board overview for hardware settings.

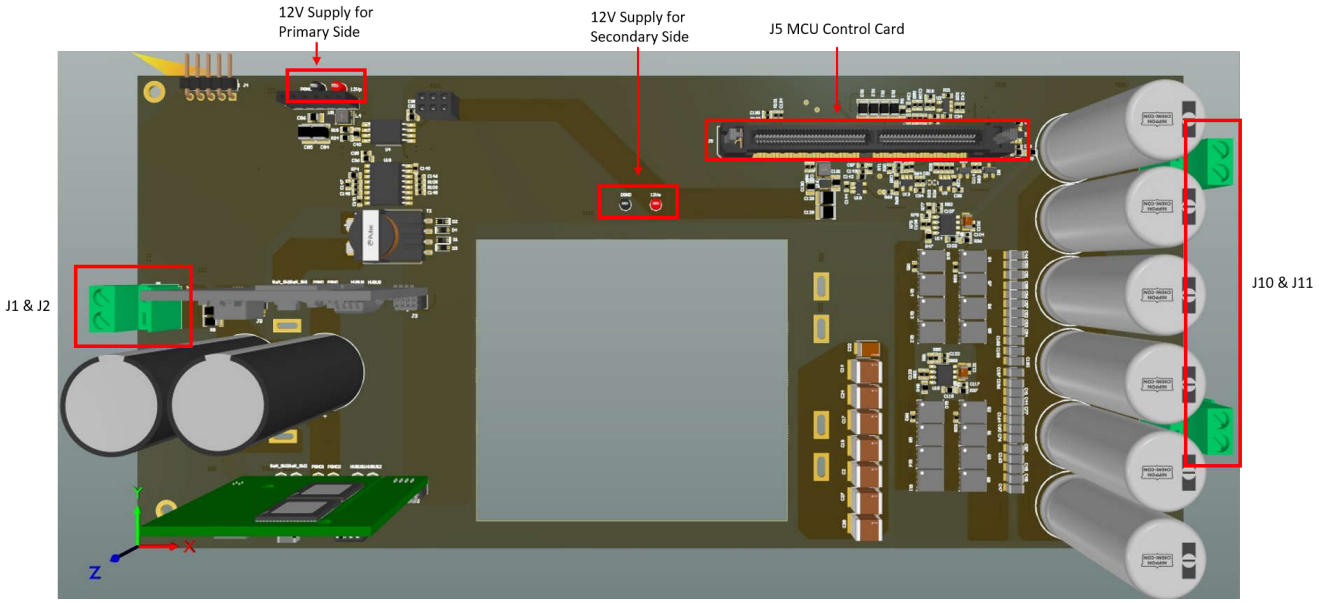


Figure 1-1. Board Overview

Use the following procedure when setting up the board:

- Make sure no power source is connected to the board.
- Insert the 280049C controlCARD in the J5 slot.
- Connect a power source for the primary and secondary side (+12 V, 1 A) at the test points
- Switch the power source on for both the primary and secondary side. A green LED on the control card lights up. This indicates the C2000 MCU device is powered.
- To connect JTAG, use a USB cable from the controlCARD and connect the cable to a host computer.
- Connect the DC power supply to the input connector (J1 and J2) and the electrical load to the output connector (J10 and J11).

1.3.2 Software Setup

Getting Started | clllc_settings.h | clllc_main.c | clllc.h | clllc.c | main.syscfg

```
136 #define CLLLC_SFRA_INJECTION_AMPLITUDE_LEVEL2 0.01
137 #define CLLLC_SFRA_INJECTION_AMPLITUDE_LEVEL3 0.015
138
139 //
140 // CLLLC LAB
141 // Power Flow Prim -> Sec
142 // 1 -> Open loop check for PWM drivers,
143 // 2 -> Open loop check for PWM drivers with protection,
144 // 3 -> Closed loop check with resistive load, voltage loop,
145 // 4 -> Closed loop check with resistive load, current loop
146 // 5 -> Closed loop check with battery emulated, current loop
147 // Power Flow Sec -> Prim
148 // 6 -> Open loop check for PWM driver,
149 // 7 -> Open loop check for PWM driver with protection,
150 // 8 -> Closed loop voltage with resistive load
151 //
152
153 #define CLLLC_LAB 3
154
```

Figure 1-2. Test Lab Selection File

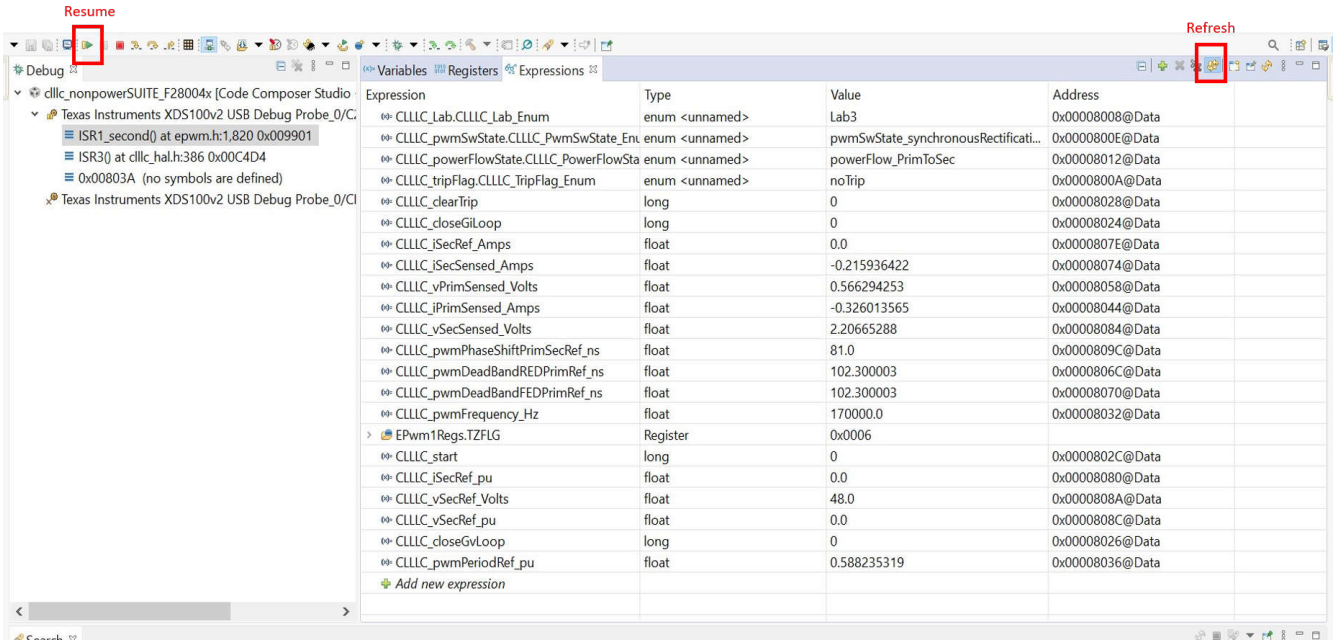


Figure 1-3. Expression Watch Window

1. Install Code Composer Studio from the Code Composer Studio (CCS) Integrated Development Environment (IDE) tools folder. Version 11.2 or above is recommended.
2. Go to *View* → *Resource Explorer*. Below the TI Resource Explorer, go to C2000Ware DigitalPower SDK. To open the reference design software as is (opens firmware as run on this design and hardware, requires the board to be exactly the same as this reference design).
3. Under C2000Ware DigitalPower SDK, select *Development Kits* → *PMP41042*, and click on *Run Project*. This action imports the project into the workspace environment.
4. To get started, click *clllc_nonpowerSUITE_F28004x* item in *Project Explorer*.
5. In the *settings.h* file, change the LAB number to select different function as shown in Figure 1-2.
6. Right click on the project name and click *Rebuild Project*. Then, click *Run* → *Debug* to launch a debugging session.
7. The project then loads on the device and the CCS debug view becomes active. The code halts at the start of the main routine.

8. To add the variables in the watch/expressions window, click *View* → *Scripting Console* to open the scripting console dialog box. On the upper right corner of this console, click on *Open* and then browse to the *setupdebugenv_labx.js* script file located inside the project folder. This populates the watch window with the appropriate variables needed to debug the system.
9. Click on the *Continuous Refresh* button on the watch window to enable continuous update of values from the controller. The watch window appears as shown in Figure 1-3.

1.4 Running the Code for Different Labs

Figure 1-4 illustrates the Expression Watch Window.

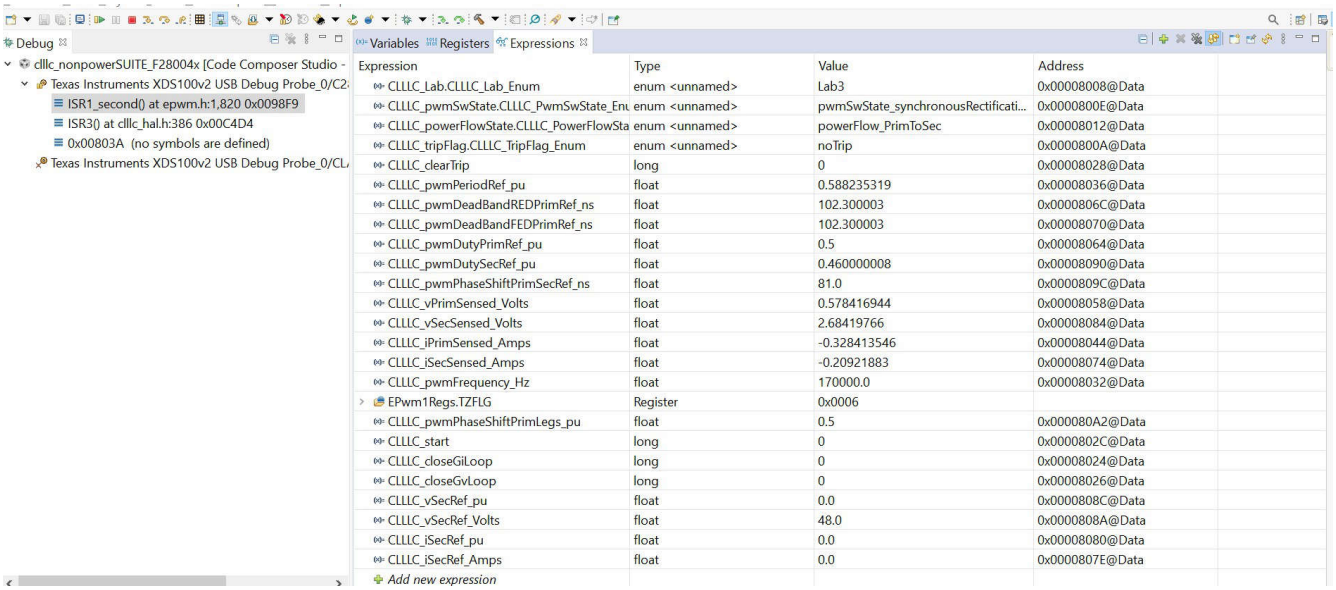


Figure 1-4. Expression Watch Window

1.4.1 Lab 1. Primary to Secondary Power Flow, Open Loop Check PWM Driver

This lab option is primarily provided as a focused test just for the PWM from a software perspective so that the lab can be run independent of the hardware connections of the reference design. With this lab, the code is executed on a C2000 controlCARD or LaunchPad™ Development Kit just to observe the PWM waveforms. This lab can be easily skipped and the user can go directly to *Lab 2* if no changes to the PWM driver are anticipated. Hence, this lab procedure is not documented since this lab is primarily for PWM driver development and debug purposes.

1.4.2 Lab 2. Primary to Secondary Power Flow, Open Loop CheckPWM Driver and ADC With Protection

In this lab, the board is excited in open-loop fashion with a specified frequency that can be changed through the watch window. The frequency is controlled with the CLLLC_pwmPeriodRef_pu variable. Set the load current above 1 A to avoid the unregulated output voltage in open loop.

1. Run the project by clicking *Resume* button in *Tool Bar*
2. Set the load current below 20 A during start up
3. Clear the trip by writing “1” to the CLLLC_clearTrip variable in the watch window
4. Change the CLLLC_pwmPhaseShiftPrimLegs_pu from 0.5 to 0
5. Now, slowly increase the input VPRIM DC voltage from 0 V to 400 V. Make sure CLLLC_vPrimSensed_Volts displays the correct values in the watch window
6. By default, the CLLLC_pwmPeriodRef_pu variable is set to 0.588, as shown in Figure 1-4, which is 170 kHz. This is close to the series resonant frequency of the converter; however, due to variation in the components on the actual hardware, it can be lower or higher than the series resonant frequency
7. The VSEC variable shows a voltage of close to 48 V per the tank gain designed. Verify that CLLLC_vSecSensed_Volts shows the correct voltage
8. Next, test to see operation under different frequencies (that is, above resonance, below resonance)

1.4.3 Lab 3. Primary to Secondary Power Flow, Closed Voltage Loop Check

In this lab, the voltage loop Gv , is closed with an electrical load (constant current mode) at the output.

1. Run the project by clicking the *Resume* button in Tool Bar
2. Set the load current below 20 A during start up
3. Increase the input PRIM DC voltage from 0 V to 400 V
4. Clear the trip by writing "1" to the *CLLLC_start* variable in the watch window as shown in Figure 1-4, this closes the voltage loop and the converter performs soft-start until the output voltage ramps up to 48 V
5. Next, test the close loop operation by varying *CLLC_vSecRef_Volts* in the watch window with different load conditions

1.4.4 Lab 4. Primary to Secondary Power Flow, Closed Current Loop Check

In this lab, the output current control loop is closed. In this Lab, using the electrical load(constant voltage mode) to emulate the battery connection on secondary side.

1. Run the project by clicking the *Resume* button in the Tool Bar
2. Set the CLLLC_iSecRef_Amps below 5 A during start up
3. Increase the input PRIM DC voltage from 0 V to 400 V
4. Clear the trip by writing "1" to the *CLLLC_start* variable in the Watch window as shown in Figure 1-4, this closes the voltage loop and the converter performs soft-start until the output voltage ramps up to 48 V
5. Next, test the close loop operation by varying *CLLLC_iSecRef_Amps* in the Watch window

1.4.5 Lab 6. Secondary to Primary Power Flow, Open Loop Check PWM Driver

This lab option is primarily provided as a focused test just for the PWM from a software perspective, so that the lab is run independent of the hardware connections of the reference design. With this lab the user can run the code on a C2000 controlCARD or LaunchPad™ just to observe the PWM waveforms.

1.4.6 Lab 7. Secondary to Primary Power Flow, Open Loop Check PWM Driver and ADC With Protection

In this build, the board is excited in open-loop fashion with a specified frequency that can be changed through the watch window. The frequency is controlled with the CLLLC_pwmPeriodRef_pu variable. The power flow is from the secondary side to the primary side. Set the load current above 1 A to avoid the unregulated output voltage in open loop.

1. Run the project by clicking the *Resume* button in the Tool Bar
2. Set the load current below 2 A during start up
3. Clear the trip by writing “1” to the CLLLC_clearTrip variable in the watch window
4. Now, slowly increase the input VSEC DC voltage from 0 V to 48 V. Make sure CLLLC_vSecSensed_Volts displays the correct values in the watch window
5. The VPRIM variable shows a voltage of close to 400 V per the tank gain designed. Verify that CLLLC_vPrimSensed_Volts shows the correct voltage.
6. Test to see operation under different frequencies (that is, above resonance, below resonance)

1.4.7 Lab 8. Secondary to Primary Power Flow, Closed Voltage Loop Check

In this lab, the voltage loop Gv , is closed with a electrical load (constant current mode) at the output.

1. Run the project by clicking the *Resume* button in the Tool Bar
2. Set the load current below 2 A during start up
3. Increase the input VSEC DC voltage from 0 V to 48 V
4. Clear the trip by writing "1" to the *CLLLC_start* variable in the watch window as shown in Figure 1-4, this closes the voltage loop and the converter performs soft-start until the output voltage ramps up to 400 V
5. Test the close loop operation by varying "CLLC_vSecRef_Volts " in the watch window

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in the following figure. The data was created in charging mode under different load conditions.

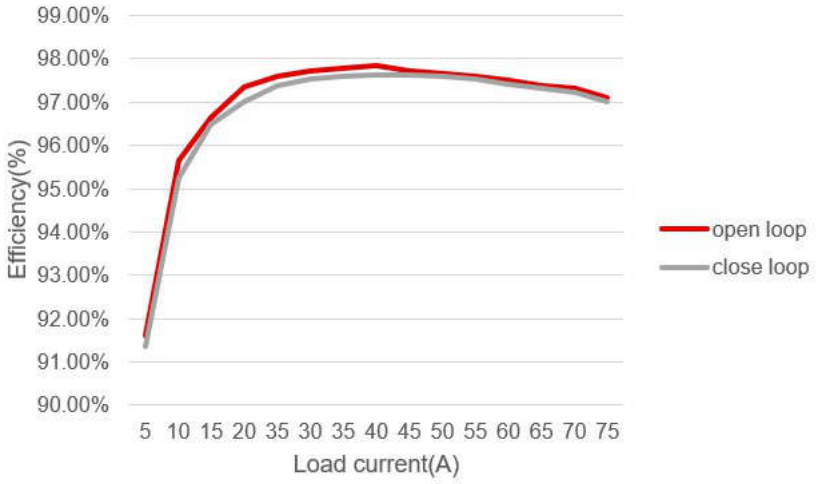


Figure 2-1. Efficiency Graph in Charging Mode

Figure 2-2 shows open loop efficiency in discharging mode under different load conditions.

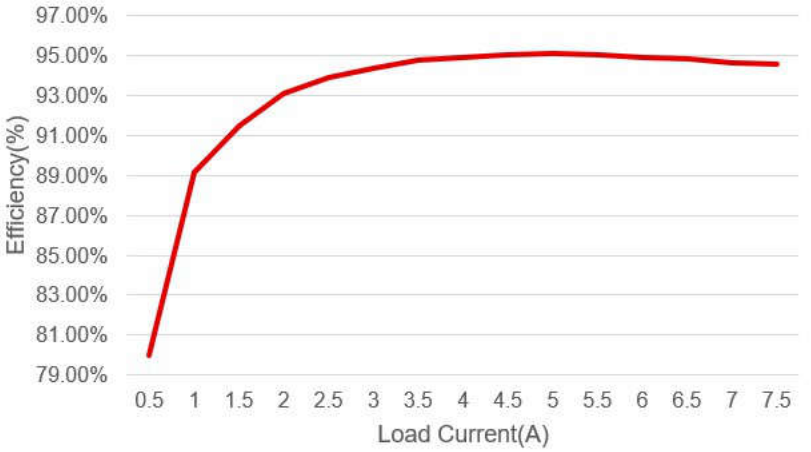


Figure 2-2. Efficiency Graph in Discharging Mode

2.2 Efficiency Data

Efficiency data is shown in the following tables.

Table 2-1. Open-Loop Efficiency Data in Charging Mode

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
399.17	0.639	46.96	4.976	255.07	233.673	91.61
398.93	1.222	46.84	9.955	487.492	466.292	95.651
398.75	1.791	46.21	14.935	714.161	690.146	96.637
398.72	2.366	46.14	19.904	943.372	918.371	97.35
398.45	2.946	46.03	24.885	1173.83	1145.46	97.583
398.33	3.525	45.94	29.865	1404.11	1372	97.713
398.13	4.104	45.85	34.847	1633.93	1597.73	97.785
398.11	4.682	45.79	39.823	1863.95	1823.5	97.83
399.33	5.284	45.86	44.966	2110.06	2026.14	97.729
399.31	5.865	45.78	49.964	2341.95	2287.35	97.669
399.26	6.446	45.7	54.967	2573.63	2511.99	97.605
399.23	7.028	45.62	59.964	2805.79	2735.56	97.497
399.18	7.607	45.52	64.97	3036.56	2957.43	97.394
399.06	8.189	45.44	69.98	3267.9	3179.89	97.307
399.05	8.768	45.32	74.97	3498.87	3397.64	97.107

Table 2-2. Close-Loop Efficiency Data in Charging Mode

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
399.05	0.642	47.08	4.971	256.19	234.035	91.35
398.93	1.233	47.08	9.951	491.881	468.493	95.245
398.76	1.827	47.08	14.931	728.535	702.951	96.488
398.6	2.423	47.08	19.901	965.808	936.939	97.011
398.42	3.02	47.08	24.885	1203.23	1171.59	97.37
398.24	3.619	47.08	29.862	1441.23	1405.9	97.549
398.13	4.22	47.07	34.841	1680.11	1639.97	97.611
398	4.824	47.07	39.822	1919.95	1874.42	97.629
399.23	5.425	47.04	44.953	2165.82	2114.59	97.634
399.18	6.032	47.04	49.954	2407.85	2349.84	97.59
399.13	6.641	47.04	54.96	2650.62	2585.32	97.536
399.08	7.255	47.04	59.963	2895.33	2820.66	97.421
399.04	7.868	47.04	64.965	3139.65	3055.95	97.334
399.08	8.461	46.91	69.98	3376.62	3282.76	97.22
398.99	9.328	46.91	76.97	3721.78	3610.66	97.014

Table 2-3. Open-Loop Efficiency Data in Discharging Mode

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
45.98	5.44	401.6	0.498	250.131	199.997	79.96
45.98	9.56	392.57	0.998	439.569	391.785	89.13
45.97	13.4	376.35	1.498	615.998	563.772	91.52
45.97	17.45	373.94	1.998	802.177	747.132	93.14
46.96	21.61	381.51	2.498	1014.81	953.012	93.91
46.96	25.71	380.17	2.998	1207.34	1139.75	94.4
46.96	29.72	378.3	3.498	1395.65	1323.29	94.82
45.95	33.82	377.06	3.998	1587.85	1507.49	94.94
45.95	37.91	376.02	4.498	1779.87	1691.34	95.03
45.94	42.01	375.22	4.998	1971.95	1875.35	95.1
45.94	46.12	374.22	5.498	2164.87	2057.46	95.04
45.94	50.24	373.25	5.998	2358.27	2238.75	94.93
47.93	54.35	372.26	6.498	2550.65	2418.95	94.84
47.93	58.5	379.75	6.99	2803.91	2654.45	94.67
47.92	62.62	378.54	7.499	3000.75	2838.67	94.6

2.3 Thermal Images

The thermal test setup is illustrated in Figure 2-3.

The setup includes forced air using 3 × 12-V fans (Delta PFR0612XHE, operated at 12 V), blowing the secondary-side metal-oxide semiconductor field-effect transistors (MOSFETs), and with that, tests are carried out up to 3 kW across the rated load and voltage for the design.

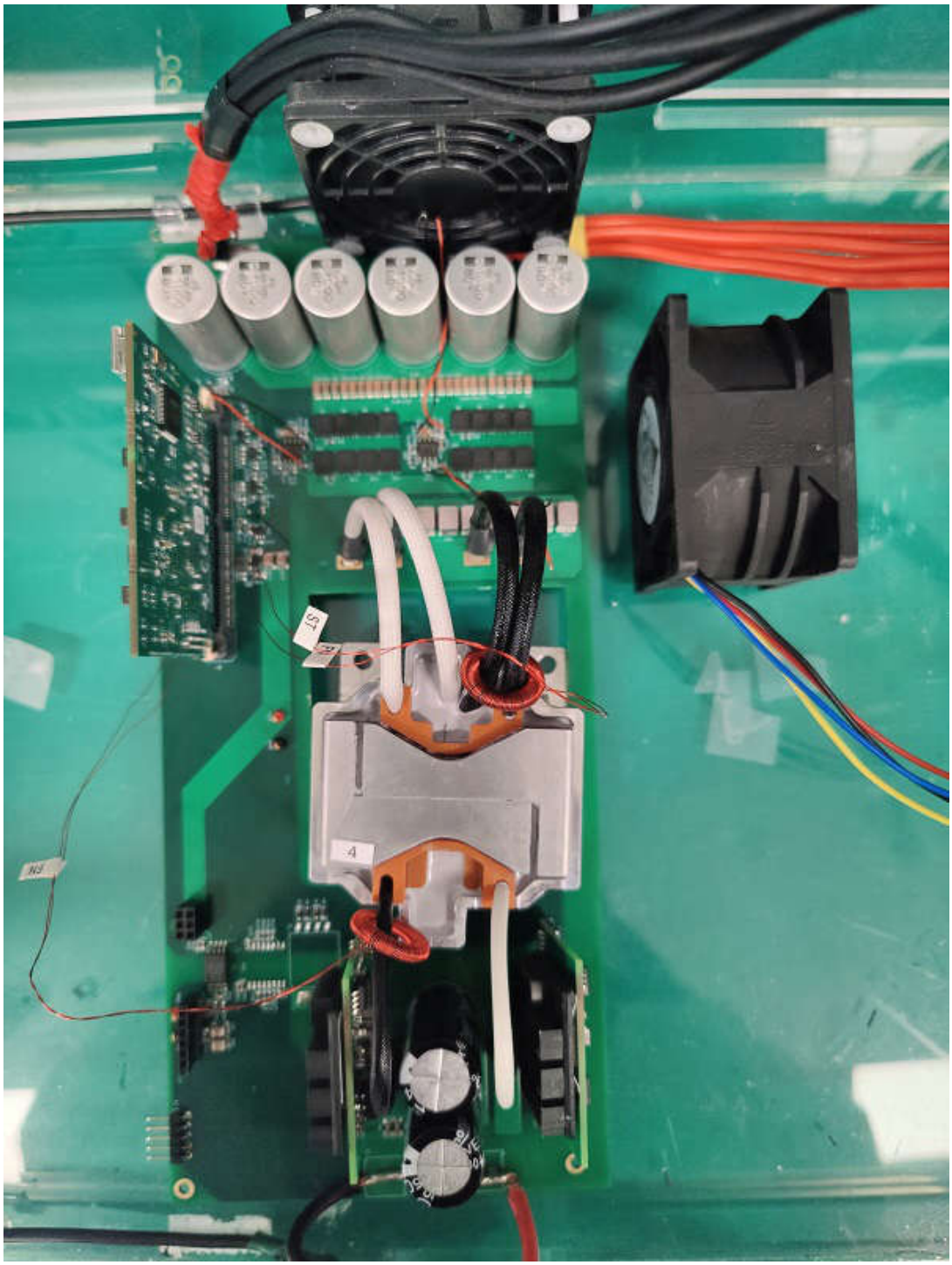
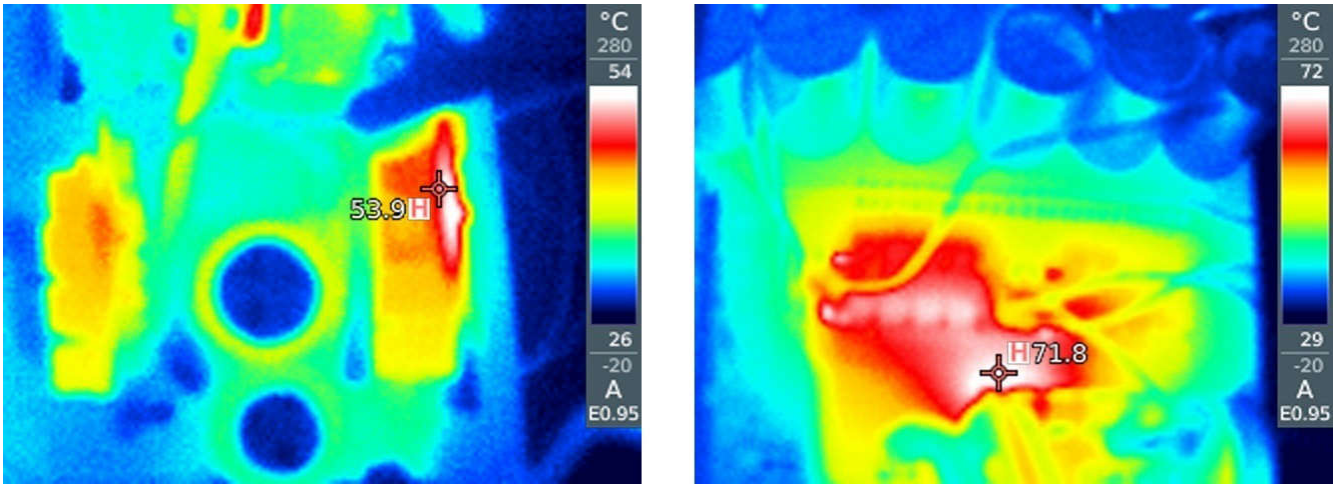


Figure 2-3. Thermal Test Setup Overview

Thermal images and information is shown in the following figures.

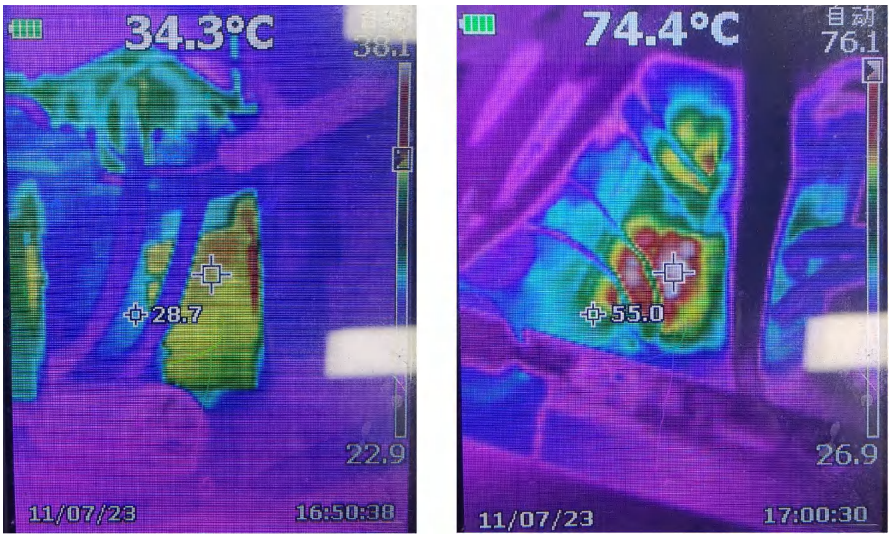


Primary side field-effect transistors (FETs) Secondary side FETs

Figure 2-4. Thermal Image of the Board Running at 3 kW, Vprim 400 V, Vsec 48 V, Charging Mode

CH1: Secondary winding, CH2: Primary winding, CH3: Core

Figure 2-5. Transformer Temperature (Without Heat Sink)



Primary side FETs Secondary side FETs

Figure 2-6. Thermal Image of the Board Running at 2 kW, Vprim 400 V, Vsec 48 V, Discharging Mode

2.4 Bode Plots

Bode plots are shown in the following figures.

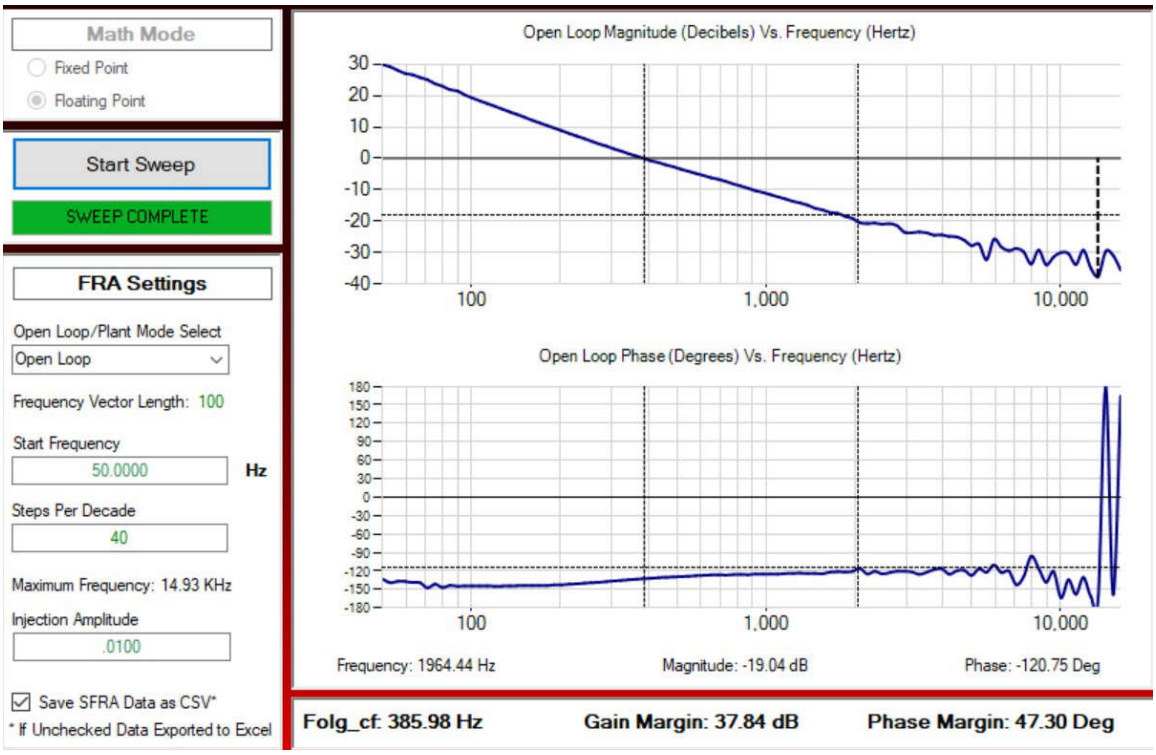


Figure 2-7. SFRA Plant Measurement for the Voltage Loop at Vprim 400 V, Vsec 40 V, 1600 W, Charging Mode

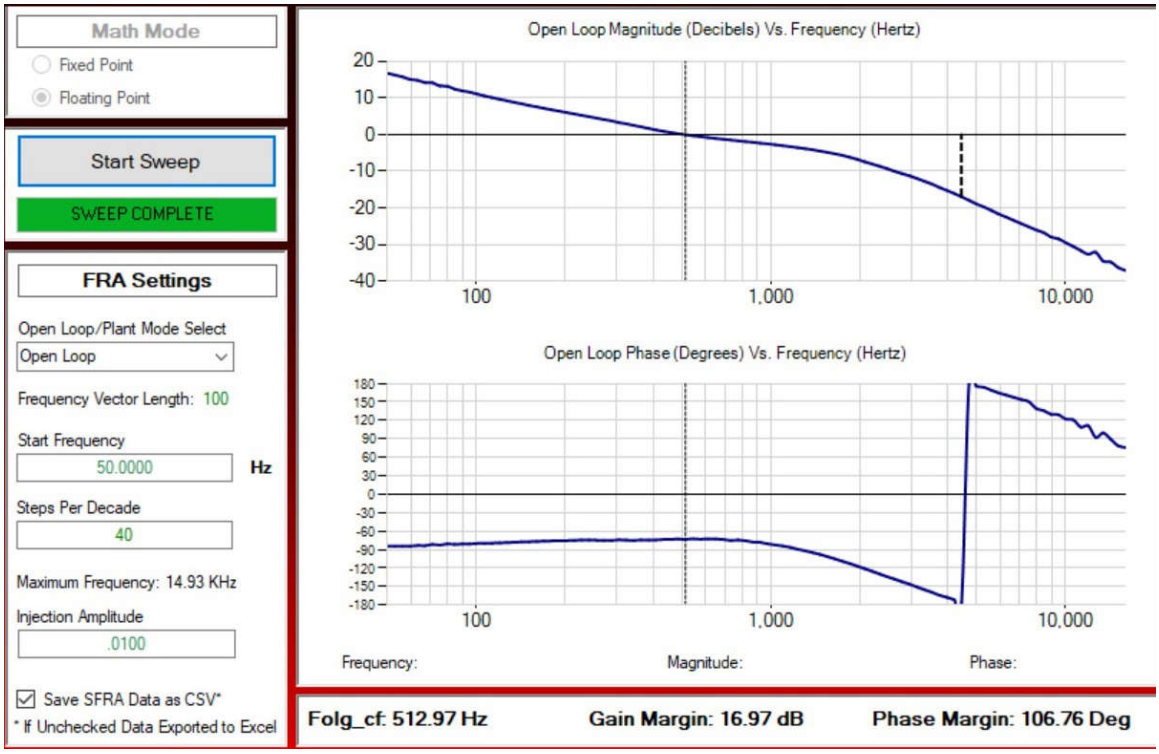


Figure 2-8. SFRA Plant Measurement for the Voltage Loop at Vprim 400 V, Vsec 48 V, 1800 W, Charging Mode

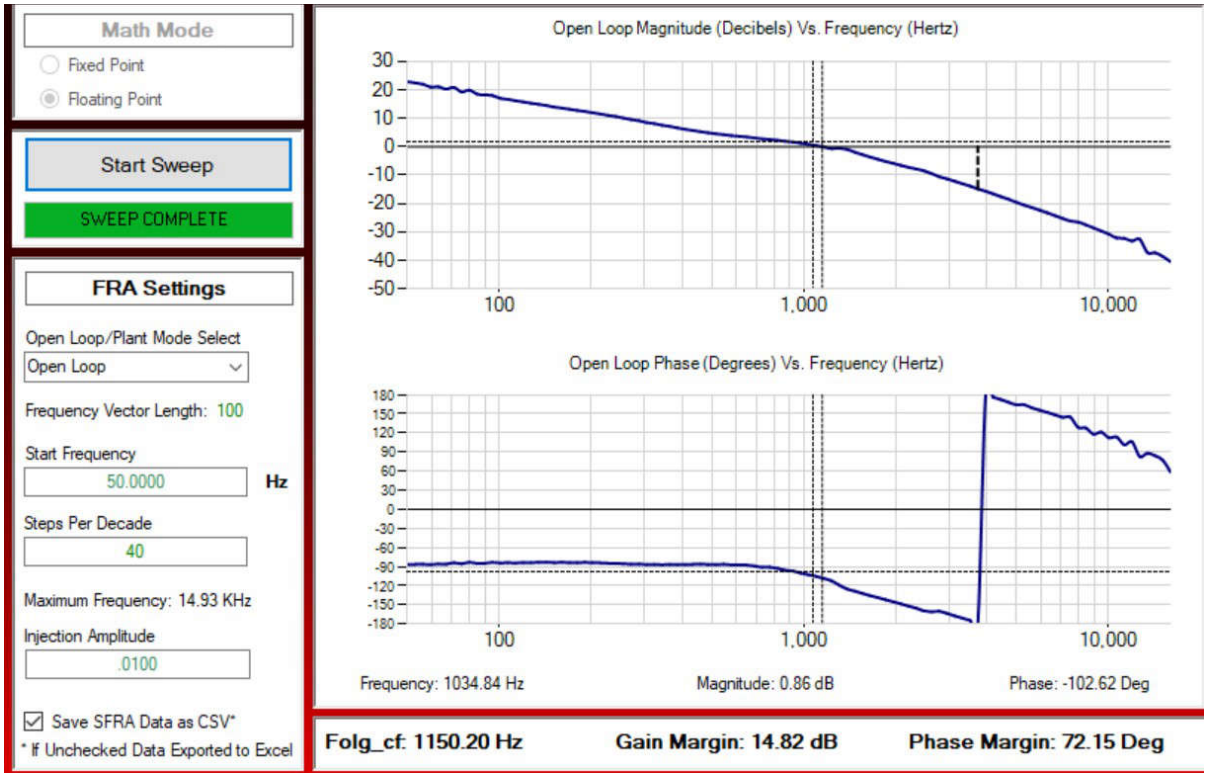


Figure 2-9. SFRA Plant Measurement for the Voltage Loop at Vprim 400 V, Vsec 60 V, 1800 W, Charging Mode

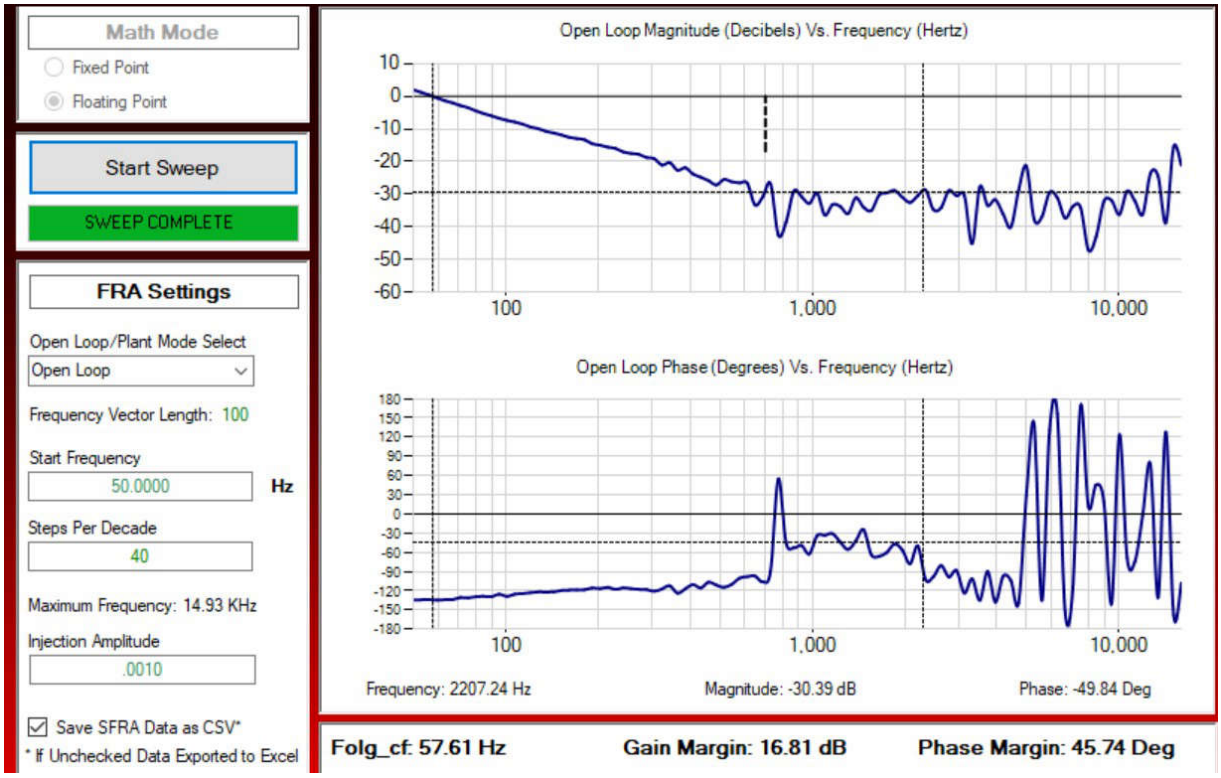


Figure 2-10. SFRA Plant Measurement for the Current Loop at Vprim 400 V, Vsec 40 V, 1200 W, Charging Mode

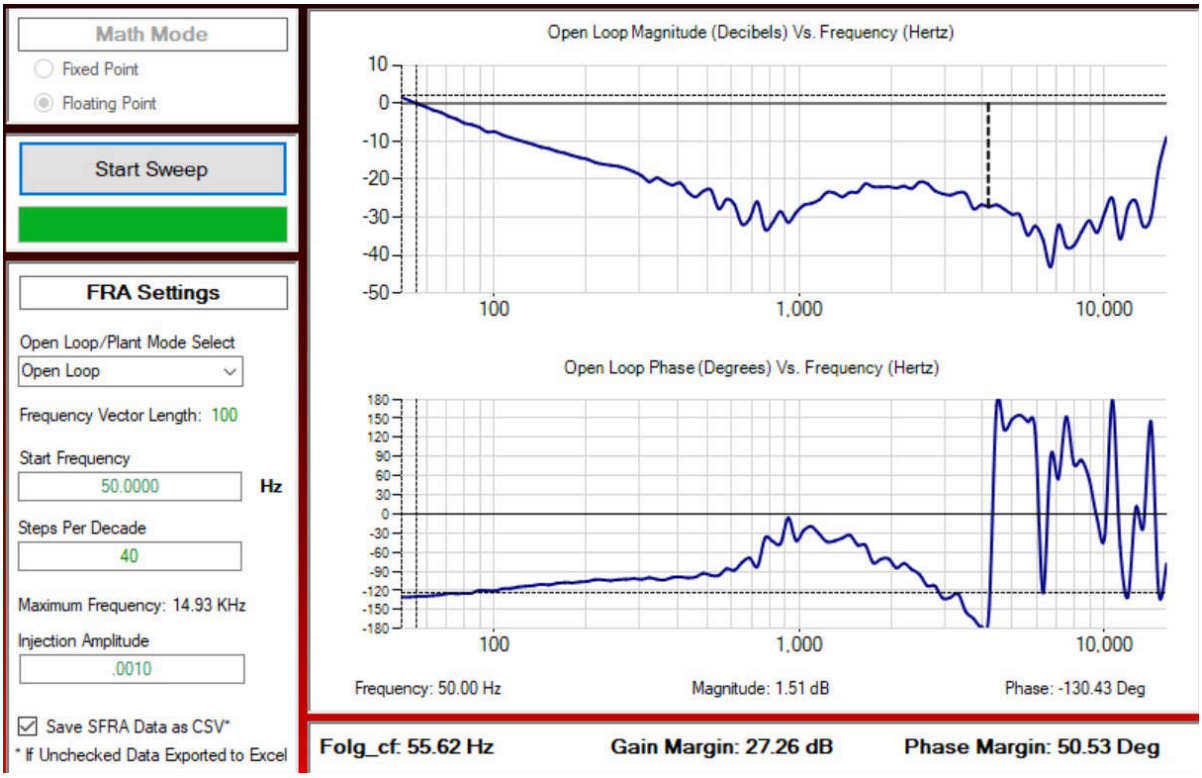


Figure 2-11. SFRA Plant Measurement for the Current Loop at Vprim 400 V, Vsec 48 V, 1800 W, Charging Mode

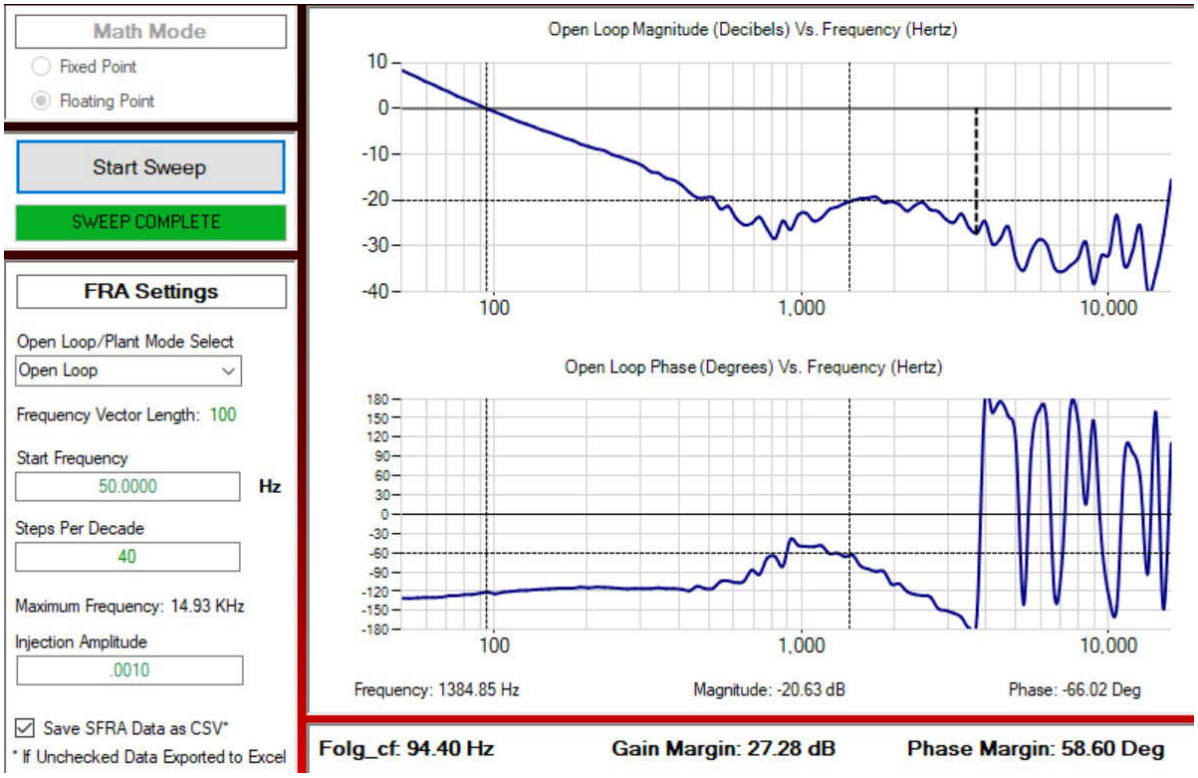
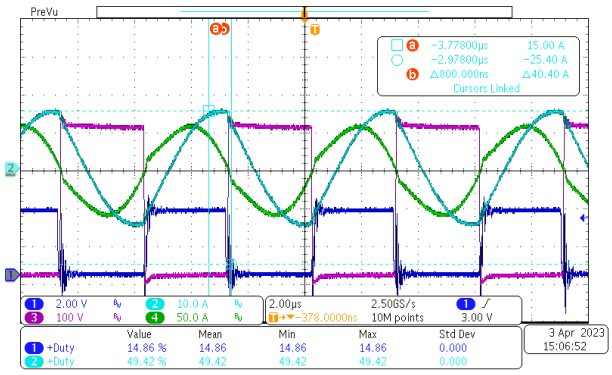


Figure 2-12. SFRA Plant Measurement for the Current Loop at Vprim 400 V, Vsec 60 V, 1800 W, Charging Mode

3 Waveforms

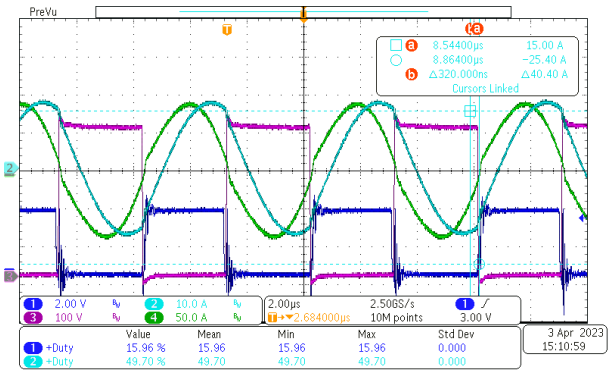
3.1 Switching

Switching behavior is shown in the following figures.



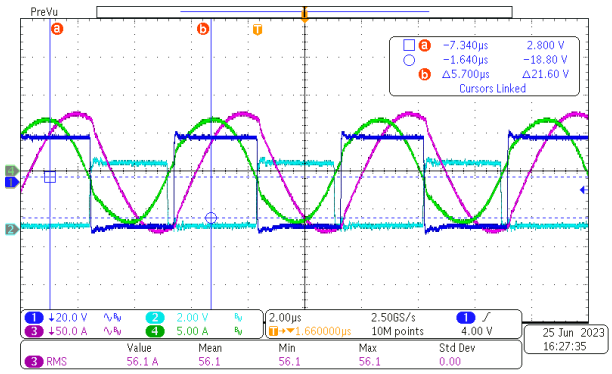
CH1: Primary VGS, CH2: Primary Tank Current,
CH3: Primary VDS, CH4: Secondary Tank Current

Figure 3-1. Charging Mode, 400 V_{IN}, 48 V_{OUT}, 2000 W



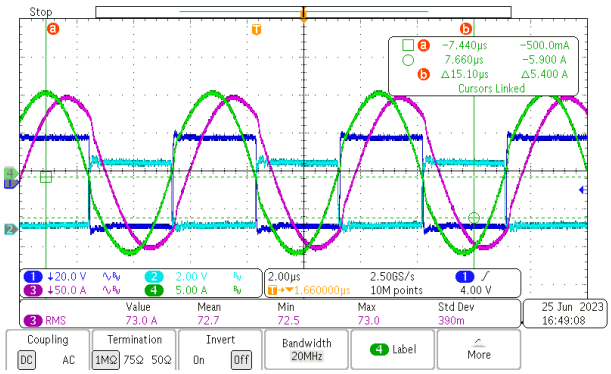
CH1: Primary VGS, CH2: Primary Tank Current,
CH3: Primary VDS, CH4: Secondary Tank Current

Figure 3-2. Charging Mode, 400 V_{IN}, 48 V_{OUT}, 3000 W



CH1: Primary VDS, CH2: Primary VGS,
CH3: Primary Tank Current, CH4: Secondary Tank Current

Figure 3-3. Discharging Mode, 400 V_{IN}, 48 V_{OUT}, 1800 W

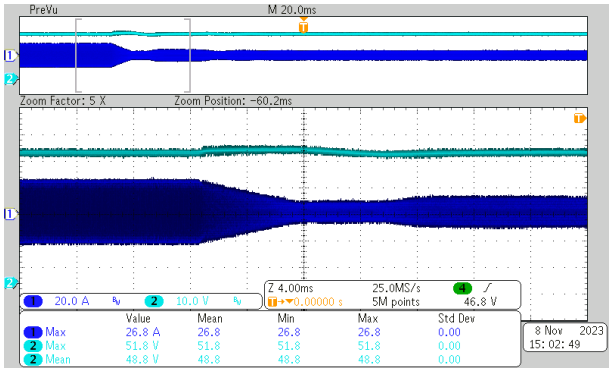


CH1: Primary VDS, CH2: Primary VGS,
CH3: Primary Tank Current, CH4: Secondary Tank Current

Figure 3-4. Discharging Mode, 400 V_{IN}, 48 V_{OUT}, 2800 W

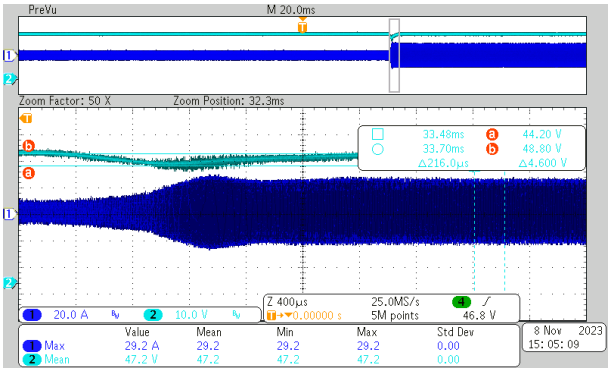
3.2 Load Transients

Load transient response is shown in the following figures.



CH1: Primary Tank Current, CH2: Output Voltage

Figure 3-5. 400 V_{IN}, 48 V_{OUT}, 50% Load to 5% Load Transient

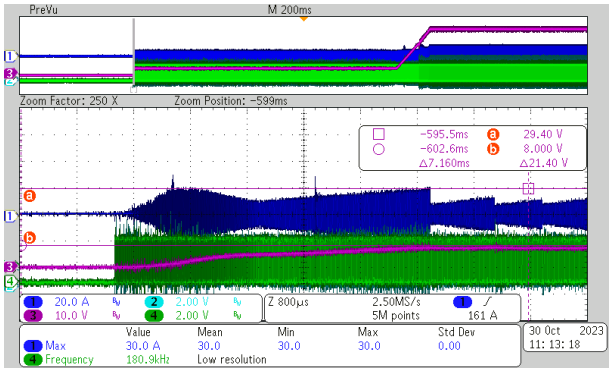


CH1: Primary Tank Current, CH2: Output Voltage

Figure 3-6. 400 V_{IN}, 48 V_{OUT}, 5% Load to 50% Load Transient

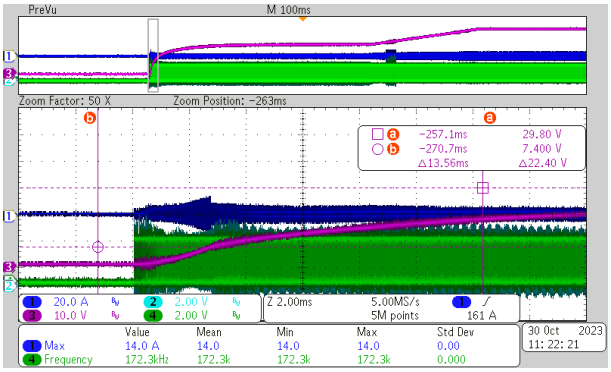
3.3 Start-Up Sequence

Start-up behavior is shown in the following figures.



CH1: Primary Tank Current, CH2 and CH4: Primary VGS, CH3: Output Voltage

Figure 3-7. Start-Up in Charging Mode With 15-A Load Current



CH1: Primary Tank Current, CH2 and CH4: Primary VGS, CH3: Output Voltage

Figure 3-8. Start-Up in Charging Mode With 0-A Load Current

3.4 Dynamic Response

The dynamic response waveform is shown in the following figure.

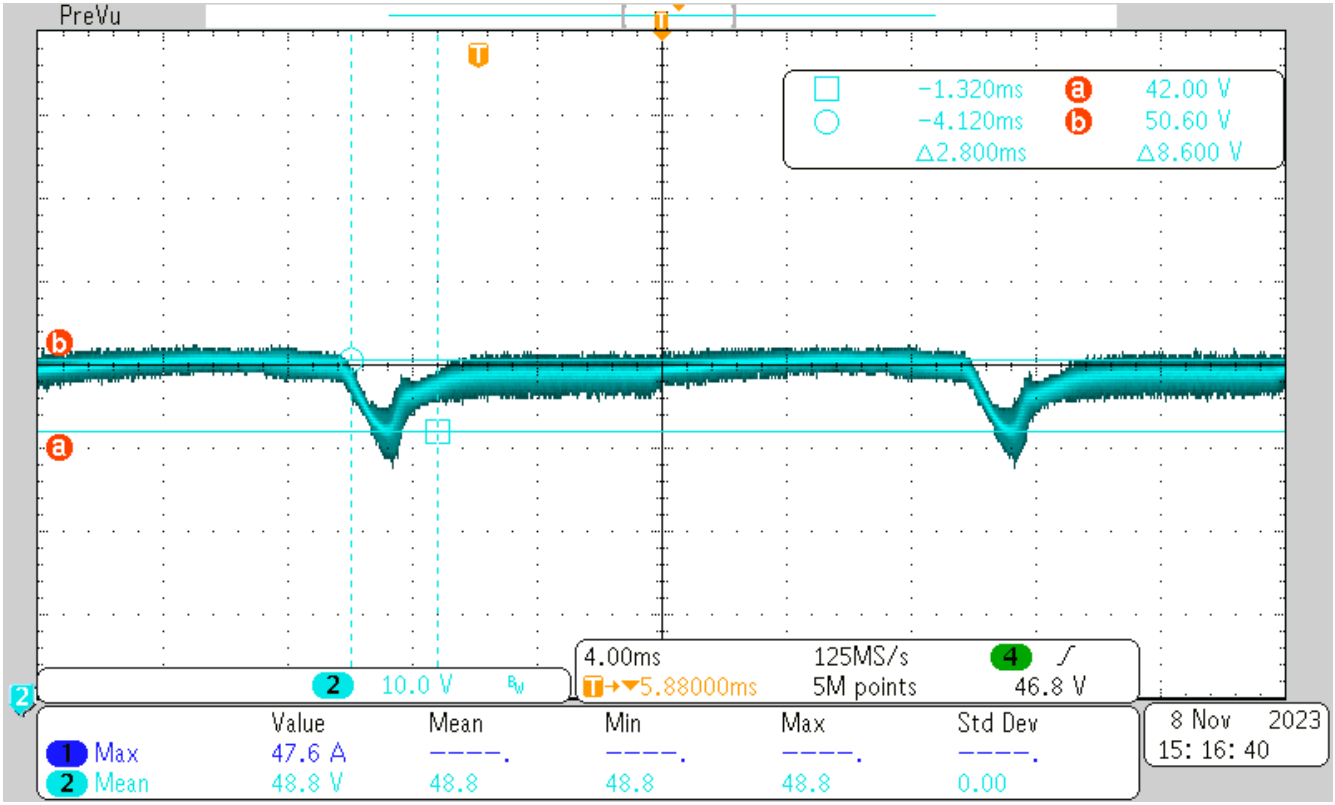
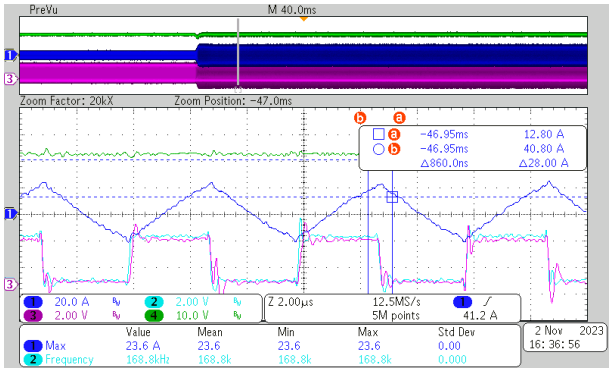


Figure 3-9. 400 V_{IN}, 48 V_{OUT}, 0% Load to 50% Load

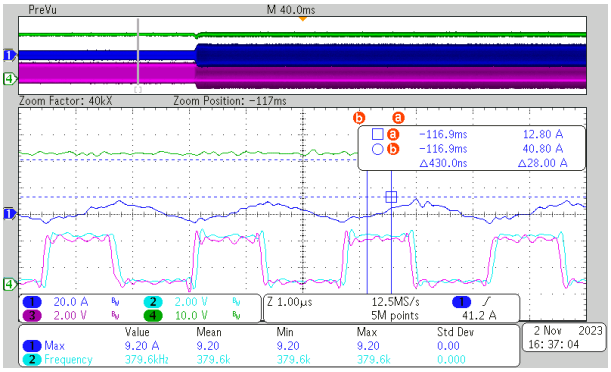
3.5 Mode Transition

Phase shift mode and frequency mode transition waveforms are shown in the following figures.



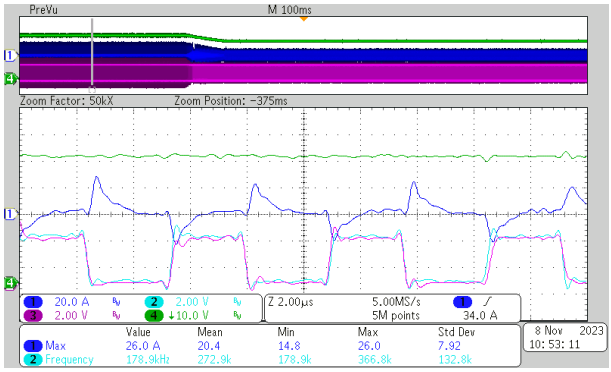
CH1: Primary Tank Current, CH2 and CH3: Primary VGS, CH4:Output Voltage

Figure 3-10. Frequency Mode With 48 V_{OUT}, 5-A Load Current, 169-kHz Switching Frequency



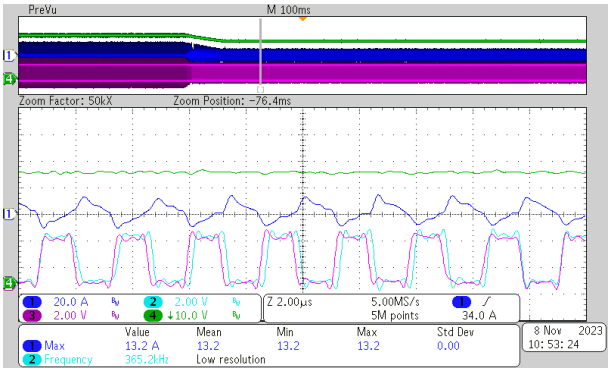
CH1: Primary Tank Current, CH2 and CH3: Primary VGS, CH4:Output Voltage

Figure 3-11. Phase Shift Mode With 48 V_{OUT}, 1-A Load Current, 380-kHz Switching Frequency



CH1: Primary Tank Current, CH2 and CH3: Primary VGS, CH4:Output Voltage

Figure 3-12. Frequency Mode With 48 V_{OUT}, 2-A Load Current, 179-kHz Switching Frequency



CH1: Primary Tank Current, CH2 and CH3: Primary VGS, CH4:Output Voltage

Figure 3-13. Phase Shift Mode With 42 V_{OUT}, 2-A Load Current, 380-kHz Switching Frequency

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