This user's guide describes the features and operation of the bq24133EVM Evaluation Module (EVM). The EVM assists users in evaluating the bq24133 synchronous battery charger. The EVM is also called the HPA715A. The manual includes the bq24133EVM bill of materials, board layout, and schematic.

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1 Introduction

1.1 EVM Features
- Evaluation module for bq24133
- Stand-alone synchronous switch-mode, battery-charge controller
- Integrated N-MOSFETs and power path selector
- CELL pin setting up to 12.6-V battery voltage; 1, 2, or 3 cells with 4.2 V/cell
- Input operating range: 4.5 V–16 V
- LED indication for charge status
- Test points for key signals available for testing purposes; easy probe hook-up.
- Jumpers available; easy-to-change setting

1.2 General Description
The bq24133 is highly integrated stand-alone Li-ion and Li-polymer switch-mode battery charge controllers with two integrated N-channel power MOSFETs and power path selector gate driver. It offers a constant-frequency synchronous PWM controller with high accuracy regulation of input current, charge current and voltage. It also provides battery detection, pre-conditioning, charge termination, and charge status monitoring.

The bq24133 automatically enters a low-quiescent current sleep mode when the input voltage falls below the battery voltage. The bq24133 charges one, two or three cells (selected by CELL pin), supporting up to a 2.5-A charge current. The bq24133 is available in a 24-pin, 3.5 x 5.5 mm², thin QFN package.

For details, see the bq24133 data sheet (SLUSA7).

1.3 I/O Description

<table>
<thead>
<tr>
<th>Jack</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1–VIN</td>
<td>Positive input</td>
</tr>
<tr>
<td>J1–PGND</td>
<td>Negative input</td>
</tr>
<tr>
<td>J2–VSY</td>
<td>Connected to system</td>
</tr>
<tr>
<td>J2–VBAT</td>
<td>Connected to charger output</td>
</tr>
<tr>
<td>J2–PGND</td>
<td>Ground</td>
</tr>
<tr>
<td>J2–TS_EXT</td>
<td>Temperature qualification voltage Input</td>
</tr>
</tbody>
</table>
1.4 Control and Key Parameters Settings

Table 2. Control and Key Parameters Settings

<table>
<thead>
<tr>
<th>Jack</th>
<th>Description</th>
<th>Factory Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1</td>
<td>Select external TS input or internal valid TS setting</td>
<td>Jumper ON 1-2 (external TS)</td>
</tr>
<tr>
<td></td>
<td>1-2 : External TS input</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2-3 : Internal valid TS setting</td>
<td></td>
</tr>
<tr>
<td>JP2</td>
<td>The pullup power source supplies the LEDs when JP2 is ON. LED has no power source when JP2 is OFF.</td>
<td>Jumper ON (LED power available)</td>
</tr>
<tr>
<td>JP3</td>
<td>TTC setting</td>
<td>Jumper OPEN (enable timer and termination)</td>
</tr>
<tr>
<td></td>
<td>2-3 : Connect TTC to VREF to enable termination and disable timer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1-2 : Connect TTC to GND to disable termination and disable timer</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OPEN : Enable timer and termination</td>
<td></td>
</tr>
<tr>
<td>JP4</td>
<td>Charger enable/disable setting. ISET is pulled to GND and the charger is disabled when JP4 OPEN; charger is enabled when JP4 is ON.</td>
<td>Jumper OPEN (disable charger)</td>
</tr>
<tr>
<td>JP5</td>
<td>CELL selection</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1-2 : CELL-GND, 1CELL</td>
<td>Jumper ON 1-2 (1 CELL) -001</td>
</tr>
<tr>
<td></td>
<td>2-3 : CELL-VREF, 3CELL</td>
<td>Jumper ON 2-3 (3 CELL) -002</td>
</tr>
<tr>
<td></td>
<td>OPEN : CELL- FLOAT, 2CELL</td>
<td></td>
</tr>
</tbody>
</table>

1.5 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BUS}$</td>
<td>Input voltage</td>
<td>4.5</td>
<td>8 V</td>
<td>8.4</td>
<td></td>
<td>001</td>
</tr>
<tr>
<td>$V_{BUS}$</td>
<td>Input voltage</td>
<td>6</td>
<td>18 V</td>
<td>12.6</td>
<td></td>
<td>002</td>
</tr>
<tr>
<td>$V_{BAT}$</td>
<td>Voltage applied at VBAT terminal of J2</td>
<td>2.1</td>
<td>4.2</td>
<td>12.6</td>
<td>V</td>
<td>001</td>
</tr>
<tr>
<td>$V_{BAT}$</td>
<td>Voltage applied at VBAT terminal of J2</td>
<td>2.1</td>
<td>4.2</td>
<td>12.6</td>
<td>V</td>
<td>002</td>
</tr>
<tr>
<td>Supply current</td>
<td>Maximum input current</td>
<td>0</td>
<td>5 A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charge current, $I_{chg}$</td>
<td>Battery charge current</td>
<td>0</td>
<td>2 A</td>
<td>2.5</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Operating junction temperature range, $T_J$</td>
<td></td>
<td>0</td>
<td>125 °C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The bq2410 EVM board requires a regulated supply approximately 1 V minimum above the regulated voltage of the battery pack to a maximum input voltage of 16 Vdc. The bq24133 uses the CELL pin to select the number of cells with a fixed 4.2 V/cell. Connecting CELL to AGND gives a 1-cell configuration, a floating CELL pin gives a 2-cell configuration, and connecting to VREF gives a 3-cell configuration. The CELL pin adjusts the internal resistor voltage divider from the BAT pin to AGND pin for voltage feedback and regulate to internal 2.1-V voltage reference.

<table>
<thead>
<tr>
<th>CELL Pin</th>
<th>Voltage Regulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>4.2V</td>
</tr>
<tr>
<td>Floating</td>
<td>8.4V</td>
</tr>
<tr>
<td>VREF</td>
<td>12.6V</td>
</tr>
</tbody>
</table>

For Note 001, the BAT voltage is set to 4.2 V and for Note 002, the BAT voltage is set to 12.6 V.

The ISET input sets the maximum charging current. Battery current is sensed by current sensing resistor $R_{SR}$ connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 40 mV maximum. The equation for charge current is:

$$I_{charge} = \frac{V_{ISET}}{20 \times R_{15}}$$

(1)

For bq24133, the precharge current is set as 1/10 of the fast-charge rate set by ISET voltage, according to the formula.
The default setting is 2 Adc for fast-charge current and 0.2 Adc for precharge current.

In the bq24133, once the voltage on OVPSET is above the 1.6-V ACOV threshold or below the 0.5-V ACUV threshold, the charge is disabled, and the battery is switched to the system instead of the adapter.

\[
V_{ACUV} = 0.5\, V \times \left( 1 + \frac{R_6}{R_9} \right)
\]

For Note 001, ACUV = 2.51 V; for Note 002, ACUV = 5.87 V.

\[
V_{ACOV} = 1.6\, V \times \left( 1 + \frac{R_6}{R_9} \right)
\]

For Note 001, ACOV = 8.03 V; for Note 002, ACOV = 18.80 V.

Similar to setting battery regulation current, the adapter current is set by the voltage on ACSET pin using the following equation:

\[
I_{DPM} = \frac{V_{ACSET}}{20 \times R_2}
\]

The default setting on the EVM is 3 Adc for adapter current regulation.
2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA715A evaluation board. On the test procedure the following naming conventions are followed.

VXXX : External voltage supply name (VIN, VBAT, VTS)
LOADW: External load name (LOADR, LOADI)
V(TPyyyy): Voltage at internal test point TPyyyy. For example, V(TP1) means the voltage at TP1.
V(jxx): Voltage at jack terminal Jxx.
V(TP(XXX)): Voltage at test point XXX. For example, V(ACSET) means the voltage at the test point which is marked as ACSET.
V(XXX, YYY): Voltage across point XXX and YYY.
I(JXX(YYY)): Current going out from the YYY terminal of jack XX.
Jxx(BBB): Terminal or pin BBB of jack xx
Jxx ON : Internal jumper Jxx terminals are shorted
Jxx OFF: Internal jumper Jxx terminals are open
Jxx (-YY-) ON: Internal jumper Jxx adjacent terminals marked as YY are shorted
Measure:→A,B Check specified parameters A, B. If measured values are not within specified limits, the unit under test has failed.
Observe: →A,B Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points, and individual components.

2.2 Safety

1. Safety Glasses are to be worn.
2. This test must be performed by qualified personnel who are trained in electronics theory and understand the risks and hazards of the assembly to be tested.
3. ESD precautions must be followed while handling electronic assemblies and performing this test.
4. Precautions must be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

2.3 Quality

1. Test data can be made available on request from Texas Instruments.

2.4 Safety Apparel

1. Electrostatic smock
2. Electrostatic gloves or finger cots
3. Safety glasses
4. Ground ESD wrist strap.
2.5 **Equipment**

2.5.1 **Power Supplies**

Power Supply #1 (PS#1): a power supply capable of supplying 30 V at 5 A is required.

2.5.2 **Loads**

LOAD#1 A 30-V (or greater), 5-A (or greater) electronic load that can operate at constant current and constant voltage mode.

LOAD#2: An HP 6060B 3-V to 60-V/0-A to 60-A, 300-W system dc electronic load or equivalent.

2.5.3 **Meters**

Seven Fluke 75 multimeters (equivalent or better) or four equivalent voltage meters and three equivalent current meters.

The current meters must be capable of measuring 5-A+ current.

2.6 **Equipment Setup**

1. Set the Power Supply #1 (PS#1) for 6-V ±200-mVdc (001), or 16-V ±0.200-mV (002), 4.5-A ±0.1-A current limit, and then turn off supply.
2. Connect the output of PS#1 in series with a current meter (multimeter) to J1 (VIN, PGND).
3. Connect a voltage meter across J1 (VIN, PGND).
4. Connect Load#1 in series with a current meter to J2 (VBAT, PGND). Turn off Load#1.
5. Connect Load#2 in series with a current meter to J2 (VSYS, PGND). Turn off Load#2.
6. Connect a voltage meter across J2 (VBAT, PGND).
7. Connect a voltage meter across J2 (VSYS, PGND).

![Figure 1. Original Test Setup for HPA715A (bq24133EVM)](image-url)
2.7 **Procedure**

Disconnect the load and power supply. Use diode-function of multimeter to check the resistance between J1-VIN and J2-VSYS. Pass only if both OPEN for bi-direction (positive J1-VIN and negative on J2-VSYS; negative J1-VIN and positive on J2-VSYS).

2.7.1 **Power Supply and VREF**

Make sure that Section 2.6 steps are followed.

Disconnect LOAD#1#2. Turn on PS#1 (6 V for 001 and 16 V for 002).

**Measure →**
- V(J2(VSYS)) = 6 V ±500 mV (001)
- V(J2(VSYS)) = 16 V ±500 mV (002)

**Measure →**
- V(J2(VBAT)) = 0.5 V ±500 mV

**Measure →**
- V(TP(VREF)) = 3.3 V ±200 mV

**Measure →**
- V(TP(REGN)) = 0.5 V ±500 mV

2.7.2 **Charger Enable and Battery Detection**

Connect 2-3 of JP1 (Internal TS); short JP4 (Charger Enable)

**Measure →**
- V(TP(VREF)) = 3.3 V ±200 mV

**Measure →**
- V(TP(REGN)) = 6 V ±200 mV

**Observe →**
- V(J2(VBAT)) = 4.2 V ±200 mV (001)
  - V(J2(VBAT)) = 12.6 V ±200 mV (002)

**Observe →**
- D1 (/STAT) BLINK

2.7.3 **Charge Current/Voltage Regulation and Battery Temperature Qualification**

Reconnect LOAD#2, and turn on. Use the constant voltage mode. Set the output voltage to 2.5 V for 001 and 8 V for 002.

**Measure →**
- I(J2(VBAT)) = 0.2 A ±100 mA

**Observe →**
- D1 (/STAT) ON

Increase the voltage of LOAD#2 to 3.5 V for 001 and 10.5 V for 002.

**Measure →**
- I(J2(VBAT)) = 2 A ±200 mA

**Observe →**
- D1 (/STAT) ON

Open 2-3 of JP1 (External TS)

**Measure →**
- I(J2(VBAT)) = 0 A ±100 mA

**Observe →**
- D1 (/STAT) BLINK

Connect 2-3 of JP1 (Internal TS)

**Measure →**
- I(J2(VBAT)) = 2 A ±200 mA

**Observe →**
- D1 (/STAT) ON

2.7.4 **Charger Termination and Recharge**

Increase the voltage of LOAD#2 slowly to approximately 4.2 V for Note 001 and 12.6 V for Note 002.

**Observe →**
- I(J2(VBAT)) decreases from 2 A while V(J2(VBAT)) becomes constant.

**Observe →**
- I(J2(VBAT)) drops to zero when LOAD#2 current is less than 0.2 A.
Decrease the voltage of LOAD#2 slowly to approximately 3.5 V for Note 001 and 10.5 V for Note 002.  
*Measure →* \( I(J2(VBAT)) = 2 \text{ A} \pm 200 \text{ mA} \).  
*Observe →* D1 (/STAT) ON.

### 2.7.5 OVP - Input Overvoltage Protection

Increase the voltage of PS#1 to 9 V for Note 001 or 20 V for Note 002.  
*Measure →* \( I(J1(VIN)) = 0 \text{ A} \pm 200 \text{ mA} \).  
*Observe →* D1 (/STAT) BLINK.

### 2.7.6 DPM - Input Current Regulation

Connect the output of the Load#1 in series with a current meter (multimeter) to J2 (SYS, PGND). Ensure that a voltage meter is connected across J2 (SYS, PGND). Resume other status as in Section 2.7.3.

Turn on the power of Load#1. Set the load current to 0.5 A. Increase the load current until \( I(J1(VIN)) = 3 \text{ A} \).

*Observe →* \( I(J2(VBAT)) \) decreases from 3 A to 0 A and \( I(J1(VIN)) \) keeps 3 A unchanged.

### 2.7.7 Test Complete

Turn off the power supply, and remove all connections from the unit under test (UUT).
3 PCB Layout Guideline

1. It is critical that the exposed thermal pad on the backside of the bq24133 package be soldered to the PCB ground. Ensure that sufficient thermal vias are right underneath the IC, connecting to the ground plane on the other layers.

2. The control stage and the power stage must be routed separately. At each layer, the signal ground and the power ground are connected only at the thermal pad.

3. Charge current sense resistor must be connected to SRP and SRN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins must be placed as close to the IC as possible.

4. Input current sense resistor must be connected to ACP, ACN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.

5. Decoupling capacitors for VREF, AVCC, and REGN must make the interconnections to the IC as short as possible.

6. Decoupling capacitors for BAT must be placed close to the corresponding IC pins, and make the interconnections to the IC as short as possible.

7. Decoupling capacitor(s) for the charger input must be placed close to SW and PGND.

8. Take the EVM layout for design reference.
## 4.1 Bill of Materials

Table 4. Bill of Materials

<table>
<thead>
<tr>
<th>Count</th>
<th>RefDes</th>
<th>Value</th>
<th>Description</th>
<th>Size</th>
<th>Part Number</th>
<th>MFR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C1, C7, C14, C15</td>
<td>10 µF</td>
<td>Capacitor, Ceramic, 25V, X7R, 10%</td>
<td>1206</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>1</td>
<td>C2</td>
<td>Open</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>C3</td>
<td>2.2 µF</td>
<td>Capacitor, Ceramic, 25V, X7R, 10%</td>
<td>0805</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>1</td>
<td>C4</td>
<td>1.0 µF</td>
<td>Capacitor, Ceramic, 25V, X7R, 10%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>1</td>
<td>C5, C18</td>
<td>0.047 µF</td>
<td>Capacitor, Ceramic, 50V, X7R, 10%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>3</td>
<td>C8, C16, C17</td>
<td>1.0 µF</td>
<td>Capacitor, Ceramic, 25V, X7R, 10%</td>
<td>0805</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>1</td>
<td>C9</td>
<td>4700 pF</td>
<td>Capacitor, Ceramic, 25V, X7R, 10%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>3</td>
<td>C10, C20, C24</td>
<td>0.1 µF</td>
<td>Capacitor, Ceramic, 50V, X7R, 10%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>0</td>
<td>C11, C12, C21, C23</td>
<td>Open</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>C22, C19</td>
<td>1.0 µF</td>
<td>Capacitor, Ceramic, 25V, X7R, 20%</td>
<td>0805</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>LTST-C190GKT Diode, LED, Green, 2.1V, 20mA, 6mcd</td>
<td>0603</td>
<td>LTST-C190GKT</td>
<td>Lite On</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>D2</td>
<td>BAT54C Diode, Dual Schottky, 200-mA, 30-V</td>
<td>SOT23</td>
<td>BAT54C-V-G</td>
<td>Vishay</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J1</td>
<td>ED120/2DS Terminal Block, 2 pin, 15A, 5.1mm</td>
<td>0.40 x 0.35 inch</td>
<td>ED120/2DS</td>
<td>OST</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>J2</td>
<td>ED120/4DS Terminal Block, 4 pin, 15A, 5.1mm</td>
<td>0.80 x 0.35 inch</td>
<td>ED120/4DS</td>
<td>OST</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>JP1, JP3, JP5</td>
<td>PEC03SAAN Header, 3 pin, 100mil spacing</td>
<td>0.100 inch x 3</td>
<td>PEC03SAAN</td>
<td>Sullins</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>JP2, JP4</td>
<td>PEC02SAAN Header, 2 pin, 100mil spacing</td>
<td>0.100 inch x 2</td>
<td>PEC02SAAN</td>
<td>Sullins</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>3.3 µH</td>
<td>Inductor, SMT, 5A, 55milliohm</td>
<td>0.204 x 0.216 inch</td>
<td>IHLP2020CZER3R3M01</td>
<td>Vishay</td>
</tr>
<tr>
<td>1</td>
<td>Q1</td>
<td>BSS138W MOSFET, Nch, 30V, 0.5A, 700 milliohms</td>
<td>SOT323</td>
<td>BSS138W-7-F</td>
<td>Diodes Inc</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Q2, Q3</td>
<td>CSD17313Q2 Trans, Nch, 30V, 5A, 26milliohm</td>
<td>SON-6</td>
<td>CSD17313Q2</td>
<td>TI</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Q4</td>
<td>CSD25302Q2 Trans, Pch NexFET, 20V, 5 A, 56 milliohm</td>
<td>SON-6</td>
<td>CSD25302Q2</td>
<td>TI</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Q5</td>
<td>2N7002 MOSFET, N-ch, 60V, 115mA, 1.2Ohms</td>
<td>SOT23</td>
<td>2N7002-7-F</td>
<td>Diodes Inc</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>1.00M</td>
<td>Resistor, Chip, 1/16W, 5%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>1</td>
<td>R2</td>
<td>0.02 Ω</td>
<td>Resistor, Chip, 1/2 watt, 1%</td>
<td>1206</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>4</td>
<td>R3, R16, R20, R29</td>
<td>0</td>
<td>Resistor, Chip, 1/16W</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>2</td>
<td>R4, R5</td>
<td>3.9</td>
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<td>1206</td>
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<td>1</td>
<td>R6</td>
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<td>Resistor, Metal Film, 1/2 watt, 1%</td>
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<td>R17</td>
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<td>1</td>
<td>R19</td>
<td>10</td>
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<td>STD</td>
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<td>5.23k</td>
<td>Resistor, Chip, 1/16W, 1%</td>
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<td>STD</td>
<td>STD</td>
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<td>1</td>
<td>R22</td>
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<td>R23</td>
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<td>STD</td>
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<td>1</td>
<td>R25</td>
<td>3.01M</td>
<td>Resistor, Chip, 1/16W, 1%</td>
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### Table 4. Bill of Materials (continued)

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<th>Count</th>
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<th>Value</th>
<th>Description</th>
<th>Size</th>
<th>Part Number</th>
<th>MFR</th>
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<td>R26</td>
<td>10k</td>
<td>Resistor, Chip, 1/16W, 5%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
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<td>1</td>
<td>R27</td>
<td>4.99k</td>
<td>Resistor, Chip, 1/16W, 1%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
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<tr>
<td>2</td>
<td>R28, R31</td>
<td>100k</td>
<td>Resistor, Chip, 1/16W, 1%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
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<td>R30</td>
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<td>Resistor, Chip, 1/16W, 1%</td>
<td>0603</td>
<td>STD</td>
<td>STD</td>
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<td>STD</td>
<td>STD</td>
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<tr>
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<td>R32</td>
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<td>0603</td>
<td>STD</td>
<td>STD</td>
</tr>
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<td>0</td>
<td>TP1, TP3–TP6</td>
<td>0.100 x 0.100 inch</td>
<td>Test Point, 0.020 Hole</td>
<td>N/A</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>TP2</td>
<td>131-5031-00</td>
<td>Adaptor, 3.5-mm probe clip</td>
<td>0.200 inch</td>
<td>131-4244-00 or 131-5031-00</td>
<td>Tektronix</td>
</tr>
<tr>
<td>13</td>
<td>TP7 - TP19</td>
<td>0.100 x 0.100 inch</td>
<td>Test Point, White, Thru Hole Color Keyed</td>
<td>5002</td>
<td>Keystone</td>
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</tr>
<tr>
<td>1</td>
<td>TP20</td>
<td>5001</td>
<td>Test Point, Black, Thru Hole Color Keyed</td>
<td>0.100 x 0.100 inch</td>
<td>5001</td>
<td>Keystone</td>
</tr>
<tr>
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<td>U1</td>
<td>BQ24133RHL</td>
<td>IC, Power Path Selector Stand-alone Charger</td>
<td>VQFN</td>
<td>BQ24133RHL</td>
<td>TI</td>
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<tr>
<td>1</td>
<td>—</td>
<td>—</td>
<td>PCB, 2.65 In x 3.00 In x 0.062 In</td>
<td>HPA715</td>
<td>Any</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>—</td>
<td>—</td>
<td>Shunt, 100-mil, Black</td>
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<td>929950-00</td>
<td>3M</td>
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<tr>
<td>1</td>
<td>—</td>
<td>—</td>
<td>Label (See Note 5)</td>
<td>1.25 x 0.25 inch</td>
<td>THT-13-457-10</td>
<td>Brady</td>
</tr>
</tbody>
</table>

**Notes:**

1. These assemblies are ESD sensitive; ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants.
   Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk (**) cannot be substituted.
   All other components can be substituted with equivalent MFG’s components.
5. Install label after final wash. Text shall be 8 pt font. Text shall be per Table 1.

### Table 1

<table>
<thead>
<tr>
<th>Assembly Number</th>
<th>Text</th>
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</thead>
<tbody>
<tr>
<td>HPA715-001</td>
<td>BQ24133EVM-715-5V</td>
</tr>
<tr>
<td>HPA715-002</td>
<td>BQ24133EVM-715-15V</td>
</tr>
</tbody>
</table>
4.2 Board Layout

Figure 2. Top Assembly
Figure 3. Top Layer
Figure 4. Second Layer
Figure 5. Third Layer
Figure 6. Bottom Layer
Figure 7. Bottom Assembly
4.3 Schematic

Figure 8. bq24133EVM Schematic
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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 20 V and the output voltage range of 0 V to 12.6 V. Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User’s Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User’s Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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