

bq25504 EVM – Ultra Low Power Boost Converter with Battery Management for Energy Harvester Applications

This user's guide describes the bq25504 evaluation module (EVM), how to perform a stand-alone evaluation and allows the EVM to interface with the system and host. This EVM is programmed from the factory for settings compatible with most MCU's and 3V coin cell batteries. The EVM is programmed to deliver a 3.1VDC maximum voltage (OV) for charging the storage element and the under voltage is programmed to 2.2VDC. The VBAT_OK indicator toggles high when VSTOR ramps up to 2.8VDC and toggles low when VSTOR ramps down to 2.4VDC.

Contents

1	Introduction	2
	1.1 EVM Features	2
	1.2 General Description	2
	1.3 Design and Evaluation Considerations	3
2	Performance Specification Summary	4
3	Test Summary	4
	3.1 Equipment	4
	3.2 Equipment and EVM Setup	4
	3.3 Test procedures	5
4	PCB Layout Guideline	11
5	Bill of Materials, Board Layout and Schematics	12
	5.1 Bill of Materials	12
	5.2 EVM Board Layout	13
	5.3 EVM Schematic	15

List of Figures

1	Test Setup for HPA674A (bq25504 EVM)	5
2	Startup with no Battery and 10k Load.....	6
3	Startup with Battery Less Than UV.....	7
4	Powering up with a Battery above UV	7
5	BAT_OK High/Low 2.8V/2.34V – Ramping Battery from 0V to 3.1V (OV) and Down to 1.8V.....	8
6	Basic Switching Converter, Vin = 1V, Vbat = 2.5V	9
7	EVM Operation Near OV With 100-Ω Battery Impedance	10
8	EVM PCB Top Assembly.....	13
9	EVM PCB Top Layer	13
10	EVM PCB Bottom Layer.....	14
11	EVM Schematic.....	15

List of Tables

1	I/O Connections and Configuration for Evaluation of bq25504 EVM.....	4
2	Bill of Materials.....	12

1 Introduction

1.1 EVM Features

- Evaluation module for bq25504
- Ultra low power boost converter/charger with battery management for energy harvester applications
- Resistor-programmable settings for under voltage, over voltage providing flexible battery management; POTs Included for fine tuning the settings (not populated)
- Programmable push-pull output Indicator for battery status (VBAT_OK)
- Test points for key signals available for testing purpose – easy probe hook-up.
- Jumpers available – easy to change settings

1.2 General Description

The bq25504 is the first of a new family of intelligent integrated energy harvesting Nano-Power management solutions that are well suited for meeting the special needs of ultra low power applications. The product is specifically designed to efficiently acquire and manage the microwatts (μW) to milliwatts (mW) of power generated from a variety of DC sources like photovoltaic (solar) or thermal electric generators. The bq25504 is the first device of its kind to implement a highly efficient boost converter/charger targeted toward products and systems, such as wireless sensor networks (WSN) which have stringent power and operational demands. The design of the bq25504 starts with a DC-DC boost converter/charger that requires only microwatts of power to begin operating. Once started, the boost converter/charger can effectively extract power from low voltage output harvesters such as thermoelectric generators (TEGs) or single / dual cell solar panels. The boost converter can be started with V_{IN} as low as 330 mV typ., and once started, can continue to harvest energy down to $V_{\text{IN}} \approx 100$ mV.

The bq25504 also implements a programmable maximum power point tracking (MPPT) sampling network to optimize the transfer of power into the device. The MPP is listed by the harvesting manufacturer as a percentage of its open circuit (OC) voltage. Typically solar cells are at their MPP when loaded to ~80% of their OC voltage. The bq25504 periodically samples the open circuit input voltage by disabling the boost converter (approximately every 16 seconds) and stores the programmed MPP ratio of the OC voltage on the external reference capacitor, C5. If the storage element is less than the maximum voltage (OV) then the boost converter will load the harvesting source until it reaches the MPP (C5 voltage reference) and then regulate the input voltage of the converter, thus transferring the maximum amount of power to the output. Alternatively, an external reference voltage can be provided, by a MCU to the REFS pin, to adjust C5 independently. The shunt on JP1 has to be moved from the Divider setting to STOR when providing this external reference (JP1-2 tied to JP1-1 – OSC/STOR).

The bq25504 was designed with the flexibility to support a variety of energy storage elements. The availability of the sources from which harvesters extract their energy can often be sporadic or time-varying. Systems will typically need some type of energy storage element, such as a re-chargeable battery, super capacitor, or conventional capacitor. The storage element will make certain constant power is available when needed for the systems. The storage element also allows the system to handle any peak currents that can not directly come from the input source.

To prevent damage to a customer's storage element, both maximum and minimum voltages are monitored against the user programmed under-voltage (UV) and over-voltage (OV) levels.

To further assist users in the strict management of their energy budgets, the bq25504 toggles the battery good flag to signal the microprocessor when the voltage on an energy storage element or capacitor has dropped below a pre-set critical level. This should trigger the shedding of load currents to prevent the system from entering an under voltage condition.

The OV, UV and battery good thresholds are programmed independently. The EVM has three 500K Ω potentiometers (not installed at factory) to allow fine tuning of the three programmable thresholds. This only need be done if the user needs precision, the POTs provide about ± 50 mV shift.

For details, see bq25504 data sheet ([SLUSAH0](#)).

1.3 Design and Evaluation Considerations

This user's guide is not a replacement for the data sheet. Reading the data sheet first will help in understanding the operations and features of this IC. Be sure to make note of the capacitor selection section when designing the EVM. Many of the IC's pin names start with a "V" and this "V" is removed on the EVM connector's label. The names are interchangeable.

This IC is a highly efficient charger for a storage element such as a battery or super capacitor. In this document, "battery" will be used but one could substitute any appropriate storage element. The main difference between a battery and a super capacitor is the capacity curve. The battery typically has little or no capacity below a certain voltage, where as the capacitor does have capacity at lower voltages.

In the lab when using a lab power supply rather than an energy harvester, one will have the output of the lab supply, V_{source} , followed by the harvester's impedance (about 20Ω) and connected to V_{IN} of the EVM. These two signals are separated by the 20Ω source impedance which represents the internal impedance of the source. V_{IN} is equal to V_{Source} when there is no load (open circuit) and is pulled down to the MPPT harvester threshold when the charger is able to deliver the maximum power before reaching OV.

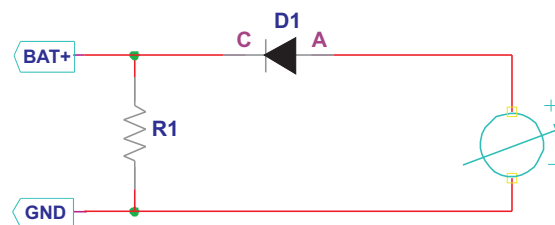
The over voltage (OV) setting initially is lower than the programmed value at startup (varies on conditions) and is updated after the first $\sim 32ms$. Subsequent updates are every $\sim 64ms$. The OV threshold is the reference for maximum voltage on VSTOR and the boost converter will stop switching if the voltage on VSTOR reaches the OV reference. The UV is checked every $\sim 64ms$ to determine if the BAT FET should be on or off. The open circuit (OC) input voltage is measured every ~ 16 seconds which is used to calculate the Maximum Power Point Tracking (MPPT) threshold (programmed with resistors to 78% at the factory). This periodic update continually optimizes maximum power delivery based on the harvesting conditions.

Harvesting ultra low power energy requires a different mind set when designing a system. Often there is not enough real time input harvested power to run the system in full operation so energy is collected over a period of time, stored in a battery and then used periodically to power the system.

The designer needs to define a "Battery OK" threshold and battery discharged threshold (Not OK) to allow successful system operation. The BAT_OK high/low threshold are programmed at the factory to 2.8V and 2.4V using resistors R7, R8, and R9. A BAT_OK high signal would typically indicate to the host that the battery is above 2.8V and ready to use and if low would indicate that the cell is discharged such that the system load should be reduced or disabled. The BAT_OK signal is checked every 64ms.

The quiescent current, which is basically the current from the battery to the IC, can be measured at the STOR pin. To measure the current the user should connect a $100k\Omega$ resistor to J5-2 (STOR) and connect a 3V supply from the other end of this resistor to the ground of the EVM. A $10M\Omega$ meter can be used to measure the voltage drop across the resistor and calculate the current. No other connections should be made to the EVM and the measurement should be taken after steady state conditions are reached (may take a few minutes). The reading should be in the range of 375nA.

The battery (storage element) can be replaced with a simulated battery. Often electronic 4 quadrant loads give erratic results with a "battery charger" due to the charger changing states (fast-charge to termination and refresh) while the electronic load is changing loads to maintain the "battery" voltage. The charging and loading get out of phase and creates a large signal oscillation which is due to the 4 quadrant meter. A simple circuit can be used to simulate a battery and works well and can quickly be adjusted for voltage. It consists of load resistor ($\sim 10\Omega$, 2W) to pull the output down to some minimum storage voltage (sinking current part of battery) and a lab supply connected to the BAT pin via a diode. The lab supply biases up the battery voltage to the desired level. It may be necessary to add more capacitance across R1.



2 Performance Specification Summary

See Data Sheet “Recommended Operating Conditions” for component adjustments. For details about the resistor programmable settings, see bq25504 data sheet ([SLUSAH0](#)).

		MIN	NOM	MAX	UNIT
V _{IN} (DC)	DC input voltage into VIN_DC	0.13		3.0	V
V _{IN_Start-up} (DC)	DC minimum Start-up Voltage		330		mV
V _{OV}	Over Voltage – Sets maximum output voltage	2.9	3.1	3.3	V
V _{UV}	Under voltage setting for shorting VSTOR to VBAT	2.1	2.2	2.3	V
V _{BAT_OK}	VBAT_OK indication toggles high when VSTOR ramps up	2.65	2.8	2.95	V
	VBAT_OK indication toggles low when VSTOR ramps down	2.25	2.4	2.55	V
MPPT	Maximum Power Point Tracking, Programmed % of Open Circuit Voltage		78%		
C _{BAT}	Battery Pin Capacitance or equivalent battery capacity	100			μF

3 Test Summary

3.1 Equipment

Power Supplies

Power Supply #1 (PS#1): Adjustable 5V Power supply with Current Limit of 100mA.

Power Supply #2 (PS#2): Adjustable 5V Power supply with 20Ω series impedance (can just be a discrete resistor) with Current Limit of 100mA.

Loads

Load #1: 10kΩ, 5%, 0.25W resistor and 1kΩ, 5%, 0.25W resistor as per procedure P/S#2 series resistance: 20Ω, 5%, 0.25W

Meters

Meter#1,2,3: Fluke 75 multi-meter, (equivalent or better) for voltage measurements

Scope

Standard scope with at least two channels

3.2 Equipment and EVM Setup

Table 1. I/O Connections and Configuration for Evaluation of bq25504 EVM

Jack	Description	Factory Setting
J1-VIN	Input Source (+)	
J1-GND	Input Source Return (-)	
J2-BAT	Battery connection (+)	
J2-GND	Battery Connection Return (-)	
J3 - VIN	Input Source Sense (+) [for J1]	
J3 -GND	Input Source Return Sense (-) [for J1]	
J4 - BAT_OK	Battery Status Indicator (+)	
J4 - GND	Battery Status Indicator Return (-)	
J5 - STOR	Charger Output (+)	
J5 - GND	Charger Output Return (-)	
J6 - STOR	Charger Output Sense (+)	
J6 - BAT	Battery Connection Sense (+) [for J2]	
J6 - GND	Battery Connection Sense (-) [for J2]	
JP1	MPPT setting: Enabled-Divider; Disabled-STOR	Place Shunt on JP1-2/3 (Divider)
JP2	OCS Setting: C5 Capacitor-No Shunt; Disabled-Shunt on REF-GND (JP1 should be Disabled)	No Shunt

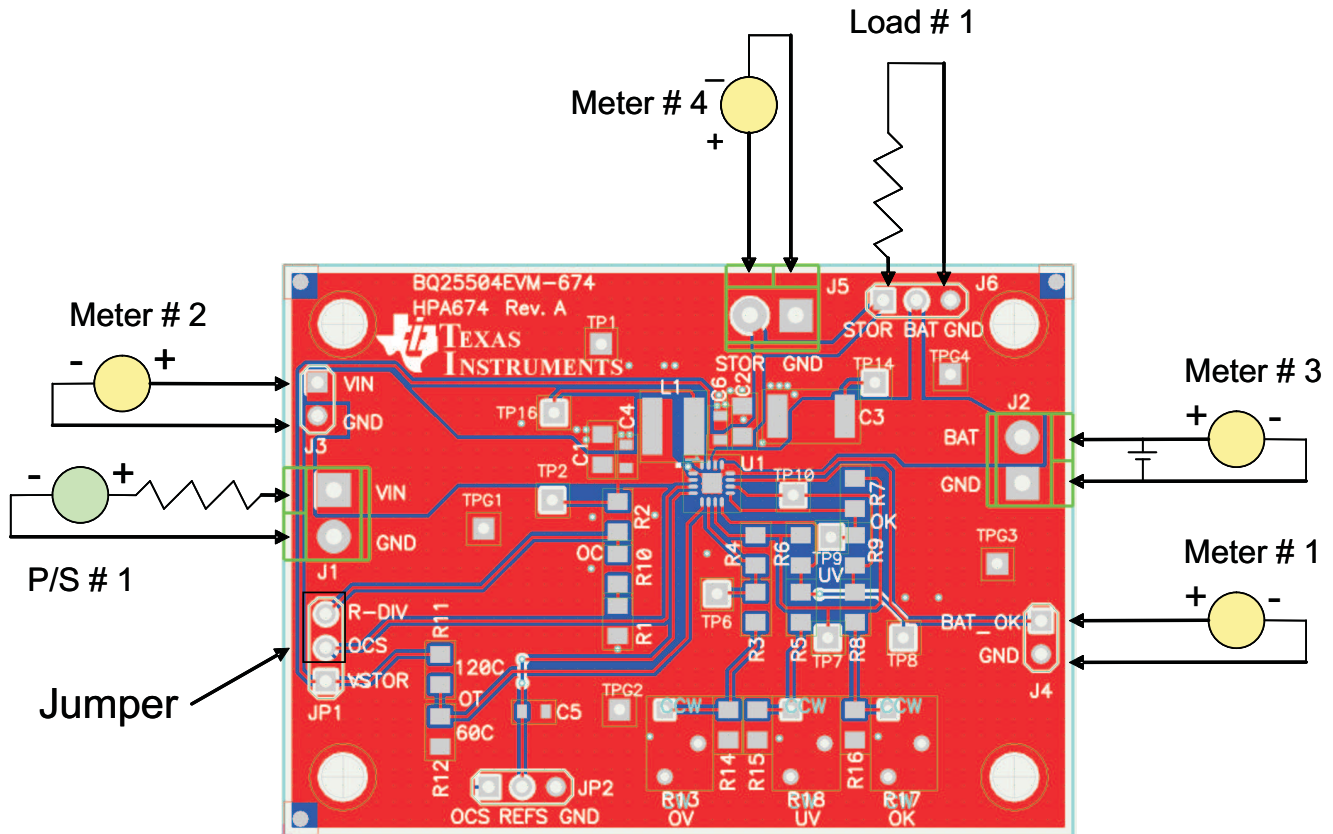


Figure 1. Test Setup for HPA674A (bq25504 EVM)

3.3 Test procedures

3.3.1 Power-up With No Battery and 10kΩ Load on STOR

1. Connect a 20Ω resistor to J1-1, 10k resistor between J6-1 and J6-3 and place shunt on JP1-DIV. Connect meters and scope probes to monitor CH1→CH4: V_{PHASE} (TP16), V_{STOR} , $V_{\text{P/S \#1}}$, V_{BAT} . Set scope to 1V per division for each channel and 20ms/div, single sequence trigger on $V_{\text{P/S\#1}}$, see Figure 2.
2. Set PS#1 to 1VDC and hot plug to input with 20Ω series resistor.

This is an example of cold startup ($V_{\text{STOR}} < 1.8\text{V}$). The input power is harvested by the boost converter and charges up to the initial OV setting, which is below the actual setting (pseudo softstart), the converter stops switching and the load discharges the STOR capacitor. Note that if the load is too great with no battery or a discharge battery the cold start may not be able to charge the battery. Therefore, it is important to manage the load with a discharged or missing battery, using BAT_OK. The converter continues to switch until V_{STOR} charges up to the OV threshold at 3.1V, the converter shuts off until V_{STOR} drops 35 mV (hysteresis) below OV and then the converter switches on periodically to maintain the output voltage. This is a similar operation to a hysteretic boost converter.

V_{PHASE} is the inductor switching node.

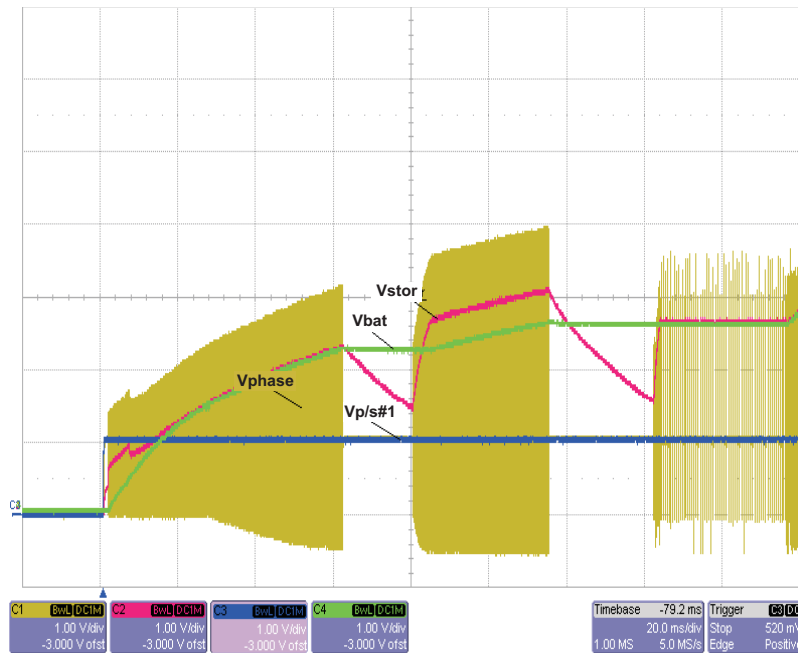


Figure 2. Startup with no Battery and 10k Load

3.3.2 Power-up with Battery less than UV (less than a diode drop below UV)

1. Same setup, as 3.3.1, except move the probe on V_{BAT} to V_{IN} and apply a charge element set to 1.9VDC between BAT and GND. Arm scope to trigger on $V_{P/S \#1}$.
2. Set PS#1 to 1VDC and hot plug to input with 20 Ω series resistor, see [Figure 3](#).

The start up is similar to the case without the battery but after the initial ~40ms period the STOR charges to 2.8V or ~0.9V above the battery and is charging the element via the BAT FET body diode. The next sampling cycle for UV detects that the VSTOR is greater than UV (2.2V) and then turns on the BAT FET. Since the battery is at 1.9V, VSTOR is pulled down to ~1.9V and the next UV sampling turns off the BAT FET. The cycling continues until the battery gets charged to the UV threshold and then finally the BAT FET stays on. A less complicated design would turn off the system load once the battery drops near the UV threshold to avoid this cycling.

If the storage element is lower than the maximum voltage (OV) then the element can theoretically take all of the available input power. As the harvesting source is loaded, its output voltage drops until reaching the MPPT threshold, which is currently programmed to 78% of the OC voltage and then the boost converter regulates the input voltage at this level by controlling the power transferred to the load. Note how V_{in} regulates to 78% of P/S#1 when the battery is lower than the OV voltage. Vary the input voltage slightly and wait for the 16 second update cycle to see how the MPPT is updated.

For a battery that is more than a diode drop below 1.8V, the charger may get stuck in cold startup which is less efficient and would take longer to recover. Once the STOR voltage gets above 1.8V and more than 32ms after power is applied, the low power cold start circuit is disabled and the main boost converter takes over.

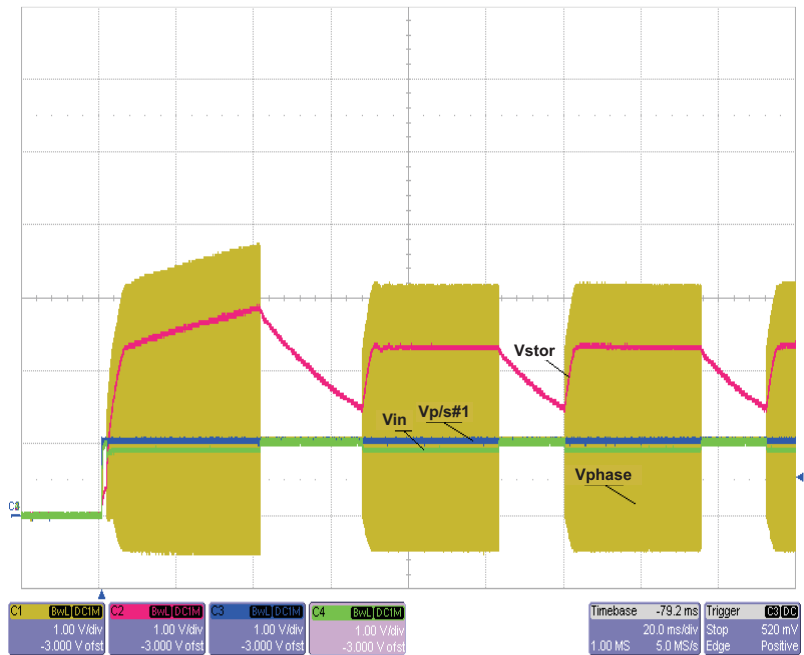


Figure 3. Startup with Battery Less Than UV

3.3.3 Power-up with Battery more than UV (2.3V to 3V), BAT FET ON

1. Same setup as 3.3.1, except change the charge element set to 2.4VDC between BAT and GND. Set scope to 2sec/div and to roll.
2. Set PS#1 to 1VDC and hot plug to input with 10Ω series resistor, see Figure 4.

Note in Figure 4 that the BAT FET is on and the STOR output is powered prior to the input being applied. This means the converter will start up in normal boost mode and after doing its initial sampling will regulate V_{IN} to the MPPT threshold.

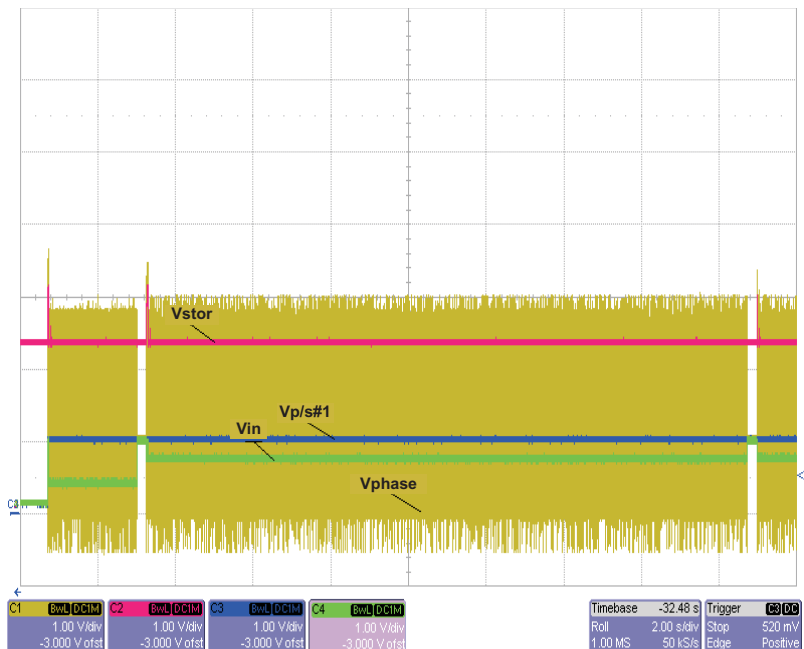


Figure 4. Powering up with a Battery above UV

3.3.4 BAT_OK Indication as Battery Charges/Discharges

1. Connect scope probes CHI→CH4: V_{PHASE} (TP16), V_{STOR} , V_{BAT_OK} , V_{BAT} and vary charge element from zero voltage to 3.15V and back down to 1.8V and observe the BAT_OK signal.

Initially P/S#1 is set to 1V and the battery is adjusted to 0V (simulated battery), which clamps V_{STOR} to ~0.5V (lower body diode drop due to lower current). As the battery voltage is swept higher one can see the different phases discussed earlier. Once the output gets to ~2.8V the BAT_OK signal goes high. Note that the BAT_OK signal goes low once the battery is discharged to ~2.34V.

This signal's high and low threshold can be programmed by R7, R8 and R9 to give an indication to the host when the battery is good (Signal high – has enough energy to complete the designed task) and when the battery is discharged (Signal low – system needs to be disabled or low power mode so the battery can recharge).

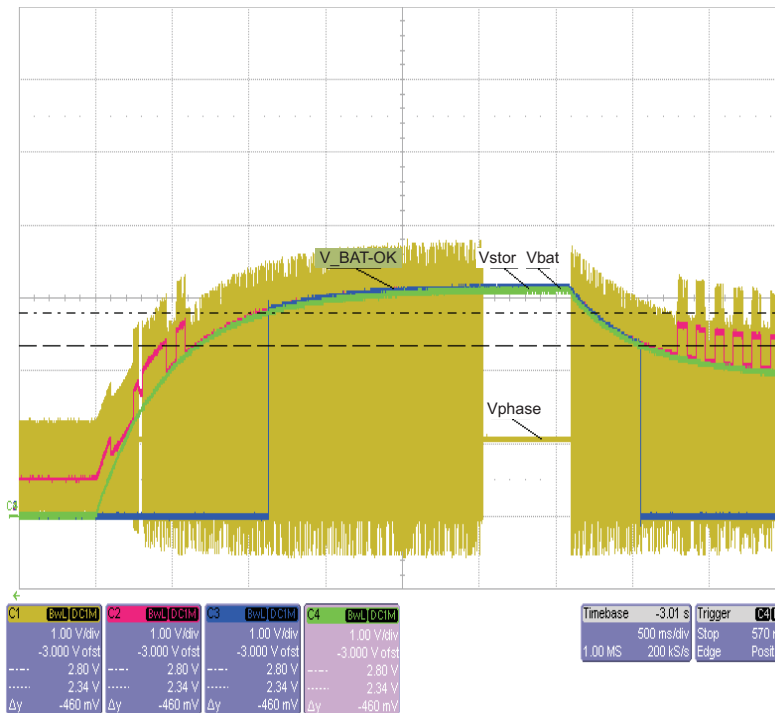


Figure 5. BAT_OK High/Low 2.8V/2.34V – Ramping Battery from 0V to 3.1V (0V) and Down to 1.8V.

3.3.5 Basic PFM Switching Waveform, $V_{in} = 1V$, $V_{bat} = 2.5V$

1. Set up scope as follows: CHI→CH4: V_{PHASE} (TP16), V_{STOR} , $V_{P/S \#1}$, V_{IN} , 10μs/DIV.

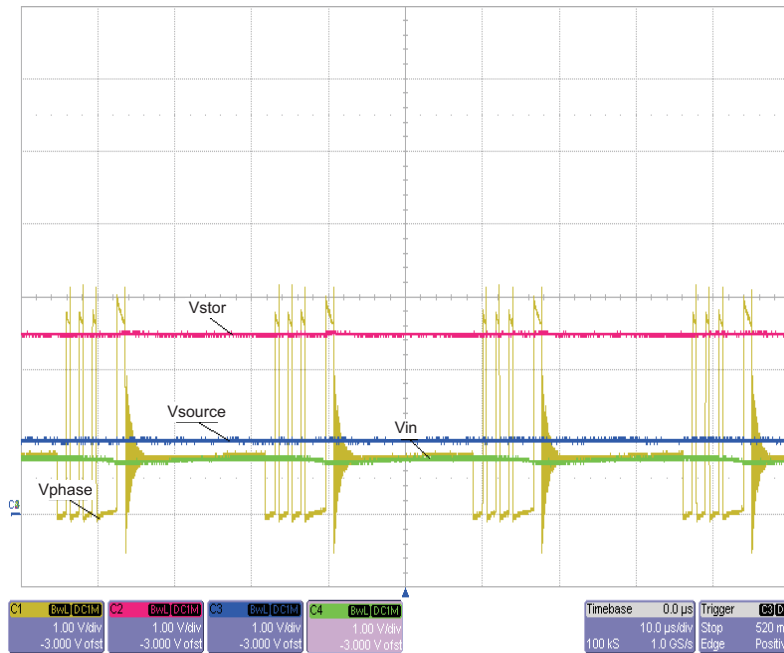


Figure 6. Basic Switching Converter, $V_{in} = 1V$, $V_{bat} = 2.5V$

Note here that V_{IN} is regulating at the MPPT threshold so the boost circuit is delivering the maximum power that the source can deliver. The user can see after about 4 pulses that the switching waveforms stops which cause the inductor to go discontinuous and ring.

3.3.6 Operation Near OV With 100-Ω Battery Impedance

1. Connect scope probes CHI→CH4: $V_{PH(TP16)}$, V_{STOR} , V_{IN} , V_{BAT} ; set $V_{P/S\#1}$ to 1.3 VDC and V_{BAT} to 3.00 VDC. Connect the power sources with their respective source impedance to the EVM. V_{IN} source impedance should be 20Ω and the battery impedance should be 100Ω. Set V_{STOR} and V_{BAT} to 20mVDC/div and 3.135VDC offset (3.135VDC was the average V_{BAT} [OV] measurement), 1 ms/div. Turn on sources.
2. The input source has enough energy to charge the V_{STOR} up to the OV setting; and, when the boost converter stops switching V_{STOR} will discharge down to the battery's cell voltage which is ~3V which is below the OV reset hysteresis. See Figure 7 for operation near OV. Note the hysteresis of V_{STOR} is around 35mV here, but this can vary depending on the input, output voltage, the source and battery impedance, and the number of pulses for each operation period of the boost converter.

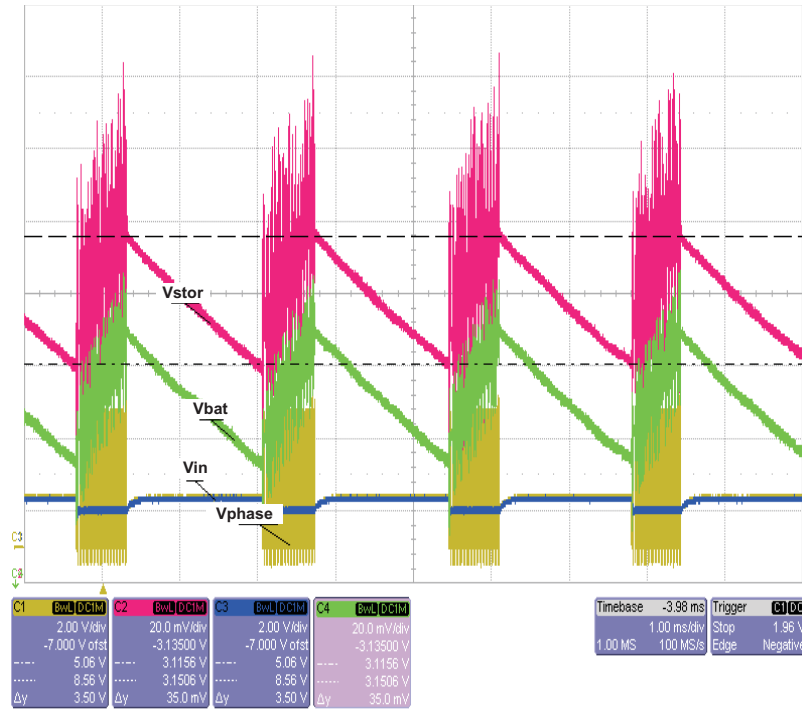


Figure 7. EVM Operation Near OV With 100-Ω Battery Impedance

4 PCB Layout Guideline

1. As with all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the boost converter/charger could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.
2. The resistors that program the thresholds should be placed as close as possible to the input pins of the IC to minimize parasitic capacitance to less than 2pF.
3. To lay out the ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. Assure that the ground traces are connected close to the device GND pins.
4. It is critical that the exposed thermal pad on the backside of the bq25504 package be soldered to the PCB ground. Make sure there are sufficient thermal vias right underneath the IC, connecting to the ground plane on the other layers.
5. Decoupling capacitors for VSTOR, VBAT should make the interconnections to the any Load as short as possible.
6. EVM layout can be used as guidance though a smaller layout is achievable.

5 Bill of Materials, Board Layout and Schematics

5.1 Bill of Materials

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
2	C1, C2**	4.7uF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM219R61A475KE19D	Murata
1	C3**	100uF	Capacitor, Ceramic, 6.3V, X5R, 20%	1812	GRM43SR60J107ME20L	Murata
2	C4, C6	0.1uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C5**	0.01uF	Capacitor, Ceramic, 50V, X7R, 10%	0603	GRM188R71H103KA01D	Murata
3	J1, J2, J5	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
2	J3, J4	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
1	J6	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
2	JP1, JP2	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
1	L1	22uH	Inductor, SMT, 0.8A, 360milliohm	0.153 x 0.153 inch	LPS4018-223MLB	Coilcraft
1	R1	10.0M	Resistor, Chip, 1/10W, 1%	0805	CRCW080510M0FKEA	Vishay
0	R11	Open	Resistor, Chip, 1/10W, 1%	0805	Std	Std
4	R12, R14, R15, R16	0	Resistor, Chip, 1/10W, 1%	0805	Std	STD
0	R13, R17, R18	Open	Potentiometer, 1/4 in. Cermet, 12-Turn, Top-Adjust	0.25x0.17	3266W-504LF	Bourns
3	R2, R6, R8	4.42M	Resistor, Chip, 1/10W, 1%	0805	CRCW08054M42FKEA	Vishay
1	R3	5.90M	Resistor, Chip, 1/10W, 1%	0805	CRCW08055M90FKEA	Vishay
1	R4	4.02M	Resistor, Chip, 1/10W, 1%	0805	CRCW08054M02FKEA	Vishay
2	R5, R10	5.60M	Resistor, Chip, 1/10W, 1%	0805	CRCW08055M60FKEA	Vishay
1	R7	1.43M	Resistor, Chip, 1/10W, 1%	0805	CRCW08051M43FKEA	Vishay
1	R9	4.22M	Resistor, Chip, 1/10W, 1%	0805	CRCW08054M22FKEA	Vishay
0	TP1, TP2, TP6, TP7, TP8, TP9, TP10, TP14, TP16, TPG1, TPG2, TPG3, TPG4	Open	Test Point, O.032 Hole		STD	STD
1	U1	BQ25504RGT	IC, NanoAmpere Integrated Boost Converter/Charger	QFN-16	BQ25504RGT	TI
1	--		PCB, 1.8 In x 1.8 In x 0.031 In		HPA674	Any
2	See Note 5		Shunt, 100-mil, Black	0.1	929950-00	3M

- Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
 2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
 4. Ref designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.
 5. Place shunt on JP1-2/3 (Divider) and JP2 (place on just one pin – ckt should be floating).

5.2 EVM Board Layout

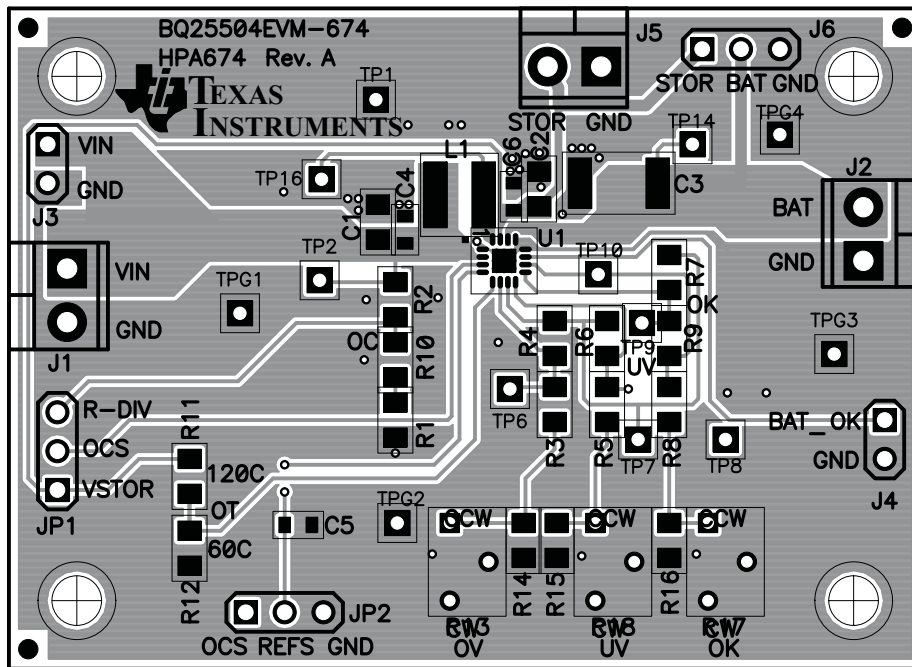


Figure 8. EVM PCB Top Assembly

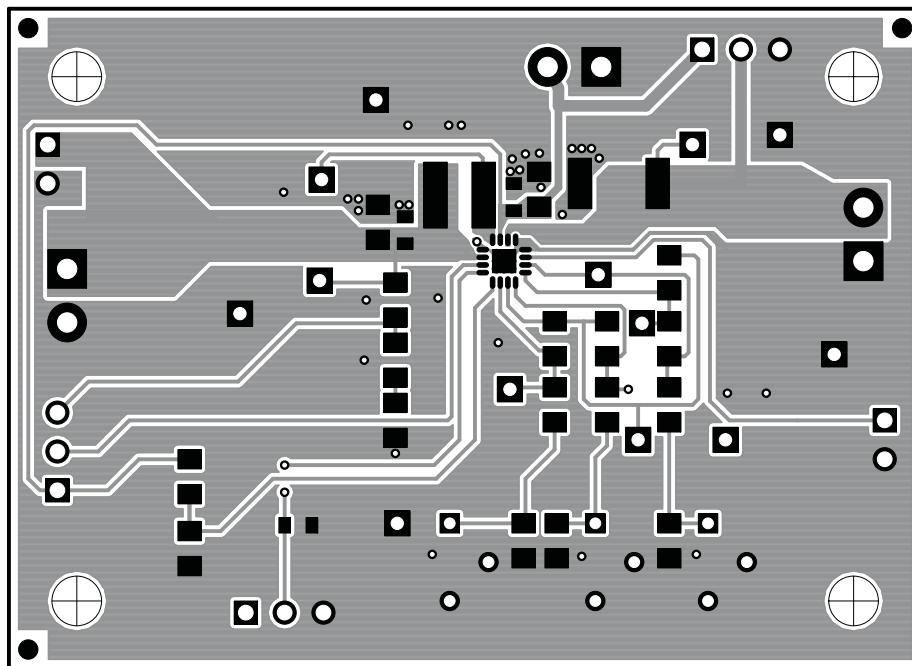


Figure 9. EVM PCB Top Layer

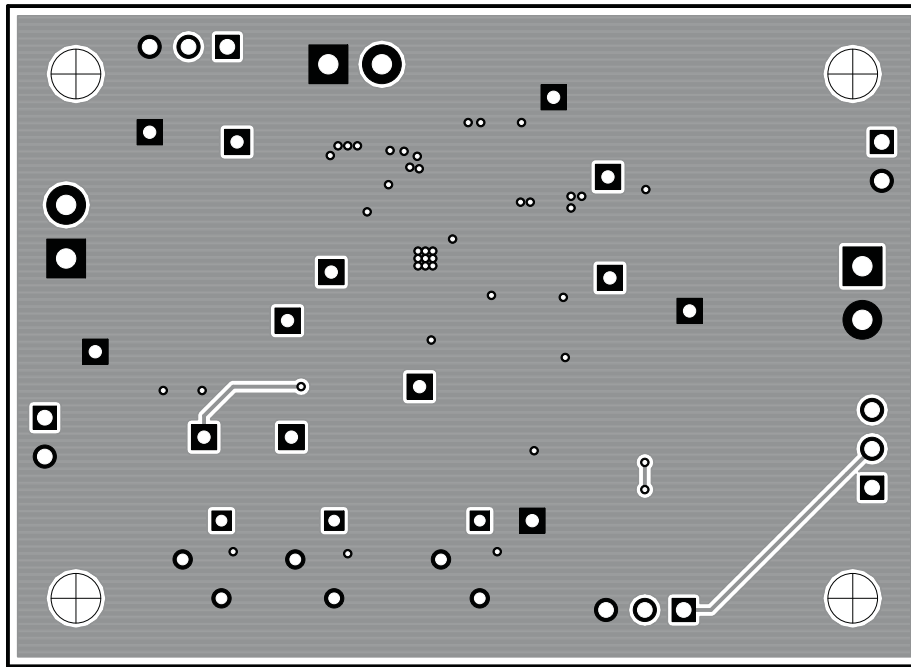


Figure 10. EVM PCB Bottom Layer

5.3 EVM Schematic

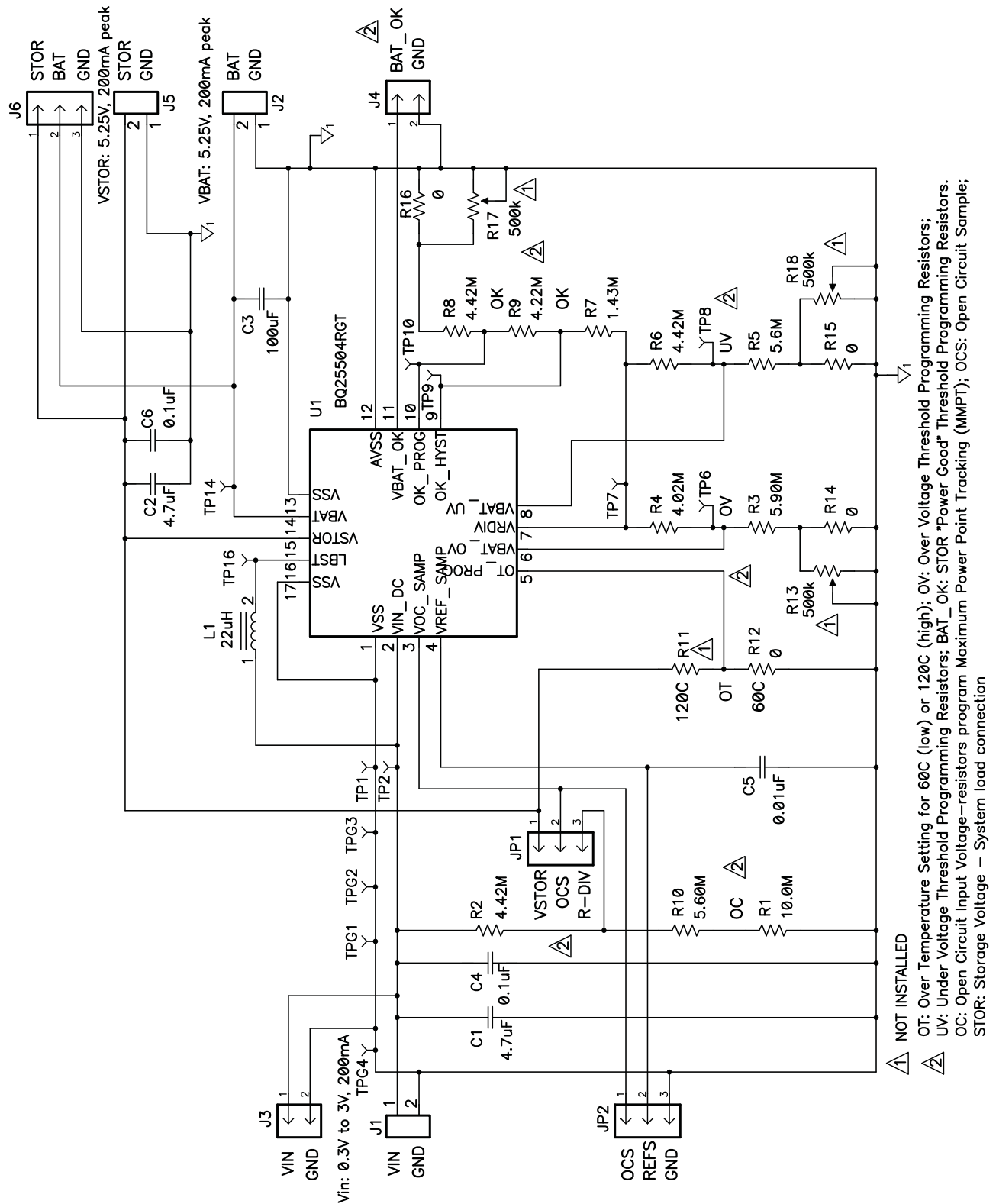


Figure 11. EVM Schematic

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to 5.5 V and the output voltage range of 0 V to 5.5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 105°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.